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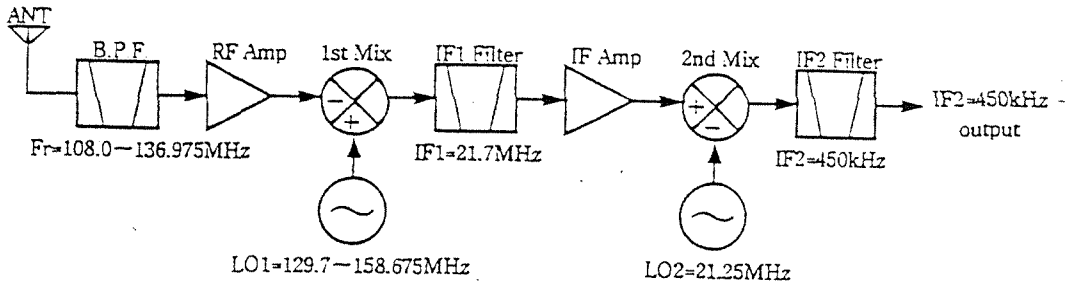
2 CIRCUITS DESCRIPTION

2.1 Receiver Section

2.1.1 Basic structure of Receiver Section

The Receiver section of the RHP-520 VHF Air Band Transceiver has the double super-heterodyne structure, which uses 21.7 MHz for the first intermediate frequency (IF1) and 450 kHz for the second intermediate frequency (IF2).

FREQUENCY BLOCK DIAGRAM



The first frequency converter circuit (1st Mixer) mixes the received signal with the first local oscillator signal, whose frequency (LO1) is higher than the selected receive frequency (Fr) by the first intermediate frequency (IF1 = 21.7 MHz), to down-convert the received signal to the first intermediate frequency band (Fr to IF1). Since LO1 is determined so that it is always higher than Fr by IF1 (21.7 MHz), Fr and LO1 has always the relation as expressed by the following equation:

LO1 - Er = IF1

(IF1=21.7MHz)

(where 108.0≤Fr≤l36.975 MHz)

To receive the 108.000 to 136.975MHZ receive band, therefore, LO1 in the frequency range of 129.700 to 158.675MHz is used. The local frequency is fed to 1st Mixer from the Synthesizer section in channel steps of 25 kHz.

The second frequency converter circuit (2nd Mixer) mixes the first IF band signal with the second local oscillator signal, whose frequency (L02) is lower than IF1 (21.7 MHz) by the second intermediate frequency (IF2: 450 kHz), to down-convert the first IF band signal to the second IF band (IF1 to IF2).

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Since LO2 is determined so that it is always lower than IF1 by IF2 (450 kHz). IF2 and LO2 has the relation as expressed by the following equation:

L02 = IF1 - IF2 = 21.7 - 0.450= 21.25 MHZ

(IF1=21.7MHZ)

(IF2=0.450MHz)

The received signal thus converted to the second intermediate frequency band (IF2: 450 kHz) is further demodulated to audio-frequency signal by the AM demodulation circuit. Finally, the audio-frequency signal is amplified in the AF amplifier section and output as sound by the speaker.

2.1.2 Operation of Receiver Section

The received signal input from the antenna terminal (J301) passes through the low-pass filter and Transmit/Receive switching circuit (CD3O1, CD302 and TR326) and then enters the band-pass filter 1 (BPF1) for the receive band in the RF unit (CMN-517). The center frequency of BPF1, together with that of the band-pass filter 2 (BPF2) in the following stage, is controlled by the voltage from the Control Section and shifted so that the receive frequency and the center frequencies of BPF1 and BPF2 always coincide. The received signal which has passed through BPF1 is amplified in the RF amplifier (TR301) and enters BPF2. The received signal from BPF2 is mixed with the first local oscillator signal (frequency: LO1) from the Synthesizer Section and converted to the first intermediate frequency signal (1st IF (IF1) = 21.7 MHZ) in the first frequency converter circuit (TR302).

Next, the 1st IF signal passes through the first intermediate frequency filter (FL301) and the first intermediate frequency amplifier (TR303), and then enters the second frequency converter circuit (2nd Mixer). The 1st IF signal is mixed with the second local oscillator signal (L02) from the Synthesizer Section and converted to the second intermediate frequency signal (IF2 = 450 kHz) in the 2nd Mixer. The 2nd IF signal from 2nd Mixer passes through the 2nd IF filters (FL302 and FL303) and then enters the 2nd IF amplifier and detection circuit in IC302, where the signal audio frequency signal is detected. The audio frequency signal is fed into the AF unit (CAB-781).

The receiver of RHP-520 has an AGC (Automatic Gain Control) circuit which controls the gain according to the level of received signal, to keep the level of demodulated signal constant. The AGC circuit controls the gates of the RF amplifier TR301 and 1st IF AMP TR303 with the level produced by IC303 from the voltage of signal after the detection in IC302.

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The receiver also has a squelch circuit for quieting the noises generated in the receiver when the received signal is too low. The squelch circuit amplifies the signal after the detection with the noise amplifier in IC302, passes the output signal of the noise amplifier through the active band-pass filter, then detects the signal with CD309, and inputs the signal from the detection to the comparator. The comparator compares the noise level of the received signal with the voltage set by the squelch control, and outputs the mute signal to the Control Unit (CMC-1086) when the noise level is greater than the set level.

The power supply for the receiving RF unit (CMN-517*)* is regulated by the regulator IC (IC304). 5V voltage is supplied to the circuits in the RF unit in the receive mode.

2.2 AF Amplifier Section

The AF signal demodulated in the RF unit (CMN-517) is input to the AF unit (CAB-781). The AF unit has a mute circuit for squelch, ANL circuit, beep circuit, low-pass filter (LPF) circuit, and audio amplifier circuit.

The AF signal fed to the AF unit first enters the ANL circuit. The ANL circuit limits the voltage amplitude of the AF signal to suppress pulse noises by clipping voltages over the forward turn-on voltage of the diode (CD1O3). The ANL function is switched on and off by the CPU through the analog switch (IC112).

The AF signal from the ANL circuit passes through the analog switch (IC103), mute circuit (TR1O3, IC104. 4/4), beep circuit (IC104. 2/4, IC104. 3/4) and BPF circuit (IC104. 1/4), and then reaches the volume control. The mute circuit mutes the AF signal when no signal is received under the control of the CPU. The beep circuit adds a beep sound corresponding to the operation according to the control of the CPU.

The AF signal is changed to the level determined by the volume control and input to the two audio amplifiers. In these audio amplifies, IC105 is used when the built-in speaker is selected, and IC106 is used when an external speaker is selected. These audio amplifiers are controlled by the mute control of the CPU, and the power supply to them is switched off when the AF signal is not present.

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2.3 Transmitter Section

The AF signal input from the MIC terminal of the AF unit (CAB-781) is amplified to the predetermined same level by the ALC (Automatic Level Control) circuit (IC107). The output signal of IC107 is input to the modulator circuit (TR321) of the RE unit (CMN-517) through the AF amplifier (IC109. 1/2) and low-pass filter (IC109. 2/2). The amplifier, active filter and other circuits in the AF unit are supplied with 5V voltage regulated by the regulator IC (TR111) through the switching transistors (TR118, TR119) only in the transmit mode.

The carrier signal input to the modulator circuit (TR321) is fed from the Synthesizer Section which generates the transmit frequency signal through the Transmit/Receive switching diode (CD315) and the attenuator. The modulator circuit (TR321) mixes the carrier signal and the audio signal to produce an AM (Amplitude Modulated) signal.

The AM signal is then amplified by the APC amplifier (TR322), driving amplifier (TR323), and power amplifier (TR324) to the level such that the power at the antenna terminal is 5 W (PEP). The AM signal amplified to the necessary level is output to the antenna terminal (J301) through the Transmit/Receive switch (CD301) and the low-pass filter circuit used for both transmission and reception.

The gain of the APC amplifier (TR322) is controlled by APC (Automatic Power Control) to keep the output constant. The APC detects the RF output of the power amplifier (TR324) into voltage level with the diode (CD318) and controls the voltage of the gate of TR322 using the voltage level so as to keep the output of the APC amplifier constant. The TR323 and TR324 amplifiers are class AB amplifiers, and have a diode (CD316, CD317) connected between the base and emitter of their transistor. These diodes prevent the thermal runaway of the transistors at high temperatures during a continuous transmission by the thermal coupling with the transistors.

The power supply for the transmitting RF unit (CMN-517) contains 12.0V voltage supplied to the driving amplifier (TR323) and the power amplifier (TR324) and 5V voltage supplied to the other circuits in the Transmitter section through the regulator IC (IC3Q6). The output of the regulator IC (IC306) is supplied to the Transmitter section when the PLL in the Synthesizer section is locking and switched off when the PLL is unlocking.

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2.4 Synthesizer Section

The Synthesizer Section feeds the first and second local oscillator signals to the Receiver Section and the carrier signal to the Transmitter Section.

The first local oscillator signal for the Receiver Section and the carrier signal for the Transmitter Section are generated as follows. One of the two VCOs (Voltage Controlled Oscillator: TR313 and TR314) selected according to the frequency is made to oscillate at the frequency twice the necessary frequency. The output of the VCO oscillator passes through the buffer amplifier (TR315), then branches into the input signal to the variable frequency divider of the PLL IC (IC301) and the input signal to the 1/2 frequency divider (IC307).

The frequency of the signal fed to the variable frequency divider of the PLL IC (IC301) is divided to the comparison frequency Fp (50 kHz) by the frequency divider (dividing ratio: N) controlled with the data from the CPU.

When the Synthesizer unit outputs 118.0 MHz, for example, the selected VCO must generate the signal of the frequency twice that frequency:

F_{osc} = 118.0 x 2 = 236.0 MHz

The dividing ratio N of the variable frequency divider is:

N = F_{osc} / Fp = 236.0 MHz / 50 kHz = 4720

Therefore, the dividing ratio N of the variable frequency divider of the PLL IC (IC307) is 4720. On the other hand, the oscillation frequency F_{osc} (21.25 MHz) of the crystal resonator (X301) is divided by the dividing ratio R (R=425) to generate the reference comparison frequency F_{ref} (F_{ref} = F_{osc}/R = 50 kHz). The phases of Fp and F_{ref} are compared in IC301. The resultant output signal passes through the charge pump in IC301 and the low-pass filter, and is applied to the varicaps (W312, W313) as the control voltage for the VCO. Since the VCO voltage is controlled so that the phases of the two inputs signals for phase comparison coincide with each other, the output frequency of the VCO is kept constant. The output frequency of the VGO in this state has the same stability and characteristics as the frequency of the X301- controlled oscillator by the control of the PLL loop.

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The other signal input to the 1/2 frequency divider (IC307) is frequency-divided to the half frequency in IC307. The signal is then fed through the buffer amplifier (TR316) to the first frequency converter circuit (TR302) as the first local oscillator signal in the receive mode or to the frequency modulator circuit (TR321) as the carrier signal in the transmit mode by means of the diode switch (CD315) operated by the transmitting and receiving operation.

The 21.25 MHz frequency generated by X301 is fed to the second frequency converter circuit in IC302 as the second local oscillator signal through the buffer-amplifier (TR312).

2.5 VOR Demodulator Section

The signal demodulated in the RE unit (CMN-517) is input to the AF unit (CAB-781) and branches to the AF amplifier section for amplifying audio- frequency signals and the VOR demodulator section for displaying the angle of the VOR signal The signal input to the VOR demodulator section passes through the buffer amplifier (IC102. 3/4) and enters the band-pass filter (BPF), by which the signal is separated into 30Hz variable phase signal (compare) and 9960Hz reference phase signal (reference). The 30Hz variable phase signal extracted by BPF (IC102. 2/4) is shaped by the comparator (IC102. 2/4) into a 30Hz square wave signal, which is output to the VOR COMP pin of the CPU. The other 9960Hz reference phase signal extracted by the other BPF (IC102. 4/4) is a frequency-modulated signal, and its modulation component (frequency deviation ±480Hz, modulation frequency 30Hz) is converted into a square-wave signal (frequency=3OHz) by the modulation IC (IC101). This square wave signal is output to the VOR REF pin of the CPU.

The phases of these two 30Hz square-wave signals are compared by the CPU to determine the angle for the angular display of the VOR signal. Further, to prevent a false display caused by voice or noises, the 9960Hz signal is monitored in IC101, and the monitor signal is output to the VOR SW pin. By using this signal. the display of the angle of the VOR signal is made only when the VOR signal is being detected.

The power supply to the VOR demodulation circuit is switched on by transistor TR101 for the receive frequency of 108.0MHz to 117.975MHz.

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2.6 Control Section

The control of various functions is all performed by the CPU (IC1). The CPU has built-in masked programs, and performs acquisition of various data and output of control signals according to the programs. The CPU has also a built-in crystal oscillating circuit, which oscillates at the frequency determined by the crystal Xl (4.9152 MHz). The signal generated by this oscillating circuit is used as the system clock.

The followings are the contents of the main controls performed on the Control unit. The other controls are also performed by sending the control signals from the assigned ports of the CPU to the respective circuits and acquiring the information necessary for the control from the circuits through the ports. For the detailed description of the CPU ports, refer to the CPU Port Table.

2.6.1 Key Input

All operations of RHP-520/500 such as frequency setup, channel selection and PTT are made with the 20 (4x5) keys on the front panel and the three keys on the sides. The key data of the front keys are read in with the key matrix consisting of S output ports and 4 input ports of the CPU. The key data of the side keys is read in through the 3 input ports of the CPU.

2.6.2 Display on LCD

The CPU controls the LCD with 28 segments and 4 common matrix to display various information on the LCD. The connection between the CPU and the LCD are made by means of the rubber connector P1 inserted between the PCB of the Control unit (CMC-1086) and the glass of the LCD1.

2.6.3 Backlighting

The backlight of the LCD and that of the front keys illuminate and go out alternately as you press the LAMP key on the side. When the CPU has detected that the LAMP key is pressed and turns on the backlights, it turns on the transistor TR2, which controls the backlights. This allows an electric current to flow through the light emitting diodes LED1 to LED2 for backlighting the LCD and the light emitting diodes LED3 to LED7 for backlighting the front keys.

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2.6.4 Variable tuning control for pass band filter

The CPU outputs 5 bits control data for setting the pass band of the band- pass filter in. the RE amplification section in the Receiver section. This digital 5 bits data is converted into analog voltage data with the ladder- type resistor circuit and fed to the band pass filter in the Receiver section through the buffer amplifier (IC3).

2.6.5 EEPROM data input and output

The CPU controls the input and output to and from EEPROM (IC2) of the data for restoring the same state as when the power is turned off when the power is turned on and allowing the frequency settings to be used in the memory channel.

2.6.6 Reset circuit

The reset IC (IC4) shuts down the CPU (IC1) when the power supply voltage to the CPU lowers below the minimum operating voltage to prevent malfunction of the CPU (IC1). The CPU stops the operation when it is shut down and resumes the operation when the power supply voltage rises to or over the minimum operating voltage.

2.6.7 Power Supply

The voltage of the Ni-Cd battery pack (NBB-487) for RHP-520/500 is supplied to the RE unit (CMN-517) and the switch in the volume control (RV602) on the panel. Since the nominal voltage of one cell of Ni-Cd battery is 1.2 V, tie voltage supplied by this battery pack is 12V (1.2 V x 10). The 12V voltage of the battery pack is supplied to the Receiver Section, Transmitter Section, Synthesizer Section, AF Amplifier Section, and Control Section.