

## CY8CKIT-062-BLE PSoC 6 BLE Pioneer Board

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### Drawing Numbers

|          |              |
|----------|--------------|
| PCBA     | 121-60367-01 |
| PCB      | 600-60380-01 |
| FAB DRW  | 610-60337-01 |
| ASSY DRW | 620-60345-01 |
| SCH DRW  | 630-60357-01 |



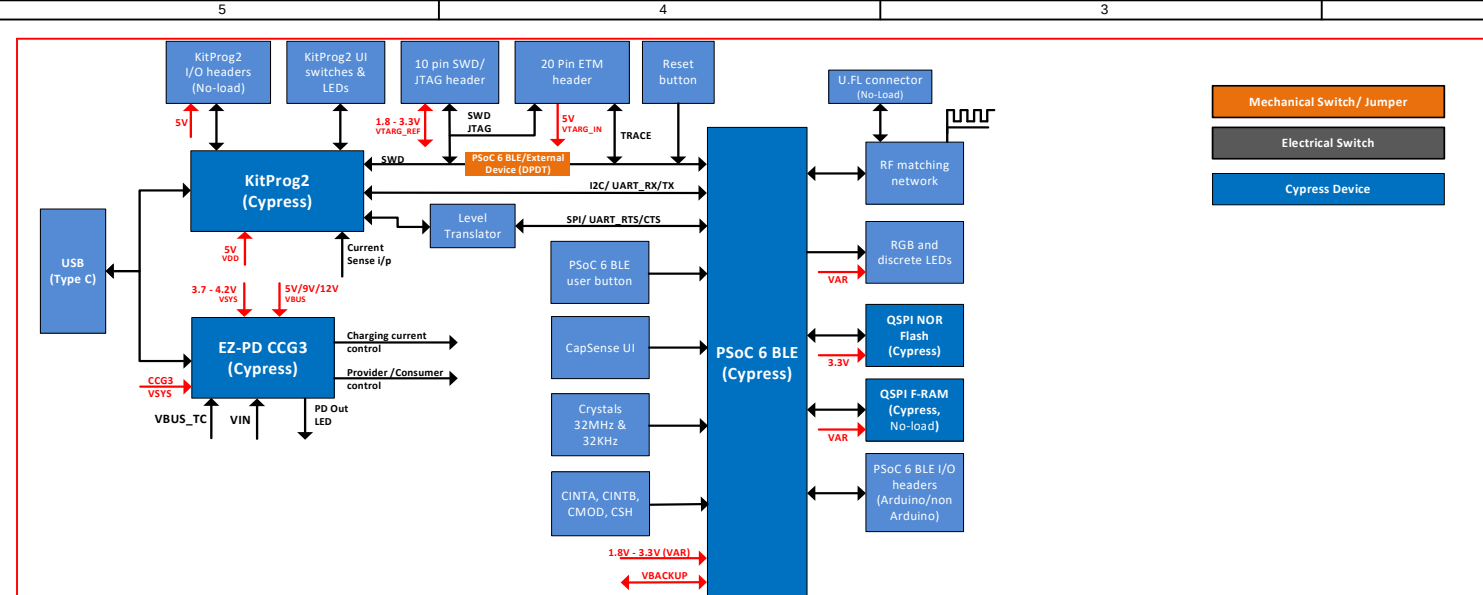
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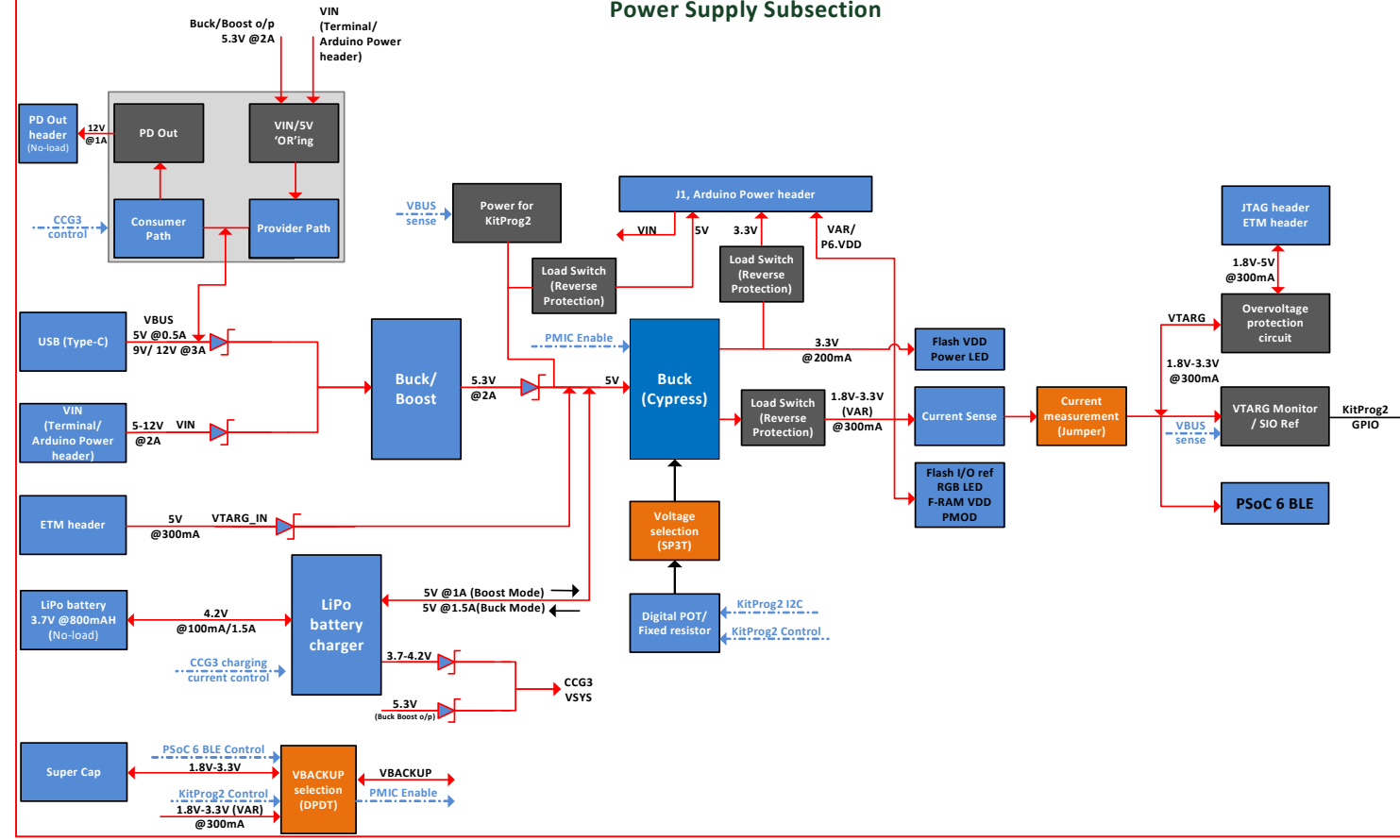
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**Page Title : Title & Table of Contents**

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### Power Supply Subsection





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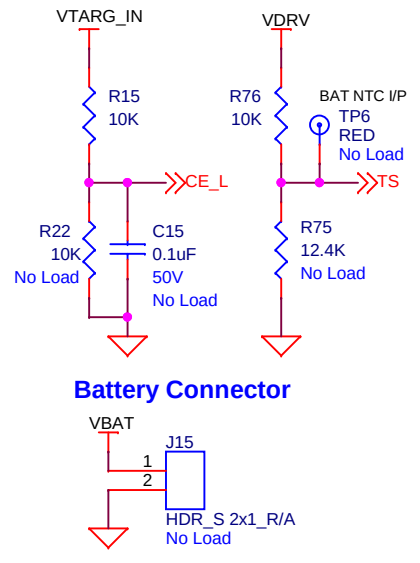
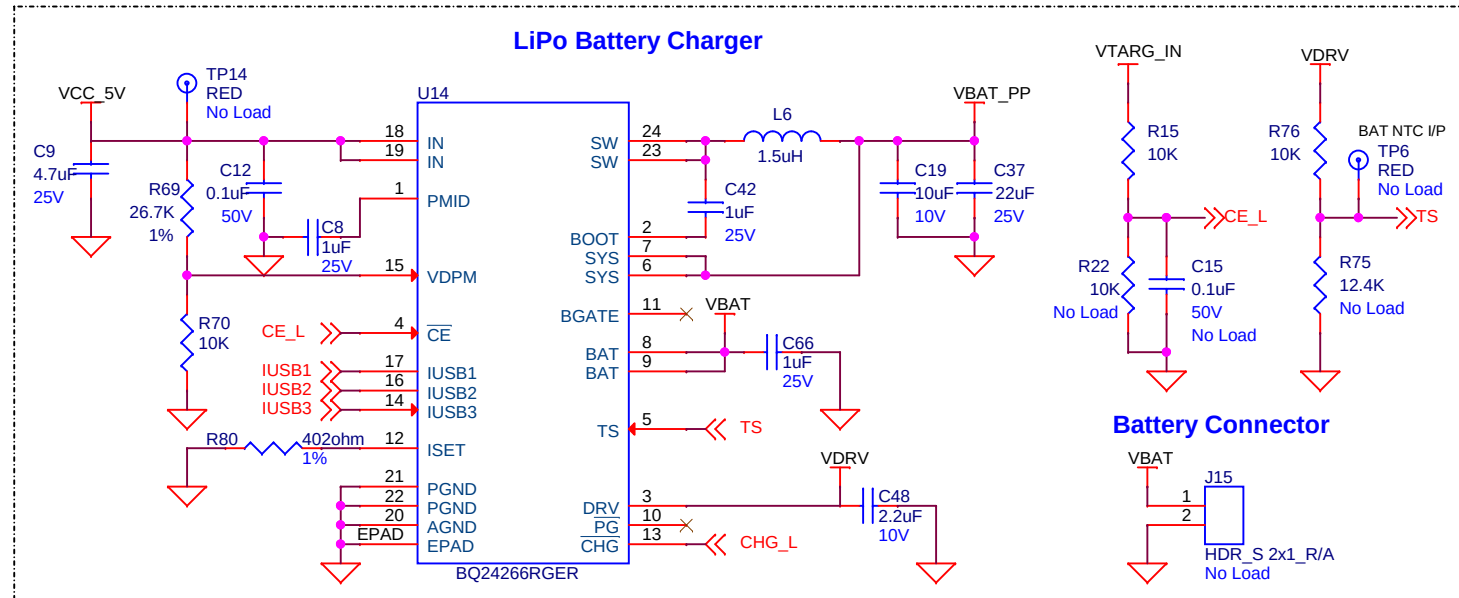
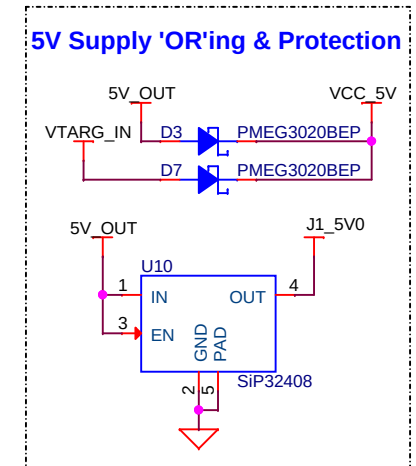
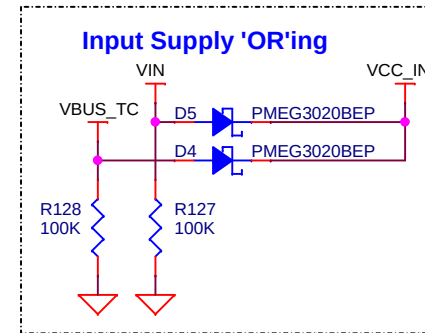
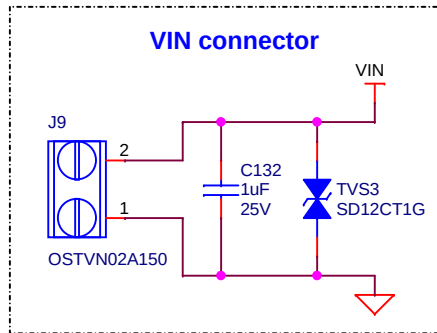
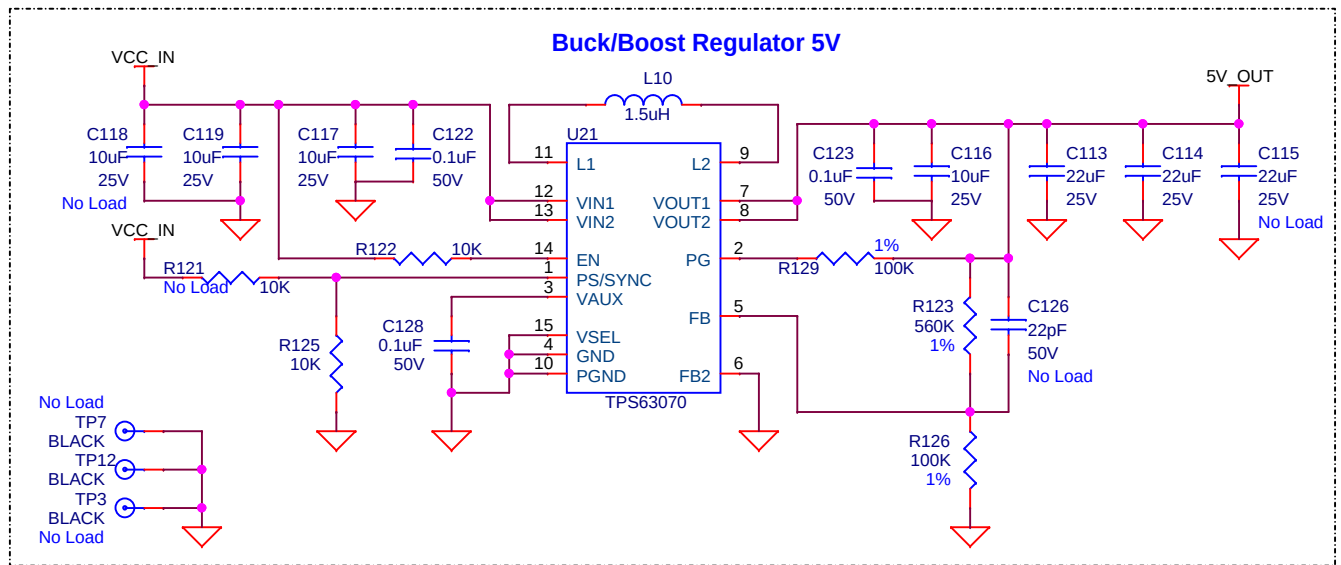
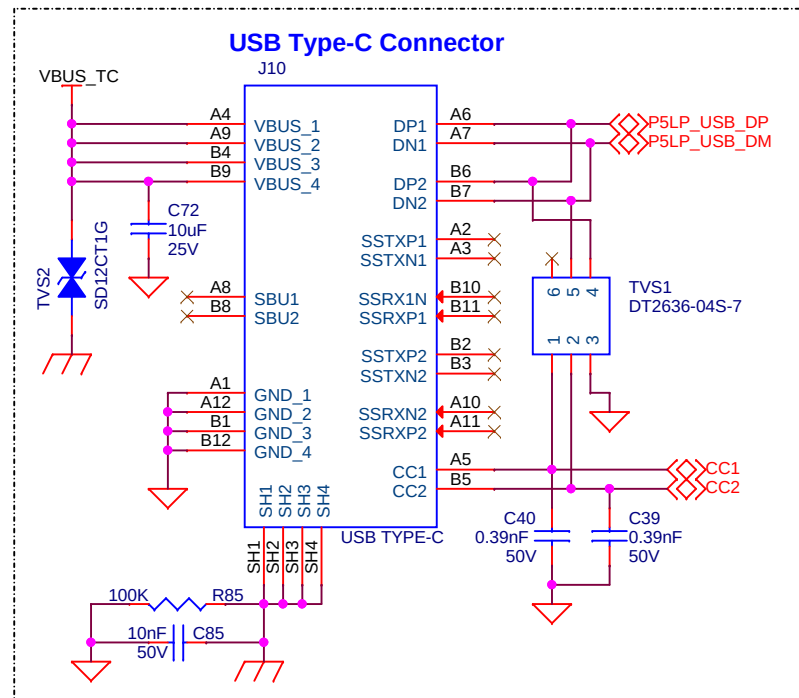
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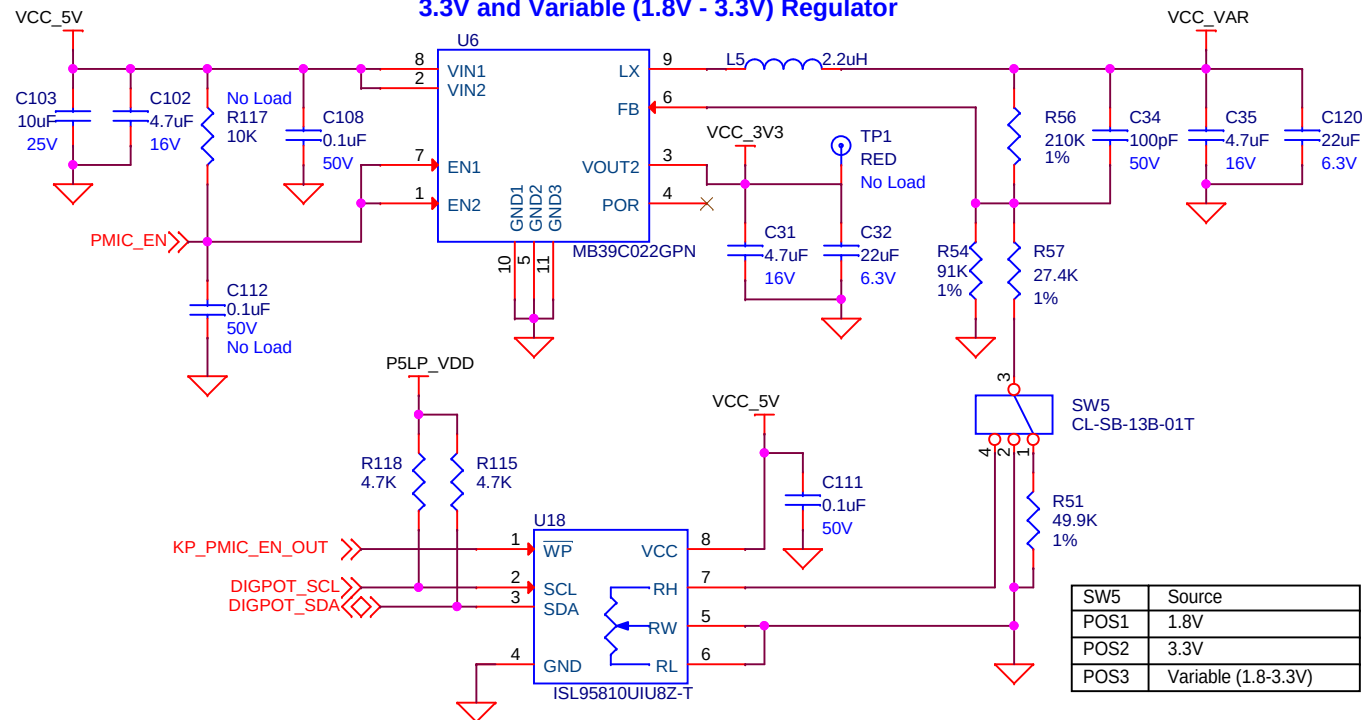
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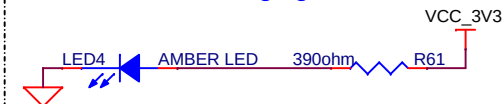
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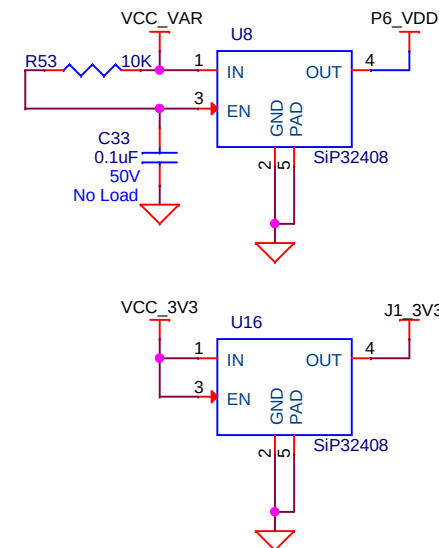
### 3.3V and Variable (1.8V - 3.3V) Regulator



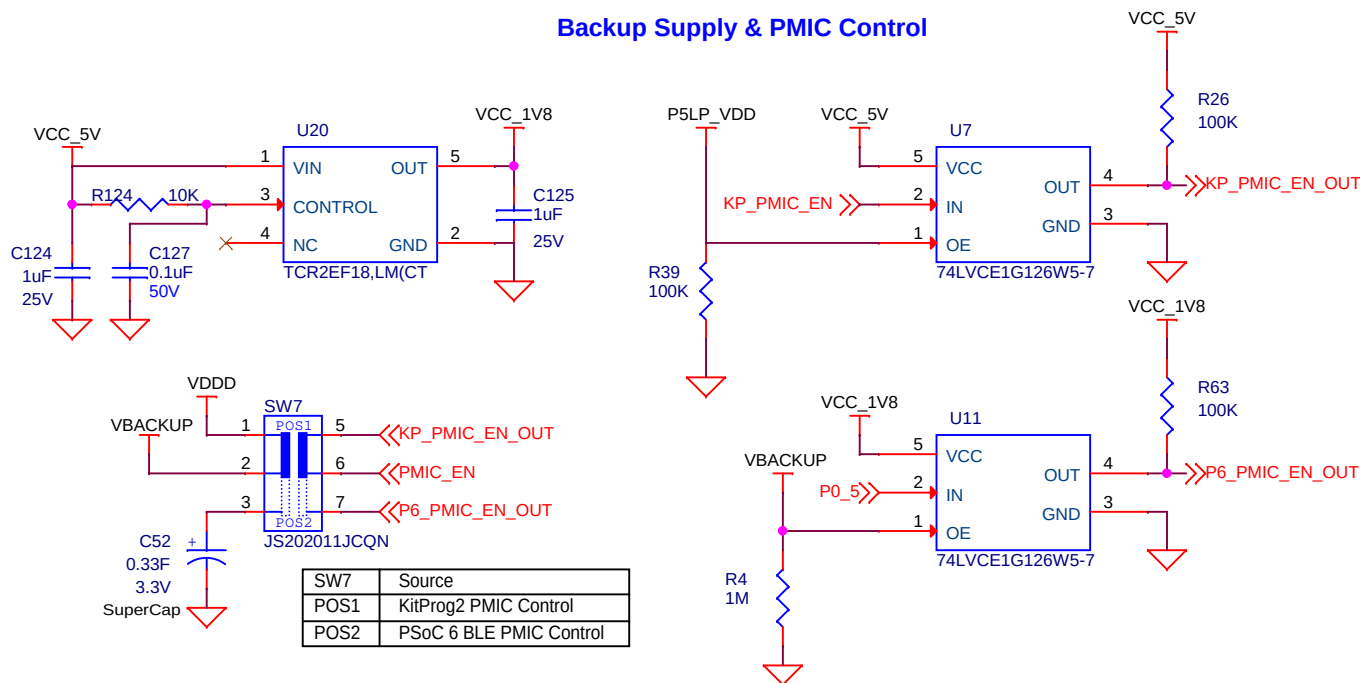
### Power & Charging LED



### Reverse protection



### Backup Supply & PMIC Control



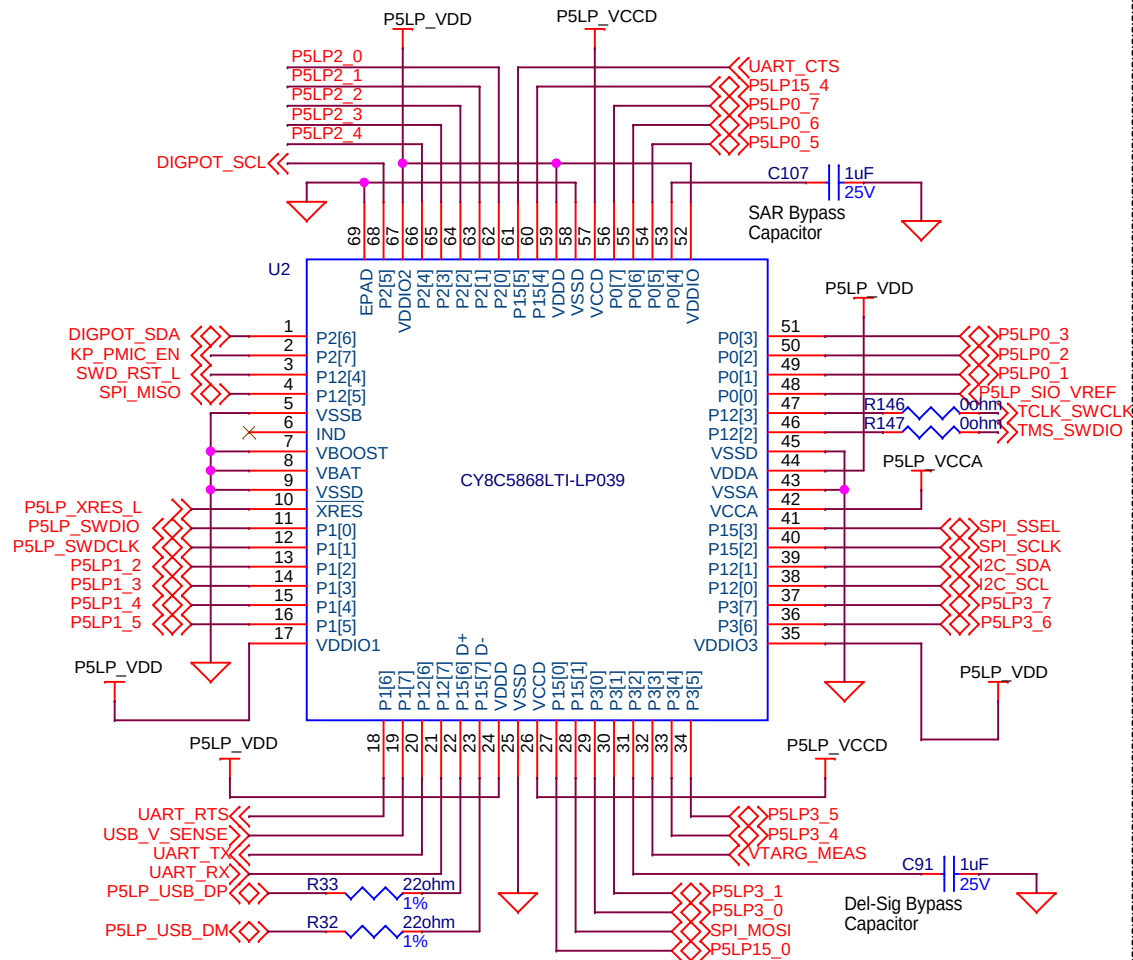
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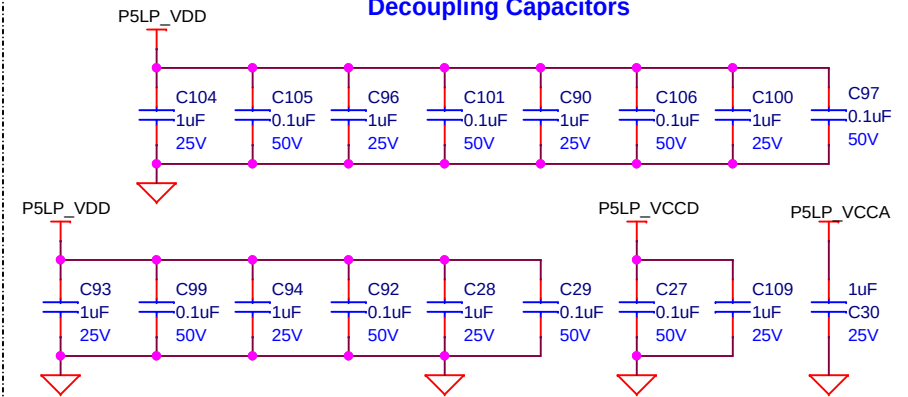
Page Title : Main Variable Regulator

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## PSoC 5LP based KitProg2



## Decoupling Capacitors



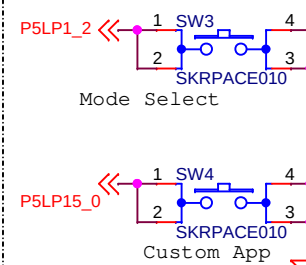
## KitProg2 HW Revision

P5LP2\_0 Bit 0  
P5LP2\_1 Bit 1  
P5LP2\_2 Bit 2  
P5LP2\_3 Bit 3  
P5LP2\_4 Bit 4

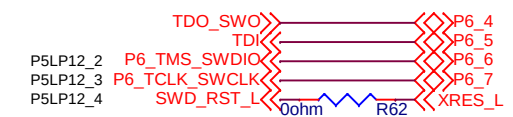
ID = 0x02

Note: GND is read as binary "1" and floating as "0"

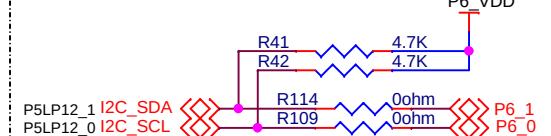
## PSoC 5LP User Switches



## SWD Interface



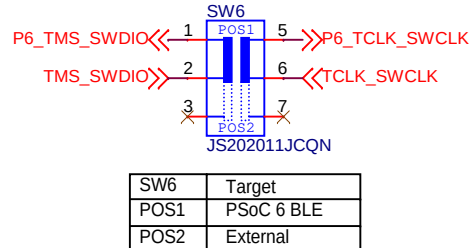
## I2C Interface



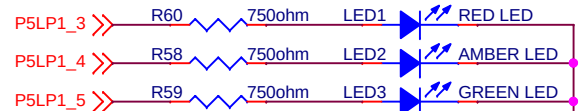
## UART Interface



## SWD Target Select



## PSoC 5LP Status LEDs



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Page Title : KitProg2 Controller

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### Target PSoC Program/Debug Header

VTARG\_REF

C133  
1uF  
25V

TVS4  
ESD3V3D5-TP

J11

1 2 3 4 5 6 7 8 9 10

HDR\_S 5x2

TMS\_SWDIO  
TCLK\_SWCLK  
TDO\_SWO  
TDI  
SWD\_RST\_L

## Program/Debug Overvoltage Protection

The diagram illustrates a Program/Debug Overvoltage Protection circuit. It includes a P6\_VDD input, a VTARG\_REF input, and a No Load output. The circuit features several components: NTR4171PT1G (MOSFET), PMV48XP,215 (MOSFET), R152 (0ohm), R151 (15K), R153 (10K), Q3, Q4, D9 (BZT52C3V9-7-F), and DMP3098L-7 (Diode).

## Voltage Monitoring

The diagram illustrates the Voltage Monitoring circuit, showing the internal structure of the U19 (SIP32401ADNP) and the external components connected to it.

**U19 (SIP32401ADNP) Internal Structure:**

- IN (3):** Connected to P6\_VDD.
- EN (4):** Connected to P5LP\_VDD.
- OUT (1):** Connected to VTARG\_MON.
- GND (2):** Connected to ground.
- PAD (5):** Connected to ground.

**Capacitors:**

- C110 (0.1uF, 50V):** Connected between P5LP\_VDD and ground.
- C121 (0.1uF, 50V):** Connected between P5LP\_VDD and ground.

**External Components:**

- P5LP\_VDD:** Connected to the EN pin of U19. It is also connected to a voltage divider consisting of R94 (15K) and R95 (30K) in series, with the midpoint connected to USB\_V\_SENSE.
- VTARG\_MON:** Connected to the OUT pin of U19. It is also connected to two voltage dividers. The first divider consists of R30 (15K) and R36 (30K) in series, with the midpoint connected to VTARG\_MEAS. The second divider consists of R55 (49.9K, 1%) and R52 (49.9K, 1%) in series, with the midpoint connected to P5LP\_SIO\_VREF. The output of this divider is labeled "No Load".

### Level Translator for SPI and UART flow control

The diagram illustrates a level translator circuit for SPI and UART flow control, centered around the FXMA108BQX IC (U13). The IC is configured as follows:

- Power Supply:**
  - VCCB:** Connected to P5LP\_VDD (pin 20) via a 1uF capacitor (C38) to ground.
  - VCCA:** Connected to P6\_VDD (pin 1) via a 1uF capacitor (C41) to ground.
  - DAP:** Connected to GND (pin 21).
  - OE:** Connected to GND (pin 10).
- Signal Connections:**
  - SPI Signals:**
    - SPI\_MOSI (pin 19) to B0
    - SPI\_SCLK (pin 18) to B1
    - SPI\_MISO (pin 17) to B2
    - SPI\_SSEL (pin 16) to B3
    - UART\_RTS (pin 15) to B4
    - UART\_CTS (pin 14) to B5
  - GPIOs:**
    - B6, B7, A7, A6, A5, A4, A3, A2, A1, A0 are connected to P12\_0 through P12\_9.
    - A8, A9, B8, B9 are marked with 'X' and are not connected.
  - UART Signals:**
    - P5LP\_SSEL\_P12\_0 (pin 5) to A2
    - P5\_3 (pin 7) to A4
    - P5\_2 (pin 8) to A5
- Other Components:**
  - R78:** A 10K pull-up resistor connected to P6\_VDD and pin 11.
  - R77:** A 10K resistor connected to pin 11 and ground.
  - Label:** "No Load" is placed near R78.

### PSoC 5LP GPIO Expansion Header

**PSoC 5LP GPIO Expansion Header**

Diagram showing the PSoC 5LP GPIO Expansion Header (J6) connections. The header is labeled **CON 8x2 No Load**.

Connections (Left side):

- P5LP\_VDD (Pin 1)
- P5LP15\_1 SPI\_MOSI (Pin 3)
- P5LP15\_2 SPI\_SCLK (Pin 5)
- P5LP15\_3 SPI\_SSEL (Pin 7)
- P5LP12\_5 SPI\_MISO (Pin 9)
- CUSTOM P5LP3\_4 (Pin 11)
- P5LP12\_7 UART\_RX (Pin 13)
- CUSTOM P5LP3\_6 (Pin 15)

Connections (Right side):

- P5LP0\_1 CUSTOM I2C\_SCL (Pin 2)
- P5LP12\_0 CUSTOM I2C\_SDA (Pin 10)
- P5LP3\_0 CUSTOM I2C\_SDA (Pin 12)
- P5LP3\_5 CUSTOM UART\_TX (Pin 14)
- P5LP12\_6 (Pin 16)

Note: Pin 4 is marked with a red X, indicating it is not connected.

### PSoC 5LP Custom Application Header

The diagram illustrates the PSoC 5LP Custom Application Header. It features a 5x2 pin connector (J7) with 10 pins. The connections are as follows:

- Pins 1, 3, 5, 7, and 9 are connected to custom signals: P5LP0\_2, P5LP0\_3, P5LP0\_7, UART\_RTS, and P5LP15\_4 respectively.
- Pins 2, 4, 6, 8, and 10 are connected to P5LP\_VDD, P5LP\_XRES\_L, P5LP\_SWDCCLK, and P5LP\_SWDIO respectively.

The connector is labeled "CON 5x2" and "No Load".

### Supply for PSoC 5LP

The diagram illustrates the power supply circuit for the PSoC 5LP. A voltage divider is used to derive the EN pin voltage from VBUS\_TC. The divider consists of a 120K resistor (R89) in series with a parallel combination of a 75K resistor (R86) and a 0.1uF capacitor (C84) connected to ground. The output of this divider is connected to the EN pin (pin 4) of the U15 regulator. The regulator's IN pin (pin 3) is connected to VCC\_5V through a 0.1uF capacitor (C89). The regulator's OUT pin (pin 1) is connected to P5LP\_VDD. The regulator is a SIP32401ADNP.

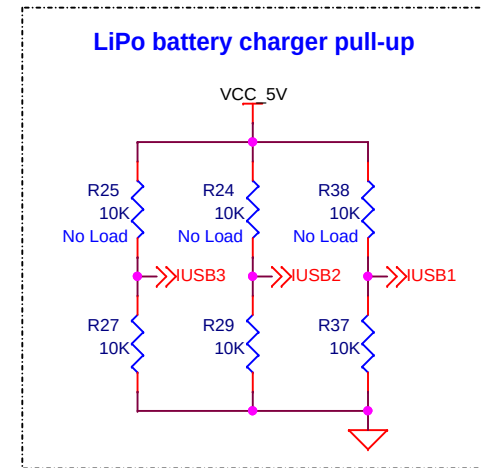
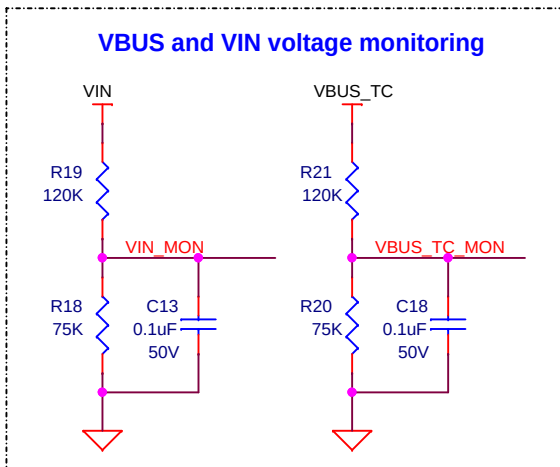
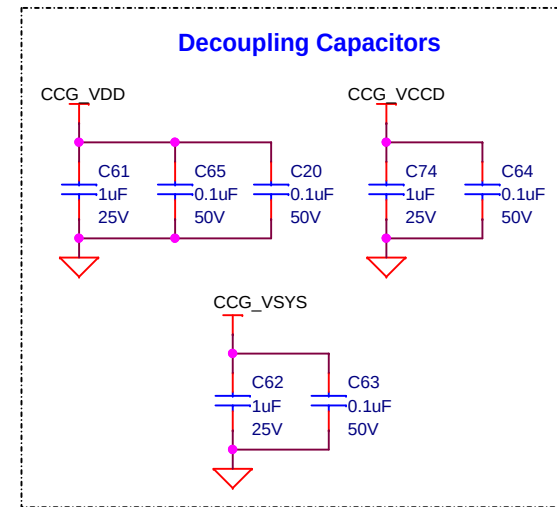
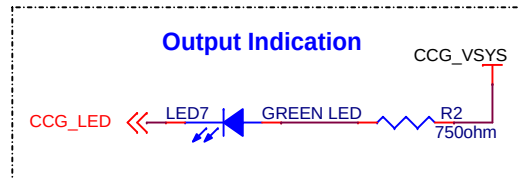
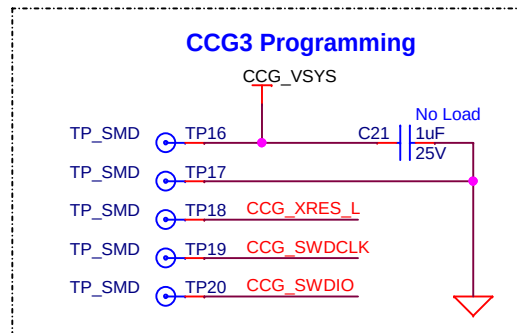
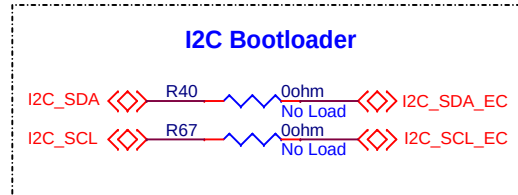
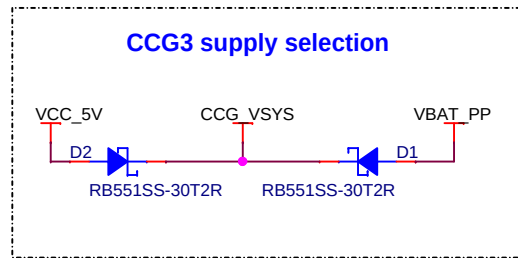
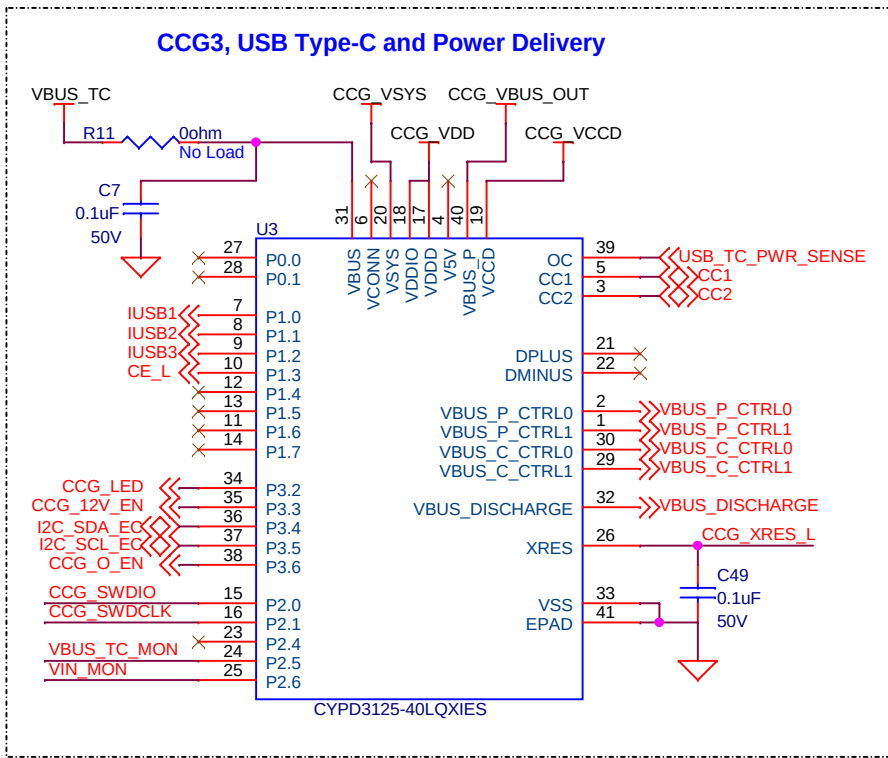


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Page Title : KitProg2 Power &amp; Headers

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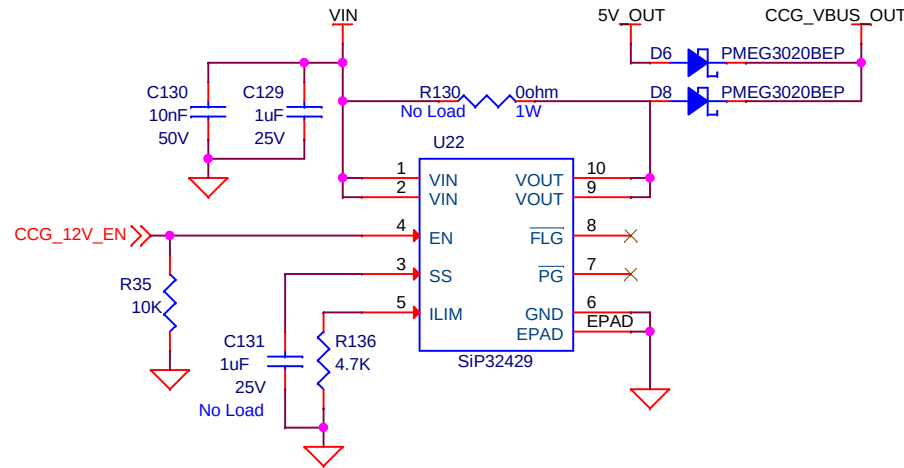


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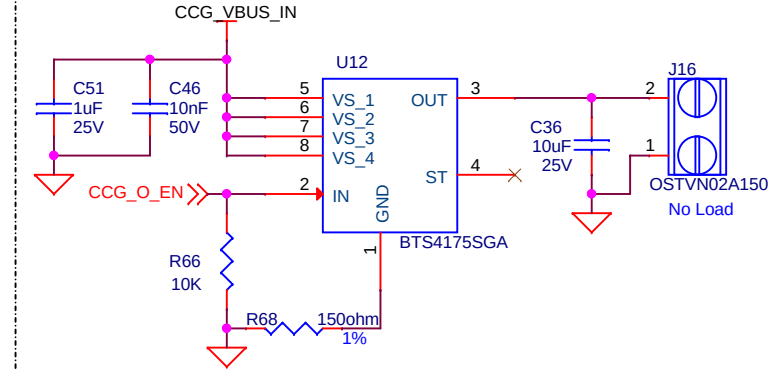
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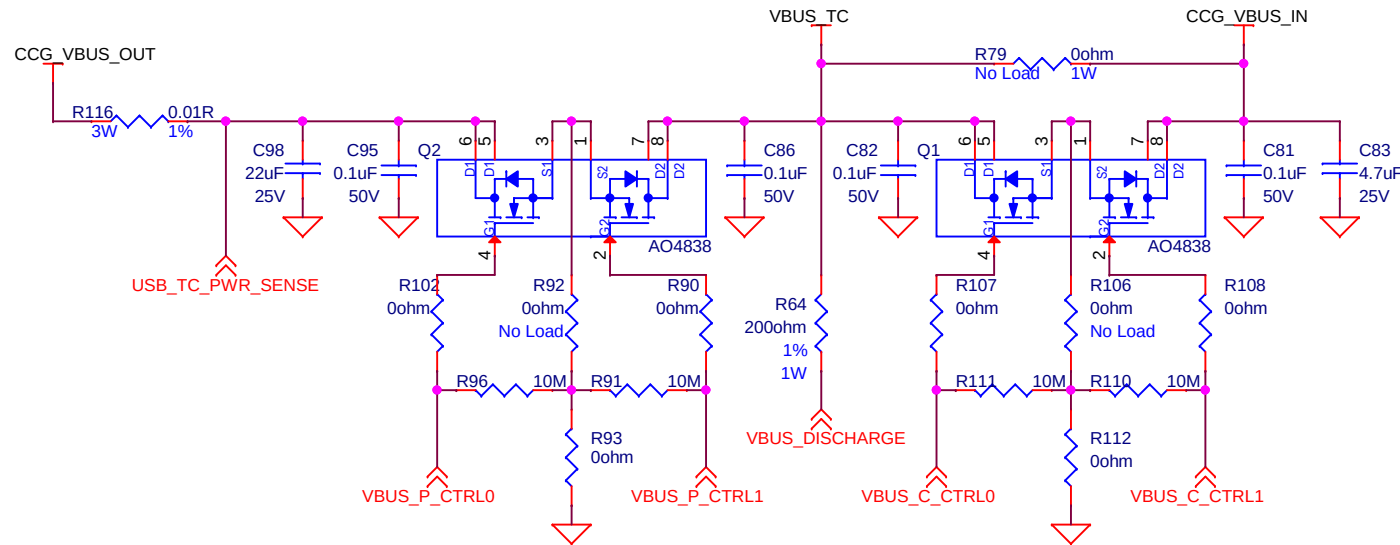
### CCG3 Provider path 'OR'ing



### CCG3 12V @1A Output



### VBUS Provider/Consumer Path



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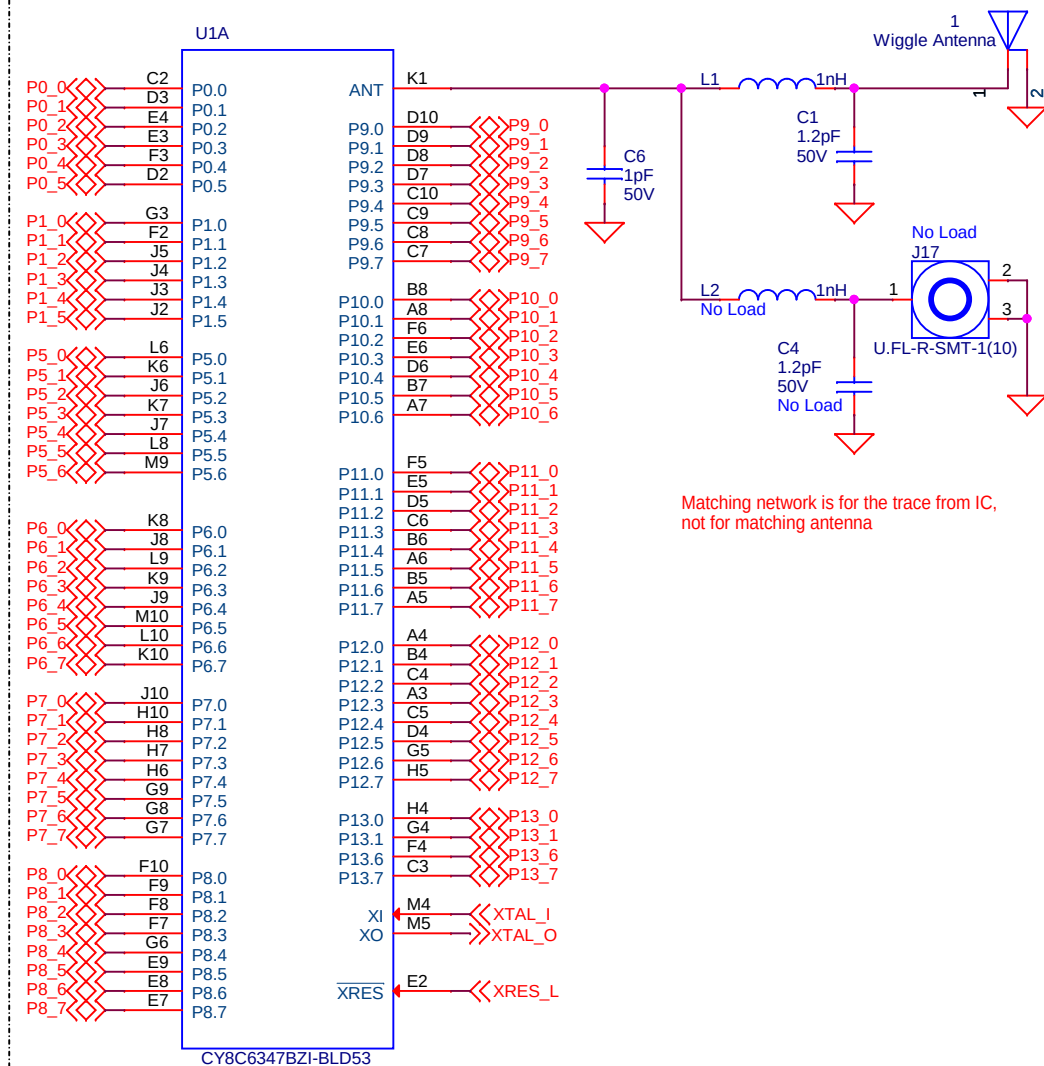
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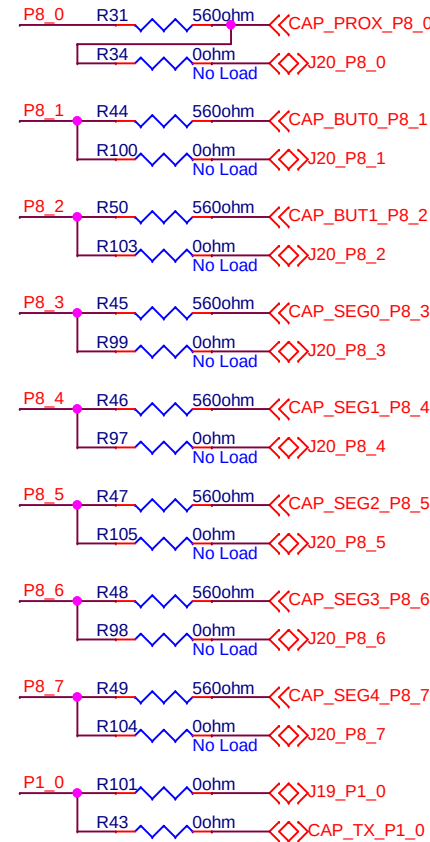




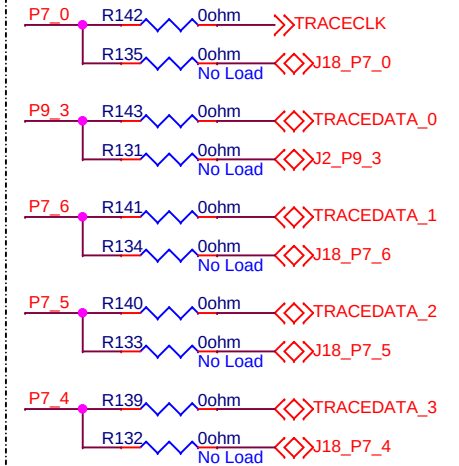
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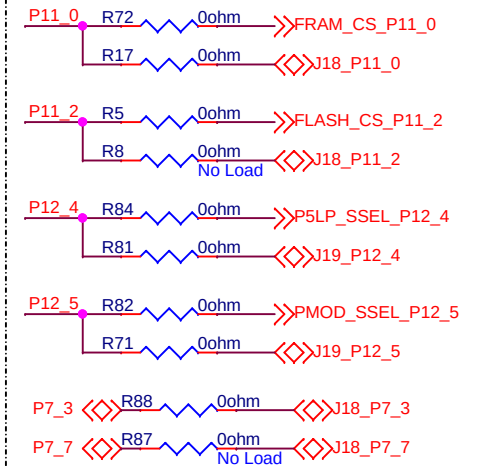
## CapSense Multiplexed pins



## TRACE Multiplexed pins



## Additional Multiplexed pins



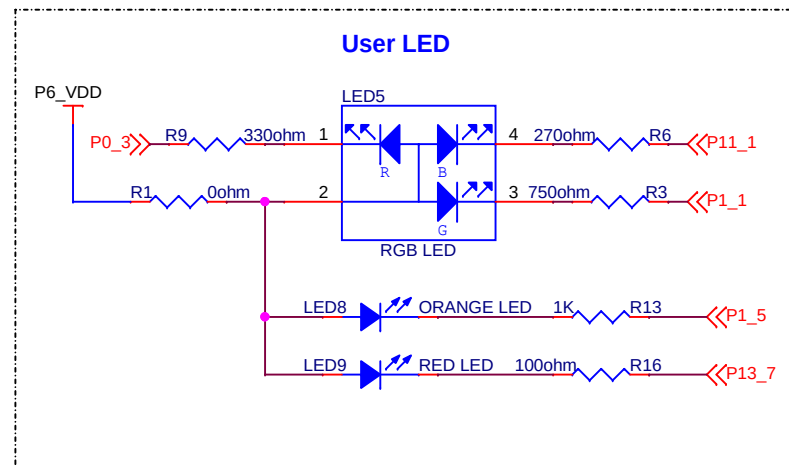
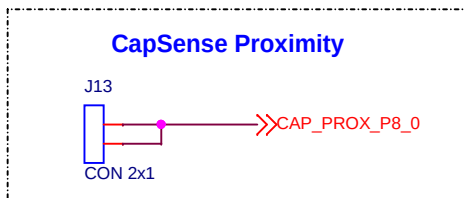
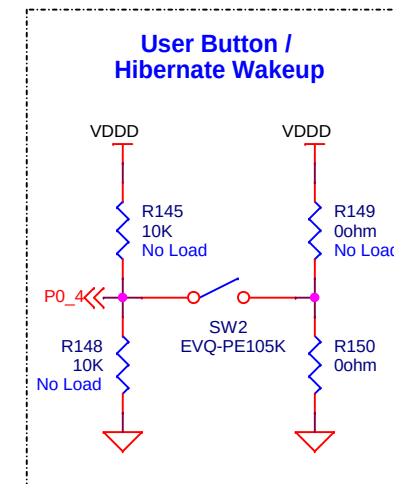
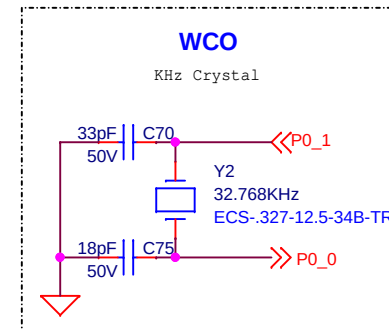
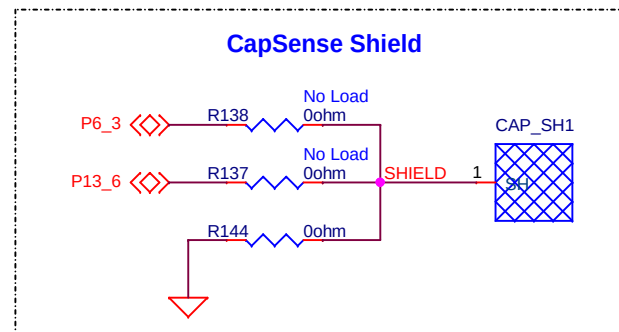
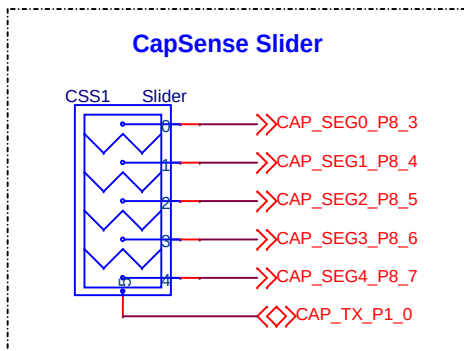
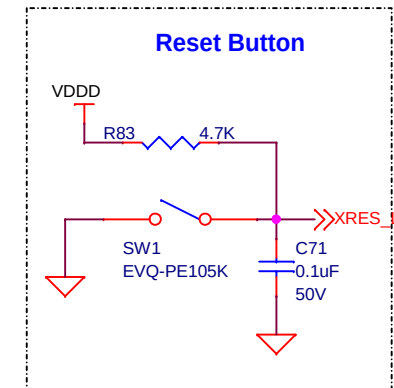
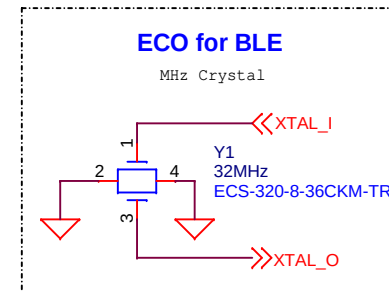
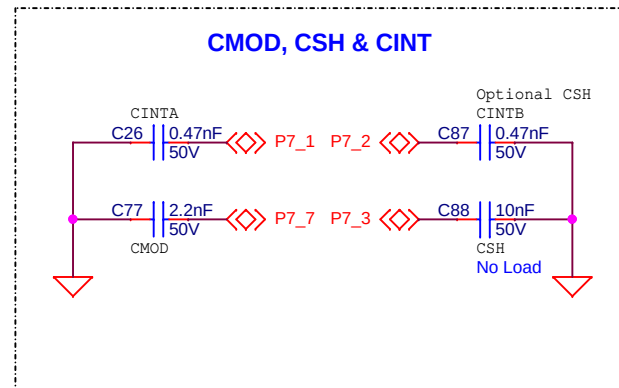
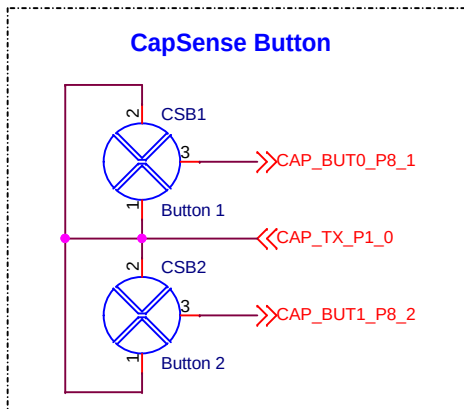
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**Page Title : PSoC 6 BLE Signals**

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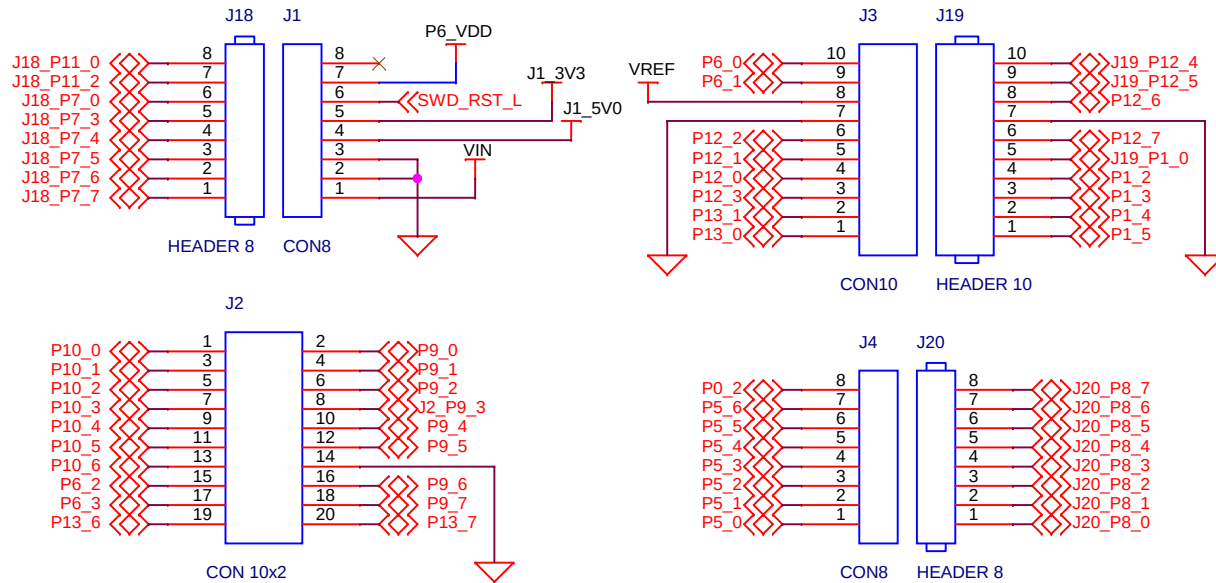
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**Page Title : On-board peripherals**

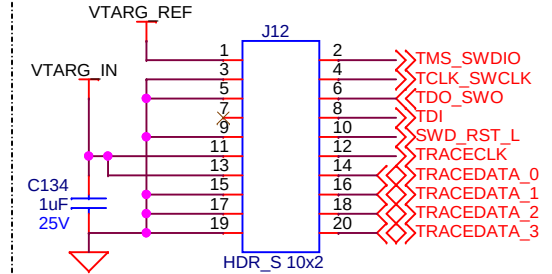
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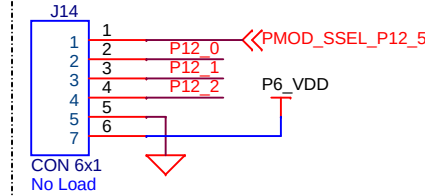
## Arduino Headers



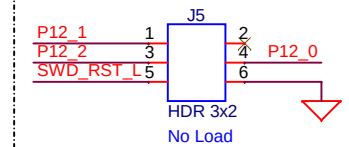
## ETM Header



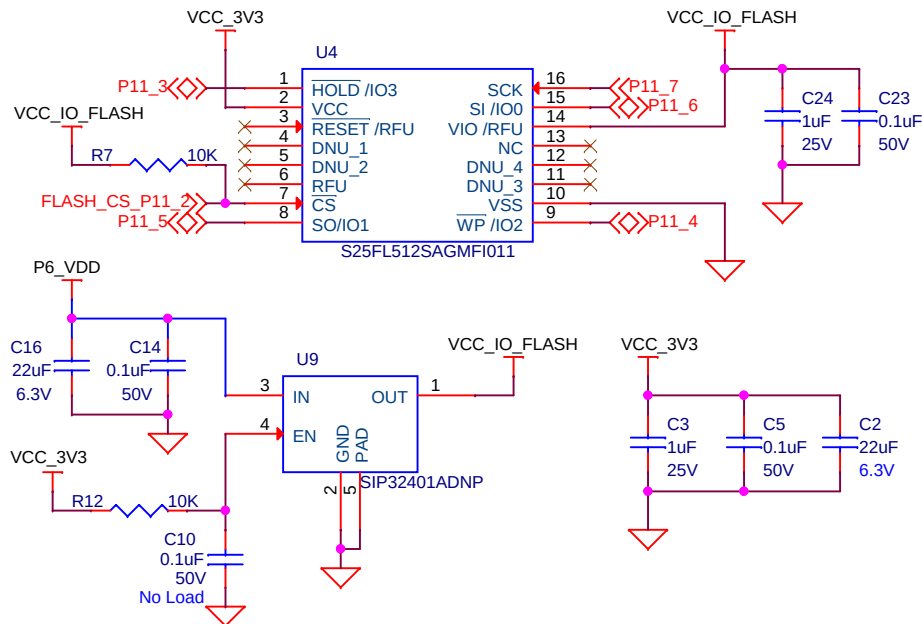
## Pmod Header



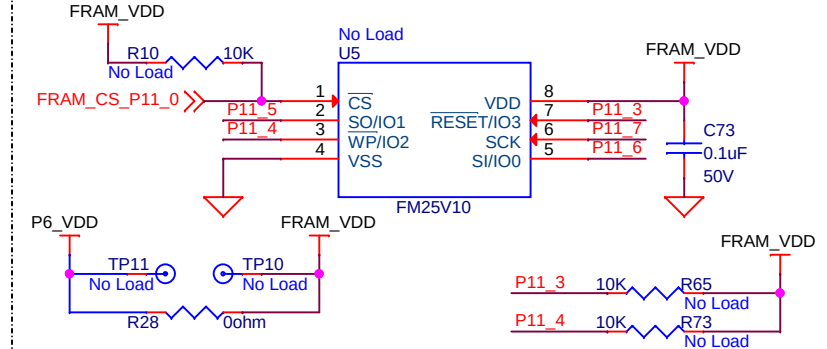
## ICSP Header



## QSPI Flash (SMIF)



## F-RAM



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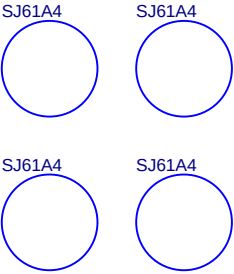
**SCH Title : CY8CKIT-062-BLE PSoC 6 BLE Pioneer Board**

**Page Title : Expansion headers & Memory**

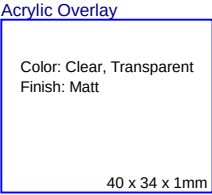
| Size  | Document Number            | Drawn By | Approved By | Rev      |
|-------|----------------------------|----------|-------------|----------|
| A4    | 630-60357-01               | RKPM     | RKAD        | 05       |
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Accessories

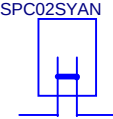
Cylindrical Bumper



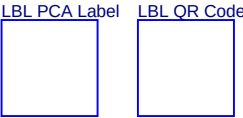
Acrylic Overlay



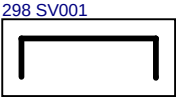
Jumper Shunt



PCBA label



USB connector bracket



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Page Title : Accessories & PCB Artwork

|            |                                        |                         |                            |                  |
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## Revision History

| Rev | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Date       |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 01  | Initial internal release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 08/29/2016 |
| 02  | Internal release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 10/03/2016 |
| 03  | Internal release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 11/25/2016 |
| 04  | Initial external release under NDA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 01/19/2017 |
| 05  | 3.3V protection diode changed to load SW (U59)<br>Added PMIC control section (U58, U56, U57 and passives)<br>Removed series resistor for SPI and UART HW flow control<br>Voltage Monitoring domain and Protection Circuit o/p changed to P6_VDD<br>Changed trace data line connection (to 9.3, 7.6, 7.5, 7.4)<br>C22 Cap on VRF changed to 10uF<br>Removed SW8 and connected CINT directly, CMOD connection changed to 7.7<br>Shield # changed to 13.6/6.3<br>Added additional LED on pin 13.7 and 1.5<br>Added option to change logic for user SW and added pull-up/down<br>Back annotated from layout | 5/2/2017   |



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Page Title : **Revision History**

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