DESCRIPTION OF MODULATION SYSTEM

SECTION 2.1033(c) (13)

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For equipment employing digital modulation techniques, a detailed description of the modulation system to be used, including response characteristics (frequency, phase and amplitude) of any filters provided, and a description of the modulating wavetrain, shall be submitted for the maximum rated conditions under which the equipment will be operated.

RESPONSE:

SRFU19 Digital Modulation Technique

Introduction

The following describes digital modulation technique used in SRFU19. All abbreviations used are described at the end of the document.

Transmit GMSK Modulator

The transmit GMSK modulator is a complete baseband digitization subsystem performing signal conversion between the digital signal processor circuits. It contains all the code necessary for performing gaussian minimum shift keying modulation.

DESIGN AND OPERATION

Figure 1 shows the functional block diagram of the integrated GSM baseband modulator.

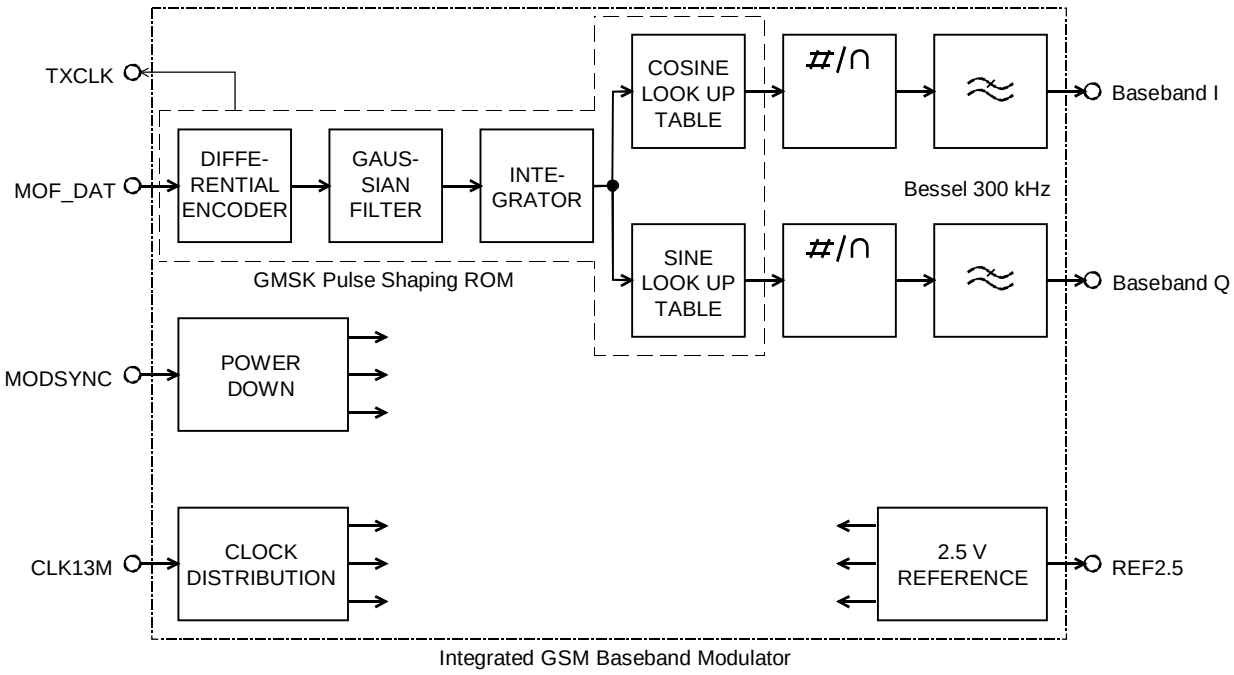


Figure 1: GMSK Modulator Block Diagram

The GMSK modulator is implemented using control logic with a ROM look-up table to generate in-phase (I) and quadrature (Q) signals oversampled at 16 times the transmitter data rate. In a GMSK pulse shaping ROM the incoming digital transmit data stream (MOF_DAT) at 270.833 kbit/s is first differentially encoded as specified by ***GSM recommendation 5.04 section 2.3.*** The encoded data stream is passed through a gaussian filter having a pulse response truncated to 4 data bits. The mathematical integration of the signal is carried out digitally before the signal is split and applied to cosine and sine look-up tables. These look-up tables generate I and Q waveforms as digital numbers in response to the encoded data.

Transmit DACs then perform the digital-to-analog conversion, while on-chip reconstruction filters smooth the DAC output signals, providing continuous time baseband I and Q waveforms. These filters are designed with a cutoff frequency of approximately 300 kHz. The filters are designed to have a linear phase response in the passband resulting in a flat passband group delay, while significantly attenuating the sampling clock frequency of 4.33 MHz and its harmonics.

Additionally, control logic in the GMSK pulse shaping ROM generates an output signal TXCLK, which is derived from the 13 MHz master clock input signal CLK13M. The transmit data MOF_DAT is clocked into the modulator on the falling edge of TXCLK. Although not actually controlling the transmitter data source in the TRXB19, TXCLK may be used to obtain information on the proper GMSK modulator timing.

The modulator can be brought into sleep mode (powering down the GMSK modulator section including the I and Q stages) by means of the input signal MODSYNC. This is used to synchronize the modulator to GSM timeslots.

A precise 2.5 V bandgap reference feeds the transmit DACs and reconstruction filters and is made available as a buffered output REF2.5 as well. REF2.5 later on biases the transmitter I/Q filter and the I/Q modulator.

Synchronization of GMSK Modulator

The fix relationship between transmitter data stream MOF_DAT and TGUPE allows the generation of a modulator synchronization pulse MODSYNC that occurs at a predefined time before the end of TGUPE

When MODSYNC is asserted, the modulator is immediately put into sleep mode, disabling TXCLK and powering down the pulse shaping ROM and I/Q stages, with I and Q outputs connected to the internal reference voltage source. When MODSYNC is brought low again, TXCLK becomes active and clocks in a data symbol 48 CLK13M clock cycles (one GSM symbol duration) after MODSYNC has gone low.

Optionally, a basestation may use a timeslot length of 157 symbol periods on timeslots 0 and 4, and 156 symbol periods on timeslots 1, 2, 3, 5, 6, 7, rather than 156.25 symbol periods on all timeslots [16]. The synchronization circuit, as depicted in Figure 1.1, is capable of handling both modes, depending on whether TXCLK is asserted to the synchronization circuit or not.

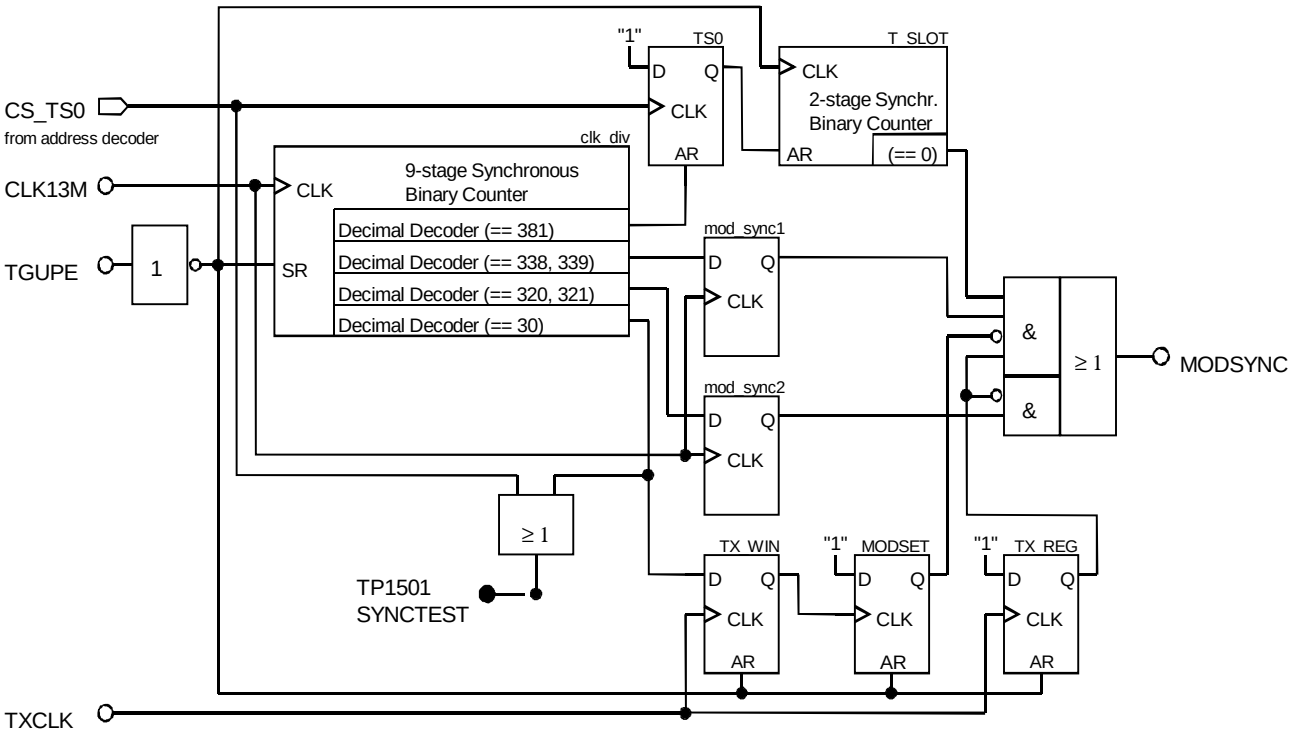


Figure 1.1: Equivalent Synchronization Circuit Diagram

If, as selected by default hardware assembly, TXCLK is not asserted to the synchronization circuit, a MODSYNC pulse is generated for each timeslot. This is achieved by enabling a certain decoded and latched state (register mod_sync2 in Figure 1.1) of a 9-stage counter to be switched through as MODSYNC output signal. The counter is clocked by CLK13M when TGUPE is logical high. In Figure 2, the corresponding timing diagram for this permanent GMSK modulator synchronization is shown. The synchronization is carried out regardless of a write access to address CS_TS0 in the RCS Bus Slave Interface.

Synchronizing the GMSK modulator on all timeslots results in a rapid phase change of at least $^{1}/_{16}$ of an I/Q vector rotation or 22.5° with additional amplitude spikes on the analog I and Q signals in each timeslot, which fall within the passband and cannot be filtered out completely. This causes unwanted spurious signals in the up-ramping transmit power slope, and the MODSYNC pulse width has to be kept short to keep down additional transient energy from increased phase changes at the analog I and Q outputs during synchronization.

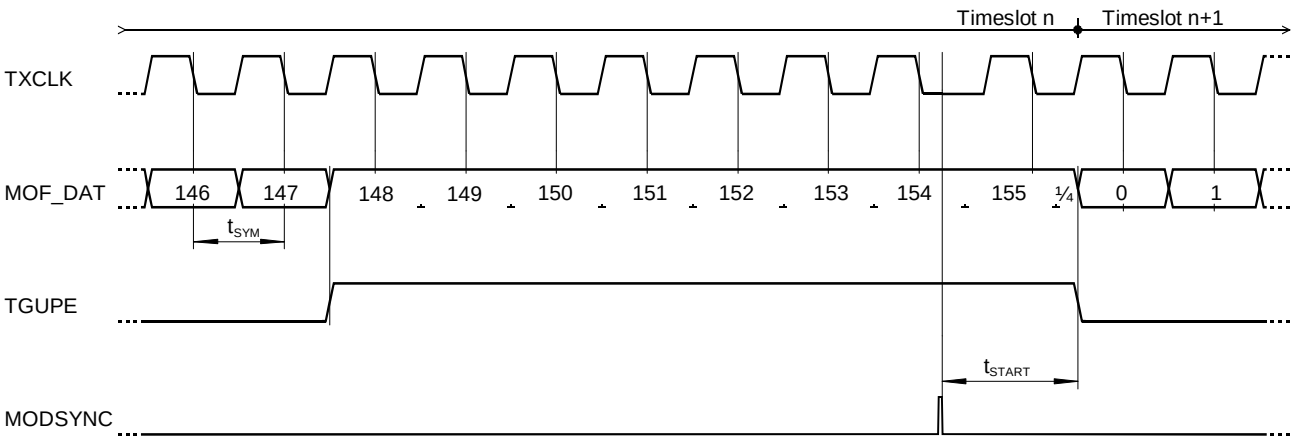


Figure 2: Permanent Synchronization Timing Diagram. TXCLK as shown, is the signal that can be seen at the output of the GMSK modulator. Since in this mode it is not fed to the synchronization circuit, the input of the synchronization circuit will be at a constant logic level.

A novel automatic synchronization circuit has been proposed to overcome this disadvantage. Since no periodic synchronization is needed in case the TRXB19 uses one timeslot of length 157 symbol periods followed by three timeslots of length 156 symbol periods, spurious signals due to GMSK modulator synchronization can be totally avoided. However, the correct timing for this mode must be achieved initially, see Figure 2.1.

It is mandatory that the GMSK modulator is synchronized to the GSM frame structure. Controlled by a 2-stage counter, GMSK modulator synchronization is enabled and can be carried out only in timeslot 0 or timeslot 4 after having received the write access in timeslot 0. The write access to address CS_TS0 in timeslot 0 shall take place while TGUPE is logical low.

After powering-up the TRXB19 and before synchronizing the GMSK modulator the signals TGUPE and TXCLK may be of arbitrary phase to each other. This is due to different clock sources on TRXB19 and RCEB that are not locked during power-up. However, in timeslot 0 and timeslot 4 the rising edge of TXCLK has to lie at $+^{5}/_{8}$ of a symbol duration with respect to the rising edge of TGUPE.

To obtain this correct timing, TXCLK from the GMSK modulator is asserted to the synchronization circuit. In timeslot 0 and timeslot 4 the rising edge of TXCLX is compared with a fixed timing window representing the $+^{5}/_{8}$ position (register TX_WIN in Figure 1.1). If the rising edge of TXCLK is not falling within the window, the GMSK modulator synchronization is carried out. If the edge falls within the window, the GMSK modulator has reached the desired timing and no further synchronization pulse will be switched through.

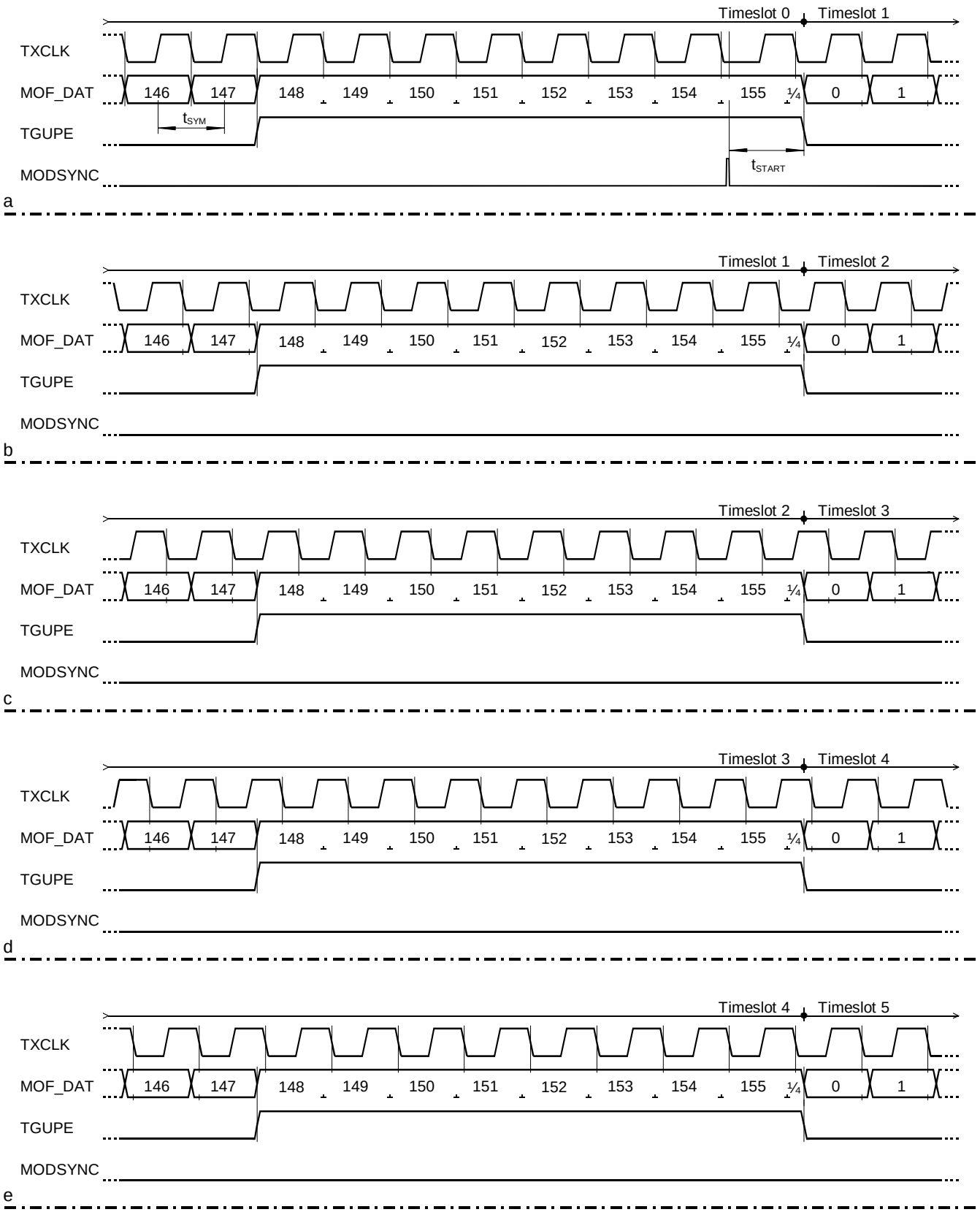
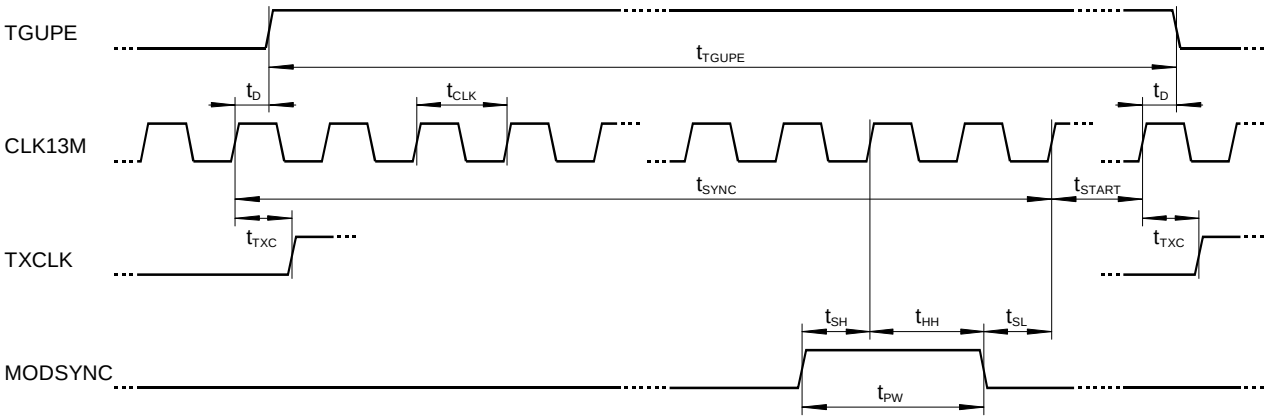

Timeslot 0
Timeslot 1
TXCLK
MOF_DAT
146
147
148
149
150
151
152
153
154
155
¼
0
1
t_{SYM}
TGUPE
t_{START}
MODSYNC
a
Timeslot 1
Timeslot 2
b
Timeslot 2
Timeslot 3
c
Timeslot 3
Timeslot 4
d
Timeslot 4
Timeslot 5
e

Figure 2.1: Automatic Synchronization Timing Diagram. a) The timing of TXCLK is arbitrarily wrong in timeslot 0. As an example, MOF_DAT is read in at data crossover points, potentially leading to bit errors. In symbol no. 155, MODSYNC is generated to force the correct modulator timing. b)...e) Once the correct timing is achieved, MODSYNC will be suppressed, as shown here in five consecutive timeslots. The instants of clocking data into the modulator are shifted from timeslot to timeslot by a quarter symbol duration. Note that symbol no. 155 in timeslot 4 (and in timeslot 0 the next frame) is read twice.



Transmit I/Q Filter and Modulator

The transmit I/Q modulator converts the baseband data from analog I and Q signals to a continuos-phase frequency modulated RF carrier at an intermediate frequency.

DESIGN AND OPERATION

The analog I and Q baseband signals coming from the GMSK modulator are buffered and post-filtered before being applied to the I/Q vector modulator (Figure 3). The post-filters are Bessel-type 3rd order passive lowpass filters with a cutoff frequency of 335 kHz. They are designed to further reject the I/Q sampling frequency 4.33 MHz while exhibiting minimum group delay distortion in the passband.

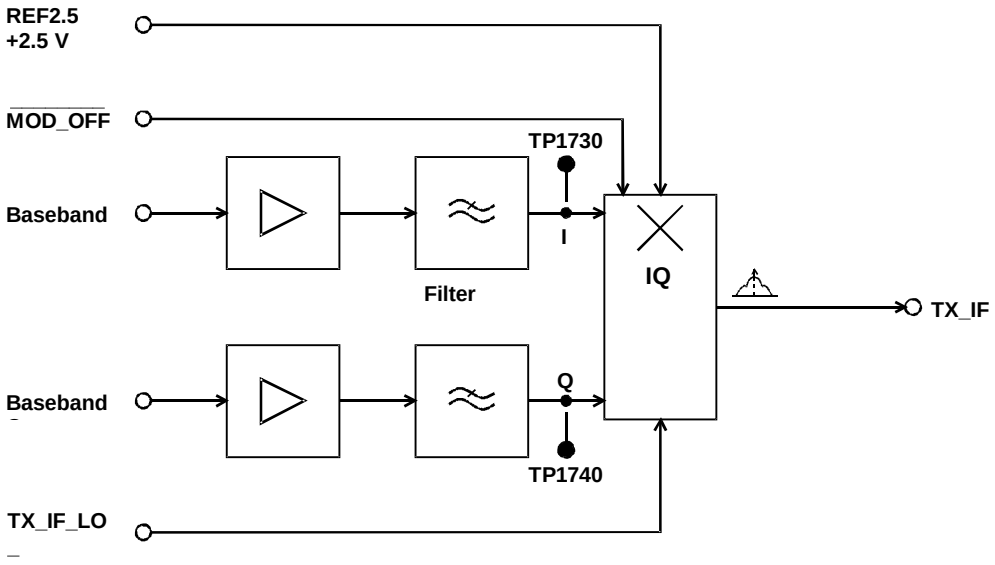


Figure 3: I/Q Filter and Modulator Block Diagram

Signal processing in the I and Q path has to maintain the static and the dynamic amplitude and phase relationship as well as a DC offset highly accurate to meet the requirement for carrier and sideband rejection, which is related to the phase error ratings specified in ***GSM recommendation 05.05.***

I/Q vector modulation is performed in an integrated active quadrature modulator. The circuit contains the in-phase and quadrature phase mixer cells and has an on-chip 0°/90° phase shifter for the local oscillator. The accurate phase shifting is achieved by a duty cycle regenerator followed by a frequency doubler and a 90° phase control loop. To form a continuos-phase frequency modulated signal the outputs of the mixer cells are summed-up and buffered on-chip. The active quadrature modulator has a power-down option that can be activated via the signal /MOD_OFF.

Carrier Rejection

Adjustment of carrier rejection is not required. To measure carrier rejection observing the IF signal with a spectrum analyzer is recommended. The transmit data, MOF_DAT, have to be all ones or all zeros or, alternatively, a 1-0-1-0 pattern. The two first produce a single-sideband spectrum appearing like a single frequency on the upper sideband at a carrier frequency offset of +67.7 kHz, while the latter produces a signal at -67.7 kHz carrier frequency offset.

The transmitter guard period signal TGUPE shall be held low during measurement to avoid a superimposed switching spectrum caused by the permanent GMSK modulator synchronization. This would not be

necessary once the auto-synchronization is enabled, since there is no superimposed switching spectrum after the correct timing has been achieved.

Sideband Rejection

Adjustment of sideband rejection is not required. Measurement of sideband rejection is similar to measurement of carrier rejection as described above.

Glossary of Terms & Abbreviations

ABBD	Advanced Baseband Digitizer
ASIC	Application Specific Integrated Circuit
BBD	Baseband Digitizer
BDF	Baseband Digitizer Function
CBA	Cluster Bus ASIC
ECIF	Electronic Calibration Information
EEPROM	Electrically Erasable Programmable Read Only Memory
EPLD	Electrically Programmable Logic Device
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communication
GUPE	Guard Period
IF	Intermediate Frequency
LO	Local Oscillator
MMIC	Monolithic Microwave Integrated Circuit
MUX	Multiplexer
OOL	Out-of-Lock
PLL	Phase-Locked Loop
PSU	Power Supply Unit
RCEB	Radio Control and Equalizer Board
RCF	Radio Controller Function
RCS	Radio Control & Status
ROM	Read Only Memory
SAW	Surface Acoustic Wave
SRFU	Standard Radio Frequency Unit
SRMB	SRFU Mother Board
SSB	Single-Sideband
TRXB	Transmit / Receive Board
TX	Transmitter
TXAM	Transmit Power Amplifier Module
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator

External to SRFU19 there is a cavity type Transmit filter which limit spurious and harmonic content. The performance characteristic of these filters is included in the following page.

Transmit Path Filter Characteristics (J4 Terminal)