SC680A&SC686A Series

Hardware Design

Smart Module Series

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At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-09-09	Rorschach GUO/Xiong XIAO	Creation of the document
0.1	2022-12-28	Rorschach GUO/Xiong XIAO	

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1 Introduction

This document defines SC680A and SC686A series module and describes its air interface and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-- Reorient or relocate the receiving antenna.
-- Increase the separation between the equipment and receiver.
-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna shall not be less than 20cm (8 inches) during normal operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Notice to OEM integrators
1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel Wireless Solutions Co., Ltd that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2022SC680AWF”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4) The max allowed antenna gain is 0.47dBi for WiFi 2.4G , 1.28 dBi for WiFi 5G Folded dipole antenna.

SC680A-NA / SC686A-NA ： PCB Antenna		
Band	Frequency (MHz)	Gain（dBi）
LTE–FDD B2	1850~1910	1.59
LTE–FDD B4	1710~1755	2
LTE–FDD B5	824~849	2.53
LTE–FDD B7	2500~2570	3
LTE–FDD B12	699~716	3.95
LTE–FDD B13	777~787	4.45
LTE–FDD B14	788~798	4.45
LTE–FDD B17	704~716	3.95
LTE–FDD B25	1850~1915	1.59
LTE–FDD B26	814~849	3.19
LTE–FDD B66	1710~1780	2
LTE–FDD B71	663~698	1.32
LTE–TDD B41	2496~2690	3.6

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.
Manual Information to the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement:
This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)
1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:
In the event that these conditions can not be met (for example certain laptop configurations or co- location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:
Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-22SC680AWF”.

Plaque signalétique du produit final
Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-22SC680AWF ".

Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final
L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.
RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or

operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.
Caution:

i) The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
ii) where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Avertissement:

i) Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
ii) lorsqu'il y a lieu, les types d'antennes (s'il y en a plusieurs), les numéros de modèle de l'antenne et les pires angles d'inclinaison nécessaires pour rester conforme à l'exigence de la
p.i.r.e. applicable au masque d'élévation, énoncée à la section 6.2.2.3, doivent être clairement indiqués.
i. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit
ii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits as appropriate; and
iii. where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

The module is a series of Smart LTE modules based on Android and Linux operating system, and provides industrial grade performance. It supports multiple audio and video codecs, built-in high performance Adreno™ GPU 610 graphics processing unit and multiple audio and video input/output interfaces as well as abundant GPIO interfaces. With these, the module is engineered to meet the demanding requirements in M2M applications, such as POS, on-board computers, multimedia terminals, smart home products, IoT terminals, etc. Its general features are listed below:

Table 2: Brief Introduction of the Module

SC680A & SC686A Series	
Packaging and pins number	152 LCC + 171 LGA
Dimensions (mm)	(43.0 ±0.15) × (44.0 ±0.15) × (2.85 ±0.2)
Weight	11.8 g
Wireless network functions	SC680A-NA & SC686A-NA: LTE SC680A-EM & SC686A-EM: GSM/LTE/WCDMA
Wi-Fi & Bluetooth functions	Wi-Fi a/b/g/n/ac/Bluetooth 5.1
GNSS functions	GPS/GLONASS/BDS/Galileo/NavIC/QZSS L1+L5
Variants	SC680A-NA/-EM/-WF SC686A-NA/-EM/-WF

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	SC680A-NA & SC686A-NA	SC680A-EM & SC686A-EM	SC680A-WF & SC686A-WF
LTE-FDD	B2/B4/B5/B7/B12 /B13/B14/B17/B25 /B26/B66/B71	B1/B2/B3/B4/B5/B7 /B8/B20/B28	-
LTE-TDD	B41	B38/B40/B41	-
Intra-band 2 x CA (DL)	CA_2A-2A, CA_2C, CA_4A-4A, CA_5A-5A, CA_5B, CA_7A-7A, CA_7C, CA_25A-25A, CA_66A-66A, CA_66B, CA_66C, CA_41A-41A, CA_41C	CA_1A-1A, CA_1C, CA_2A-2A, CA_2C, CA_3A-3A, CA_3C, CA_4A-4A, CA_5A-5A, CA_5B, CA_7A-7A, CA_7B, CA_7C, CA_38C, CA_40A-40A, CA_40C, CA_41A-41A, CA_41C	
WCDMA	-	B1/B2/B4/B5/B8	-
GSM	-	GSM850/EGSM900/ DCS1800/PCS1900	-
GNSS	GPS/GLONASS/ BDS/Galileo/NavIC/QZSS	GPS/GLONASS/ BDS/Galileo/NavIC/QZSS	-
Wi-Fi 802.11 a/b/g/n/ac	2412–2462 MHz 5180–5825 MHz	2412–2462 MHz 5180–5825 MHz	2412–2462 MHz 5180–5825 MHz
Bluetooth	2402–2480 MHz	2402–2480 MHz	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Features	Details
Application Processors	● 64-bit ARM v8.0 compliant applications processor ● Quad high-performance Kryo cores 2.0 GHz – Gold cluster with 1 MB L2 cache

	● Quad low-power Kryo cores 1.8 GHz – Silver cluster with 512 KB L2 cache
Modem DSP	Hexagon DSP, dual-HVX at 1.0 GHz
GPU	Adreno™ GPU 610 at 950 MHz, 3D graphics accelerator with 64-bit addressing
Memory	SC680A Series: ● 32 GB eMMC + 3 GB LPDDR4X (default) ● 64 GB eMMC + 4 GB LPDDR4X (optional) SC686A Series: ● 32 GB eMMC + 3 GB LPDDR4X (default) ● 64 GB eMMC + 4 GB LPDDR4X (optional)
Operating System	SC680A series: Android 12/13*/14* SC686A series: Linux
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
LCM Interface	● Supports 1 group of 4-lane MIPI_DSI, up to 1.5 Gbps/lane ● Supports FHD+ (1080 × 2520) @ 60 fps.
Camera Interfaces	● Support 3 groups of 4-lane MIPI_CSI, up to 2.5 Gbps/lane ● Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) ● Up to 3 × ISP: (13 MP + 13 MP) @ 30 fps, (25 MP + 5 MP) @ 30 fps or (16 MP + 16 MP) @ 24 fps
Video Codec	● Video encode: 1080p @ 60 fps 8-bit HEVC (H.265); 1080p @ 60 fps 8-bit H.264 ● Video decode: 1080p @ 60 fps 8-bit H.264; 1080p @ 60 fps 8-bit HEVC (H.265), VP9 ● Encoding + decoding: 1080p @ 30 fps decode + 1080p @ 30 fps encode
Analog Audio Interfaces	**Audio Inputs** 3 analog microphone inputs, integrated with MIC1 and MIC2 internal bias voltage **Audio Outputs** ● Class AB stereo headphone output ● Class AB earpiece differential output ● Class K speaker differential amplifier output
Audio Codec	● EVS, EVRC, EVRC-B, EVRC-WB ● G.711 and G.729A/AB ● GSM-FR, GSM-EFR, and GSM-HR ● AMR-NB, AMR-WB

(U)SIM Interfaces	● Two (U)SIM interfaces ● Support USIM/SIM card: 1.8/2.95 V ● Support Dual SIM Dual Standby (supported by default)
UART Interfaces [1]	Support up to four groups of UART interfaces. Two of them are default configurations and two of them can be multiplexed from other interfaces ● Default UART interfaces: UART5 and Debug UART – UART5: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 115200 bps – Debug UART: 2-wire UART interface, used for debugging, Linux console and log output, up to 115200 bps ● For details about two UART interfaces that can be multiplexed form other interfaces, see ***Table 18***
SPI	Supports up to three groups of SPI interfaces. One of them is default configuration and two of them can be multiplexed from other interfaces ● The default SPI supports master mode only ● For details about two SPI that can be multiplexed from other interfaces, see ***Table 18*** ● Dedicated to one-to-one connection, without chip selection ● 1.8 V operation voltage with clock rates up to 50 MHz
I2S Interface	Supports up to two groups of I2S interfaces ● Two I2S interfaces can be multiplexed from other interfaces, see ***Table 19***
I2C Interface	Supports up to seven groups of I2C interfaces ● Four of them are dedicated I2C interfaces, used for camera, TP and sensor peripherals ● One of them is generic I2C interface ● For details about two I2C interfaces that can be multiplexed from other interfaces, see ***Table 18*** ● Comply with I2C-bus specification version 3.0 ● Multi-master mode is not supported
ADC Interfaces	2 generic ADC interfaces
Real Time Clock	Supported
USB Interface	● Compliant with USB 3.1 Gen 1 and USB 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● Supports USB OTG ● Used for AT command communication, data transmission, software debugging, firmware upgrade.
SD Card Interface	● Supports SD 3.0 protocol

[1] For details about the multiplexing and conflict relationships of UART, I2C and SPI interfaces, see ***Table 18***

	● Supports SD card hot-plug ● Supports 1.8/2.95 V SD card
Bluetooth Features	Bluetooth 5.1
GNSS Features	GPS/GLONASS/BDS/Galileo/NavIC/QZSS L1 + L5
Antenna Interfaces	● ANT_MAIN ● ANT_DRX ● ANT_WIFI/BT ● ANT_GNSS ● 50 Ω impedance
LTE Features	● Supports Rel-10 Cat 6 for FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports Multiuser MIMO in DL direction ● Uplink modulations: QPSK, 16QAM ● Downlink modulations: QPSK, 16QAM, 64QAM and 256QAM ● FDD max. data rate: 300 Mbps (DL)/50 Mbps (UL) ● TDD max. Data rate: 265 Mbps (DL)/30 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-9 DC-HSDPA/HSPA+/HSDPA/HSUPA/ WCDMA ● Supports QPSK, 16QAM, 64QAM modulation ● DC-HSDPA max. data rate: 42 Mbps (DL) ● HSUPA max. data rate: 5.72 Mbps (UL) ● WCDMA max. data rate: 384 kbps (DL)/384 kbps (UL)
GSM Features	**R99:** ● CSD transmit speed rate: 9.6 kbps, 14.4 kbps **GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. data rate 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. data rate: 296 kbps (DL)/236.8 kbps (UL)
WLAN Features	● 2.4 GHz and 5 GHz, supports 802.11 a/b/g/n/ac, maximally up to 433 Mbps ● Supports STA modes
Temperature Range	● Operating temperature range [2]: -35 to +75 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Use USB interface or OTA to upgrade

[2] Within the operating temperature range, the module meets 3GPP specifications.

RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PU	Pull Up
PD	Pull Down

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 3.0 A. It is suggested to use a TVS

					to increase voltage surge withstand capability.
LDO9A_1V8	9	PO	1.8 V output (1.8 V output power for external GPIO's pull up circuits and level-shifting circuit.)	Vnom = 1.8 V $I_O$max = 20 mA	Cannot be used for peripheral power supply. No external capacitor is required.
ELDO3_1V8	10	PO	1.8 V output (1.8 V output power for I/O VDD of cameras, LCDs and sensors.)	Vnom = 1.8 V $I_O$max = 300 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open. The maximum external capacitance must not exceed 9 μF.
ELDO1_2V8	11	PO	2.8 V output (2.8 V output power for VDD of sensors and TPs.)	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open. The maximum external capacitance must not exceed 9 μF.
ELDO2_2V85	12	PO	2.85 V output (2.85 V output power for cameras and LCDs.)	Vnom = 2.85 V $I_O$max = 300 mA	Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open. The maximum external capacitance must not exceed 9 μF.
LDO2C_1V1	13	PO	1.1 V output (1.1 V output power for DVDD of rear camera.)	Vnom = 1.1 V $I_O$max = 800 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open. The maximum external capacitance must not exceed 15.3 μF.
LDO3C_2V8	14	PO	2.8 V output (2.8 V output power for AVDD of camera.)	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open. The maximum external capacitance must not exceed 47.8 μF.
LDO1C_1V2	15	PO	1.2 V output (1.2 V output power for DVDD of front camera.)	Vnom = 1.2 V $I_O$max = 800 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open. The maximum external

					capacitance must not exceed 15.3 µF.
VPH_PWR	220, 221	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 1000 mA	It can provide a maximum continuous current of 1 A.
VRTC	16	PIO	Power supply for RTC	Vmin = 2.0 V Vnom = 3.0 V Vmax = 3.25 V	
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 154, 157, 159, 160, 163, 166, 170, 173, 176, 182, 193, 195, 219, 225, 243, 257–323				Ground
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	AO	Bias voltage output for microphone	Vmin = 1.0 V Vmax = 2.85 V	
MIC1_P	44	AI	Microphone input for channel 1 (+)		Internally integrated hardware bias.
MIC1_M	45	AI	Microphone input for channel 1 (-)		
MIC_GND	168		Microphone reference ground		If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone input for headset (+)		Internally integrated hardware bias.
MIC3_P	169	AI	Microphone input for channel 2 (+)		No internal hardware bias is integrated.
EAR_P	53	AO	Earpiece output (+)		
EAR_M	52	AO	Earpiece output (-)		
SPK_P	55	AO	Speaker output (+)		
SPK_M	54	AO	Speaker output (-)		
HPH_R	51	AO	Headphone right channel output		

HPH_L	49	AO	Headphone left channel output		
HPH_GND	50		Headphone reference ground		It should be connected to main GND.
HS_DET	48	AI	Headset hot-plug detect		Pulled up internally.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	41, 42	AI	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	Vmax = 10.0 V Vmin = 4.0 V Vnom = 5.0 V	
USB_DM	33	AIO	USB differential data (-)		90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	32	AIO	USB differential data (+)		
USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)		90 Ω differential impedance. USB 3.1 Gen1 standard compliant.
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)		
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)		
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)		
USB_SS2_RX_P	156	AI	USB 3.1 Channel 2 super-speed receive (+)		
USB_SS2_RX_M	155	AI	USB 3.1 Channel 2		

			super-speed receive (-)		
USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)		
USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)		
UUSB_TYPEC	217	AI	uUSB & USB Type-C configuration		If Micro USB is intended to be used, this pin should be connected to ground via a 1 kΩ resistor. If Type-C is intended to be used, this pin should be left open.
USB_CC1	224	AI	USB Type-C detect 1		
USB_CC2	223	AI	USB Type-C detect 2		
USB_SS_SEL	226	DO	USB Type-C switch control		
SS_DIR_IN	212	DI	CC status detect	1.8 V	When using USB Type-C, connect the pin to SS_DIR_OUT. When using Micro USB, connect it to ground with a 7.32 kΩ resistor.
SS_DIR_OUT	213	AO	CC status output		When using USB Type-C, connect the pin to SS_DIR_IN. When using Micro USB, leave this pin open.
USB_ID	30	AI	USB ID detect		High level by default.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	141	PO	(U)SIM1 card power supply	1.8/2.95 V	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external capacitor cannot exceed 2.2 μF.

USIM1_DATA	142	DIO	(U)SIM1 card data		Internally pull up to USIM1_VDD with 20 kΩ resistor.
USIM1_CLK	143	DO	(U)SIM1 card clock		
USIM1_RST	144	DO	(U)SIM1 card reset		
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	1.8 V	Active low. Require externally pull up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply	1.8/2.95 V	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external capacitor cannot exceed 2.2 μF.
USIM2_DATA	209	DIO	(U)SIM2 card data		Internally pull up to USIM2_VDD with 20 kΩ resistor.
USIM2_CLK	208	DO	(U)SIM2 card clock		
USIM2_RST	207	DO	(U)SIM2 card reset		
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect	1.8 V	Active low. Require external pull-up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	SD card clock	1.8/2.95 V	50 Ω impedance.
SD_CMD	69	DIO	SD card command		
SD_DATA0	68	DIO	SDIO data bit 0		
SD_DATA1	67	DIO	SDIO data bit 1		

SD_DATA2	66	DIO	SDIO data bit 2		
SD_DATA3	65	DIO	SDIO data bit 3		
SD_DET	64	DI	SD card hot-plug detect		Active low.
SD_VDD	63	PO	SD card power supply	Vnom =1.8/2.95 V $I_O$max = 800 mA	No external capacitor is required.
SD_PU_VDD	179	PO	1.8 /2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_O$max = 50 mA	The maximum external capacitance must not exceed 2.2 μF.
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	138	DO	TP reset	1.8 V	
TP_INT	139	DI	TP interrupt		
TP_I2C_SCL	140	OD	TP I2C clock		TP I2C requires external pull-up circuit.
TP_I2C_SDA	206	OD	TP I2C data		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_BL_A	21	PO	Current output for LCD backlight	$V_O$max = 29.5V	
LCD_BL_K1	22	AI	Current sink for LCD backlight	ILEDmax = 25mA	
LCD_BL_K2	23	AI	Current sink for LCD backlight	ILEDmax = 25mA	
LCD_BL_K3	24	AI	Current sink for LCD backlight	ILEDmax = 25mA	
LCD_BL_K4	25	AI	Current sink for LCD backlight	ILEDmax = 25mA	
PWM	152	DO	PWM output		
LCD_RST	127	DO	LCD reset	1.8 V	
LCD_TE	126	DI	LCD tearing effect		
DSI_CLK_P	115	AO	LCD MIPI clock (+)		100 Ω differential impedance.

DSI_CLK_N	116	AO	LCD MIPI clock (-)		
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)		
DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)		
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	121	AO	LCD MIPI lane 2 data (+)		
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)		100 Ω differential impedance. Used for front camera by default.
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)		
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)		
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)		100 Ω differential impedance. Used for rear

CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)		camera by default.
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)		
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)		
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)		100 Ω differential impedance. Used for depth camera by default.
CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)		
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)		
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)		
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)		
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)		
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)		
CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)		
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)		
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)		
SCAM_MCLK	100	DO	Master clock of front camera	1.8 V	
SCAM_RST	72	DO	Reset of front camera		
SCAM_PWDN	71	DO	Power down of front camera		

MCAM_MCLK	99	DO	Master clock of rear camera		
MCAM_RST	74	DO	Reset of rear camera		
MCAM_PWDN	73	DO	Power down of rear camera		
DCAM_MCLK	194	DO	Master clock of depth camera		
DCAM_RST	180	DO	Reset of depth camera		
DCAM_PWDN	181	DO	Power down of depth camera		
CAM4_MCLK	236	DO	Master clock of fourth camera		
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	1.8 V	Only used for camera interface.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras		
DCAM_I2C_SDA	197	OD	I2C data of depth camera		
DCAM_I2C_SCL	196	OD	I2C clock of depth camera		
Flash & Torch Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH1_LED	26	AO	Flash/torch driver output		Support flash and torch modes.
FLASH2_LED	162	AO	Flash/torch driver output		
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module	1.8 V	Pull up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up		If unused, keep this pin open.
VOL_DOWN	147	DI	Volume down		If unused, keep this pin open.
UART Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	5	DO	Debug UART transmit.	1.8 V	If unused, keep this pin open.
DBG_RXD	6	DI	Debug UART receive.		
UART5_TXD	199	DO	UART5 transmit	1.8 V	
UART5_RXD	198	DI	UART5 receive		
UART5_RTS	245	DO	DCE request to send signal to DTE		
UART5_CTS	246	DI	DCE clear to send signal from DTE		
Sensor I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	1.8 V	External pull-up is required for external sensors. Cannot be used for touch panel, NFC, I2C keyboard, etc. Cannot be used as generic GPIO.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor		
Sensor Interrupt Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ACCEL_INT	252	DI	Acceleration sensor interrupt	1.8 V	
ALPS_INT	253	DI	Ambient light/proximity sensor interrupt		
MAG_INT	254	DI	Geomagnetic sensor interrupt		
GYRO_INT	255	DI	Gyroscope sensor interrupt		
I2C interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

I2C1_SDA	204	OD	I2C1 serial data	1.8 V	The module's internal power chip has occupied the addresses 0x47, 0x02 and 0x36 of the I2C bus. 2.2 kΩ pull-up resistance has been integrated inside the module. Cannot be used as generic GPIO.
I2C1_SCL	205	OD	I2C1 serial clock		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	134	AI	GNSS antenna interface		50 Ω impedance.
ANT_MAIN	19	AIO	Main antenna interface		
ANT_DRX	149	AI	Diversity antenna interface		
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface		
Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_8	241	DIO	Generic RF controller	1.8 V	Only used for RF tuner control.
GRFC_9	242	DIO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI0_CS	58	DO	SPI0 chip select	1.8 V	The module supports SPI as a master only.
SPI0_CLK	59	DO	SPI0 clock		
SPI0_MOSI	60	DO	SPI0 master-out slave-in		
SPI0_MISO	61	DI	SPI0 master-in slave-out		
ADC Interfaces					
Pin Name	**Pin**	**I/O**	**Description**	**DC**	**Comment**

	No.			Characteristics	
ADC0	151	AI	General-purpose ADC interface		Maximum input voltage 1.8 V.
ADC1	153	AI	General-purpose ADC interface		
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	27	AI	Battery voltage detect (+)		Must be connected to the battery anode.
BAT_M	28	AI	Battery voltage detect (-)		Must be connected to the battery GND.
BAT_THERM	29	AI	Battery temperature detect		If used, connect it to external 47 kΩ NTC thermistor. If unused, connect it to a ground with a 47 kΩ resistor.
BAT_ID	17	AI	Battery type detect		If unused, keep this pin open.
Vibration Motor Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_P	161	PO	Vibration motor driver output control	Vmin = 1.50 V Vmax= 3.54 V	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	57	DI	Force the module into emergency download mode	1.8 V	Pull-up to 1.8 V internally. Active low.
CBL_PWR_N	240	DI	Cable power-on; initiates power on when grounded		If unused, keep this pin open.
GNSS_LNA_EN	202	DO	GNSS LNA enable control	1.8 V	For internal testing only. Cannot be used as a general GPIO. Keep this pin open.

S1A	215	S1A and S1B are connected inside the module			
S1B	216				
S2A	211	S2A and S2B are connected inside the module			
S2B	233				
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_65	247	DIO	General-purpose input/output	1.8 V	
GPIO_66	248	DIO			
GPIO_67	136	DIO			
GPIO_68	137	DIO			
GPIO_71	7	DIO			
GPIO_80	8	DIO			
GPIO_83	200	DIO			
GPIO_84	201	DIO			
GPIO_86	237	DIO			
GPIO_96	113	DIO			
GPIO_97	114	DIO			
GPIO_98	232	DIO			
GPIO_99	231	DIO			
GPIO_100	178	DIO			
GPIO_101	177	DIO			
GPIO_102	250	DIO			
GPIO_103	203	DIO			
GPIO_104	249	DIO			
GPIO_105	251	DIO			

GPIO_107	238	DIO		
GPIO_108	234	DIO		
GPIO_111	230	DIO		
GPIO_112	229	DIO		

Reserved pin	
Pin Name	**Pin No.**
RESERVED	1, 2, 102–111, 158, 214, 218, 222, 227, 228, 235, 239, 244

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to the ground network.

2.4. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (Smart EVB G2) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides three VBAT pins, two VPH_PWR pins. VBAT pins must be connected to an external power supply to supply power to the module. VPH_PWR pins are used to power other devices.

Table 7: Pins Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT	36, 37, 38	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 3.0 A. It is suggested to use a TVS to increase voltage surge withstand capability.
VPH_PWR	220, 221	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 1000 mA	It can provide a maximum continuous current of 1 A.

3.1.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current up to 3 A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source.

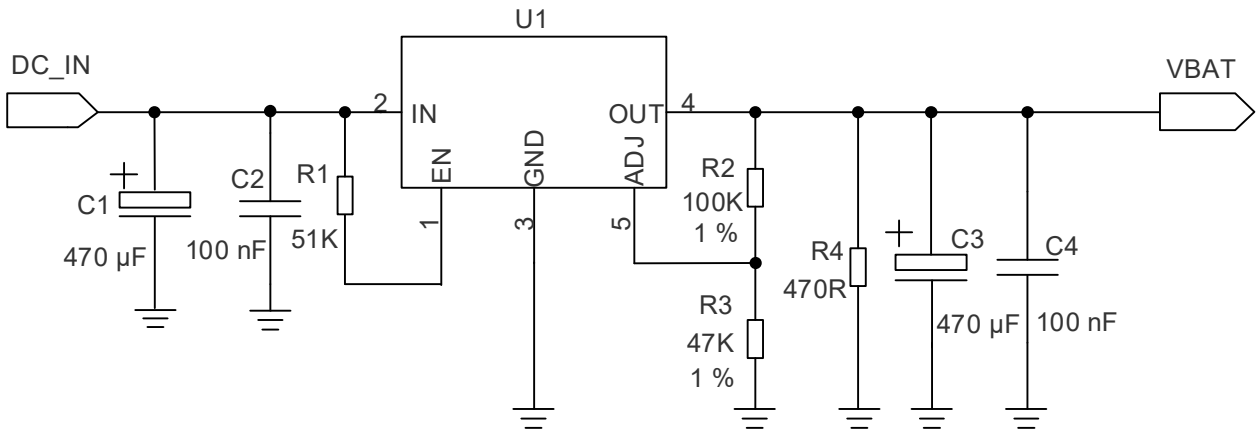


Figure 1: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY, then you can cut off the power supply.

3.1.3. Voltage Stability Requirements

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1 V, the module will power off automatically. Therefore, make sure the input voltage never drops below 3.1 V.

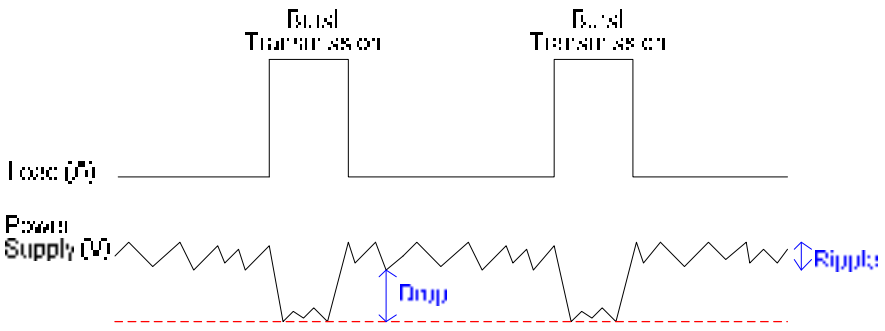


Figure 2: Power Supply Limits during Burst Transmission

To prevent the voltage from dropping below 3.1 V, use a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array, and place these capacitors close to VBAT pins. Additionally, add a 4.7 μF capacitor in parallel. The width of VBAT trace should be not less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use a 2000 W TVS and place it as close to the VBAT pins as possible to enhance surge protection.

The following figure shows the structure of the power supply.

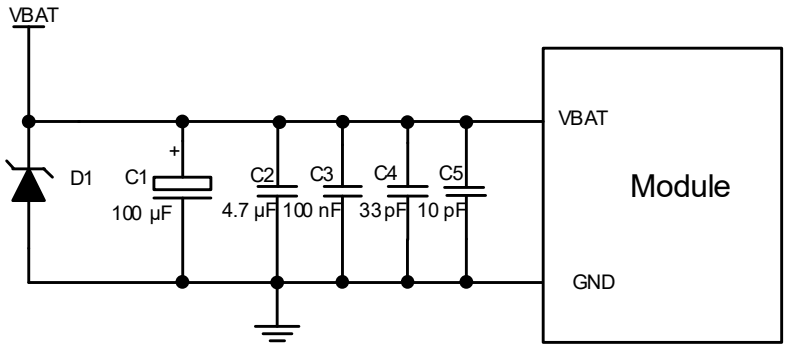


Figure 3: Structure of Power Supply

3.1.4. Battery Charge and Management

The module can recharge batteries. The battery charger in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** When the battery voltage is below 2.1 V, a 75 mA trickle charging current is applied to the battery.
- **Pre-charge mode:** When the battery voltage is between 2.1 V and the pre-charge cut-off voltage (software programmable range: 2.4–3.0 V, 3.0 V by default), the system will switch to pre-charge mode. The charging current software programmable range is from 100 mA to 450 mA (450 mA by default).
- **Constant current mode (CC mode):** When the battery is increased to 3 V, the system will switch to CC mode. The maximum charging current is 3000 mA when an adapter is used for battery charging, and the maximum charging current is 500 mA for USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100 mA, charging is completed.

Table 8: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	27	AI	Battery voltage detect (+)	Must be connected to the battery anode.
BAT_M	28	AI	Battery voltage detect (-)	Must be connected to the battery GND.
BAT_THERM	29	AI	Battery temperature detect	If used, connect it to external 47 kΩ NTC thermistor. If unused, connect it to a ground with a 47 kΩ resistor.
BAT_ID	17	AI	Battery type detect	If unused, keep this pin open.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (45 KΩ 1 % NTC thermistor with a B-constant of 4050K by default); and the thermistor is connected to BAT_THERM pin, or there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for the battery charging circuit is shown below.

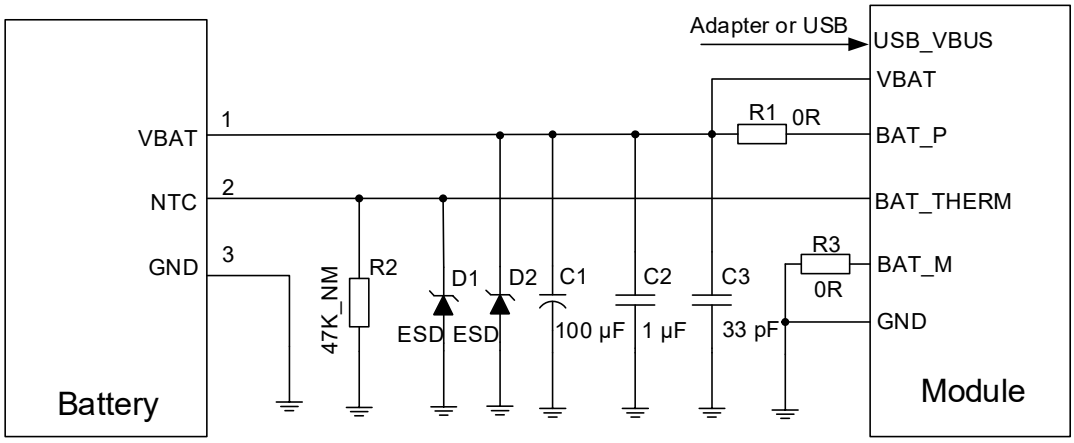


Figure 4: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve must be modified correspondingly to achieve the best effect.

If the thermistor is not available in the battery, or an adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may mistakenly judge that the battery temperature is abnormal, which will cause battery charging failure. To avoid this, BAT_THERM should be connected to GND via a 47 KΩ resistor. If BAT_THERM is unconnected, the

system will be unable to detect the battery, resulting in unsuccessful battery charging.

BAT_P and BAT_M must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as associated power on/off issues and battery charging/discharging issues.

3.2. Turn On

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pull up to 1.8 V internally. Active low.

The module can be turned on by driving the PWRKEY pin to a low level for at least 1.6 s. PWRKEY pin is pulled up to 1.8 V internally.

It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

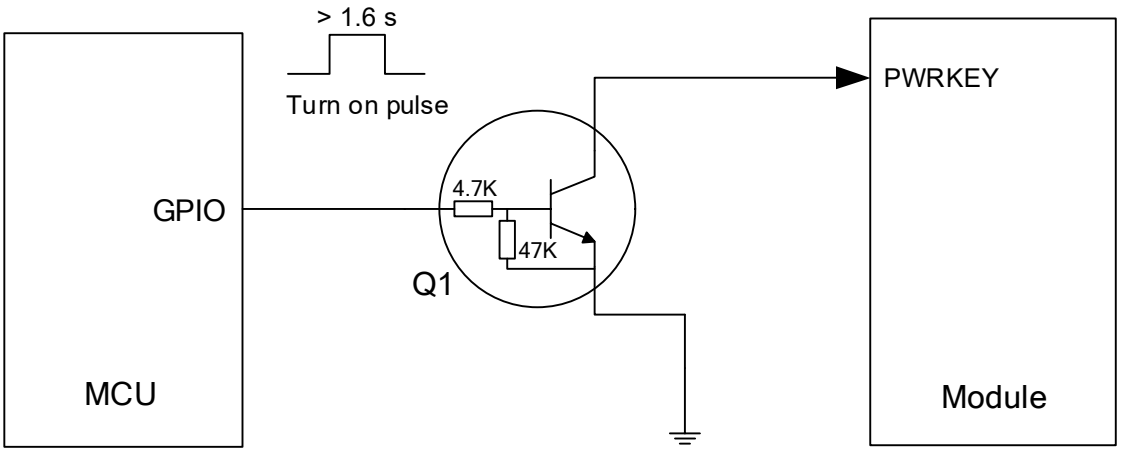


Figure 5: Reference Design of Turn On with Driving Circuit

The other way to control the PWRKEY is by using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

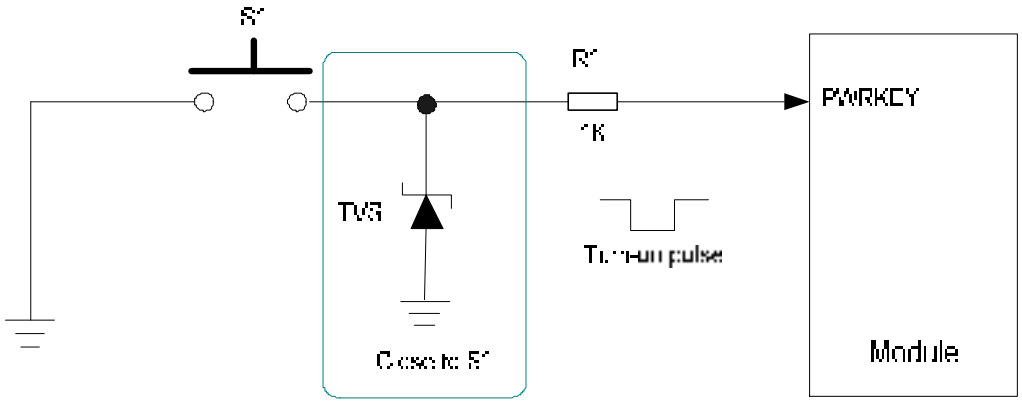


Figure 6: Reference Design of Turn On with Keystroke

The turn-on timing is illustrated in the following figure.

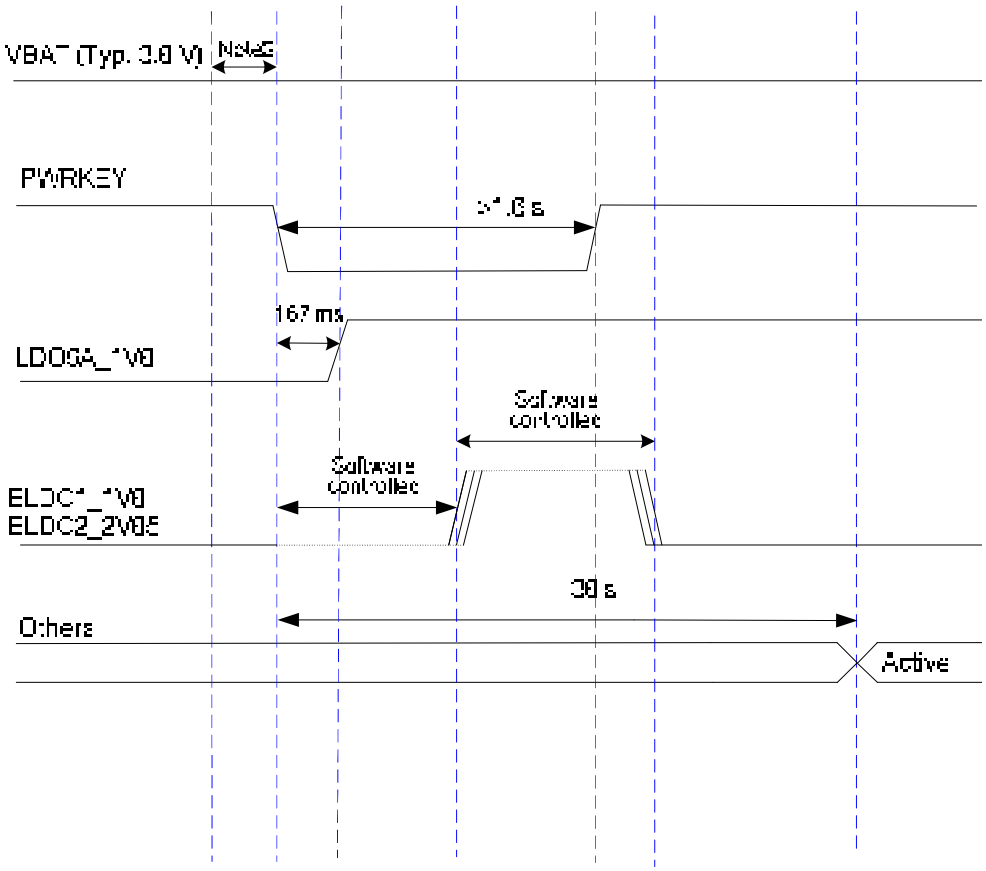


Figure 7: Timing of Turn On with PWRKEY

NOTE

1. When the module is turned on for the first time, its turn-on timing may be different from that shown above.
2. Ensure that VBAT is stable before pulling down the PWRKEY pin, and the recommended time interval is not less than 30 ms. PWRKEY pin cannot be driven low all the time.

3.3. Turn Off/Restart

Drive the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY to a low level for at least 8 s. The module will execute the forced shutdown. The forced turn-off timing is illustrated in the following figure.

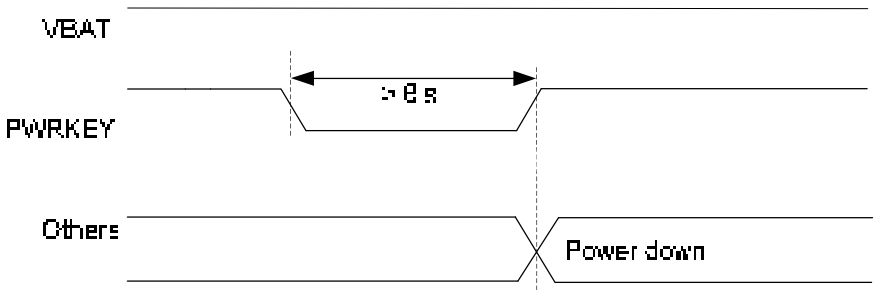


Figure 8: Timing of Turn Off with PWRKEY

3.4. VRTC

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands.

The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

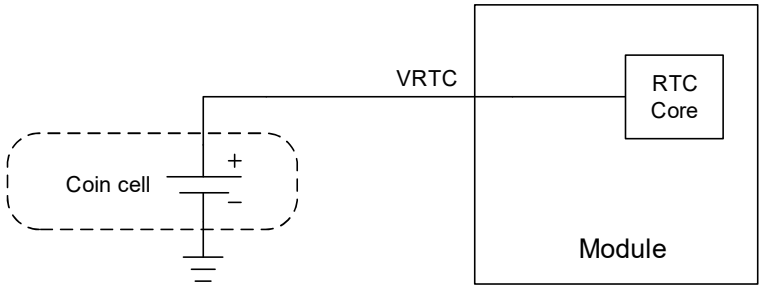


Figure 9: RTC Powered by a Rechargeable Coin Cell Battery

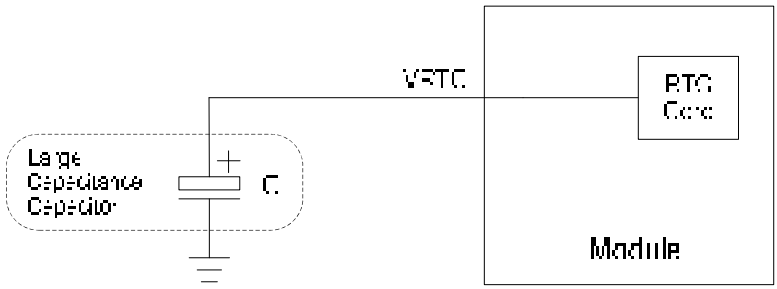


Figure 10: RTC Powered by Large Capacitance Capacitor

- When VBAT is disconnected, the recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3 V.
- When powered by VBAT, the RTC deviation is 50 ppm. When powered by VRTC, the RTC deviation is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.
- If RTC function is not needed, then it is recommended to connect a 0.1 μF capacitor to the VRTC interface.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to connect a 33 pF and a 10 pF capacitor in parallel to suppress high-frequency noise.

Table 10: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
LDO9A_1V8	1.8	20	Keeps ON
ELDO3_1V8	1.8	300	
ELDO1_2V8	2.8	300	
ELDO2_2V85	2.85	300	
LDO2C_1V1	1.1	800	
LDO3C_2V8	2.8	300	
LDO1C_1V2	1.2	800	
USIM1_VDD	1.8/2.95	150	
USIM2_VDD	1.8/2.95	150	
SD_VDD	1.8/2.95	800	
SD_PU_VDD	1.8 /2.95	50	

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 1 and USB 2.0 specifications, and supports SuperSpeed (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) for USB 2.0. The USB interface supports USB OTG function, and is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	AI	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	
USB_DM	33	AIO	USB differential data (-)	90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	32	AIO	USB differential data (+)	
USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)	90 Ω differential impedance. USB 3.1 Gen1 standard compliant.
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)	
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)	
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)	
USB_SS2_RX_P	156	AI	USB 3.1 Channel 2 super-speed receive (+)	90 Ω differential impedance. USB 3.1 Gen1 standard compliant.
USB_SS2_RX_M	155	AI	USB 3.1 Channel 2 super-speed receive (-)	

USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)	
USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)	
UUSB_TYPEC	217	AI	uUSB & USB Type-C configuration	If Micro USB is intended to be used, this pin should be connected to ground via a 1 kΩ resistor. If Type-C is intended to be used, this pin should be left open.
USB_CC1	224	AI	USB Type-C detect 1	
USB_CC2	223	AI	USB Type-C detect 2	
USB_SS_SEL	226	DO	USB Type-C switch control	
SS_DIR_IN	212	DI	CC status detect	When using USB Type-C, connect the pin to SS_DIR_OUT. When using Micro USB, connect it to ground with a 10 kΩ resistor.
SS_DIR_OUT	213	AO	CC status output	When using USB Type-C, connect the pin to SS_DIR_IN. When using Micro USB, leave this pin open.
USB_ID	30	AI	USB ID detect	High level by default.

4.1.1. Micro USB Mode

A reference circuit of Micro USB mode is shown below.

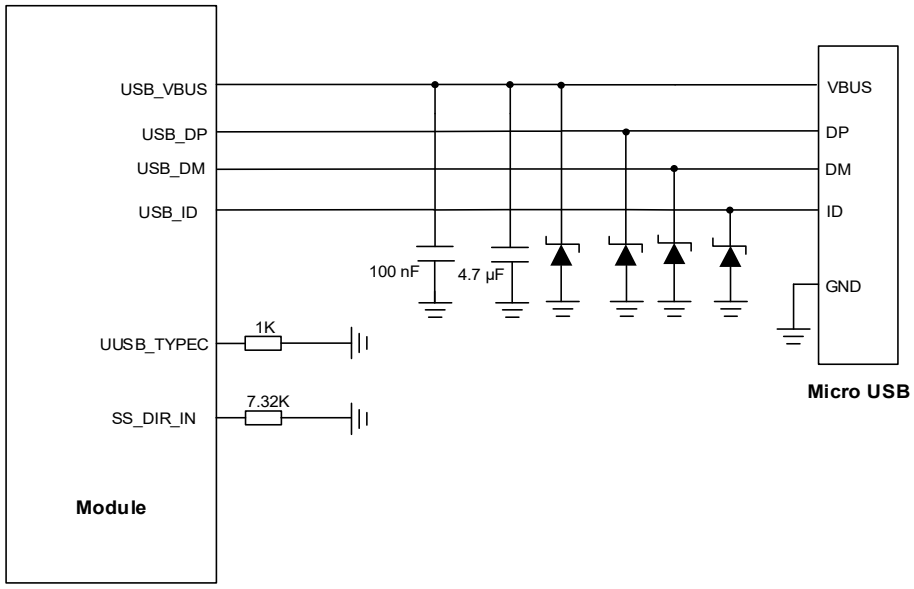


Figure 11: Reference Design of Micro USB Interface

4.1.2. USB Type-C Mode

A reference circuit of USB Type-C mode shown below.

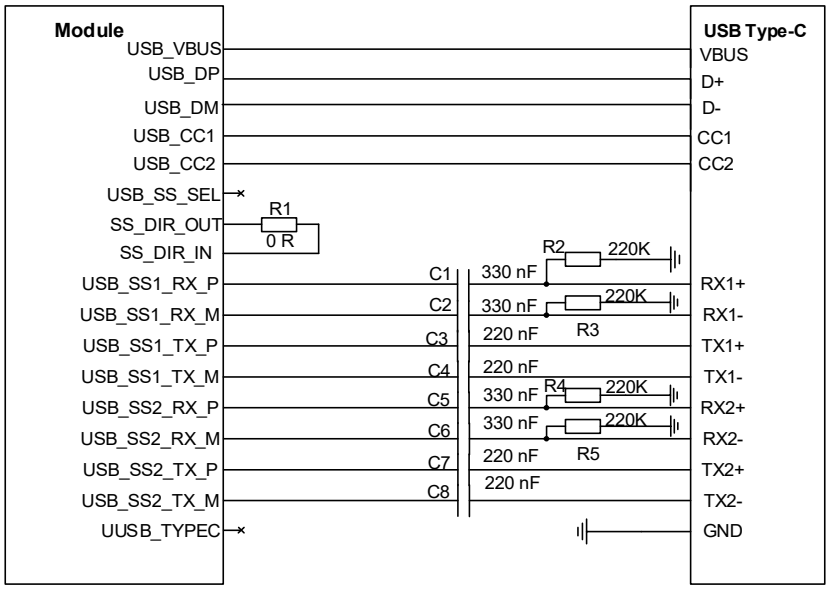


Figure 12: Reference Design of USB Type-C Mode

To ensure USB performance, please follow the following principles while designing USB interface.

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- The ground reference plane under the USB signals must be continuous without any cuts or any holes to ensure impedance continuity.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1. Keep the ESD protection components as close as possible to the USB connector.
- For USB 2.0, the total trace length of each signal should be less than 200 mm, and the length matching (P/M) of each differential pair should be less than 2 mm.
- For USB 3.1, intra-pair length matching (P/M) should be less than 0.7 mm, while the inter-pair length matching (Tx/Rx) should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

Table 12: USB Trace Length Inside the Module

Signal	Pin No.	Length (mm)	Length Difference (mm)
USB_DP	32	37.12	0.54
USB_DM	33	37.66	
USB_SS1_RX_P	171	22.08	0
USB_SS1_RX_M	172	22.08	
USB_SS1_TX_P	174	19.87	0.31
USB_SS1_TX_M	175	20.18	
USB_SS2_RX_P	156	38.27	0.04
USB_SS2_RX_M	155	38.23	
USB_SS2_TX_P	165	33.68	0.02
USB_SS2_TX_M	164	33.70	

4.2. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to LDO9A_1V8 before turning on the module, thus the module will enter emergency download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 13: Pins Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	57	DI	Force the module into emergency download mode	Pull-up to 1.8 V internally. Active low.

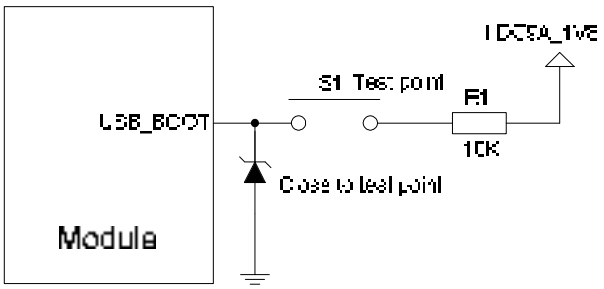


Figure 13: Reference Design of USB_BOOT

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators in the module.

Table 14: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external

				capacitor cannot exceed 2.2 μF.
USIM1_DATA	142	DIO	(U)SIM1 card data	Internally pull up to USIM1_VDD with 20 kΩ resistor.
USIM1_CLK	143	DO	(U)SIM1 card clock	
USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	Active low. Require externally pull up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external capacitor cannot exceed 2.2 μF.
USIM2_DATA	209	DIO	(U)SIM2 card data	Internally pull up to USIM2_VDD with 20 kΩ resistor.
USIM2_CLK	208	DO	(U)SIM2 card clock	
USIM2_RST	207	DO	(U)SIM2 card reset	
USIM2_DET	256	DI	(U)SIM2 card detect	Active low. Require external pull-up to 1.8 V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration.

A reference design for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

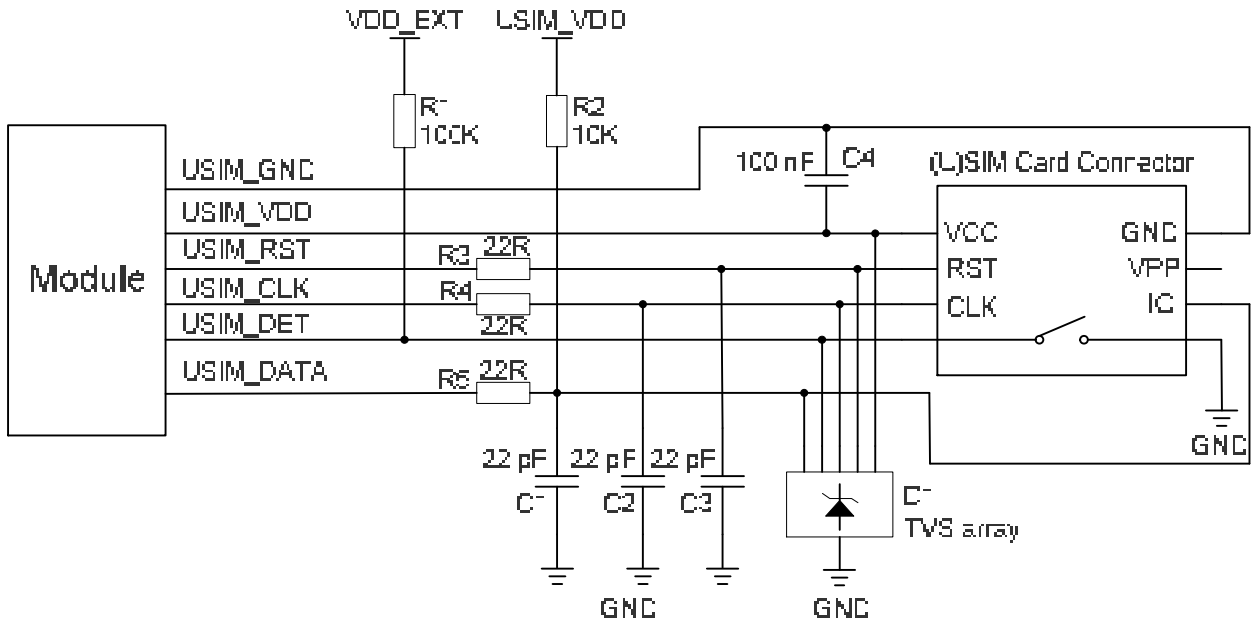


Figure 14: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

A reference design for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

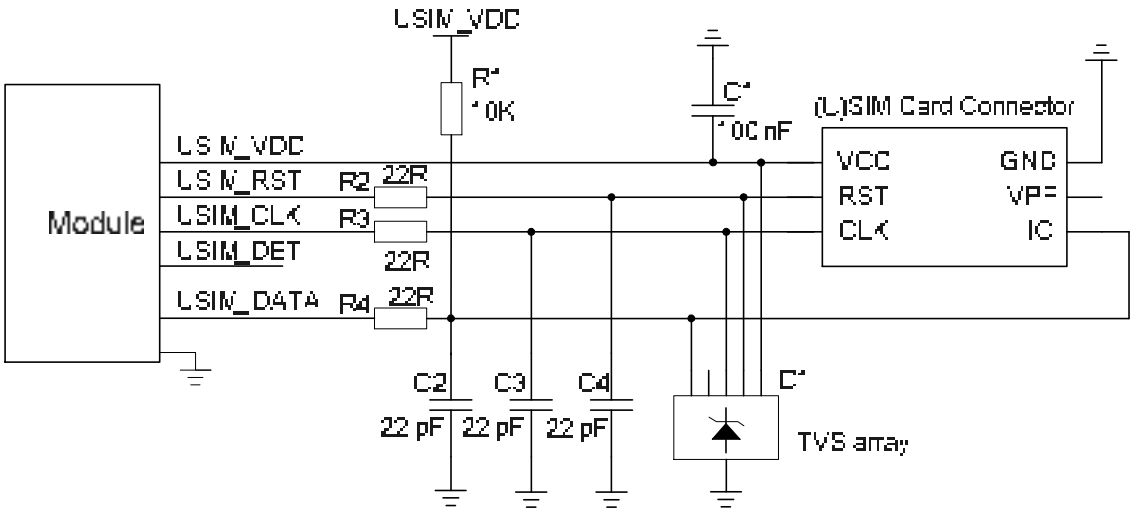


Figure 15: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short

as possible, at most 200 mm.

- Keep (U)SIM card signal traces away from RF and power supply traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 30 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and filter out RF interference.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.
- Add 22 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference, and place them as close to the (U)SIM card connector as possible.

4.4. SPI Interfaces

The module supports up to three groups of SPI interfaces. One of them is default configuration, and supports master mode only. Two of them can be multiplexed from other interfaces, see ***Table 18*** for details.

Table 15: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description
SPI0_CS	58	DO	SPI0 chip select
SPI0_CLK	59	DO	SPI0 clock
SPI0_MOSI	60	DO	SPI0 master-out slave-in
SPI0_MISO	61	DI	SPI0 master-in slave-out

4.5. UART Interfaces

The module supports up to four groups of UART interfaces. Two of them are default configurations and two of them can be multiplexed from other interfaces, see ***Table 18*** for details.

Two default UART interfaces are:

- **UART5:** 4-wire UART interface, supports hardware flow control.
- **Debug UART:** 2-wire UART interface, used for debugging by default.

Pin definition of the UART interfaces is here as follows:

Table 16: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	5	DO	Debug UART transmit.	If unused, keep this pin open.
DBG_RXD	6	DI	Debug UART receive.	
UART5_TXD	199	DO	UART5 transmit	
UART5_RXD	198	DI	UART5 receive	
UART5_RTS	245	DO	DCE request to send signal to DTE	
UART5_CTS	246	DI	DCE clear to send signal from DTE	

UART5 is a 4-wire UART interface with 1.8 V power domain. A level-shifting chip should be used if your application is equipped with a 3.3 V UART interface. A level-shifting chip is recommended. The following figure shows a reference design.

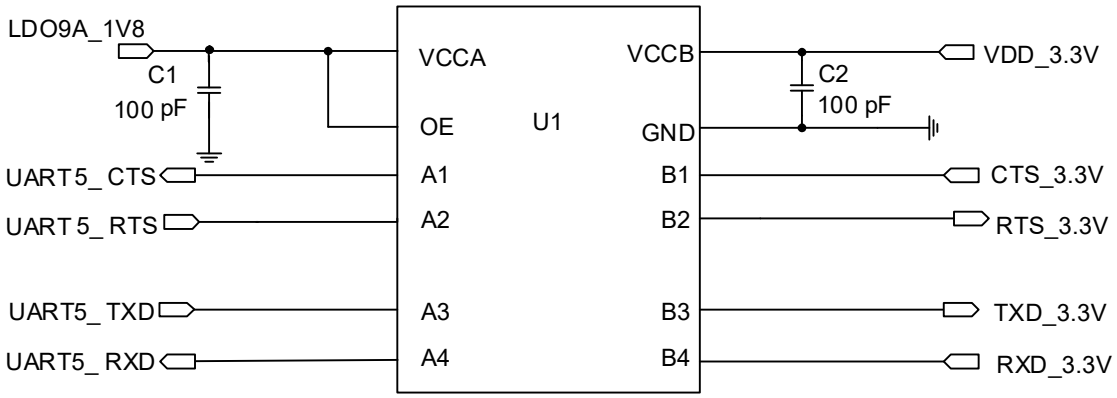


Figure 16: Reference Design of UART with Level-shifting Chip (for UART5)

The following figure is an example of connection between the module and PC. A voltage-level translator and an RS-232 level-shifting chip are recommended to be added between the module and PC, as shown below:

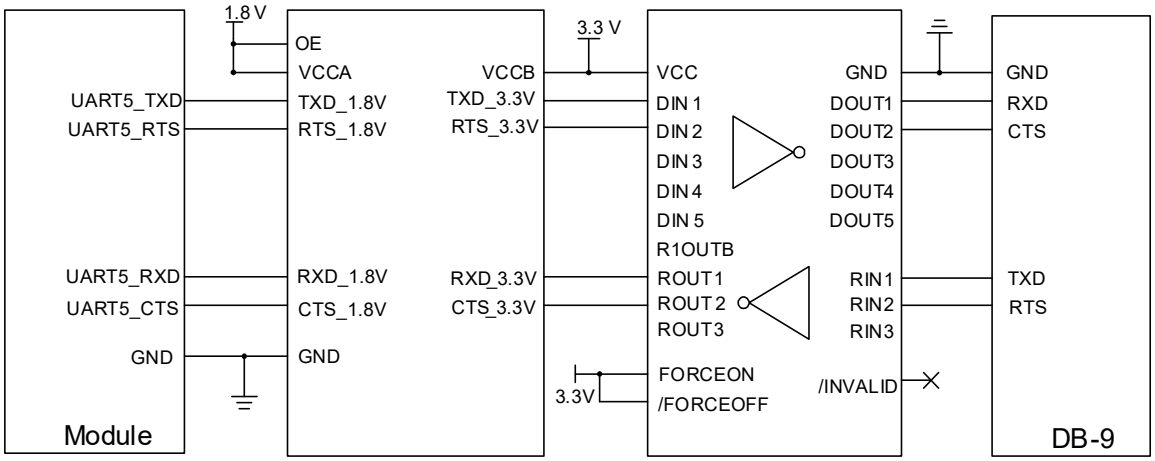


Figure 17: Reference Design of UART with RS-232 Level-shifting Chip (for UART5)

NOTE

Debug UART is similar to UART5. For the reference designs, refer to that for UART5.

4.6. I2C Interfaces

The module provides up to seven groups of I2C interfaces. Four of them are dedicated I2C interfaces used for camera, TP and sensor peripherals. One of them is generic I2C interface. Two of them can be multiplexed from other interfaces, see ***Table 18*** for details.

All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The SENSOR_I2C interface only supports sensors of the ADSP architecture. CAM_I2C signals are controlled by Linux Kernel code and support connection with video output related devices.

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	204	OD	I2C1 serial data	The module's internal power

I2C1_SCL	205	OD	I2C1 serial clock	chip has occupied the addresses 0x47, 0x02 and 0x36 of the I2C bus. 2.2 kΩ pull-up resistance has been integrated inside the module. Cannot be used as generic GPIO.

4.7. I2S Interfaces

The module does not support I2S interface by default, but it can be multiplexed from GPIO interfaces. The module supports up to two groups of I2S interfaces, one of which is a low-power I2S. Data signals of both interfaces can be configured as input or output, and the reference power domain of the interfaces is 1.8 V.

4.8. UART/SPI/I2C/I2S Multiplexing Relationship

UART/SPI/I2C/I2S multiplexing relationship is shown in the following tables.

Table 18: UART/SPI/I2C Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplexing Functions		
				UART	SPI	I2C
QUP0 SE0	58	SPI0_CS	GPIO_3	UART0_RX	SPI0_CS	
	59	SPI0_CLK	GPIO_2	UART0_TX	SPI0_CLK	
	60	SPI0_MOSI	GPIO_1	UART0_RTS	SPI0_MOSI	I2C0_SCL
	61	SPI0_MISO	GPIO_0	UART0_CTS	SPI0_MISO	I2C0_SDA
QUP0 SE1	204	I2C1_SDA	GPIO_4			I2C1_SDA
	205	I2C1_SCL	GPIO_5			I2C1_SCL
QUP0 SE2	7	GPIO_71	GPIO_71	UART2_TX	SPI2_SCLK	
	8	GPIO_80	GPIO_80	UART2_RX	SPI2_CS_N	

	140	TP_I2C_SCL	GPIO_7	UART2_RTS	SPI2_MOSI	I2C2_SDA
	206	TP_I2C_SDA	GPIO_6	UART2_CTS	SPI2_MISO	I2C2_SCL
QUP0 SE5	198	UART5_RXD	GPIO_17	UART5_RX	SPI5_CS_N	
	199	UART5_TXD	GPIO_16	UART5_TX	SPI5_SCLK	
	245	UART5_RTS	GPIO_15	UART5_RTS	SPI5_MOSI	I2C5_SCL
	246	UART5_CTS	GPIO_14	UART5_CTS	SPI5_MISO	I2C5_SDA

NOTE

1. QUP-SE is flexible and supports four types of interfaces: UART, SPI, I2C and I2S.
2. Note that the same set of QUP-SE cannot support two protocols at the same time. For example: the same set of QUP cannot support UART and I2C at the same time. If a protocol only occupies part of the pins of this group of QUP, other pins can only be used for GPIO.

Table 19: I2S Multiplex Relationship Table

Channel	Pin No.	Pin Name	GPIO No.	I2S Multiplex Function
1	234	GPIO_108	GPIO_108	MI2S_MCLK1_A
2	231	GPIO_99	GPIO_99	LPI_MI2S0_WS
	232	GPIO_98	GPIO_98	LPI_MI2S0_CLK
	177	GPIO_101	GPIO_101	LPI_MI2S0_DATA1
	178	GPIO_100	GPIO_100	LPI_MI2S0_DATA0
3	203	GPIO_103	GPIO_103	LPI_MI2S1_WS
	250	GPIO_102	GPIO_102	LPI_MI2S1_CLK
	249	GPIO_104	GPIO_104	LPI_MI2S1_DATA0
	251	GPIO_105	GPIO_105	LPI_MI2S1_DATA1

4.9. Analog Audio Interfaces

The module provides 3 analog input channels and 3 analog output channels. The following table shows the pin definition.

Table 20: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS	167	AO	Bias voltage output for microphone	
MIC1_P	44	AI	Microphone input for channel 1 (+)	Internally integrated hardware bias.
MIC1_M	45	AI	Microphone input for channel 1 (-)	
MIC_GND	168		Microphone reference ground	If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone input for headset (+)	Internally integrated hardware bias.
MIC3_P	169	AI	Microphone input for channel 2 (+)	No internal hardware bias is integrated.
EAR_P	53	AO	Earpiece output (+)	
EAR_M	52	AO	Earpiece output (-)	
SPK_P	55	AO	Speaker output (+)	
SPK_M	54	AO	Speaker output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_L	49	AO	Headphone left channel output	
HPH_GND	50		Headphone reference ground	It should be connected to main GND.
HS_DET	48	AI	Headset hot-plug detect	Pulled up internally.

- The module offers 3 audio input channels, including 1 differential input pair and 2 single-ended channels.
- The output voltage range of MIC_BIAS is programmable between 1.0 V and 1.85 V, and the maximum output current is 3 mA.
- The earpiece interface uses differential output.

- The loudspeaker interface uses the differential output as well. The output channel is available with a Class K amplifier whose output power is 1.2 W when the load is 8 Ω.
- The headphone interface features stereo left and right channel output, and headphone insert detection function is supported.

4.9.1. Microphone Interfaces Reference Design

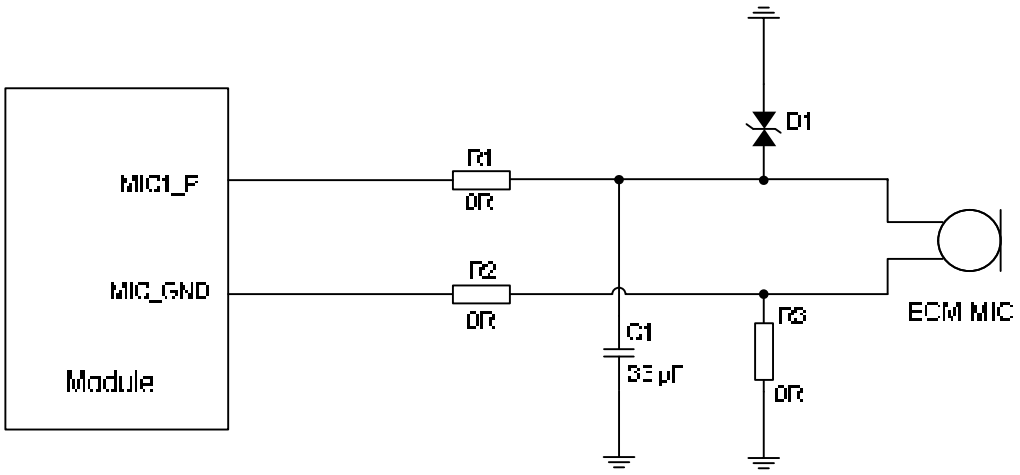


Figure 18: Reference Design of ECM Microphone Interface

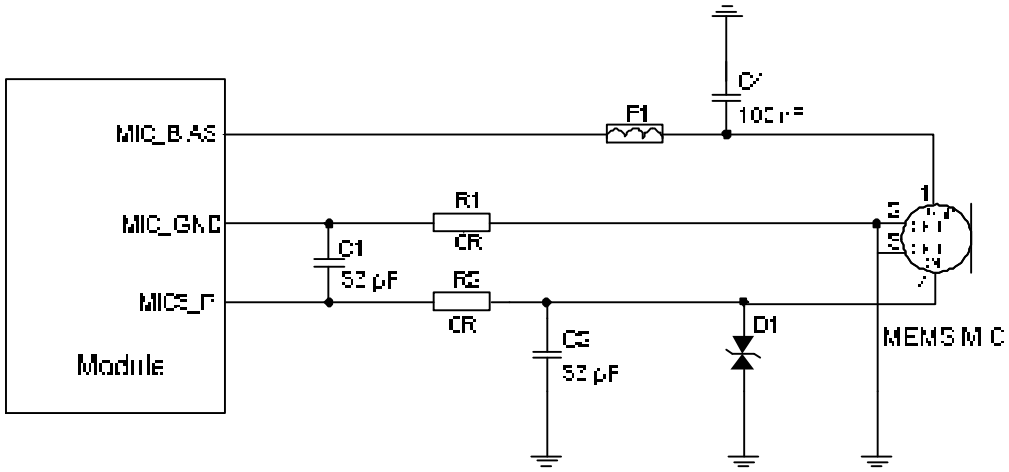


Figure 19: Reference Design of MEMS Microphone Interface

4.9.2. Earpiece Interface Reference Design

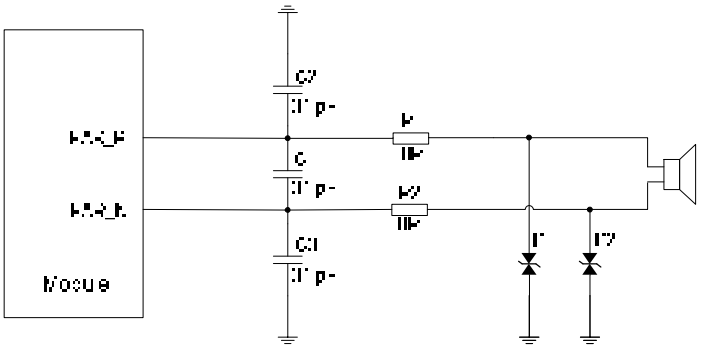


Figure 20: Reference Design of Earpiece Interface

4.9.3. Headset Interface Reference Design

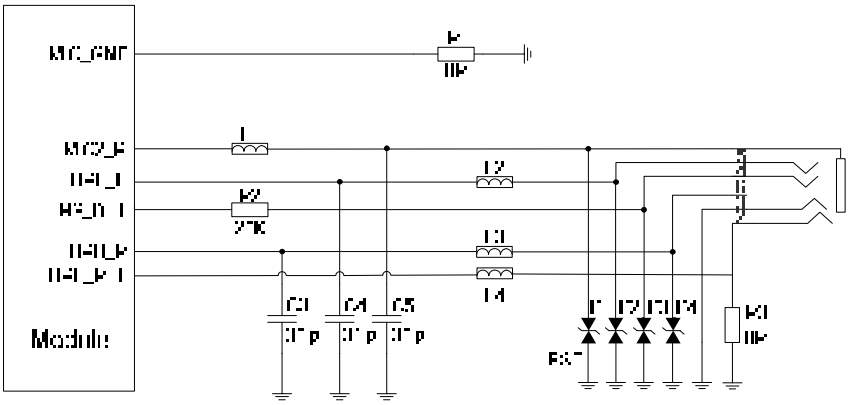


Figure 21: Reference Design of Headset Interface

4.9.4. Loudspeaker Interface Reference Design

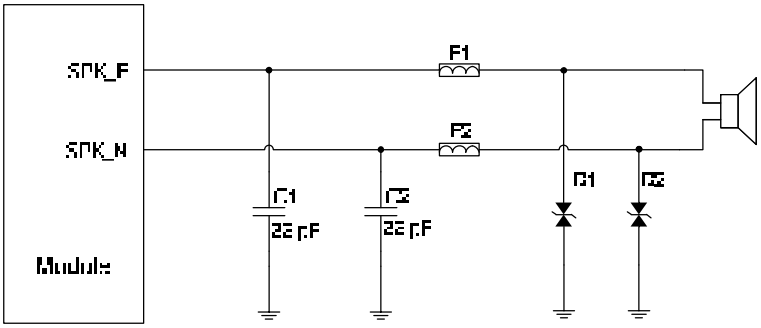


Figure 22: Reference Design of Loudspeaker Interface

4.9.5. Analog Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out RF interference when the module is transmitting on EGSM900. Without this capacitor, TDD noise could be heard. The 10-pF capacitor here is used to filter out RF interference on DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor should be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease radio or other signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.10. ADC Interfaces

The module provides 2 Analog-to-Digital Converter (ADC) interfaces which support up to 15-bit resolution, and the pin definition is shown below.

Table 21: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	151	AI	General-purpose ADC interface	Maximum input voltage 1.8 V.
ADC1	153	AI		

4.11. SD Card Interface

The module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 22: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	70	DO	SD card clock	50 Ω impedance.
SD_CMD	69	DIO	SD card command	
SD_DATA0	68	DIO	SDIO data bit 0	
SD_DATA1	67	DIO	SDIO data bit 1	
SD_DATA2	66	DIO	SDIO data bit 2	
SD_DATA3	65	DIO	SDIO data bit 3	
SD_DET	64	DI	SD card hot-plug detect	Active low.
SD_VDD	63	PO	SD card power supply	No external capacitor is required.
SD_PU_VDD	179	PO	1.8/2.95 V output power for SD card pull-up circuits	The maximum external capacitance must not exceed 2.2 μF.

A reference circuit for SD card interface is shown below.

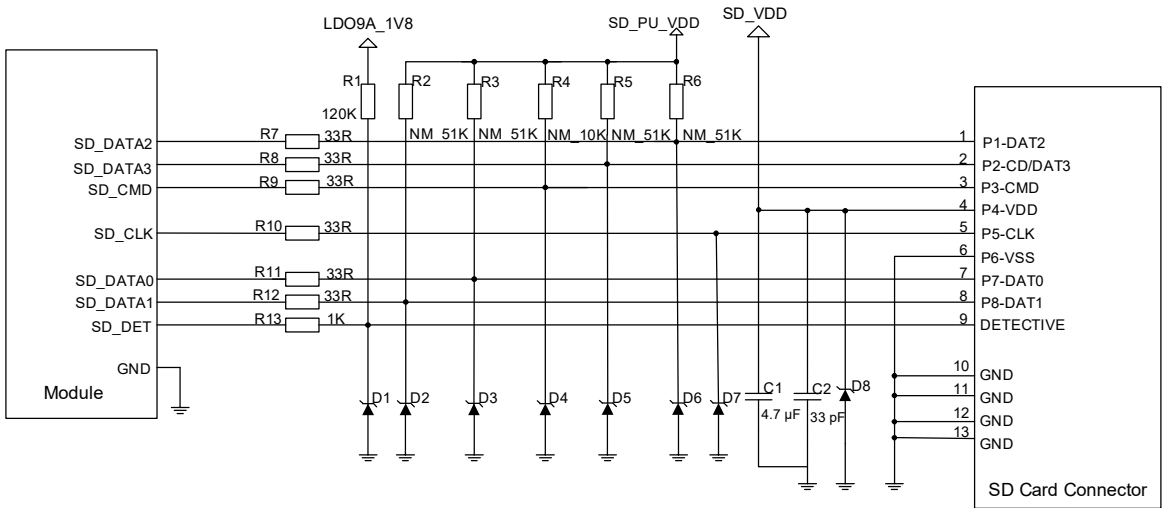


Figure 23: Reference Design of SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 800 mA. Because of the high drive current, it is recommended to keep the trace width as 0.5 mm at least. To ensure the stability of drive power, add a 4.7 μF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 50 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- The total trace length of each signal (except for SD_DET) should be less than 150 mm for 50 MHz DDR/100 MHz SDR clock frequency modes, and less than 50 mm for 208 MHz DDR clock frequency modes;
- The trace length difference between SD_CLK and SD_CMD/SD_DATA[0:3] should not exceed 6 mm for 50 MHz DDR/100 MHz SDR clock frequency modes, and not exceed 2 mm for 208 MHz DDR/100 MHz SDR clock frequency modes.

Table 23: SD Card Interface Trace Length Inside the Module (Unit: mm)

Signal	Pin No.	Length
SD_CLK	70	50.15
SD_CMD	69	50.69
SD_DATA0	68	51.05
SD_DATA1	67	51.21
SD_DATA2	66	50.53
SD_DATA3	65	50.88

4.12. LCM Interface

The module provides an LCM interface, which is MIPI_DSI standard compliant. The interface supports high-speed differential data transmission and supports FHD+ display (1080 × 2520 @ 60 fps). The maximum rate can reach up to 1.5 Gbps/lane. The pin definition of the LCM interface is shown below.

Table 24: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_BL_A	21	PO	Current output for LCD backlight	
LCD_BL_K1	22	AI	Current sink for LCD backlight	
LCD_BL_K2	23	AI	Current sink for LCD backlight	
LCD_BL_K3	24	AI	Current sink for LCD backlight	
LCD_BL_K4	25	AI	Current sink for LCD backlight	
PWM	152	DO	PWM output	
LCD_RST	127	DO	LCD reset	
LCD_TE	126	DI	LCD tearing effect	
DSI_CLK_P	115	AO	LCD MIPI clock (+)	100 Ω differential impedance.
DSI_CLK_N	116	AO	LCD MIPI clock (-)	
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)	
DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)	
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)	
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)	
DSI_LN2_P	121	AO	LCD MIPI lane 2 data (+)	
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)	
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)	
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)	

The following figures show the reference design for LCM interface.

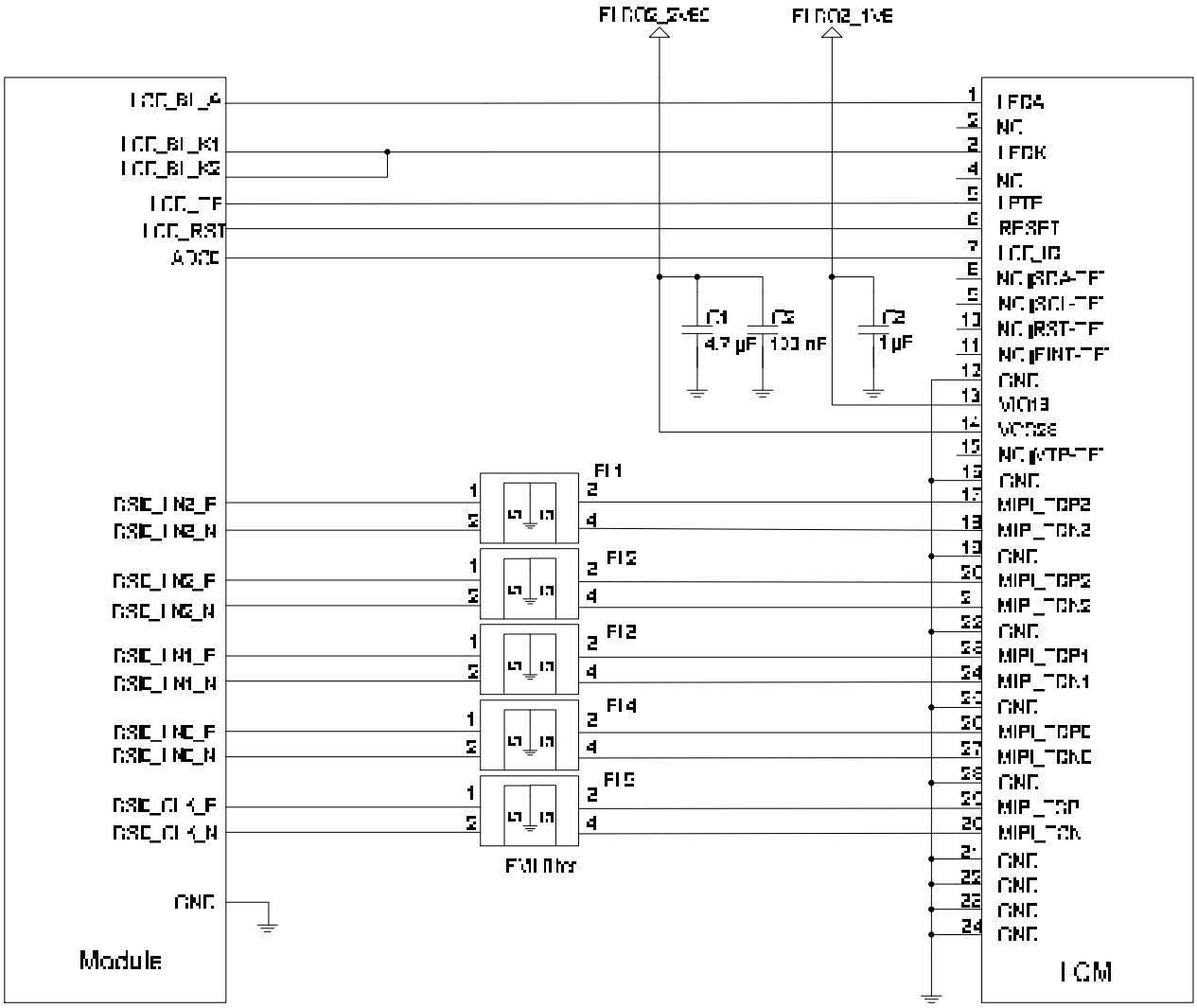


Figure 24: Reference Design of LCM Interface

MIPI are high-speed signal lines. It is recommended to add common-mode chokes in series near the LCM connector to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM module factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pins of the module, but note that the output voltage of LCD_ID should not exceed the voltage range of the ADC pins.

4.13. Camera Interfaces

Based on MIPI_CSI standard, the module supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane), and the maximum pixel of the camera can reach up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor, camera lens quality, etc.

Table 25: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)	100 Ω differential impedance.
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)	
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)	
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)	
CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)	
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)	
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)	

CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)	
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)	
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)	
CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)	
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)	
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)	
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)	
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)	
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)	
CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)	
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)	
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)	
SCAM_MCLK	100	DO	Master clock of front camera	
SCAM_RST	72	DO	Reset of front camera	
SCAM_PWDN	71	DO	Power down of front camera	
MCAM_MCLK	99	DO	Master clock of rear camera	
MCAM_RST	74	DO	Reset of rear camera	
MCAM_PWDN	73	DO	Power down of rear camera	
DCAM_MCLK	194	DO	Master clock of depth camera	
DCAM_RST	180	DO	Reset of depth camera	
DCAM_PWDN	181	DO	Power down of depth camera	
CAM4_MCLK	236	DO	Master clock of fourth camera	
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	Only used for camera interface.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	
DCAM_I2C_SDA	197	OD	I2C data of depth camera	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	

The following is a reference design for triple-camera applications.

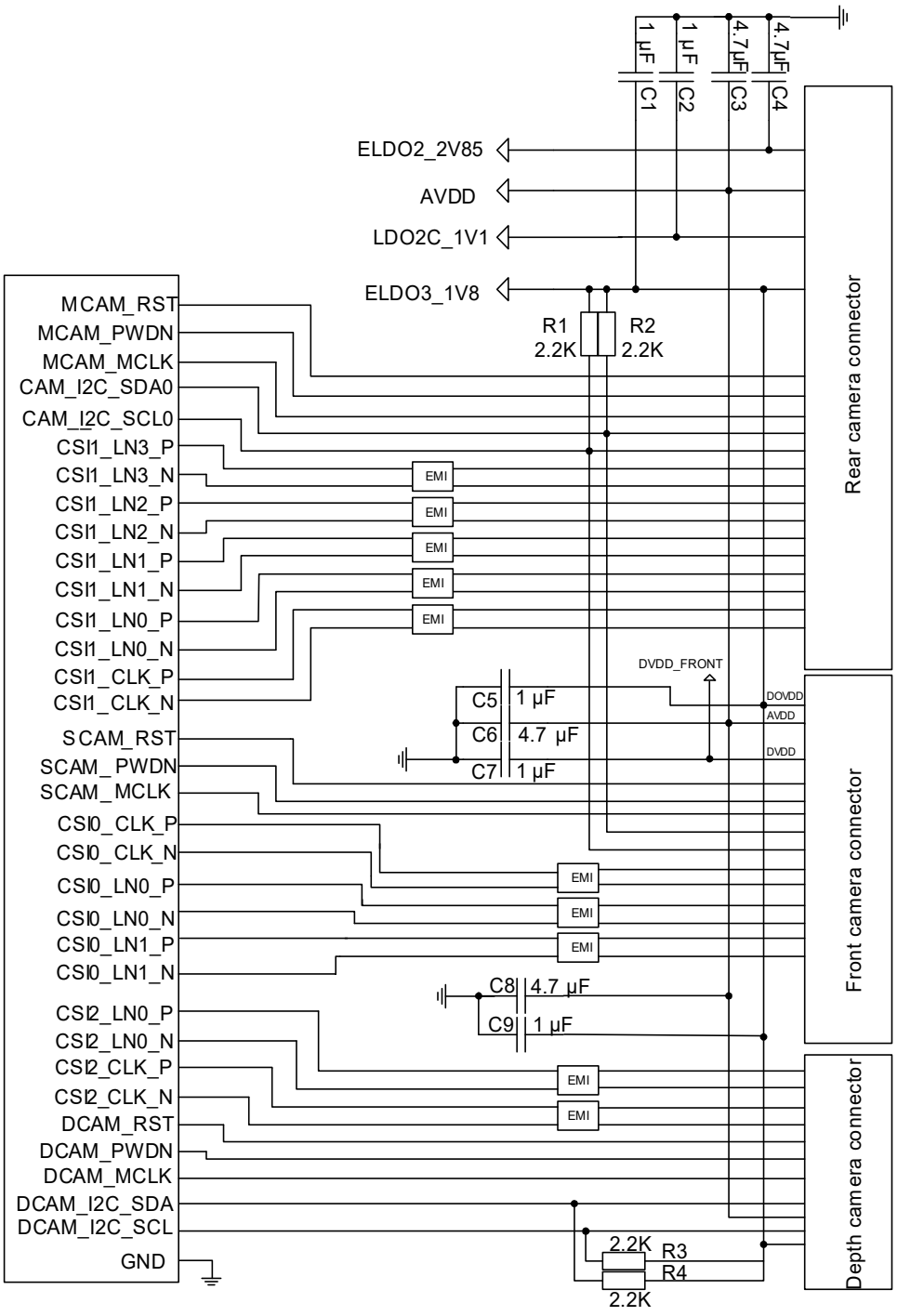


Figure 25: Reference Design of Triple-Camera Applications

4.13.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces be of the same length. To avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal traces is recommended. During impedance matching, do not connect MPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS component of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- The intra-pair length matching (P/N) should be less than 0.7 mm, while the inter-pair length matching should be less than 2.1 mm.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length difference within 0.7 mm;
  d) Control inter-lane length difference within 1.4 mm.

Table 26: MIPI Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Difference
DSI_CLK_P	115	64.61	0.27
DSI_CLK_N	116	64.88	
DSI_LN0_P	117	64.77	0.11
DSI_LN0_N	118	64.66	
DSI_LN1_P	119	64.84	0.17
DSI_LN1_N	120	64.67	
DSI_LN2_P	121	64.73	0.25
DSI_LN2_N	122	64.98	
DSI_LN3_P	123	64.92	0.31

DSI_LN3_N	124	65.23	
CSI0_CLK_P	77	21.23	0.06
CSI0_CLK_N	78	21.29	
CSI0_LN0_P	79	21.08	0.07
CSI0_LN0_N	80	21.01	
CSI0_LN1_P	81	20.79	0.26
CSI0_LN1_N	82	21.05	
CSI0_LN2_P	83	21.15	0.21
CSI0_LN2_N	84	21.36	
CSI0_LN3_P	85	21.12	0.31
CSI0_LN3_N	86	21.43	
CSI1_CLK_P	88	13.48	0.24
CSI1_CLK_N	89	13.72	
CSI1_LN0_P	90	13.49	0.32
CSI1_LN0_N	91	13.81	
CSI1_LN1_P	92	13.37	0.30
CSI1_LN1_N	93	13.67	
CSI1_LN2_P	94	13.43	0.12
CSI1_LN2_N	95	13.55	
CSI1_LN3_P	96	13.35	0.29
CSI1_LN3_N	97	13.64	
CSI2_CLK_P	183	21.10	0.12
CSI2_CLK_N	184	20.98	
CSI2_LN0_P	185	13.64	0.16
CSI2_LN0_N	186	13.48	

CSI2_LN1_P	187	13.37	0.43
CSI2_LN1_N	188	12.94	
CSI2_LN2_P	189	6.38	0.53
CSI2_LN2_N	190	5.85	
CSI2_LN3_P	191	9.66	0.08
CSI2_LN3_N	192	9.58	

Table 27: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rate	Flex Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/Lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/Lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/Lane	76.2	-0.75	< 200
	152.4	-1.4	< 125
1.5 Gbps/Lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/Lane	76.2	-1.3	< 170
	152.4	-2.3	< 90
2.5 Gbps/Lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 28: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rate	Flex Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/Lane	76.2	-0.5	< 280
	152.4	-1.0	< 210

750 Mbps/Lane	76.2	-0.7	< 210
	152.4	-1.15	< 150
1.0 Gbps/Lane	76.2	-0.75	< 200
	152.4	-1.4	< 100
1.5 Gbps/Lane	76.2	-0.9	< 135
	152.4	-1.8	< 40
2.1 Gbps/Lane	76.2	-1.3	< 110
	152.4	-2.3	< 80
2.5 Gbps/Lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

4.14. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins. The pin definition of touch panel interface is illustrated below.

Table 29: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	138	DO	TP reset	
TP_INT	139	DI	TP interrupt	
TP_I2C_SCL	140	OD	TP I2C clock	TP I2C requires external pull-up circuit.
TP_I2C_SDA	206	OD	TP I2C data	

A reference design of TP interface is shown below.

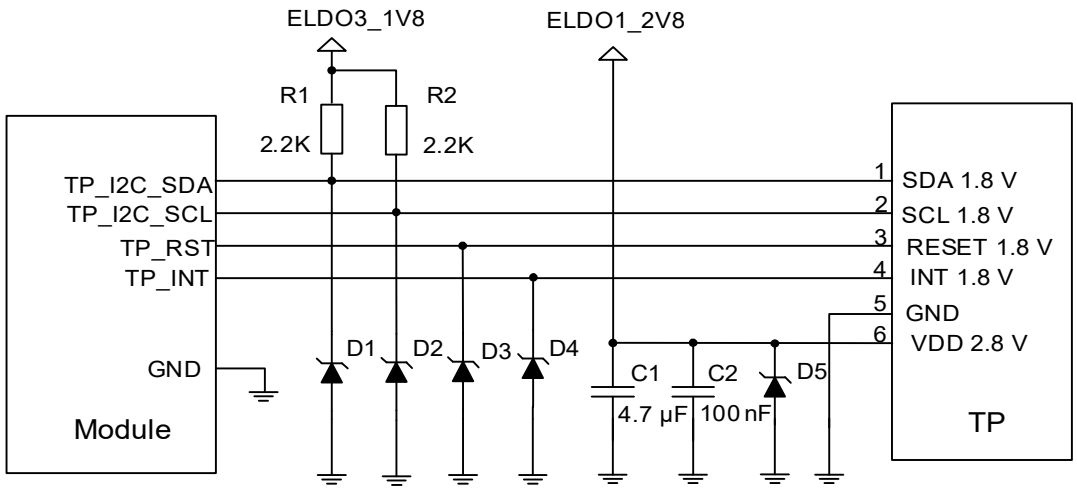


Figure 26: Reference Design of Touch Panel Interface

4.15. Sensor Interfaces

The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, etc.

Table 30: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ACCEL_INT	252	DI	Acceleration sensor interrupt	
ALPS_INT	253	DI	Ambient light/proximity sensor interrupt	
MAG_INT	254	DI	Geomagnetic sensor interrupt	
GYRO_INT	255	DI	Gyroscope sensor interrupt	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	External pull-up is required for external sensors. Cannot be used for touch panel, NFC, I2C keyboard, etc. Cannot be used
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	

				as generic GPIO.

4.16. Flash Interfaces

The module supports 2 flash LED drivers, with maximum output current up to 1.5 A per channel. The default output current is 1000 mA in flash mode and 300 mA in torch mode.

Table 31: Pin Definition of Flash Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH1_LED	26	AO	Flash/torch driver output	Support flash and torch modes.
FLASH2_LED	162	AO	Flash/torch driver output	

A reference design is shown below.

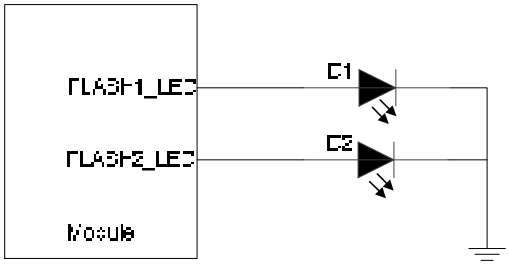


Figure 26: Reference Design of Flashlight Interfaces

4.17. Keypad Interfaces

The module supports three keypads: PWRKEY to turn module on/off and VOL_UP and VOL_DOWN to adjust the volume.

Table 32: Pin Definition of Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pull up to 1.8 V internally.

				Active low.
VOL_UP	146	DI	Volume up	If unused, keep this pin open.
VOL_DOWN	147	DI	Volume down	If unused, keep this pin open.

4.18. Vibration Driver Motor Interface

The module supports eccentric rotating machines (ERM). The pin definition of vibration drive motor interface is listed below.

Table 33: Pin Definition of Vibration Driver Motor Interface

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV_P	161	PO	Vibration motor driver output control	

The vibrator is driven by an exclusive circuit, and a reference design is shown below.

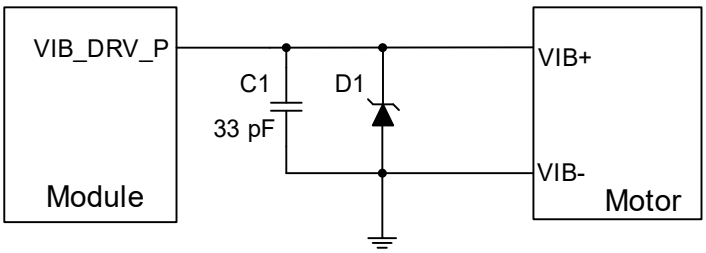


Figure 27: Reference Design of Vibrator Connection

4.19. GPIOs

The module has abundant GPIO interfaces with power domain of 1.8 V. The pin definition is listed below.

Table 34: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description
GPIO_65	247	DIO	General-purpose input/output
GPIO_66	248	DIO	
GPIO_67	136	DIO	
GPIO_68	137	DIO	
GPIO_71	7	DIO	
GPIO_80	8	DIO	
GPIO_83	200	DIO	
GPIO_84	201	DIO	
GPIO_86	237	DIO	
GPIO_96	113	DIO	
GPIO_97	114	DIO	
GPIO_98	232	DIO	
GPIO_99	231	DIO	
GPIO_100	178	DIO	
GPIO_101	177	DIO	
GPIO_102	250	DIO	
GPIO_103	203	DIO	
GPIO_104	249	DIO	
GPIO_105	251	DIO	
GPIO_107	238	DIO	

GPIO_108	234	DIO
GPIO_111	230	DIO
GPIO_112	229	DIO

NOTE

For more details about GPIO configuration, see ***document [2]***.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

The pin definition is shown below:

Table 35: Pin Definition of Cellular Network Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AIO	Main antenna interface	50 Ω impedance.
ANT_DRX	149	AI	Diversity antenna interface	

NOTE

Only passive antennas are supported.

Table 36: Operating Frequency of SC680A-NA & SC686A-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE–FDD B2	1850–1910	1930–1990
LTE–FDD B4	1710–1755	2110–2155
LTE–FDD B5	824–849	869–894

LTE–FDD B7	2500–2570	2620–2690
LTE–FDD B12	699–716	729–746
LTE–FDD B13	777–787	746–756
LTE–FDD B14	788–798	758–768
LTE–FDD B17	704–716	734–746
LTE–FDD B25	1850–1915	1930–1995
LTE–FDD B26	814–849	859–894
LTE–FDD B66	1710–1780	2110–2200
LTE–FDD B71	663–698	617–652
LTE–TDD B41	2496–2690	2496–2690

Table 37: Operating Frequency of SC680A-EM & SC686A-EM

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE–FDD B1	1920–1980	2110–2170
LTE–FDD B2	1850–1910	1930–1990
LTE–FDD B3	1710–1785	1805–1880
LTE–FDD B4	1710–1755	2110–2155
LTE–FDD B5	824–849	869–894
LTE–FDD B7	2500–2570	2620–2690
LTE–FDD B8	880–915	925–960
LTE–FDD B20	832–862	791–821
LTE–FDD B28	703–748	758–803
LTE–TDD B38	2570–2620	2570–2620
LTE–TDD B40	2300–2400	2300–2400
LTE–TDD B41	2496–2690	2496–2690

WCDMA B1	1920–1980	2110–2170
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990

5.1.2. Tx Power

The following table shows the RF output power of the module.

Table 38: SC680A-EM & SC686A-EM Tx Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE	23 dBm ±2 dB	< -39 dBm
WCDMA	23 dBm ±2 dB	< -49 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 3.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.1.3. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 39: Conducted RF Receiving Sensitivity of SC680A-NA & SC686A-NA (Unit: dBm)

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	-98.4	-98	-101.2	-94.3
LTE-FDD B4 (10 MHz)	-97.1	-98.4	-100.8	-96.3
LTE-FDD B5 (10 MHz)	-99	-99.4	-102.2	-94.3
LTE-FDD B7 (10 MHz)	-95.9	-97.9	-100.1	-94.3
LTE-FDD B12 (10 MHz)	-98.6	-97.2	-101.1	-93.3
LTE-FDD B13 (10 MHz)	-98.6	-97.9	-101.4	-93.3
LTE-FDD B14 (10 MHz)	-98.2	-96.9	-100.7	-93.3
LTE-FDD B17 (10 MHz)	-97.3	-97.2	-100.4	-93.3
LTE-FDD B25 (10 MHz)	-98.2	-98	-101.1	-92.8
LTE-FDD B26 (10 MHz)	-98.8	-99.7	-102	-93.8
LTE-FDD B66 (10 MHz)	-96.8	-98.4	-100.7	-95.8
LTE-FDD B71 (10 MHz)	-97	-97.1	-100.2	-93.5
LTE-TDD B41 (10 MHz)	-96.2	-96.8	-99.5	-94.3

Table 40: Conducted RF Receiving Sensitivity of SC680A-EM & SC686A-EM (Unit: dBm)

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109.5	-	-	-102.4

EGSM900	-110	-	-	-102.4
DCS1800	-109.5	-	-	-102.4
PCS1900	-108	-	-	-102.4
WCDMA B1	-109.2	-109.8	-	-106.7
WCDMA B2	-108.5	-108.5	-	-104.7
WCDMA B4	-109.2	-110	-	-106.7
WCDMA B5	-109.5	-112.5	-	-104.7
WCDMA B8	-109.3	-112	-	-104.7
LTE-FDD B1 (10 MHz)	-97.5	-98	-101	-96.3
LTE-FDD B2 (10 MHz)	-97.3	-96.8	-100.2	-94.3
LTE-FDD B3 (10 MHz)	-97.5	-97.5	-101	-93.3
LTE-FDD B4 (10 MHz)	-97.3	-98	-101	-96.3
LTE-FDD B5 (10 MHz)	-98.5	-100	-102.5	-94.3
LTE-FDD B7 (10 MHz)	-95.1	-97.2	-99.5	-94.3
LTE-FDD B8 (10 MHz)	-99.3	-99.5	-102.5	-93.3
LTE-FDD B20 (10 MHz)	-99	-99	-102	-93.3
LTE-FDD B28 (10 MHz)	-99.3	-99	-102.2	-94.8
LTE-TDD B38 (10 MHz)	-96.5	-97.5	-99.3	-96.3
LTE-TDD B40 (10 MHz)	-96.5	-97.5	-100.5	-96.3
LTE-TDD B41 (10 MHz)	-95.3	-96.3	-99	-94.3

5.1.4. Reference Design

The module provides main and Rx-diversity RF antenna interfaces for antenna connection.

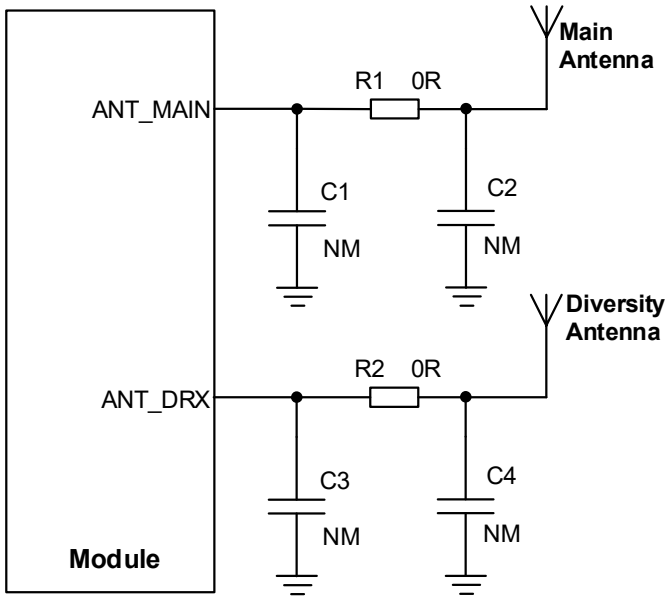


Figure 28: Reference Design of RF Antenna Interfaces

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Use a π-type matching circuit for all the antenna interfaces for better cellular performance and for the ease of debugging.
3. Capacitors are not mounted by default.
4. Place the π-type matching components (R1/C1/C2 and R2/C3/C4) to antennas as close as possible.

5.2. GNSS

The module integrates the IZat™ GNSS engine (Gen 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, BDS, Galileo and NavIC. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 41: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna interface	

Table 42: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023 1176.45 ±10.23 (L5)	MHz
GLONASS	1597.5–1605.8	
Galileo	1575.42 ±2.046	
BDS	1561.098 ±2.046	
QZSS	1575.42 ±1.023 1176.45 ±10.23 (L5)	
NavIC	1176.45 ±10.23 (L5)	

5.2.2. GNSS Performance

Table 43: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	
	Tracking	Autonomous	-158	
TTFF	Cold start @ open sky	Autonomous	34.5	s
		XTRA enabled	9.3	
	Warm start @ open sky	Autonomous	25.4	
		XTRA enabled	1.3	
	Hot start @ open sky	Autonomous	2.2	
		XTRA enabled	1.4	

Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Recommended Design of Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference design is given below.

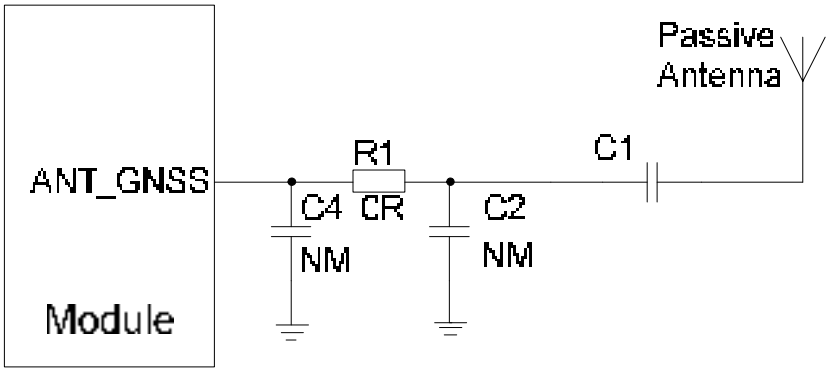


Figure 29: Reference Design of GNSS Passive Antenna

NOTE

It is not recommended to add an external LNA when using a passive GNSS antenna.

5.2.3.2. Recommended Design of Active Antenna

In any case, it is recommended to use a passive antenna. If active antenna is indeed needed in your

application, it is recommended to reserve a π-type attenuation circuit provision and use high-performance LDO as the power supply. The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high-performance LDO as the power supply. A reference design of the GNSS active antenna is shown below.

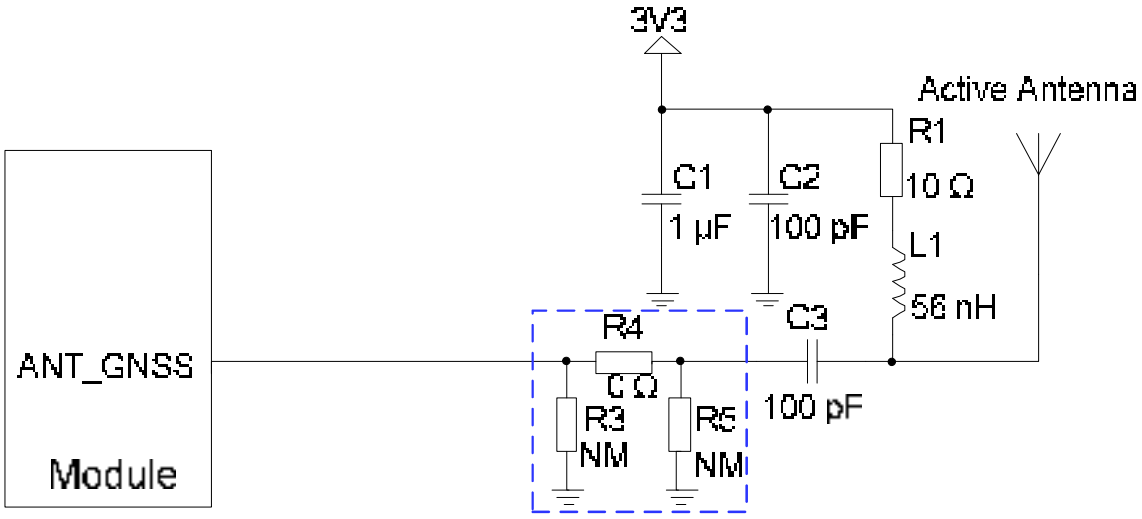


Figure 30: Reference Design of GNSS Active Antenna

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.2.3.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid this, please follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high-speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection components for the antenna interface. Only components with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, there

will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.

- Keep the impedance of either feeder line or PCB trace as 50 Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 5.2*** for the GNSS reference circuit design.

5.3. Wi-Fi/Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 44: Pin Definition of Wi-Fi/Bluetooth Application Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface	

Table 45: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi 802.11a/b/g/n/ac	2412–2462 5180–5825	MHz
BLE 5.1	2402-2480	MHz

5.3.1. Wi-Fi

The module supports 2.4 GHz and 5 GHz dual-band Wi-Fi wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. The features are as below:

- Wake-on-WLAN (WoWLAN)
- STA mode
- Wi-Fi Direct
- MCS 0–7 for HT20 and HT40
- MCS 0–8 for VHT20
- MCS 0–9 for VHT40 and VHT80

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 46: Wi-Fi Transmitting Performance

Bands	Standard	Speed Rates
2.4 GHz	802.11b	1 Mbps
	802.11b	11 Mbps
	802.11g	6 Mbps
	802.11g	54 Mbps
	802.11n HT20	MCS 0
	802.11n HT20	MCS 7
	802.11n HT40	MCS 0
	802.11n HT40	MCS 7
5 GHz	802.11a	6 Mbps
	802.11a	54 Mbps
	802.11n HT20	MCS 0
	802.11n HT20	MCS 7
	802.11n HT40	MCS 0
	802.11n HT40	MCS 7
	802.11ac VHT20	MCS 0
	802.11ac VHT20	MCS 8
	802.11ac VHT40	MCS 0
	802.11ac VHT40	MCS 9
	802.11ac VHT80	MCS 0
	802.11ac VHT80	MCS 9

Table 47: Wi-Fi Receiving Performance

Bands	Standard	Speed Rates	Sensitivity (dBm)

2.4 GHz	802.11b	1 Mbps	-97
	802.11b	11 Mbps	-89
	802.11g	6 Mbps	-90
	802.11g	54 Mbps	-74
	802.11n HT20	MCS 0	-89
	802.11n HT20	MCS 7	-71
	802.11n HT40	MCS 0	-89
	802.11n HT40	MCS 7	-69
5 GHz	802.11a	6 Mbps	-89
	802.11a	54 Mbps	-74
	802.11n HT20	MCS 0	-89
	802.11n HT20	MCS 7	-71
	802.11n HT40	MCS 0	-87
	802.11n HT40	MCS 7	-67
	802.11ac VHT20	MCS 0	-91
	802.11ac VHT20	MCS 8	-68
	802.11ac VHT40	MCS 0	-86
	802.11ac VHT40	MCS 9	-63
	802.11ac VHT80	MCS 0	-83
	802.11ac VHT80	MCS 9	-60

NOTE

The product conforms to the *IEEE 802.11a/b/g/n/ac* specifications.

5.3.2. Bluetooth

The module supports Bluetooth 5.1 (BR/EDR+BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 PICONETs at the same time.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 48: Bluetooth Data Rates and Versions

Version	Data rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 Kbit/s
2.0+EDR	3 Mbit/s	> 80 Kbit/s
3.0+HS	24 Mbit/s	Refer to 3.0 + HS
4.0	24 Mbit/s	Refer to 4.0 LE
5.1	48 Mbit/s	Refer to 5.1 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.1 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 49: Bluetooth Transmitting and Receiving Performance

Transmitting Performance			
Packet Types	DH5	2-DH5	3-DH5

Receiving Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-92	-92	-86

5.3.3. Reference Design

A reference design of Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted and a 0 Ω resistor is mounted on R1 by default.

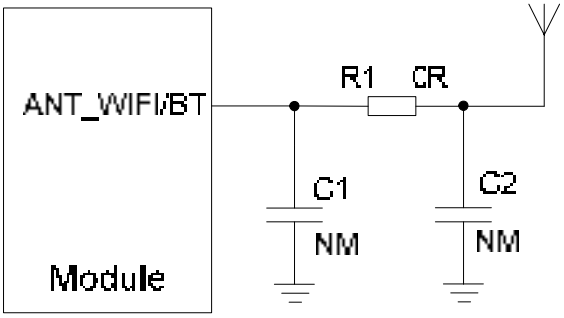


Figure 31: Reference Design of Wi-Fi/Bluetooth Antenna

5.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

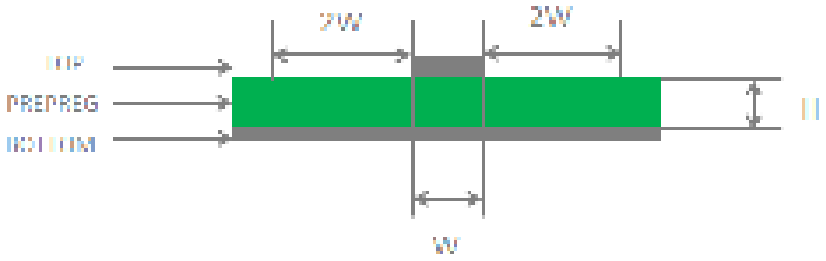


Figure 32: Microstrip Design on a 2-layer PCB

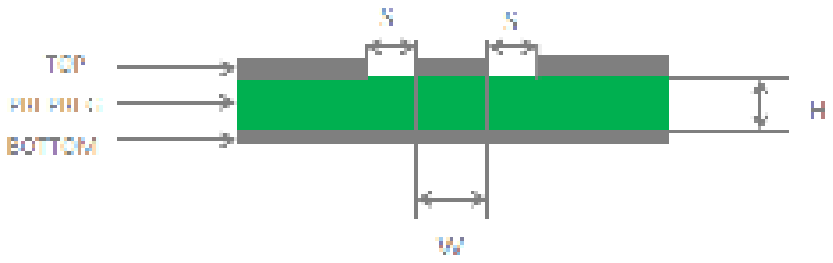


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

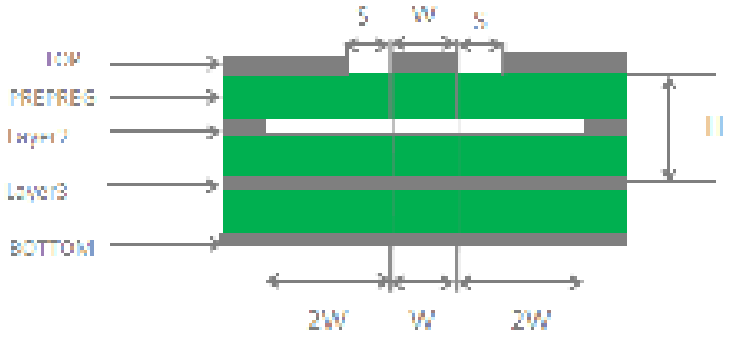


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

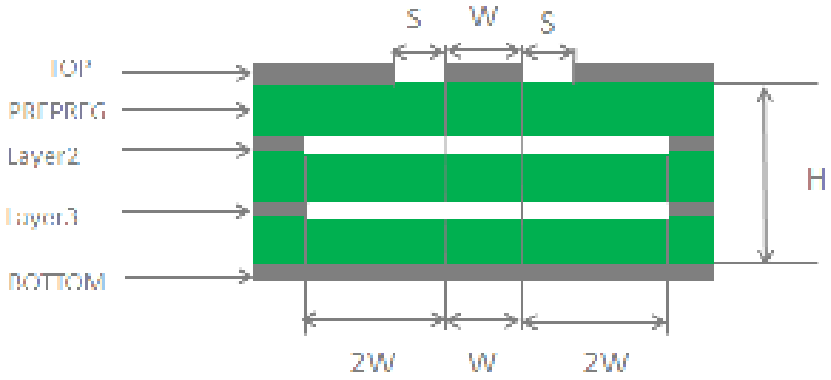


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.

- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

5.5. Antenna Design Requirements

Table 50: Antenna Design Requirements

Antenna Type	Requirements
GNSS	Frequency range :1559–1609 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB (Typ.) Active antenna embedded LNA gain: < 17 dB (Typ.)
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
Wi-Fi/Bluetooth	VSWR: ≤ 2 Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: < 1 dB

5.6. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

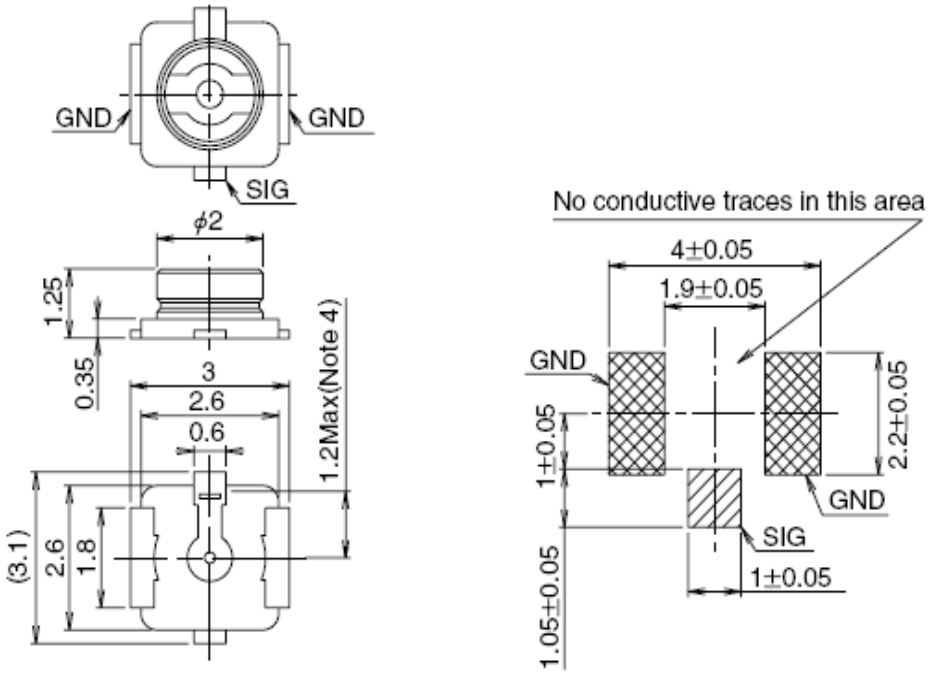


Figure 36: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

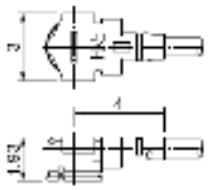
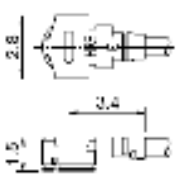
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.6	45.5	71.7
RoHS			YES		

Figure 37: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

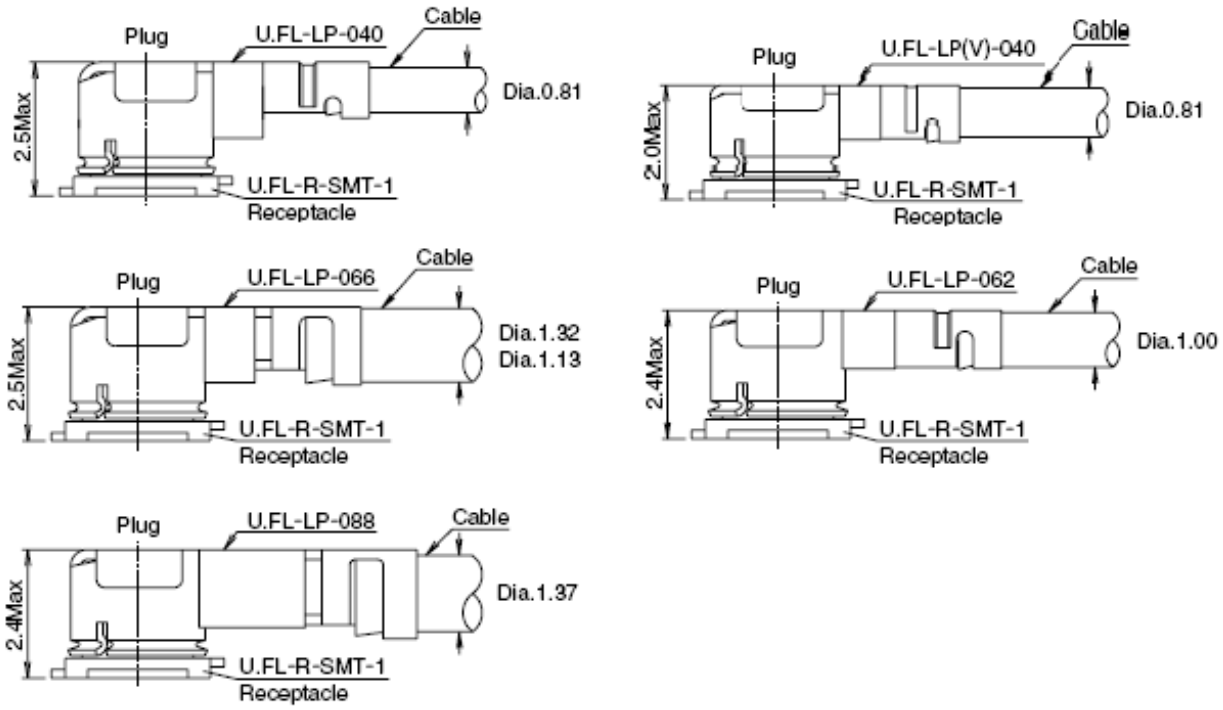


Figure 38: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 51: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	4.75	V
USB_VBUS	-0.3	16	V
Peak Current of VBAT	-	3	A
Voltage at Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 52: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.55	3.8	4.4	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900	0	0	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900	-	1.8	3.0	A

USB_VBUS	USB connection detection	4	-	10	V

6.3. Power Consumption

Table 53: SC680A-NA & SC686A-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	100	μA
Sleep state	Screen out	4.1	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	6.08	mA
	LTE-FDD PF = 64	4.93	mA
	LTE-FDD PF = 128	4.40	mA
	LTE-FDD PF = 256	4.09	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	6.24	mA
	LTE-TDD PF = 64	5.10	mA
	LTE-TDD PF = 128	4.45	mA
	LTE-TDD PF = 256	4.10	mA
LTE data transfer	LTE-FDD B2 @ max. power	657	mA
	LTE-FDD B4 @ max. power	608	mA
	LTE-FDD B5 @ max. power	595	mA
	LTE-FDD B7 @ max. power	901	mA
	LTE-FDD B12 @ max. power	749	mA
	LTE-FDD B13 @ max. power	617	mA
	LTE-FDD B14 @ max. power	593	mA
	LTE-FDD B17 @ max. power	771	mA
	LTE-FDD B25 @ max. power	736	mA

	LTE-FDD B26 @ max. power	633	mA
	LTE-FDD B66 @ max. power	583	mA
	LTE-FDD B71 @ max. power	582	mA
	LTE-TDD B41 @ max. power	402	mA

Table 54: SC680A-EM & SC686A-EM Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	TBD	μA
Sleep state	Screen out	TBD	mA
GSM supply current Sleep state (USB disconnected)	Sleep state (USB disconnected) @ DRX=2	5.63	mA
	Sleep state (USB disconnected) @ DRX=5	4.66	mA
	Sleep state (USB disconnected) @ DRX=9	4.44	mA
WCDMA supply current Sleep state (USB disconnected)	WCDMA PF = 64	4.94	mA
	WCDMA PF = 128	4.43	mA
	WCDMA PF = 256	4.23	mA
	WCDMA PF = 512	4.14	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	6.42	mA
	LTE-FDD PF = 64	5.15	mA
	LTE-FDD PF = 128	4.57	mA
	LTE-FDD PF = 256	4.26	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	6.53	mA
	LTE-TDD PF = 64	5.31	mA
	LTE-TDD PF = 128	4.67	mA
	LTE-TDD PF = 256	4.22	mA
WCDMA voice call	B1 @ max. power	582	mA

	B2 @ max. power	566	mA
	B4 @ max. power	547	mA
	B5 @ max. power	508	mA
	B8 @ max. power	510	mA
GPRS data transmission	GSM850 @ 1DL 4UL	602	mA
	GSM900 @ 1DL 4UL	568	mA
	DCS1800 @ 1DL 4UL	430	mA
	PCS1900 @ 1DL 4UL	435	mA
EDGE data transfer	GSM850 @ 1DL 4UL	598	mA
	GSM900 @ 1DL 4UL	554	mA
	DCS1800 @ 1DL 4UL	477	mA
	PCS1900 @ 1DL 4UL	473	mA
LTE data transfer	LTE-FDD B1 @ max. power	630	mA
	LTE-FDD B2 @ max. power	578	mA
	LTE-FDD B3 @ max. power	601	mA
	LTE-FDD B4 @ max. power	576	mA
	LTE-FDD B5 @ max. power	551	mA
	LTE-FDD B7 @ max. power	809	mA
	LTE-FDD B8 @ max. power	581	mA
	LTE-FDD B20 @ max. power	599	mA
	LTE-FDD B28 @ max. power	567	mA
	LTE-TDD B38 @ max. power	417	mA
	LTE-TDD B40 @ max. power	432	mA
	LTE-TDD B41 @ max. power	417	mA
GSM voice call	GSM850 @ PCL 5	318	mA
	GSM900 @ PCL 5	303	mA

	DCS1800 @ PCL 0	249	mA
	PCS1900 @ PCL 0	222	mA
WCDMA data transfer	B1 (HSDPA) @ max. power	542	mA
	B2 (HSDPA) @ max. power	514	mA
	B4 (HSDPA) @ max. power	531	mA
	B5 (HSUPA) @ max. power	472	mA
	B8 (HSDPA) @ max. power	470	mA
	B1 (HSUPA) @ max. power	547	mA
	B2 (HSUPA) @ max. power	518	mA
	B4 (HSUPA) @ max. power	537	mA
	B5 (HSUPA) @ max. power	492	mA
	B8 (HSUPA) @ max. power	490	mA

6.4. Digital I/O Characteristics

Table 55: 1.8 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.17	2.09	V
V_{IL}	Input low voltage	-0.3	0.63	V
V_{OH}	Output high voltage	1.35	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 56: SDIO 1.8 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
SD_VDD	Power supply	1.7	1.9	V

V_{IH}	Input high voltage	1.27	2	V
V_{IL}	Input low voltage	-0.3	0.58	V
V_{OH}	Output high voltage	1.4	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 57: SDIO 2.95 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
SD_VDD	Power supply	2.7	3.1	V
V_{IH}	Input high voltage	1.84	3.25	V
V_{IL}	Input low voltage	-0.3	0.74	V
V_{OH}	Output high voltage	2.21	-	V
V_{OL}	Output low voltage	-	0.37	V

Table 58: (U)SIM 1.8 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.26	2.1	V
V_{IL}	Input low voltage	-0.3	0.36	V
V_{OH}	Output high voltage	1.44	-	V
V_{OL}	Output low voltage	-	0.4	V

Table 59: (U)SIM 2.95 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.1	V
V_{IH}	Input high voltage	2.06	3.25	V

V_{IL}	Input low voltage	-0.3	0.59	V
V_{OH}	Output high voltage	2.36	-	V
V_{OL}	Output low voltage	-	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 60: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.25	-	kV

6.6. Operating and Storage Temperatures

Table 61: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	°C
Storage temperature range	-40	-	+95	°C

[3] Within the operating temperature range, the module meets 3GPP specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

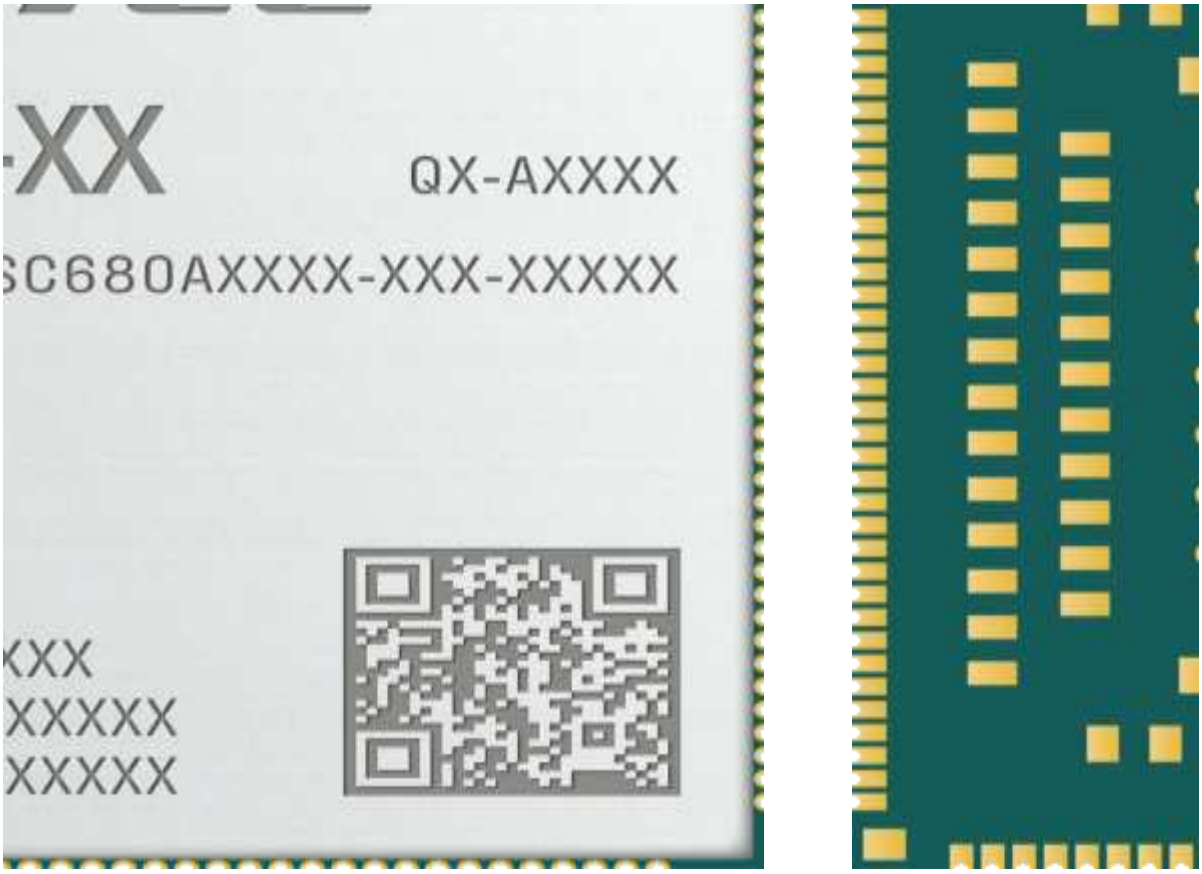


Figure 39: Module Top and Side Dimensions (Unit: mm)

Figure 40: Bottom Dimensions (Bottom View, Unit: mm)

NOTE

1. Copper leakage is prohibited at the triangle mark at the bottom of the module.
2. The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

Figure 41: Recommended Footprint (Top View)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

7.3. Top and Bottom Views

Figure 42: Top and Bottom Views of SC680A Series

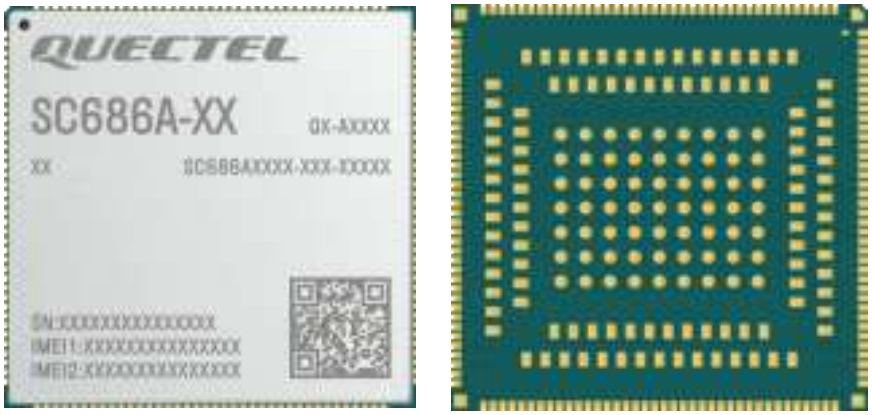


Figure 43: Top and Bottom Views of SC686A Series

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [4] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[4] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm–0.20 mm. For more details, please refer to ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

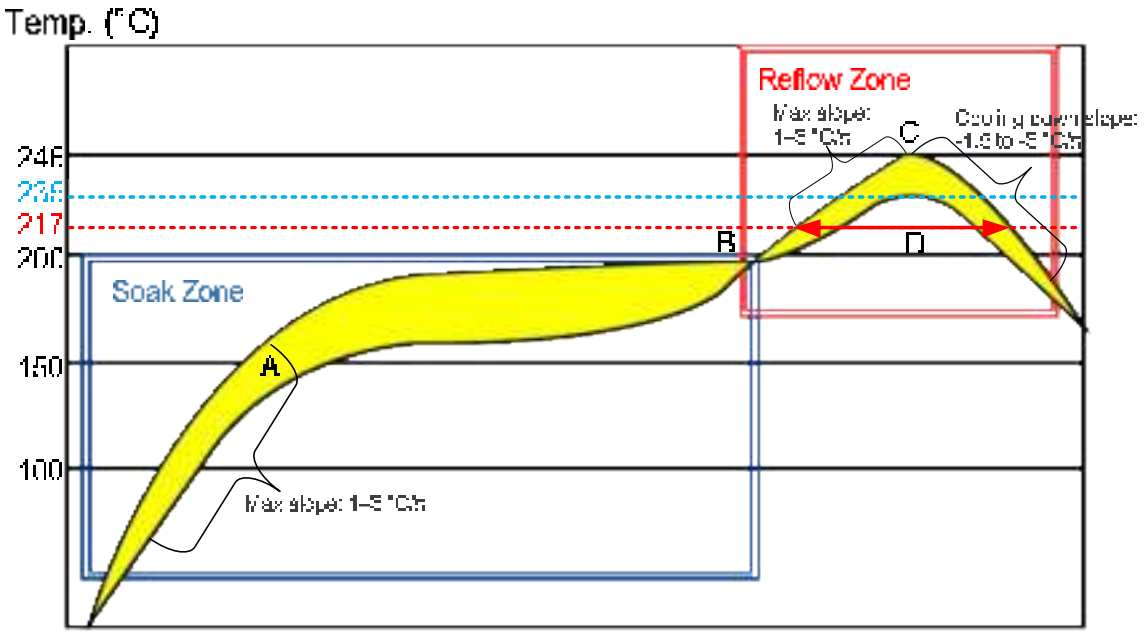


Figure 44: Recommended Reflow Soldering Thermal Profile

Table 62: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 s
Reflow Zone	
Max slope	1 to 3 °C/s
Reflow time (D: over 217 °C)	40 to 70 s
Max temperature	235 to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery. The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

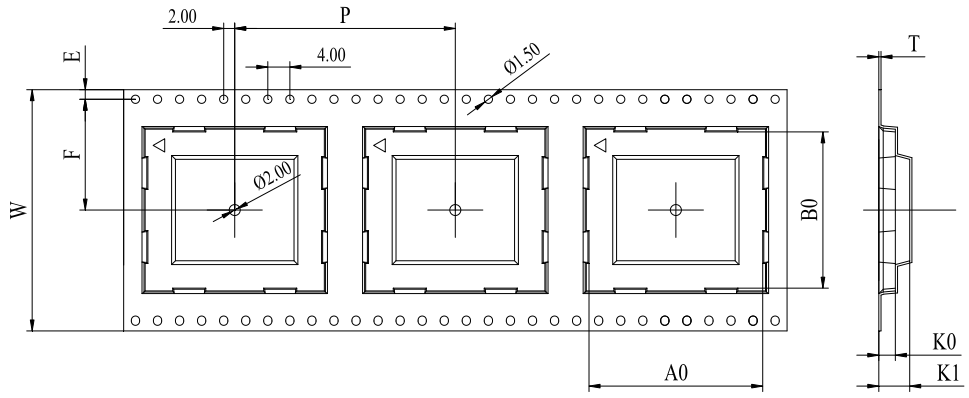


Figure 45: Carrier Tape Dimension Drawing

Table 63: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.35	44.5	43.5	4.1	5.4	34.2	1.75

8.3.2. Plastic Reel

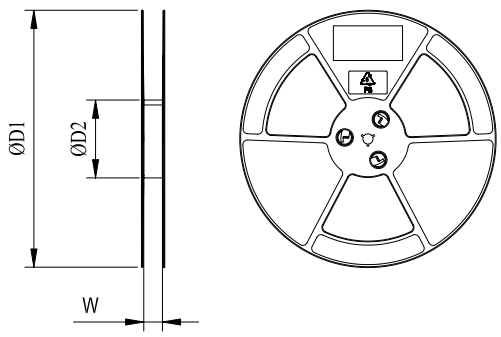
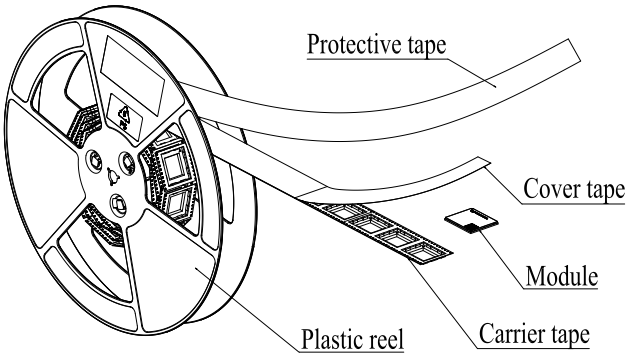


Figure 46: Plastic Reel Dimension Drawing

Table 64: Plastic Reel Dimension Table (Unit: mm)

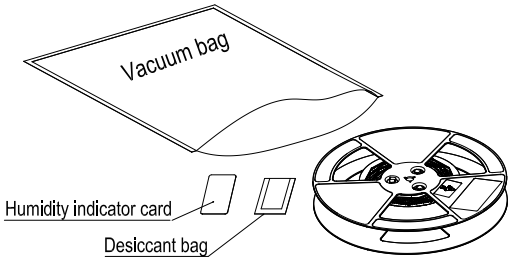
øD1	øD2	W
380	180	72.5

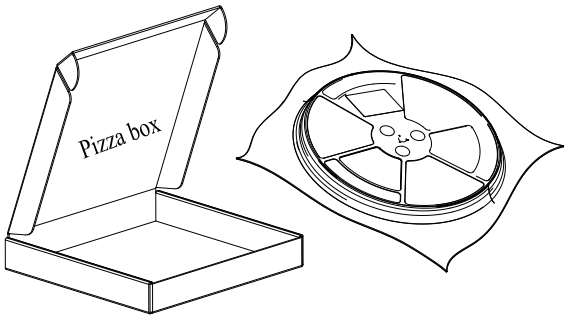
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 800 modules.

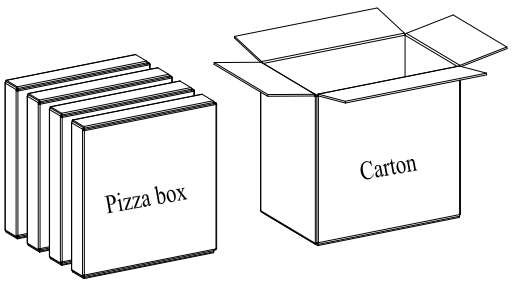


Figure 47: Packaging Process

9 Appendix References

Table 65: Related Documents

Document Name
[1] Quectel_Smart_EVB_G2_User_Guide
[2] Quectel_SC680A&SC686A_Series_GPIO_Configuration
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_User_Guide
[5] Quectel_SC680A&SC686A_Series_Reference_Design

Table 66: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
ARM	Advanced RISC Machine
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme

CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear To Send
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DCS	Data Coding Scheme
DDR	Double Data Rate
DL	Downlink
DRX	Diversity Receive
DSI	Display Serial Interface
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
eMMC	Embedded Multimedia Card
ESD	Electrostatic Discharge
EVRC	Enhanced Variable Rate Coder
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output

GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
GRFC	General RF Control
HB	High Band
HEVC	High Efficiency Video Coding
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
IoT	Internet of Things
Inom	Normal Current
ISP	Image Signal Processor
LB	Low Band
LCC	Leadless Chip Carrier (package)
LCM	Liquid Crystal Monitor
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control

MB	Middle Band
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MO	Mobile Originated
MP	Main Profile
MS	Mobile Station
MT	Mobile Terminated
NavIC	Indian Regional Navigation Satellite System (IRNSS)
NSA	Non-Stand Alone
OTA	Over-the-air programming
OTG	On-The-Go
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PHY	Physical Layer
POS	Point of Sale
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RI	Ring Indicator
RF	Radio Frequency

RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SD	Secure Digital
SIMO	Single Input Multiple Output
SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
STA	Station
TDD	Time Division Duplexing
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage

V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
ILEDmax	Maximum LED Current (per string)
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network