ATS2819 Datasheet

Version: 1.9

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Revision History

Date	Revision	Description
2018-04-16	1.0	First Release
2018-05-09	1.1	Modify
2018-05-24	1.2	Modify
2018-08-04	1.3	Modify
2018-10-09	1.4	Modify
2018-11-28	1.5	Modify
2019-01-22	1.6	Get the Bluetooth 5.0 Certification
2019-02-12	1.7	Add the description of BLE
2019-02-28	1.8	Add harmonic description of BT RF signal
2019-03-22	1.9	Modify the description of Ambient Temperature

1 Introduction

Features

- 32bit RISC processor Core, up to 180MHz.
- Internal ROM
- Internal RAM for data and program
- Internal 1MByte Nor flash
- Supports Bluetooth V5.0/4.2/2.1+EDR
- Supports AFH to dynamically detect channel quality to improve Bluetooth transmission quality
- Bluetooth Piconet and Scatternet support
- Bluetooth TX power: 4dBm(typical)
- Bluetooth RX sensitivity: -86dBm(typical) when packet Type is 2-DH5
- Built-in high performance stereo DAC& stereo ADC
- Supports two single-ended Analog microphone or one DMIC
- PA Support non-direct or direct drive output.
- Supports two stereo AUXIN sharing two ADCs
- I2S TX&RX support master/slave mode separately, and support sample rate of 192k/96k/48k/44.1k/32k/24k/22.05k/16k/12 k/11.025k/8k
- Support Voice Active Trigger
- Support 7/8pin Segment Matrix LED
- Integrated PMU supports multiple low energy states, Linear regulators outputs
- Support low power mode (sniff/sniff sub-rating)
- 1*WIO which can used for charging detection.
- Standby current 45uA (typical).
- Support two SD/SDIO interfaces at most
- Rich Interfaces support: USB1.1FS, 2xUART, 2xTWI, 2xSPI, IR RX, 9xPWM
- 22 Programmable GPIOs, and 10 analog IOs can also config as GPIOs.
- LQFP-48, 7mm*7mm*1.4mm

Applications

- Stereo speakers and speakerphones
- Bluetooth car audio unit
- Bluetooth alarm clock
- Other Bluetooth audio applications

Actions® ATS2819™ LQFP48

Bluetooth Audio Solution

Wireless Audio Applications
MMC/SD Card Audio Playback

Bluetooth V5.0

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1.1 Overview

The ATS2819 is a highly integrated single-chip Bluetooth audio device. It also can act as traditional card speakers and card-reader for data transmission.

The ATS2819 integrates the high-performance transceiver, rich features baseband processor and Bluetooth audio profile. It meets Bluetooth V5.0 and compliant with V4.2/2.1+EDR, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2819 integrates high quality and low latency SBC decoder and CVSD codec. It also supports PLC technique and AEC in voice call providing a high audio quality.

The ATS2819 integrates a complete set of power management circuits, flexible memory configuration, Matrix LED controller for UI display and rich interfaces, such as SD/SDIO/SPI/USB/UART/TWI/PWM/IR /I2S TX&RX and so on. The architecture is fully programmable with any application. It also has the minimum package and the most compact BOM.

1.2 Application Diagram

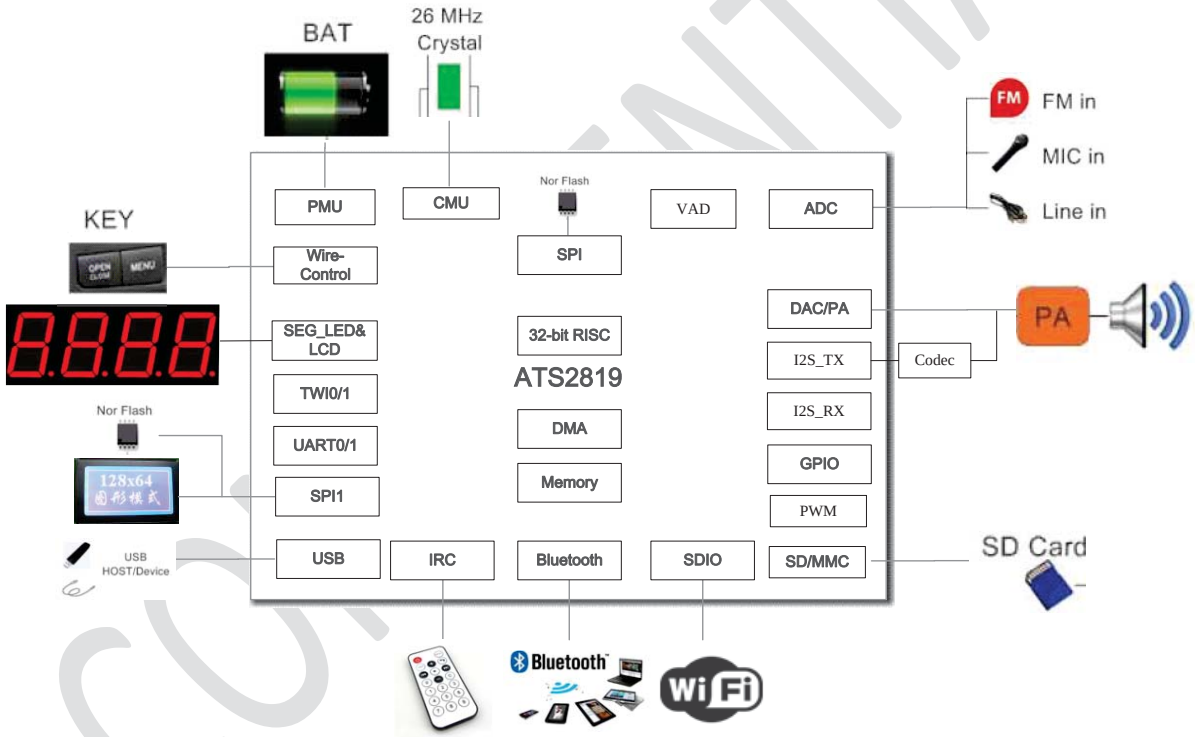


Figure 1-1 ATS2819 Application Diagram

1.3 Detail Features

System

- 32bit RISC processor Core, up to 180MHz.
- Internal RAM for data and program storage
- Internal 1MByte Nor flash
- 5-channel DMA, including DMA0, DMA1, DMA2, DMA3 and DMA4, support for transmission in burst 8 mode
- Fully configurable PEQ, up to 14 segments
- Support for echo cancellation and noise reduction
- Support for packet loss concealment
- Support USB/SDCard firmware upgrade

Bluetooth

- Bluetooth V5.0 Dual Mode
- Compatible with Bluetooth V4.2/V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Support all packet types in basic rate and enhanced data rate
- Bluetooth Dual Mode support: Simultaneous LE and BR /EDR
- Support SCO/eSCO link
- Support secure simple pairing
- Support low power mode (sniff/sniff sub-rating)
- Bluetooth Piconet and Scatternet support
- Bluetooth TX power: 4dBm(typical)
- Bluetooth RX sensitivity: -88dBm(typical) when packet Type is 2-DH5

Audio

- Built-in stereo 16-bit input sigma-delta DACs, SNR>93dB, SNR (A-Weighting)>96dB, THD+N < -80dB, THD+N (A-Weighting) < -81dB @0dBFS output amplitude
- Built-in stereo 16-bit input sigma-delta ADC, SNR>87dB, SNR(A-Weighting)>89dB, THD+N < -80dB, THD+N(A-Weighting)<-82dB @PA 1.6Vpp output
- DAC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48kHz
- PA Support non-direct or direct drive output.
- ADC supports sample rate of 8k/11.025k /12k/16k/22.05k/24k/32k/44.1k/48kHz
- Supports two single-ended Analog microphone or one DMIC
- Supports two stereo AUX IN sharing two ADCs
- I2S TX&RX support master and slave mode separately, and support sample rate of 192k/96k/48k/44.1k/32k/24k/22.05k/16k/12k/11.025k/8k
- Support Voice Active Trigger

Display

- 7/8pin Segment Matrix LED

Power Management

- Support Li-Ion battery power supply with battery insert wake up.
- Support power on button & reset button.
- Linear regulators outputs VCC, AVCC, SVCC.
- Standby current 45uA (typical).
- 10-bit A/D converters for system monitor and wire-control, 10 channels can be externally used by user. The ADC sample rate can support 2/4/8KHz per channel.
- 1*WIO which can used for charging detection.

Physical Interfaces

- Maximum 2*SD/MMC/eMMC card interface
- USB1.1FS host or device, support 2 IN endpoint and 1 OUT endpoint except endpoint0
- Maximum 2*UART support master or slave mode with RTS/CTS hardware flow control
- Maximum 2*TWI supports master or slave mode
- Maximum 2*SPI interface controllers.
- Support 22 Programmable GPIO interfaces, and 10 analog IOs can also be config as GPIOs.
- All 22 Programmable GPIOs can be SIRQs
- Maximum 9*PWM output integrated
- 1* infrared remote control RX

Package

- LQFP-48, 7mm*7mm*1.4mm

1.4 Pin Assignment

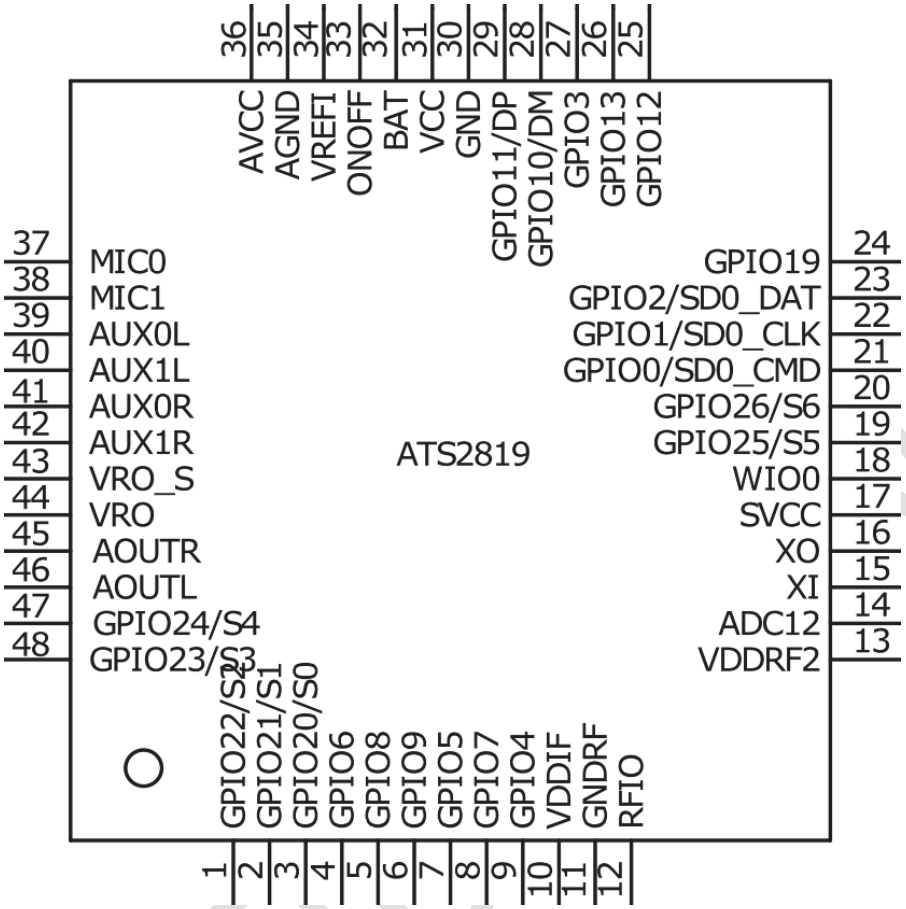


Figure 1-2 ATS2819 Pin Assignment

1.5 Pin Descriptions

Table 1-1 ATS2819 Pin Description

Pin No.	Pin Name	Pin Type	Pad drive level	GPIO Initial state	Description		Power domain
					AD_SELECT=0	AD_SELECT=1	
1	GPIO22	I/O	2/4/6/8/10/12/14/16mA	Z	Bit22 of GPIO 0x0: LCD_SEG2 0x1: GPIO22 0x2: LED_SEG2 0x3: LCD_D2 0x4: EM_D2 0x5: PWM3 0x6: I2STX_MCLK 0x7: SD1_DAT0 0x8: SPI1_MOSI	LRADC6	VCC

2	GPIO21	I/O	2/4/6/8/10/12/14/16mA	Z	Bit21 of GPIO 0x0: LCD_SEG1 0x1: GPIO21 0x2: LED_SEG1 0x3: LCD_D1 0x4: EM_D1 0x5: PWM2 0x6: I2STX_LRCLK 0x7: SD1_CLK 0x8: SPI1_CLK	LRADC5	VCC
3	GPIO20	I/O	2/4/6/8/10/12/14/16mA	Z	Bit20 of GPIO 0x0: LCD_SEG0 0x1: GPIO20 0x2: LED_SEG0 0x3: LCD_D0 0x4: EM_D0 0x5: PWM1 0x6: I2STX_BCLK 0x7: SD1_CMD 0x8: SPI1_SS	LRADC4	VCC
4	GPIO6	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade(X), Firmware boot(Z)	Bit6 of GPIO 0x0: UART0_TX 0x1: GPIO6 0x2: CK802_TMS 0x3: TWI0_SCL 0x4: Reserved 0x5: PWM5 0x6: I2STX_LRCLK 0x7: TWI1_SCL 0x8: LCD_SEG21 0x9: SPI0_CLK	AVCC	VCC
5	GPIO8	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade(X), Firmware boot(Z)	Bit8 of GPIO 0x0: UART1_TX 0x1: GPIO8 0x2: I2STX_MCLK 0x3: TWI0_SDA 0x4: SPI1_MISO 0x5: PWM6 0x6: LCD_SEG15 0x7: DMIC_CK 0x8: LCD_SEG18 0x9: SPI0_MOSI		VCC

6	GPIO9	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade(X), Firmware boot(Z)	Bit9 of GPIO 0x0: UART1_RX 0x1: GPIO9 0x2: I2STX_DOUT 0x3: TWI0_SCL 0x4: SPI1_MOSI 0x5: PWM7 0x6: SPI0_MISO 0x7: DMIC_DAT 0x8: LCD_SEG19		VCC
7	GPIO5	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade(X), Firmware boot(Z)	Bit5 of GPIO 0x0: UART0_RX 0x1: GPIO5 0x2: CK802_TCK 0x3: TWI0_SDA 0x4: IR_RX 0x5: PWM4 0x6: I2STX_BCLK 0x7: TWI1_SDA 0x8: LCD_SEG20 0x9: SPI0_SS	AVCC	VCC
8	GPIO7	I/O	2/4/6/8/10/12/14/16mA	Z	Bit7 of GPIO GPIO7	LRADC1	VCC
9	GPIO4	I/O	2/4/6/8/10/12/14/16mA	Z	Bit4 of GPIO 0x0: FMCLKOUT 0x1: GPIO4 0x2: UART0_RTS 0x3: PWM3 0x4: Reserved 0x5: UART0_TX 0x6: IR_RX 0x7: TIMER2_CAPIN 0x8: LCD_SEG17 0x9: CK802_TRST 0xA: SPI0_IO3	LRADC10	VCC
10	VDDIF	PWR			IF Power for BT		
11	GNDRF	GND			RF GND		
12	RFIO	I/O			Bluetooth transmitter output/receiver input		
13	VDDRF2	PWR			RF Power for BT		
14	ADC12	PWR			ADC Power for BT		
15	XI	AI			High frequency crystal OSC input		
16	XO	AO			High frequency crystal OSC output		
17	SVCC	PWR			Power supply for SIO and hosc		
18	WIO0	I/O		Z	Wake up IO0. It's also		SVCC

					can used as SIO, the Maximum frequency can no more than 10KHz.		
19	GPIO25	I/O	2/4/6/8/10/12/14/16mA	Z	Bit25 of GPIO 0x0: LCD_SEG5 0x1: GPIO25 0x2: LED_SEG5 0x3: LCD_D5 0x4: EM_D5 0x5: PWM6 0x6: I2SRX_MCLK 0x7: SD1_DAT3 0x8: UART0_RX	LRADC9	VCC
20	GPIO26	I/O	2/4/6/8/10/12/14/16mA	Z	Bit26 of GPIO 0x0: LCD_SEG6 0x1: GPIO26 0x2: LED_SEG6 0x3: LCD_D6 0x4: EM_D6 0x5: PWM7 0x6: Reserved 0x7: IR_RX 0x8: UART1_TX	LRADC10	VCC
21	GPIO0	I/O	2/4/6/8/10/12/14/16mA	Firmware upgrade/ card boot(X), Firmware Nor boot(Z)	Bit0 of GPIO 0x0: SD0_CMD 0x1: GPIO0 0x2: UART0_CTS 0x3: FMCLKOUT 0x4: SPI1_SS 0x5: PWM0 0x6: I2STX_BCLK 0x7: I2SRX_BCLK		VCC
22	GPIO1	I/O	2/4/6/8/10/12/14/16mA	Firmware upgrade/ card boot(X), Firmware Nor boot(Z)	Bit1 of GPIO 0x0: SD0_CLK 0x1: GPIO1 0x2: UART0_RTS 0x3: UART0_RX 0x4: SPI1_CLK 0x5: PWM1 0x6: I2STX_LRCLK 0x7: I2SRX_LRCLK		VCC

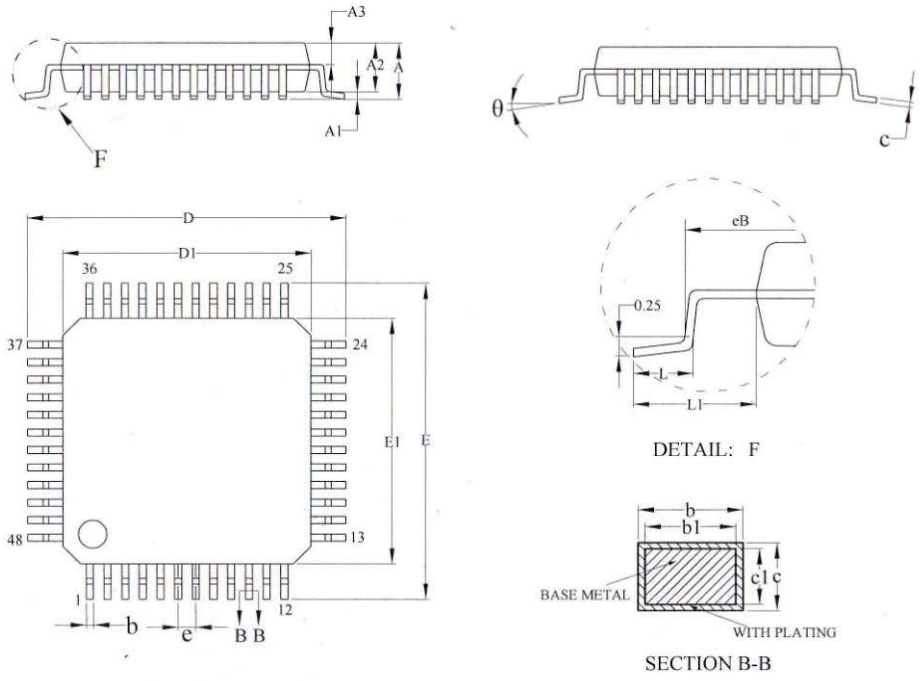
23	GPIO2	I/O	2/4/6/8/10/12/14/16mA	Firmware upgrade/ card boot(X), Firmware Nor boot(Z)	Bit2 of GPIO 0x0: SD0_DAT 0x1: GPIO2 0x2: UART0_TX 0x3: TWI0_SDA 0x4: SPI1_MOSI 0x5: IR_RX 0x6: I2STX_MCLK 0x7: I2SRX_MCLK		VCC
24	GPIO19	I/O	2/4/6/8/10/12/14/16mA	Z	Bit19 of GPIO 0x0: LCD_COM5 0x1: GPIO19 0x2: LCD_SEG23 0x3: IR_RX 0x4: EM_CEB2 0x5: PWM8 0x6: TIMER3_CAPIN 0x7: SD1_CLK 0x8: CK802_TMS	LRADC3	VCC
25	GPIO12	I/O	2/4/6/8/10/12/14/16mA	Z	Bit12 of GPIO 0x0: SPI0_IO2 0x1: GPIO12 0x2: UART0_TX 0x3: TWI1_SDA 0x4: SPI1_SS 0x5: PWM8 0x6: I2SRX_BCLK 0x7: UART1_CTS 0x8: TIMER3_CAPIN	LRADC2	VCC
26	GPIO13	I/O	2/4/6/8/10/12/14/16mA	Z	Bit13 of GPIO 0x0: SPI0_IO3 0x1: GPIO13 0x2: UART0_RX 0x3: TWI1_SCL 0x4: SPI1_CLK 0x5: IR_RX 0x6: I2SRX_LRCLK 0x7: UART1_RTS 0x8: PWM0 0x9: LED_SEG7	LRADC3	VCC

27	GPIO3	I/O	2/4/6/8/10/12/14/16mA	Z	Bit3 of GPIO 0x0: TWI0_SCL 0x1: GPIO3 0x2: UART0_CTS 0x3: PWM2 0x4: SPI1_MISO 0x5: Reserved 0x6: I2STX_DOUT 0x7: I2SRX_DI 0x8: LCD_SEG16 0x9: SPI0_IO2	LRADC9	VCC
28	GPIO10	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade (X), Firmware boot(Z)	Bit10 of GPIO 0x0: DM 0x1: GPIO10 0x2: UART1_CTS 0x3: UART0_CTS 0x4: I2SRX_DI 0x5: PWM8		VCC
29	GPIO11	I/O	2/4/6/8/10/12/14/16mA	Firmware USB upgrade (X), Firmware boot(Z)	Bit11 of GPIO 0x0: DP 0x1: GPIO11 0x2: UART1_RTS 0x3: UART0_RTS 0x4: I2SRX_MCLK 0x5: PWM0		VCC
30	GND	GND			GND		
31	VCC	PWR			IO power pin		
32	BAT	AI			Battery Voltage input		
33	ONOFF	AI			All-purpose hardware switch		
34	VREFI	AI			Voltage reference input		
35	AGND	GND			Analog GND		
36	AVCC	PWR			Power supply of Analog(3.3V)		
37	MIC0	A/I/O		Z	GPIO46	Microphone input0	AVCC
38	MIC1	A/I/O		Z	GPIO47	Microphone input1	AVCC
39	AUX0L	A/I/O		Z	GPIO40	Left channel of AUX input0	AVCC
40	AUX1L	A/I/O		Z	GPIO44	Left channel of AUX input1	AVCC
41	AUX0R	A/I/O		Z	GPIO41	Right channel of AUX input0	AVCC
42	AUX1R	A/I/O		Z	GPIO45	Right channel of AUX input1	AVCC
43	VRO_S	A/I/O		Z	GPIO39	VRO Sense for PA	VCC

44	VRO	A/I/O		Z	GPIO38	Virtual Ground for PA	VCC
45	AOUTR	A/I/O		Z	GPIO43	Right channel of AUDIO Analog output	VCC
46	AOUTL	A/I/O		Z	GPIO42	Left channel of AUDIO Analog output	VCC
47	GPIO24	I/O	2/4/6/8/10/12/14/16mA	Z	Bit24 of GPIO 0x0: LCD_SEG4 0x1: GPIO24 0x2: LED_SEG4 0x3: LCD_D4 0x4: EM_D4 0x5: PWM5 0x6: I2SRX_DI 0x7: SD1_DAT2 0x8: UART0_TX	LRADC8	VCC
48	GPIO23	I/O	2/4/6/8/10/12/14/16mA	Z	Bit23 of GPIO 0x0: LCD_SEG3 0x1: GPIO23 0x2: LED_SEG3 0x3: LCD_D3 0x4: EM_D3 0x5: PWM4 0x6: I2STX_DOUT 0x7: SD1_DAT1 0x8: SPI1_MISO	LRADC7	VCC

Note: H: high level; L:low level; Z: high resistance; X: May be change in power on;

1.6 Package and Drawings



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°

Figure 1-3 ATS2819 Package and Dimension

2 Bluetooth

- Bluetooth 5.0 Dual Mode
- Compatible with Bluetooth V4.2/ V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Support all packet types in basic rate and enhanced data rate
- Bluetooth Dual Mode support: Simultaneous LE and BR /EDR
- Support SCO/eSCO link
- Support secure simple pairing
- Support low power mode (sniff/sniff sub-rating)
- Support multiple low energy states
- Support bitpool up to 53 in SBC decoding
- Bluetooth Piconet and Scatternet support

Performance

- Bluetooth transmitting power: 4dBm(typical)
- Bluetooth RX sensitivity: -86dBm(typical) when packet Type is 2-DH5

3 Processor Core

- 32bit RISC processor Core, up to 180MHz.
- Internal RAM for data and program storage
- 5-channel DMA, including DMA0, DMA1, DMA2, DMA3 and DMA4, support for transmission in burst 8 mode

4 Memory Controller

- Operation clock rate up to 180MHz
- Memory Management Unit (MMU)
- Providing channel for DMA accessing internal memory
- Providing channel for CPU accessing internal memory
- Arbitrate the priority of CPU and DMA accessing internal memory
- Providing address remap function, biggest mapping address space is 4G Byte
- Memory Protect Unit(MPU) Support.

5 DMA Controller

5.1 Features

- DMA transmission is independent of the CPU.
- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory.
- 5-channel ordinary DMA, including DMA0, DMA1, DMA2, DMA3 and DMA4, supports for transmission in burst 8 mode. Only one of the four DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3/DMA4 transmission can be triggered on the occurrence of selected events as following
  - I2S-RX DRQ
  - ADC DRQ
  - SD/MMC DRQ
  - SD1 DRQ
  - I2S-TX/DAC DRQ
  - UART0-RX DRQ
  - UART0-TX DRQ
  - UART1-RX DRQ
  - UART1-TX DRQ
  - SPI1-RX DRQ
  - SPI1-TX DRQ
  - LCD DRQ
  - Baseband DRQ
  - modem DRQ (RF-TX debug)
  - RF-ADC DRQ (modem debug)
  - modem-TX DRQ (modem debug)
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
  - DMA4HFIP
  - DMA3HFIP
  - DMA2HFIP
  - DMA1HFIP
  - DMA0HFIP
  - DMA4TCIP
  - DMA3TCIP
  - DMA2TCIP
  - DMA1TCIP
  - DMA0TCIP
- Transmission width includes 8-bit, 16-bit, 24-bitand 32-bit, which is determined by DMA transmission type as following:
  - 8-bit: UART
  - 16-bit: ADC, DAC, I2S,LCD
  - 24-bit: I2S tx/rx
  - 32-bit: memory, BT-baseband, BT-modem, SD/MMC/SD1 and SPI1

5.2 Memory and Peripheral Access Description

5.2.1 DMA channel priority

The DMA can access the memory block, once the DMA obtains a highest priority and the DMA channel

occupies the DMA bus according to the following internal priority table of DMA channels. The possible combinations of priority of each DMA channel are listed below:

Table 5-1 Priority of Each DMA Channel

Priority	Priority0 x0 (High Priority)	Priority1 x1	Priority2 x2	Priority3 x3	Priority3 x4 (Low priority)
0	DMA0	DMA1	DMA2	DMA3	DMA4
1	DMA1	DMA0	DMA2	DMA3	DMA4
2	DMA2	DMA0	DMA1	DMA3	DMA4
3	DMA3	DMA0	DMA1	DMA2	DMA4
4	DMA4	DMA0	DMA1	DMA2	DMA3

5.3 DMA Register List

Table 5-2 DMA Control Group Base Address

Name	Physical Base Address	KSEG1 Base Address
DMAController	0xC00C0000	0xC00C0000

Table 5-3 DMA Controller Register List

Offset	Register Name	Description
0x00000000	DMAPRIORITY	DMA priority register
0x00000004	DMAIP	DMA interrupt pending register
0x00000008	DMAIE	DMA interrupt enable register
0x00000010	DMA0CTL	DMA0 control register
0x00000014	DMA0SADDR	DMA0 source address register
0x00000018	DMA0DADDR	DMA0 destination address register
0x0000001c	DMA0FRAMELEN	DMA0 frame length register
0x00000020	DMA1CTL	DMA1 control register
0x00000024	DMA1SADDR	DMA1 source address register
0x00000028	DMA1DADDR	DMA1 destination address register
0x0000002c	DMA1FRAMELEN	DMA1 frame length register
0x00000030	DMA2CTL	DMA2 control register
0x00000034	DMA2SADDR	DMA2 source address register
0x00000038	DMA2DADDR	DMA2 destination address register
0x0000003c	DMA2FRAMELEN	DMA2 frame length register
0x00000040	DMA3CTL	DMA3 control register
0x00000044	DMA3SADDR	DMA3 source address register
0x00000048	DMA3DADDR	DMA3 destination address register
0x0000004c	DMA3FRAMELEN	DMA3 frame length register
0x00000050	DMA4CTL	DMA4 control register
0x00000054	DMA4SADDR	DMA4 source address register
0x00000058	DMA4DADDR	DMA4 destination address register
0x0000005c	DMA4FRAMELEN	DMA4 frame length register
0x00000100	DMA0RemainFrameLen	DMA0 Remain Frame Length Register
0x00000104	DMA1RemainFrameLen	DMA0 Remain Frame Length Register
0x00000108	DMA2RemainFrameLen	DMA0 Remain Frame Length Register
0x0000010c	DMA3RemainFrameLen	DMA0 Remain Frame Length Register
0x00000110	DMA4RemainFrameLen	DMA0 Remain Frame Length Register

5.4 DMA Register Description

5.4.1 DMAPRIORITY

DMAPRIORITY (DMA Priority Register, offset = 0x00000000)

Bit(s)	Name	Description	Access	Reset
31:3	Reserved	Reserved	R	x
2:0	PRIORITYTAB	DMA Priority table : 3'd0 : DMA0>DMA1>DMA2>DMA3> DMA4 3'd1 : DMA1>DMA0>DMA2>DMA3> DMA4 3'd2 : DMA2>DMA0>DMA1>DMA3> DMA4 3'd3 : DMA3>DMA0>DMA1>DMA2> DMA4 3'd3 : DMA4>DMA0>DMA1>DMA2> DMA3 Other: DMA0>DMA1>DMA2>DMA3> DMA4	R/W	0x0

5.4.2 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000004)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
7:5	Reserved	Reserved	R	x
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

5.4.3 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000008)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable:	RW	0x0

		0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.		
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
7:5	Reserved	Reserved	R	x
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

5.4.4 DMA0CTL

DMA0CTL (DMA0 control Register, offset = 0x00000010)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DATAWIDTH	The data width to write to DAC/I2S TX FIFO or read from I2S RX FIFO: 0: 16bit 1: 24bit The data width to write to SPI1 TX FIFO or read from SPI1 RX FIFO: 0: 8bit 1: 32bit	RW	0x0
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: modem debug FIFO 4'b0011: UART0 TX FIFO 4'b0100: reserved 3'b0101: I2S TX/DAC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: reserved 4'b1011: reserved	RW	0x0

		4'b1100: LCD FIFO 4'b1101: SPI0 TX FIFO Other: reserved		
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0100: modem debug FIFO 4'b0101: ADC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2S RX FIFO 4'b1011: reserved 4'b1100: reserved 4'b1101: SPI0 RX FIFO Other: reserved	RW	0x0
3:2	Reserved	Reserved	R	x
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA0START	DMA0 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

5.4.5 DMA0SADDR

DMA0SADDR (DMA0 Source Address Register, offset = 0x00000014)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA0SADDR	The source address of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.6 DMA0DADDR

DMA0DADDR (DMA0 Destination Address Register, offset = 0x00000018)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA0DADDR	The destination address of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.7 DMA0FRAMELEN

DMA0FRAMELEN (DMA0 Frame Length Register, offset = 0x0000001c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMA0FRAMELEN	The frame length of DMA0 transmission. If DSTTYPE is LCD/I2S-TX/DAC/SPI **/modem FIFO,** the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is LCD/ADC/SPI/**RF-ADC FIFO/ modem-TX FIFO**, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.8 DMA1CTL

DMA1CTL (DMA1 control Register, offset = 0x00000020)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DATAWIDTH	The data width to write to DAC/I2S TX FIFO or read from I2S RX FIFO: 0: 16bit 1: 24bit The data width to write to SPI1 TX FIFO or read from SPI1 RX FIFO: 0: 8bit 1: 32bit	RW	0x0
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: modem debug FIFO 4'b0011: UART0 TX FIFO 4'b0100: reserved 3'b0101: I2S TX/DAC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: reserved 4'b1011: reserved 4'b1100: LCD FIFO 4'b1101: SPI0 TX FIFO Other: reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0100: modem debug FIFO 4'b0101: ADC FIFO 4'b0110: SD/MMC FIFO	RW	0x0

		4'b0111: SD1 FIFO 4'b1000: UART1 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2S RX FIFO 4'b1011: reserved 4'b1100: reserved 4'b1101: SPI0 RX FIFO Other: reserved		
3:2	Reserved	Reserved	R	x
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA1START	DMA1 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

5.4.9 DMA1SADDR

DMA1SADDR (DMA1 Source Address Register, offset = 0x00000024)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA1SADDR	The source address of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.10 DMA1DADDR

DMA1DADDR (DMA1 Destination Address Register, offset = 0x00000028)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA1DADDR	The destination address of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.11 DMA1FRAMELEN

DMA1FRAMELEN (DMA1 Frame Length Register, offset = 0x0000002c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMA1FRAMELEN	The frame length of DMA0 transmission. If DSTTYPE is LCD/I2S-TX/DAC/SPI **/modem FIFO,** the value of DMA0FrameLen is equal to the times	RW	0x0

		that DMA writes FIFO. If SRCTYPE is LCD/ADC/SPI/**RF-ADC FIFO/ modem-TX FIFO**, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.		

5.4.12 DMA2CTL

DMA2CTL (DMA2 control Register, offset = 0x00000030)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DATAWIDTH	The data width to write to DAC/I2S TX FIFO or read from I2S RX FIFO: 0: 16bit 1: 24bit The data width to write to SPI1 TX FIFO or read from SPI1 RX FIFO: 0: 8bit 1: 32bit	RW	0x0
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: modem debug FIFO 4'b0011: UART0 TX FIFO 4'b0100: reserved 3'b0101: I2S TX/DAC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: reserved 4'b1011: reserved 4'b1100: LCD FIFO 4'b1101: SPI0 TX FIFO Other: reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0100: modem debug FIFO 4'b0101: ADC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2S RX FIFO 4'b1011: reserved 4'b1100: reserved 4'b1101: SPI0 RX FIFO Other: reserved	RW	0x0
3:2	Reserved	Reserved	R	x

1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA2START	DMA2 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

5.4.13 DMA2SADDR

DMA2SADDR (DMA2 Source Address Register, offset = 0x00000034)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA2SADDR	The source address of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.14 DMA2DADDR

DMA2DADDR (DMA2 Destination Address Register, offset = 0x00000038)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA2DADDR	The destination address of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.15 DMA2FRAMELEN

DMA2FRAMELEN (DMA2 Frame Length Register, offset = 0x0000003c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMA2FRAMELEN	The frame length of DMA0 transmission. If DSTTYPE is LCD/I2S-TX/DAC/SPI **/modem FIFO,** the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is LCD/ADC/SPI/**RF-ADC FIFO/ modem-TX FIFO**, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.16 DMA3CTL

DMA3CTL (DMA3 control Register, offset = 0x00000040)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DATAWIDTH	The data width to write to DAC/I2S TX FIFO or read from I2S RX FIFO: 0: 16bit 1: 24bit The data width to write to SPI1 TX FIFO or read from SPI1 RX FIFO: 0: 8bit 1: 32bit	RW	0x0
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: modem debug FIFO 4'b0011: UART0 TX FIFO 4'b0100: reserved 3'b0101: I2S TX/DAC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: reserved 4'b1011: reserved 4'b1100: LCD FIFO 4'b1101: SPI0 TX FIFO Other: reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0100: modem debug FIFO 4'b0101: ADC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2S RX FIFO 4'b1011: reserved 4'b1100: reserved 4'b1101: SPI0 RX FIFO Other: reserved	RW	0x0
3:2	Reserved	Reserved	R	x
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA3START	DMA3 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically	RW	0x0

		cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.		

5.4.17 DMA3SADDR

DMA3SADDR (DMA3 Source Address Register, offset = 0x00000044)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA3SADDR	The source address of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.18 DMA3DADDR

DMA3DADDR (DMA3 Destination Address Register 0, offset = 0x00000048)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA3DADDR	The destination address of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.19 DMA3FRAMELEN

DMA3FRAMELEN (DMA3 Frame Length Register, offset = 0x0000004c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMA3FRAMELEN	The frame length of DMA0 transmission. If DSTTYPE is LCD/I2S-TX/DAC/SPI **/modem FIFO,** the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is LCD/ADC/SPI/**RF-ADC FIFO/ modem-TX FIFO**, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.20 DMA4CTL

DMA4CTL (DMA4 control Register, offset = 0x00000050)

Bit(s)	Name	Description	Access	Reset
31:13	Reserved	Reserved	R	x
12	DATAWIDTH	The data width to write to DAC/I2S TX FIFO or read from I2S RX FIFO: 0: 16bit 1: 24bit The data width to write to SPI1 TX FIFO or read from SPI1 RX FIFO: 0: 8bit 1: 32bit	RW	0x0

11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: modem debug FIFO 4'b0011: UART0 TX FIFO 4'b0100: reserved 3'b0101: I2S TX/DAC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: reserved 4'b1011: reserved 4'b1100: LCD FIFO 4'b1101: SPI0 TX FIFO Other: reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0001: baseband ram 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0100: modem debug FIFO 4'b0101: ADC FIFO 4'b0110: SD/MMC FIFO 4'b0111: SD1 FIFO 4'b1000: UART1 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2S RX FIFO 4'b1011: reserved 4'b1100: reserved 4'b1101: SPI0 RX FIFO Other: reserved	RW	0x0
3:2	Reserved	Reserved	R	x
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA4START	DMA4 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

5.4.21 DMA4SADDR

DMA4SADDR (DMA4 Source Address Register, offset = 0x00000054)

Bit(s)	Name	Description	Access	Reset

31:19	Reserved	Reserved	R	x
18:0	DMA4SADDR	The source address of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.22 DMA4DADDR

DMA4DADDR (DMA4 Destination Address Register 0, offset = 0x00000058)

Bit(s)	Name	Description	Access	Reset
31:19	Reserved	Reserved	R	x
18:0	DMA4DADDR	The destination address of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.4.23 DMA4FRAMELEN

DMA4FRAMELEN (DMA4 Frame Length Register, offset = 0x0000005c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMA4FRAMELEN	The frame length of DMA0 transmission. If DSTTYPE is LCD/I2S-TX/DAC/SPI **/modem FIFO,** the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is LCD/ADC/SPI/**RF-ADC FIFO/ modem-TX FIFO**, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.24 DMA0RemainFrameLen

DMA0RemainFrameLen (DMA0 Remain Frame Length Register, offset = 0x00000100)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	-	-	-
17:0	DMA0RemainFrameLen	The remain frame length of DMA0 transmission. If DSTTYPE is I2S TX (DAC) FIFO or ASRC TX FIFO or PCM TX FIFO or LCD FIFO, the value of DMA0RemainFrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or ASRC RX FIFO or PCM RX FIFO, the value of DMA0RemainFrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0RemainFrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.25 DMA1RemainFrameLen

DMA1RemainFrameLen (DMA1 Remain Frame Length Register, offset = 0x00000104)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	-	-	-

17:0	DMA1Remain FrameLen	The remain frame length of DMA1 transmission. If DSTTYPE is I2S TX (DAC) FIFO or ASRC TX FIFO or PCM TX FIFO or LCD FIFO, the value of DMA1RemainFrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or ASRC RX FIFO or PCM RX FIFO, the value of DMA1RemainFrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA1RemainFrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.26 DMA2RemainFrameLen

DMA2RemainFrameLen (DMA2 Remain Frame Length Register, offset = 0x00000108)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	-	-	-
17:0	DMA2Remain FrameLen	The remain frame length of DMA2 transmission. If DSTTYPE is I2S TX (DAC) FIFO or ASRC TX FIFO or PCM TX FIFO or LCD FIFO, the value of DMA2RemainFrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or ASRC RX FIFO or PCM RX FIFO, the value of DMA2RemainFrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA2RemainFrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.27 DMA3RemainFrameLen

DMA3RemainFrameLen (DMA3 Remain Frame Length Register, offset = 0x0000010c)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	-	-	-
17:0	DMA3Remain FrameLen	The remain frame length of DMA3 transmission. If DSTTYPE is I2S TX (DAC) FIFO or ASRC TX FIFO or PCM TX FIFO or LCD FIFO, the value of DMA3RemainFrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or ASRC RX FIFO or PCM RX FIFO, the value of DMA3RemainFrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA3RemainFrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

5.4.28 DMA4RemainFrameLen

DMA4RemainFrameLen (DMA4 Remain Frame Length Register, offset = 0x00000110)

Bit(s)	Name	Description	Access	Reset
31:18	Reserved	-	-	-

17:0	DMA4Remain FrameLen	The remain frame length of DMA4 transmission. If DSTTYPE is I2S TX (DAC) FIFO or ASRC TX FIFO or PCM TX FIFO or LCD FIFO, the value of DMA4RemainFrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or ASRC RX FIFO or PCM RX FIFO, the value of DMA4RemainFrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA4RemainFrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6 PMU

6.1 Features

The ATS2819 integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery power supply with battery insert wake up and fully charged wakeup.
- Supports power on button & reset button.
- Supports 1*WIO which can used for charging detection.
- Supports alarm wake up.
- Standby current 45uA (typical).
- 10bit A/D converters for Battery voltage monitor, and wire-controller.
- Linear regulators output SVCC, VCC and AVCC.

6.2 Module Description

6.2.1 Linear Regulators

The ATS2819 integrates multiple linear regulators; they generate SVCC, VCC and AVCC.

6.2.1.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within ±2%. Table below shows data of maximum output current.

Table 6-1 Regulators Maximum Output Current

LDO	Default Output Voltage (V)	capacitance	Load Capacity (mA)
SVCC	3.1	1UF	10
VCC	3.1	1~10UF	300
AVCC	2.95	1~10UF	40
VDD	1.2	CAPLESS	60

6.2.2 A/D Converters

ATS2819 integrates one 10-bit SRADC module which can be separated to 12 channels, one channel used to sample battery voltage called BATADC, one channel used to sample AVCC voltage called AVCCADC, the other 10 channels used to sample external analog inputs called LRADC.
The ADC sample rate can set to be 2/4/8KHz by setting the LRADC Controller Clock Divisor. The input

range of BATADC is 0 to 4.8V.The input range of AVCCADC and LRADC is 0 to 3V.The reference voltage is 1.5V. LRADC1 can use internal 100K pull up resistor. The 100K resistor precision will be 2% after trimming.

6.2.3 WIO Wake Up

ATS2819 supports wake up from standby by 1 WIO: WIO0 with High level, low level, rising edge or falling edge signal. It's also can used as SIO, the Maximum frequency can no more than 10KHz.

6.3 Register List

Table 6-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address
PMU	0xc0020000	0xc0020000

Table 6-3 PMU Block Configuration Registers List

Offset	Register Name	Description
0x00	VOUT_CTL	VCC/VDD/AVCC/AVDD voltage set Register
0x04	PMUADC_CTL	PMU ADC enable Register
0x08	BATADC_DATA	BATADC data Register
0x10	LRADC1_DATA	LRADC1 data Register
0x14	LRADC2_DATA	LRADC2 data Register
0x18	LRADC3_DATA	LRADC3 data Register
0x1C	LRADC4_DATA	LRADC4 data Register
0x20	LRADC5_DATA	LRADC5data Register
0x24	LRADC6_DATA	LRADC6 data Register
0x28	LRADC7_DATA	LRADC7 data Register
0x2C	LRADC8_DATA	LRADC8 data Register
0x30	LRADC9_DATA	LRADC9 data Register
0x34	LRADC10_DATA	LRADC10 data Register
0x44	POWER_CTL	Power on/off control Register
0x4c	WKEN_CTL	Wake up source select Register
0x50	WAKE_PD	Wake up source pending Register
0x54	ONOFF_KEY	On/off Key control Register

6.4 Register Description

6.4.1 VOUT_CTL

Voltage set register (VDD) offset:0x00

Bit(s)	Name	Description	R/W	Reset
31:20	-	Reserved for analog future use	R /W	X
19	SEG_DISP_VCC_EN	SEG LCD power control 0: disable 1: enable	R/W	0
18	SEG_LED_EN	SEG LED power control	R/W	0

		0: disable 1: enable		
17:0	-	Forbidden to be operated	R/W	0x30c48

6.4.2 PMUADC_CTL

PMUADC Control Register offset:0x04

Bit(s)	Name	Description	R/W	Reset
31:12	-	RESERVED	R	0
11	LRADC10_EN	LRADC10 enable. 0: Disable 1: Enable	R/W	0
10	LRADC9_EN	LRADC9 enable. 0: Disable 1: Enable	R/W	0
9	LRADC8_EN	LRADC8 enable. 0: Disable 1: Enable	R/W	0
8	LRADC7_EN	LRADC7 enable. 0: Disable 1: Enable	R/W	0
7	LRADC6_EN	LRADC6 enable. 0: Disable 1: Enable	R/W	0
6	LRADC5_EN	LRADC5 enable. 0: Disable 1: Enable	R/W	0
5	LRADC4_EN	LRADC4 enable. 0: Disable 1: Enable	R/W	0
4	LRADC3_EN	LRADC3 enable. 0: Disable 1: Enable	R/W	0
3	LRADC2_EN	LRADC2 enable. 0: Disable 1: Enable	R/W	0
2	LRADC1_EN	LRADC1 enable. 0: Disable 1: Enable	R/W	1
1	-	RESERVED	R/W	1
0	BATADC_EN	BATADC enable 0: Disable 1: Enable	R/W	1

6.4.3 BATADC_DATA

BATADC DATA Register Offset=0x08

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	BATADC	10-bit data, used to indicate Battery voltage. Input voltage range is:0~4.8V	R	xx

6.4.4 LRADC1_DATA

LRADC1 DATA Register Offset=0x10

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC1	10-bit data, used to indicate external analog channel 0 voltage	R	xx

6.4.5 LRADC2_DATA

LRADC2 DATA Register Offset=0x14

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC2	10-bit data, used to indicate external analog channel 1 voltage	R	xx

6.4.6 LRADC3_DATA

LRADC3 DATA Register Offset=0x18

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC3	10-bit data, used to indicate external analog channel 2 voltage	R	xx

6.4.7 LRADC4_DATA

LRADC4 DATA Register Offset=0x1C

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC4	10-bit data, used to indicate external analog channel 3 voltage	R	xx

6.4.8 LRADC5_DATA

LRADC5 DATA Register Offset=0x20

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC5	10-bit data, used to indicate external analog channel 5 voltage	R	xx

6.4.9 LRADC6_DATA

LRADC6 DATA Register Offset=0x24

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC6	10-bit data, used to indicate external analog channel 6 voltage	R	xx

6.4.10 LRADC7_DATA

LRADC7 DATA Register Offset=0x28

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC7	10-bit data, used to indicate external analog channel 7 voltage	R	xx

6.4.11 LRADC8_DATA

LRADC8 DATA Register Offset=0x2C

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC8	10-bit data, used to indicate external analog channel 8 voltage	R	xx

6.4.12 LRADC9_DATA

LRADC9 DATA Register Offset=0x30

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC9	10-bit data, used to indicate external analog channel 9 voltage	R	xx

6.4.13 LRADC10_DATA

LRADC10 DATA Register Offset=0x34

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC10	10-bit data, used to indicate external analog channel 10 voltage	R	xx

6.4.14 POWER_CTL

Power on/off Control Register (RTCVDD) Offset = 0x44 default:0x1

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	X
0	EN_S1	0: power off 1: power on	R/W	1

6.4.15 WKEN_CTL

Wake up source enable register Offset = 0x4C

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0
19:18	-	Reserved	R/W	0
17:16	WIO0_WKDIR	WIO0 wake up type: 00: High level 01: Low level 10: rising edge 11: falling edge	R/W	0
15:8	-	Reserved for future use	R/W	0
7	-	Reserved	R/W	0
6	WIO0_WKEN	WIO0 wake up control: 0: disable	R/W	0

		1: enable		
5	ALARM_WKEN	ALARM wake up control: 0: disable 1: enable	R/W	1
4	BAT_WKEN	Battery insertion wake up control: 0: disable 1: enable	R/W	1
3	UVLO_WKEN	BAT>4.3V wake up control: 0: disable 1: enable	R/W	1
2	RESET_WKEN	Reset key wake up enable: 0: disable 1: enable	R/W	1
1	SHORT_WKEN	Onoff key short press wake up enable: 0: disable 1: enable	R/W	0
0	LONG_WKEN	Onoff key long press wake up enable: 0: disable 1: enable	R/W	1

6.4.16 WAKE_PD

Wake up source pending register Offset = 0x50

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	X
7	-	Reserved	R/W	0
6	WIO0_PD	WIO0 wake up pending: 0: noWIO0 wake up 1: WIO0 wake up	R/W	0
5	ALARM_PD	ALARM wake up pending: 0: no ALARM wake up 1: ALARM wake up	R/W	0
4	BATIN_PD	Battery insertion wake up pending bit: 0: no battery insertion wake up 1: battery insertion wake up	R/W	0
3	UVLO_PD	BAT>4.3V wake up pending: 0: no BAT>4.3V wake up 1: BAT>4.3V wake up	R/W	0
2	RESET_PD	Reset key press pending: 0: no reset key pressed 1: reset key pressed Write 1 to clear to 0	R/W	0
1	ONOFF_PD	ONOFF wake up pending bit: 0: no ONOFF wake up 1: ONOFF wake up Write 1 to clear to 0	R/W	0
0	LONG_ONOFF	Long press onoff key pending bit: 0: no long press on play key 1: long press on play key Write 1 to clear to 0	R/W	0

6.4.17 ONOFF_KEY

ONOFF key control & detect register Offset = 0x54

Bit(s)	Name	Description	R/W	Reset
31:11	-	Reserved	R	X
10	RESTART_SET	RESET key function setting: 0: reset vdd domain register, generate pending 1: restart, press reset and enter standby, key uplift will wake up and enter active	RW	0

9:7	ONOFF_PRESS_TIME	ONOFF key time setting:
		000: 50ms < t < 0.125s, short press;
		t >= 0.125s, long press;
		001: 50ms < t < 0.25s, short press;
		t >= 0.25s, long press;
		010: 50ms < t < 0.5s, short press;
		t >= 0.5s, long press;
		011: 50ms < t < 1s, short press;
		t >= 1s, long press;
		100: 50ms < t < 1.5s, short press;
		t >= 2s, long press;
		101: 50ms < t < 2s, short press;
		t >= 2s, long press;
		110: 50ms < t < 3s, short press;
		t >= 3s, long press;
		111: 50ms < t < 4s, short press;
		t >= 4s, long press;
			RW	001

6	ONOFF_RST_EN	ONOFF long press reset function: 0: disable 1: enable	RW	1
5:4	ONOFF_RST_T_SEL	Long press ONOFF key send reset signal, time selection: 00: 8s 01: 12s 10: 16s 11: 24s	R/W	00
3:2	-	Reserved	R	X
1	ONOFF_PRESS_1	RESET/RESTART key pressed or not: 0: RESET key not pressed down 1: RESET key pressed down	R	0
0	ONOFF_PRESS_0	ONOFF key pressed or not: 0: ONOFF key not pressed down 1: ONOFF key pressed down	R	0

7 Audio

- Built-in stereo 16-bit input sigma-delta DACs, SNR>93dB, SNR (A-Weighting)>96dB, THD+N < -80dB, THD+N (A-Weighting) < -81dB @0dBFS output amplitude
- Built-in stereo 16-bit input sigma-delta ADC, SNR>87dB, SNR(A-Weighting)>89dB, THD+N < -80dB, THD+N(A-Weighting)<-82dB @PA 1.6Vpp output
- DAC supports sample rate of 8k/11.025k/12k/16k/22.05k/24k/32k/44.1k/48kHz
- PA Support non-direct or direct drive output.
- ADC supports sample rate of 8k/11.025k/12k/16k/22.05k/24k/32k/44.1k/48kHz
- Supports two single-ended Analog microphone or one DMIC
- Supports two stereo AUX IN sharing two ADC
- I2S TX&RX support master and slave mode separately, and support sample rate of 192k/96k/48k/44.1k/32k/24k/22.05k/16k/12k/11.025k/8k

8 UI

8.1 SEG LCD/LED controller

8.1.1 Features

- Support 7/8 pin COM and SEG Matrix LED Driver
- Support LED segment analog constant current configuration
- Support HOSC/LOSC for clock source

8.1.2 Register List

Table 8-1SEG_SREEN Registers Address

Name	Physical Base Address	KSEG1 Base Address
SEG_SCREEN	0xc019_0000	0xc0190000

Table 8-2 CMU Controller Registers

Offset	Register Name	Description
0x0000	SEG_DISP_CTL	Seg LCD control register
0x0004	SEG_DISP_DATA0	Seg LCD data register0
0x0008	SEG_DISP_DATA1	Seg LCD data register1
0x000C	SEG_DISP_DATA2	Seg LCD data register2
0x0010	SEG_DISP_DATA3	Seg LCD data register3
0x0014	SEG_DISP_DATA4	Seg LCD data register4
0x0018	SEG_DISP_DATA5	Seg LCD data register5
0x001c	SEG_RC_EN	LED SEG Restrict Current Enable
0x0020	SEG_BIAS_EN	LED SEG Bias Current Enable

8.1.3 Register Description

8.1.3.1 SEG_DISP_CTL

Offset=0x0000
Seg-screen control register

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:8	LED_COM_DZ	Dead zone:The com of LED will got a “dead zone”, this register define the width of the dead zone: 000b: no dead zone between LED COM Beats 001b: 1/32 of the LED COM beat will be dead zone 010b: 2/32 of the LED COM beat will be dead zone 011b: 3/32 of the LED COM beat will be dead zone 100b: 4/32 of the LED COM beat will be dead zone 101b: 5/32 of the LED COM beat will be dead zone 110b: 6/32 of the LED COM beat will be dead zone 111b: 7/32 of the LED COM beat will be dead zone	R/W	0x0
7	SEGOFF	Segment Off 0:Segment is always off 1:Segment value is according to LCD_DATA P.S. Only active in COM/SEG or Digit-LED Mode	R/W	0x0
6	-	Reserved	R	0x0
5	LCD_OUT_EN	LCD&LED pad output Enable select: 0: the pads of seg_LCD and LED will output “high_Z”. 1: the pads of seg_LCD and LED output signal as it’s timing.	R/W	0x0
4	REFRSH	Refresh LCD/LED Data 0:Hold Display, Display RAM_DATA buffer value 1:Update RAM _DATA buffer from RAM _DATA register When updating the value of LCD_DATA register, write “1” to this bit, the hardware will clear this bit when the LCD_DATA has been updated.	R/W	0x0
3:0	MODE_SEL	Mode Select 0000b: 3Com,1/3 Bias SEG/COM LCD Frame-Invert 0001b: 3Com,1/3 Bias SEG/COM LCD Row-Invert 0010b: 4Com,1/3 Bias SEG/COM LCD Frame-Invert 0011b: 4Com,1/3 Bias SEG/COM LCD Row-Invert 0100b: 5Com,1/3 Bias SEG/COM LCD Frame-Invert 0101b: 5Com,1/3 Bias SEG/COM LCD Row-Invert 0110b: 6Com,1/3 Bias SEG/COM LCD Frame-Invert 0111b: 6Com,1/3 Bias SEG/COM LCD Row-Invert 1000b: 4Com Digit-LED Common-Cathode Mode 1001b: 4Com Digit-LED Common- Anode Mode 1010b: 8Com Digit-LED Common-Cathode Mode 1011b: 8Com Digit-LED Common- Anode Mode 1100b: 7Pin Matrix_LED Common-Cathode mode 1101b: 7Pin Matrix_LED Common- Anode mode 1110b: 8Pin Matrix_LED Common-Cathode mode 1111b: 8Pin Matrix_LED Common- Anode mode	R/W	0x0

8.1.3.2 SEG_DISP_DATA0

Offset=0x0004
Seg-screen data register0

Bits	Name	Description	Access	Reset
31:24	DISP_DATA0_BYTE3	SEG-LED Mode: COM3_SEG[7:0] Matrix_LED: COM3_SEG[7:0]	R/W	0x0
23:16	DISP_DATA0_BYTE2	SEG/COM Mode: COM0_SEG[23:16]. SEG-LED Mode: COM2_SEG[7:0] Matrix_LED: COM2_SEG[7:0]	R/W	0x0
15:8	DISP_DATA0_BYTE1	SEG/COM Mode:COM0_SEG[15:8]. SEG-LED Mode: COM1_SEG[7:0] Matrix_LED: COM1_SEG[7:0]	R/W	0x0
7:0	DISP_DATA0_BYTE0	SEG/COM Mode:COM 0_SEG[7:0]. SEG-LED Mode: COM0_SEG[7:0] Matrix_LED: COM0_SEG[7:0]	R/W	0x0

8.1.3.3 SEG_DISP_DATA1

Offset=0x0008
Seg-screen data register1

Bits	Name	Description	Access	Reset
31:24	COM1_byte3	SEG-LED Mode: COM7_SEG[7:0] Matrix_LED: COM7_SEG[7:0]	R/W	0x0
23:16	COM1_byte2	SEG/COM Mode:COM1_SEG[23:16]. SEG-LED Mode: COM6_SEG[7:0] Matrix_LED: COM6_SEG[7:0]	R/W	0x0
15:8	COM1_byte1	SEG/COM Mode:COM1_SEG[15:8]. SEG-LED Mode: COM5_SEG[7:0] Matrix_LED: COM5_SEG[7:0]	R/W	0x0
7:0	COM1_byte0	SEG/COM Mode:COM1_SEG[7:0]. SEG-LED Mode: COM4_SEG[7:0] Matrix_LED: COM4_SEG[7:0]	R/W	0x0

8.1.3.4 SEG_DISP_DATA2

Offset=0x000c
Seg-screen data register2

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	COM2_word	SEG/COM Mode: OM2_SEG[23:0]. if the xTH bit of this register is “1”, Com2_seg-x will on.	R/W	0x0

8.1.3.5 SEG_DISP_DATA3

Offset=0x0010

Seg-screen data register3

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	COM3_word	SEG/COM Mode:COM3_SEG[23:0]. if the xTH bit of this register is “1”, Com3_seg-x will on.	R/W	0x0

8.1.3.6 SEG_DISP_DATA4

Offset=0x0014

Seg_screen data register4

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	COM4_word	SEG/COM Mode:COM4_SEG[23:0]. if the xTH bit of this register is “1”, Com4_seg-x will on.	R/W	0x0

8.1.3.7 SEG_DISP_DATA5

Offset=0x0018

Seg_screen data register5

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	COM5_word	SEG/COM Mode:COM5_SEG[23:0]. if the xTH bit of this register is “1”, Com5_seg-x will on.	R/W	0x0

8.1.3.8 SEG_RC_EN

LED SEG Restrict Current Enable

Offset=0x1C

Bit(s)	Name	Description	R/W	Reset
31:9	Reserved	Reserved	R	0x0
7	LED_SEG7	LED SEG7 Restrict Current Enable	R/W	0x0
6	LED_SEG6	LED SEG6 Restrict Current Enable	R/W	0x0
5	LED_SEG5	LED SEG5 Restrict Current Enable	R/W	0x0
4	LED_SEG4	LED SEG4 Restrict Current Enable	R/W	0x0
3	LED_SEG3	LED SEG3 Restrict Current Enable	R/W	0x0
2	LED_SEG2	LED SEG2 Restrict Current Enable	R/W	0x0
1	LED_SEG1	LED SEG1 Restrict Current Enable	R/W	0x0
0	LED_SEG0	LED SEG0 Restrict Current Enable	R/W	0x0

8.1.3.9 SEG_BIAS_EN

LED SEG Bias Current Enable
Offset=0x20

Bit(s)	Name	Description	R/W	Reset
31:5	Reserved	Reserved	R	0x0
4	LED_SEG_ALL_EN	LED SEG Restrict Current ALL Enable 0:Disable 1:Enable	R/W	0x0
3	LED_Cathode_Anode_Mode	LED Cathode/Anode Mode 0: Cathode Mode 1: Anode Mode	R	0x0
2:0	LED_SEG_BIAS	LED SEG BIAS: 000:2mA 001:3mA 010:4mA 011:5mA 100:6 mA 101:7 mA 110:8 mA 111:9 mA	R/W	0x1

9 System Control

9.1 RMU

9.1.1 Features

The RMU Controller of ATS2819 has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.

9.1.2 Register List

Table 9-1 RMU digital part base address

Name	Physical Base Address	KSEG1 Base Address
RMU_DIGITAL	0xC0000000	0xC0000000

Table 9-2 RMU digital part register list

Offset	Register Name	Description
0x00000000	MRCR	Module Reset Control Register

9.1.3 Register Description

9.1.3.1 MRCR

MRCR (Module Reset Control Register, offset = 0x00000000)

Bit Number	Bit Mnemonic	Description	Access	Reset
31:25	RESERVED	Be read as zeros	-	-
24	IRC_RESET	IRC Reset 0: reset 1: normal	R/W	0
23	UART1_RESET	UART1 Reset 0: reset 1: normal	R/W	0
22	RESERVED	Be read as zeros	-	-
21	SEG_LCD_LED_RESET	SEG_LCD_LED Reset 0: reset 1: normal	R/W	0
20	LCD_RESET	LCD Reset 0: reset 1: normal	R/W	0
19	VAD_RESET	VAD Reset 0: reset 1: normal	R/W	0
18	IIC1_RESET	IIC Controller1 Reset 0: reset 1: normal	R/W	0
17	SPI1_RESET	SPI Controller1 Reset	R/W	0

		0: reset 1: normal		
16	SDIO_RESET	SDIO Reset: 0: reset 1: normal	R/W	0
15	MODEM_DBG_IQ_RST	MODEM debug mode IQ assemble disassemble circuit Reset 0: reset 1: normal	R/W	1
14	SPI_CACHE_RESET	SPI cache Controller Reset 0: reset 1: normal	R/W	1
13	FMCLK_RESET	FMCLK Reset: 0: reset 1: normal	R/W	0
12	AUDIO_RESET	AUDIO Controller Reset(ADC DAC IIS): 0: reset 1: normal	R/W	0
11	SDC_RESET	SDC Controller Reset 0: reset 1: normal	R/W	0
10	USB_RESET2	USB Controller Reset2 0: reset 1: normal	R/W	0
9	USB_RESET1	USB Controller Reset1 0: reset 1: normal	R/W	0
8	PWM_RESET	PWM Controller Reset 0: reset 1: normal	R/W	0
7	IIC0_RESET	IIC Controller0 Reset 0: reset 1: normal	R/W	0
6	SPI0_RESET	SPI Controller0(for SPI Nor) Reset 0: reset 1: normal	R/W	1
5	BIST_RESET	RAM BIST Reset 0: reset 1: normal	R/W	0
4	UART0_RESET	UART0 Controller Reset 0: reset 1: normal	R/W	0
3	BT_RF_RESET	RF Reset 0: reset 1: normal	R/W	0
2	BT_MODEM_RESET	Modem Reset 0: reset 1: normal	R/W	0
1	BT_BB_RESET	BaseBand Reset 0: reset 1: normal	R/W	0
0	DMA_RESET	DMA Reset 0: reset	R/W	0

		1: normal The reset bit of DMA controller is active while it is driven by MCU clock.		

9.2 CMU Digital

9.2.1 Features

The CMU (Clock Management Unit) Controller selects HOSC, CORE_PLL, CK_24M, CK_32K as the clock of each peripheral.

9.2.2 Register List

Table 9-3 CMU Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_Control_Register	0xC0001000	0xC0001000

Table 9-4 CMU Controller Registers

Offset	Register Name	Description
0x0000	CMU_SYSCLK	CMU System Clock Control Register
0x0004	CMU_DEVCLKEN	CMU Device Clock Enable Control Register
0x0008	CMU_ADDACLK	CMU ADC/DAC Clock Control Register
0x0010	CMU_I2SCLK	CMU I2S Clock Control Register
0x0014	CMU_UARTCLK	CMU UART Clock Control Register
0x0018	CMU_SD0CLK	CMU SD0 Clock Control Register
0x001C	CMU_SD1CLK	CMU SD1 Clock Control Register
0x0020	CMU_LCDCLK	CMU LCD Clock Control Register
0x0024	CMU_SEGLCDCLK	CMU SEGLCD Clock Control Register
0x0028	CMU_SPICLK	CMU SPI Clock Control Register
0x002C	CMU_FMCLK	CMU FM Clock Control Register
0x0030	CMU_VADCLK	CMU VAD Clock Control Register
0x0034	CMU_LRADCCLK	CMU LRADC Clock Control Register
0x0038	CMU_PWM0CLK	CMU PWM0 Clock Control Register
0x003C	CMU_PWM1CLK	CMU PWM1 Clock Control Register
0x0040	CMU_PWM2CLK	CMU PWM2 Clock Control Register
0x0044	CMU_PWM3CLK	CMU PWM3 Clock Control Register
0x0048	CMU_PWM4CLK	CMU PWM4 Clock Control Register
0x004C	CMU_PWM5CLK	CMU PWM5 Clock Control Register
0x0050	CMU_PWM6CLK	CMU PWM6 Clock Control Register
0x0054	CMU_PWM7CLK	CMU PWM7 Clock Control Register
0x0058	CMU_PWM8CLK	CMU PWM8 Clock Control Register
0x005C	CMU_BTCLK	CMU Bluetooth Clock Control Register
0x0060	CMU_HCL_3K2CLK	CMU HCL 3K2 Clock Control Register
0x0064	CMU_MEMCLKEN	CMU Memory Clock Enable Control Register
0x0068	CMU_MEMCLKSEL	CMU Memory Clock Select Register

9.2.3 Register Description

9.2.3.1 CMU_SYSCLK

CMU System Clock Control Register
Offset = 0x00

Bits	Name	Description	RW	Reset
31:9	-	Reserved	R	0x0
8	AHBCLKDIV	S_CLK divisor 0: /2 1: /4	R/W	0x0
7:6	-	Reserved	R	0x0
5:4	CPUCLKDIV	CPU_CLK divisor: 00: /1 01: /2 10: /4 11: /8	R/W	0x0
3:2	-	Reserved	R	0x0
1:0	CORE_CLKSEL	CORE_CLK select: 00: CK_32K 01: HOSC 10: CORE_PLL 11: CK_52M	R/W	0x0

9.2.3.2 CMU_DEVCLKEN

CMU Device Clock Enable Control Register
Offset = 0x04

Bits	Name	Description	RW	Reset
31	-	Reserved	R	0x0
30	BT_RFCLK_EN	BT RF digital clock enable bit : 0: disable 1: enable	R/W	0x0
29	BT_MODEMCLK_EN	BT MODEM clock enable bit: 0: disable; 1: enable;	R/W	0x0
28	BT_BBCLK_EN	BT BB clock enable bit: 0: disable; 1: enable;	R/W	0x0
27	BT_BB3P2K_EN	BT BB 3.2K clock enable bit: 0: disable; 1: enable;	R/W	0x0
26	-	Reserved	R	0x0
25	PWMCLKEN	PWM0/1/2/3/4/5/6/7/8 clock enable bit: 0: disable 1: enable	R/W	0x0
24	LRADCCLKEN	LRADC Controller clock enable bit : 0: disable 1: enable	R/W	0x0
23	VADCLKEN	VAD Controller clock enable bit	R/W	0x0

		0: disable 1: enable		
22	FMCLKEN	FM clock enable bit: 0: disable 1: enable	R/W	0x0
21	IRCLKEN	IR clock enable bit: 0: disable 1: enable	R/W	0x0
20	USBCLKEN	USB controller clock enable bit: 0: disable 1: enable	R/W	0x0
19	TIMER3CLKEN	Timer3 controller clock: 0: disable 1: enable	R/W	0x0
18	TIMER2CLKEN	Timer2 controller clock: 0: disable 1: enable	R/W	0x0
17	TIMER1CLKEN	Timer1 controller clock: 0: disable 1: enable	R/W	0x0
16	TIMER0CLKEN	Timer0 controller clock: 0: disable 1: enable	R/W	0x0
15	SPI1CLKEN	SPI1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
14	SPI0CLKEN	SPI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
13	TWI1CLKEN	TWI1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
12	TWI0CLKEN	TWI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
11	SEGLCDCLKEN	SEGLCD controller clock enable bit: 0: disable 1: enable	R/W	0x0
10	LCDCLKEN	LCD controller clock enable bit: 0: disable 1: enable	R/W	0x0
9	SD1CLKEN	SD1 card controller clock enable bit: 0: disable 1: enable	R/W	0x0
8	SD0CLKEN	SD0 card controller clock enable bit: 0: disable 1: enable	R/W	0x0
7	UART1CLKEN	UART1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
6	UART0CLKEN	UART0 controller clock enable bit: 0: disable 1: enable	R/W	0x0

5	I2SRXCLKEN	I2S RX Mclock enable bit: 0: disable 1: enable	R/W	0x0
4	I2STXCLKEN	I2S TX Mclock enable bit: 0: disable 1: enable	R/W	0x0
3	-	Reserved	R/W	0x0
2	DACCLKEN	DAC controller clock enable bit: 0: disable 1: enable	R/W	0x0
1	ADCCLKEN	ADC controller clock enable bit: 0: disable 1: enable	R/W	0x0
0	DMACLKEN	DMA clock enable bit: 0: disable 1: enable	R/W	0x0

9.2.3.3 CMU_ADDACLK

CMU ADC/DAC Clock Control Register
Offset = 0x08

Bits	Name	Description	RW	Reset
31:8	-	Reserved	R	0x0
7	ADCCLKPREDIV	ADC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
6:4	ADCCLKDIV	ADC_CLK Clock Divisor. see note	R/W	0x0
3	DACCLKPREDIV	DAC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
2:0	DACCLKDIV	DAC_CLK Clock Divisor. see note	R/W	0x0

9.2.3.4 CMU_I2SCLK

CMU I2S Clock Control Register
Offset = 0x10

Bits	Name	Description	RW	Reset
31:10	-	Reserved	R	0x0
9:8	I2SRXCLKSEL	I2SRX Clock Source Select: 0: I2S_CLK 1: DAC_CLK 2: CLK_I2SRX_External 3: Reserved	R/W	0x0
7	-	Reserved	R	0x0
6	I2STXCLKDIV	I2STX Clock Divisor: 0: /1 1: /2	R/W	0x0
5:4	I2STXCLKSEL	I2STX Clock Source Select: 0: I2S_CLK 1: DAC_CLK/ADC_D_CLK(loopback) 2: CLK_I2STX_External 3: Reserved	R/W	0x1

3	-	Reserved	R	0x0
2:0	I2SCLKDIV	I2S_CLK Clock Divisor. see note below	R/W	0x0

9.2.3.5 CMU_UARTCLK

CMU UART Clock Control Register
Offset = 0x14

Bits	Name	Description	RW	Reset
31:5	-	Reserved	R	0x0
4	SEL1	UART1 clock select: 0: HOSC 1: CK_24M	R/W	0x0
3:1	-	Reserved	R	0x0
0	SEL0	UART0 clock select: 0: HOSC 1: CK_24M	R/W	0x0

9.2.3.6 CMU_SD0CLK

CMU SD0 Clock Control Register
Offset = 0x18

Bits	Name	Description	RW	Reset
31:9	-	Reserved	R	0x0
8	SD0CLKSEL1	SD0 card controller clock select 1: 0: /1 1: /256	R/W	0x0
7:5	-	Reserved	R	0x0
4	SD0CLKSEL0	SD0 card controller clock select 0: 0: HOSC 1: CORE_PLL	R/W	0x0
3	-	Reserved	R	0x0
2:0	SD0CLKDIV	SD0 card controller clock divisor 000: /1 001: /2 010: /3 011: /4 100: /5 101: /6 110: /7 111: /8	R/W	0x0

9.2.3.7 CMU_SD1CLK

CMU SD1 Clock Control Register
Offset = 0x1C

Bits	Name	Description	RW	Reset
31:9	-	Reserved	R	0x0
8	SD1CLKSEL1	SD1 card controller clock select 1: 0: /1 1: /256	R/W	0x0

7:5	-	Reserved	R	0x0
4	SD1CLKSEL0	SD1 card controller clock select 0: 0: HOSC 1: CORE_PLL	R/W	0x0
3	-	Reserved	R	0x0
2:0	SD1CLKDIV	SD1 card controller clock divisor 000: /1 001: /2 010: /3 011: /4 100: /5 101: /6 110: /7 111: /8	R/W	0x0

9.2.3.8 CMU_LCDCLK

CMU LCD Clock Control Register
Offset = 0x20

Bits	Name	Description	RW	Reset
31:5	-	Reserved	R	0x0
4	LCDCLKSEL	LCD controller clock select: 0: HOSC 1: CORE_PLL	R/W	0x0
3	-	Reserved	R	0x0
2:0	LCDCLKDIV	LCD controller clock divisor: 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: reserved	R/W	0x0

9.2.3.9 CMU_SEGLCDCLK

CMU SEGLCD Clock Control Register
Offset = 0x24

Bits	Name	Description	RW	Reset
31:5	-	Reserved	R	0x0
4	CLKSEL	SEGLCD controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
3	CLKDIV1	SEGLCD controller clock divisor1: 0: /1 1: /512	R/W	0x0
2:0	CLKDIV0	SEGLCD controller clock divisor0: 0: /1 1: /2 2: /4 3: /8	R/W	0x0

		4: /16 5: /32 6~7: reserved		

9.2.3.10 CMU_SPICLK

CMU SPI Clock Control Register
Offset = 0x28

Bits	Name	Description	RW	Reset
31:14	-	Reserved	R	0x0
15:14	SEL1	SPI1 clock select: 00: CPU_CLK 01: HOSC 10: CORE_PLL 11: CK_48M	R/W	0x0
13	-	Reserved	R	0x0
12:8	DIV1	SPI1 Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0
7:6	SEL0	SPI0 clock select: 00: CPU_CLK 01: HOSC 10: CORE_PLL 11: CK_48M	R/W	0x0
5	-	Reserved	R	0x0
4:0	DIV0	SPI0 Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0

9.2.3.11 CMU_FMCLK

CMU FM Clock Control Register
Offset = 0x2C

Bits	Name	Description	RW	Reset
31:2	-	Reserved	R	0x0
1:0	FMCLKSEL	FM clock select: 00: CK_32K 01: HOSC	R/W	0x0

		10: CORE_PLL/10 11: CK_24M		

9.2.3.12 CMU_VADCLK

CMU VAD Clock Control Register
Offset = 0x30

Bits	Name	Description	RW	Reset
31:2	-	Reserved	R	0x0
1:0	CLKDIV	VAD controller clock divisor: 0: /1 1: /2 2: /4 3: /8	R/W	0x0

9.2.3.13 CMU_LRADCCLK

CMU LRADC Clock Control Register
Offset = 0x34

Bits	Name	Description	RW	Reset
31:2	-	Reserved	R	0x0
1:0	CLKDIV	LRADC Controller Clock Divisor: 00: /100 260KHz 01: /50 520KHz 10: /25 1040KHz 11: reserved	R/W	0x0

9.2.3.14 CMU_PWM0CLK

CMU PWM0 Clock Control Register
Offset = 0x38

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM0 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM0 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.15 CMU_PWM1CLK

CMU PWM1 Clock Control Register
Offset = 0x3C

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM1 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM1 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.16 CMU_PWM2CLK

CMU PWM2 Clock Control Register
Offset = 0x40

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM2 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM2 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.17 CMU_PWM3CLK

CMU PWM3 Clock Control Register
Offset = 0x44

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM3 controller clock select: 0: CK_32K	R/W	0x0

		1: HOSC		
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM3 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.18 CMU_PWM4CLK

CMU PWM4 Clock Control Register
Offset = 0x48

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM4 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM4 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.19 CMU_PWM5CLK

CMU PWM5 Clock Control Register
Offset = 0x4C

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM5 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM5 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512	R/W	0x0

		257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved		

9.2.3.20 CMU_PWM6CLK

CMU PWM6 Clock Control Register
Offset = 0x50

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM6 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM6 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.21 CMU_PWM7CLK

CMU PWM7 Clock Control Register
Offset = 0x54

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM7 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM7 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.22 CMU_PWM8CLK

CMU PWM8 Clock Control Register
Offset = 0x58

Bits	Name	Description	RW	Reset
31:13	-	Reserved	R	0x0
12	CLKSEL	PWM8 controller clock select: 0: CK_32K 1: HOSC	R/W	0x0
11:9	-	Reserved	R	0x0
8:0	CLKDIV	PWM8 controller clock divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

9.2.3.23 CMU_BTCLK

Bluetooth Clock Control Register
Offset = 0x5C

Bits	Name	Description	RW	Reset
31:10	-	Reserved	R	0x0
9:4	BT_ADDA_CLK_D	BT_ADDA_CLK delay chain select bits: BT_ADDA_CLK delay chain =BT_ADDA_CLK_D * 0.5ns;	R/W	0x00
3	BT_ADDA_CLK_INVERT	BT_ADDA_CLK invert enable: 0: disable 1: enable	R/W	0x0
2	-	Reserved	R	0x0
1	BT_MODEM_RXEN_SEL	MODEM_RXEN From BB control enable 0: MODEM_RXEN From BB control disable 1: MODEM_RXEN From BB control enable	R/W	0x0
0	BT_MODEMCLK_SEL	BT_MODEM clock gating signal select: 0: BT_MODEMCLK_EN(CLKEN_BIT29) 1: modem_en from BT_BB	R/W	0x0

9.2.3.24 CMU_HCL_3K2CLK

HCL control register
Offset = 0x60

Bit(s)	Name	Description	R/W	Reset
31:16	HCL_INTERVAL	HCL calibration interval select: HCL_INTERVAL*2 Cycle of 3.2K	R/W	0x800
15:10	Reserved	Reserved	R	X

9	HCL_BUSY	HCL circuit calibration processing status indicator: 0: HCL finish calibrated status. 1: HCL is in calibrating status.	R	X
8	HCL_SOFT_START	HCL software start bit. Write 1 to start HCL process; when HCL process is finished, this bit will be auto clear to 0;	R/W	0
7:6	HOSC_OSC_TIME	HOSC calibrate LOSC circuit HOSC oscillator time: 00: 8 Cycle of 3.2K 01: 16 Cycle of 3.2K 10: 32 Cycle of 3.2K 11: 64 Cycle of 3.2K	R/W	10
5:4	CAL_DELAY_TIME	HOSC calibrate LOSC circuit wait for HOSC oscillator time: 00: 128 Cycle of CK_32K*** 01: 256 Cycle of CK_32K 10: 512 Cycle of CK_32K 11: 1024 Cycle of CK_32K	R/W	00
3:2	HCL_PRECISION	HCL Precision select: 00: HCL CNT remain, 1 RC precision*** 01: HCL CNT remain, 1 RC precision 10: HCL CNT+1, 1 RC precision 11: HCL CNT fix, 1/2 RC precision	R/W	11
1	HCL_HCM_EN	HCL hardware calibration mode enable: 0: disable 1: enable	R/W	0
0	HCL_EN	HOSC calibrate LOSC circuit enable: 0: disable 1: enable***	R/W	0

9.2.3.25 CMU_MEMCLKEN

CMU Memory Clock Enable Control Register
Offset = 0x64

Bits	Name	Description	RW	Reset
31:12	-	Reserved	R	0x0
11	SPICACHERAMCLKEN	SPICACHERAM clock enable bit: 0: disable 1: enable	R/W	0x1
10:9	-	Reserved	R	0x0
8	URAMCLKEN	URAM clock enable bit: 0: disable 1: enable	R/W	0x1
7	PCMRAMCLKEN	PCMRAM clock enable bit: 0: disable 1: enable	R/W	0x1
6	RAM4CLKEN	RAM4 clock enable bit : 0: disable 1: enable	R/W	0x1
5	RAM3CLKEN	RAM3 clock enable bit : 0: disable	R/W	0x1

		1: enable		
4	RAM2CLKEN	RAM2 clock enable bit : 0: disable 1: enable	R/W	0x1
3	RAM1CLKEN	RAM1 clock enable bit : 0: disable 1: enable	R/W	0x1
2	RAM0CLKEN	RAM0 clock enable bit : 0: disable 1: enable	R/W	0x1
1	ROM1CLKEN	ROM1 clock enable bit : 0: disable 1: enable	R/W	0x1
0	ROM0CLKEN	ROM0 clock enable bit : 0: disable 1: enable	R/W	0x1

9.2.3.26 CMU_MEMCLKSEL

CMU Memory Clock Select Register
Offset = 0x68

Bits	Name	Description	RW	Reset
31:5	-	Reserved	R	0x0
4	URAMCLKSEL	URAM clock selection bit: 0: CPU_CLK 1: USBctl_URAM_CLK	R/W	0x0
3	PCMRAMCLKSEL	PCMRAM clock selection bit: 0: CPU_CLK 1: DAC_CLK	R/W	0x0
2:1	RAM4CLKSEL	RAM4 clock selection bit: 00: CPU_CLK 01: VAD_CLK 10: DAC_CLK	R/W	0x0
0	RAM3CLKSEL	RAM3 clock selection bit: 0: CPU_CLK 1: VAD_CLK	R/W	0x0

9.3 RTC&Watchdog

9.3.1 Features

- Built-in a 32K oscillator
- Calendar with a alarm IRQ which can wake up the PMU
- A watch dog which can be configured optional as IRQ or Reset

9.3.2 Register List

Table 9-7 RTC block base address

Name	Physical Base Address	KSEG1 Base Address
RTC	0xC0120000	0xC0120000

Table 9-8 RTC Controller Registers

Offset	Register Name	Description
0x00	RTC_CTL	RTC Control Register
0x04	RTC_REGUPDATA	RTC Register update Register
0x08	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x0C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x10	RTC_YMD	RTC Year Month Date Register
0x14	RTC_ACCESS	RTC freely access Register
0x1c	WD_CTL	Watch Dog Control register

9.3.3 Register Description

9.3.3.1 RTC_CTL

Calendar Control Register
Offset=0x00(RTCVDD)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	TEST_EN	Test enable 0: Disable 1: Enable. The RTC clock is changed to HOSC	R/W	0x0
15:8	-	Reserved	R	0x0
7	LEAP	RTC Leap Year bit 0: not leap year 1: leap year	R	0x1
6:5	-	Reserved	R	0x0
4	CAL_EN	Calendar Enable 0: Disable 1: Enable	R/W	0x0
3	-	Reserved	R	0x0
2	HCL_SELECT	Calendar clock select 0:select HCL_4Hz 1: select HOSC divisor	R/W	0x0
1	ALIE	Alarm IRQ Enable 0: Disable 1: Enable	R/W	0x0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	R/W	0x0

NOTE:
The CAL_EN bit must be disabled when The RTC_DHMS / RTC_YMD register being written. And RTC_DHMS / RTC_YMD register must be written before CAL_EN is enabled when set the time, Or error will occur.

9.3.3.2 RTC_REGUPDATA

Offset=0x04(RTCVDD)

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0

15:0	UPDATA	The RTCVDD register update control Register. When writing the RTC registers (except RTCREGUPDATE register or bit “ALIP”), the RTC registers’ values are not update immediately. The value is written to backup registers(in VDD) first. Just when writing RTCREGUPDATE register “A596H”, the RTCVDD registers’ values are update with the backup registers’ value. RTCREGUPDATE register is automatically reset as “5A69H” after the RTCVDD register is update. NOTE: Do not write RTCVDD registers when this register value is “A5C3E283H” NOTE: When writing the bit “alm_ip” and “timeout_sta”, it will take effect immediately. Do not need writing this register.	R/W	0x5A69

9.3.3.3 RTC_DHMSALM

Offset=0x08(RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	0
15:14	-	Reserved	R	0
13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	0
7:6	-	Reserved	R	0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0

9.3.3.4 RTC_DHMS

Offset=0x0C(RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0
20:16	HOUR	Time hour setting 00H – 17H	R/W	0
15:14	-	Reserved	R	0
13:8	MIN	Time minute setting 00H – 3BH	R/W	0
7:6	-	Reserved	R	0
5:0	SEC	Time second setting 00H – 3BH	R/W	0

9.3.3.5 RTC_YMD

Offset=0x10(RTCVDD)

Bits	Name	Description	Access	Reset
31:23	-	Reserved	R	0
22:16	YEAR	Time year setting 00H – 63H	R/W	00

15:12	-	Reserved	R	0
11:8	MON	Time month setting 01H – 0CH	R/W	01
7:5	-	Reserved	R	0
4:0	DATE	Time day setting 01H – 1FH	R/W	01

9.3.3.6 RTC_ACCESS

Offset=0x14(RTCVDD)

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0
7:0	ACCESS	These bits can be accessed by CPU freely.	R/W	0

9.3.3.7 WD_CTL

Offset=0x1C(VDD)

Bits	Name	Description	R/W	Reset
31:7	-	reserved	R	0
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset,1: irq-. 0: Send Reset signal when watchdog overflow. 1: Send IRQ signal when watchdog overflow.	Rw	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable	Rw	0
3:1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms 011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 10ms	Rw	0
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

9.4 TIMER

9.4.1 Features

- Four Timers with IRQS, while two as universal timer and two timer had get capture timer

9.4.2 Register List

Table 9-9 TIMER block base address

Name	Physical Base Address	KSEG1 Base Address
TIMER	0xC0120100	0xC0120100

Table 9-10 TIMER Controller Registers

Offset	Register Name	Description
0x00	T0_CTL	Timer0 Control register
0x04	T0_VAL	Timer0 Value register
0x08	T0_CNT	Timer0 count register
0x40	T1_CTL	Timer1 Control register
0x44	T1_VAL	Timer1 Value register
0x48	T1_CNT	Timer1 count register
0x80	T2_CTL	Timer2 Control register
0x84	T2_VAL	Timer2 Value register
0x88	T2_CNT	Timer2 count register
0xC0	T3_CTL	Timer3 Control register
0xC4	T3_VAL	Timer3 Value register
0xC8	T3_CNT	Timer3 count register

9.4.3 Register Description

9.4.3.1 T0_CTL

Timer0 control register
Offset=0x00(VDD)

Bits	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

9.4.3.2 T0_VAL

Timer0 value register
Offset=0x04(VDD)

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write Timer/Counter value register	RW	0x0

9.4.3.3 T0_CNT

Timer0 current counter register
Offset=0x08(VDD)

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

9.4.3.4 T1_CTL

Timer1 control register
Offset=0x40(VDD)

Bits	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

9.4.3.5 T1_VAL

Timer1 value register
Offset=0x44(VDD)

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write current Timer0 value	RW	0x0

9.4.3.6 T1_CNT

Timer1 current counter register
Offset=0x48(VDD)

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

9.4.3.7 T2_CTL

Timer2 control register
Offset=0x80(VDD)

Bits	Name	Description	R/W	Reset
31:12	-	Reserved	R	0

11	DIR	Timer direction； 0: down 1: up	RW	0x0
10	MODE_SEL	Timer mode select: 0: normal timer 1: input capture mode and counter mode	RW	0x0
9	CLK_SEL	Timer clock select 0: hosc 1: external clock or signal Used only in timer mode.	RW	0x0
8	CAPTURE_IP	Capture event irq pending Writing 1 to clear this bit.	RW	0x0
7:6	CAPTURE_SE	Capture signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge	RW	0x0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable In timer/counter mode: When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared. **If DIR='0',T2_CNT compare with ZERO** **If DIR='1',T2_CNT compare with T2_VAL.** **For more detail reference to timer0/1 block diagram** **In input capture mode** **Every trigger**	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

9.4.3.8 T2_VAL

Timer2 value register
Offset=0x84(VDD)

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write current Timer0 value	RW	0x0

9.4.3.9 T2_CNT

Timer2 current counter register
Offset=0x88(VDD)

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

9.4.3.10 T3_CTL

Timer3 control register
Offset=0xC0(VDD)

Bits	Name	Description	R/W	Reset
31:12	-	Reserved	R	0
11	DIR	Timer direction； 0: down 1: up	RW	0x0
10	MODE_SEL	Timer mode select: 0: normal timer, include timer mode and counter mode 1: input capture mode	RW	0x0
9	CLK_SEL	Timer mode clock select 0: hosc 1: external clock or signal Used only in timer mode.	RW	0x0
8	CAPTURE_IP	Input Capture mode event irq pending Writing 1 to clear this bit.	RW	0x0
7:6	CAPTURE_SE	Input Capture mode signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge	RW	0x0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable. Include timer mode and input capture mode. In timer mode, When this bit is enabled, Timer_IRQ sent out the irq signal until the pending bit was cleared. **If DIR='0',T2_CNT compare with ZERO** **If DIR='1',T2_CNT compare with T2_VAL.** **For more detail reference to timer2/3 block diagram** **In input capture mode, this bit would set be '1'when every trigger edge was found, which was set in CAPTURE_SE**	RW	0x0
0	ZIPD	Timer mode IRQ Pending, Writing 1 to clear this bit.	RW	0x0

9.4.3.11 T3_VAL

Timer3 value register
Offset=0xC4(VDD)

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write current Timer0 value	RW	0x0

9.4.3.12 T3_CNT

Timer3 current counter register

Offset=0xC8(VDD)

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

9.5 INTC (Exceptions and Interrupts Controller)

9.5.1 Features

The ATS2819 uses RISC32 processor. The ATS2819 also adds additional controller to manage up to 32 interrupt sources.

Table below shows all interrupt sources.

Table 9-11 Interrupt sources

Interrupt Number	Sources	Type
0	Reserved	-
1	PMU	High Level
2	WatchDog	High Level
3	TIMER1	High Level
4	TIMER0	High Level
5	RTC	High Level
6	UART0	High Level
7	GPIO	High Level
8	I2S	High Level
9	SPI0	High Level
10	USB	High Level
11	TWI0	High Level
12	TWI1	High Level
13	VAD	High Level
14	DAC or IIS tx	High Level
15	ADC	High Level
16	UART1	High Level
17	SD/MMC	High Level
18	DMA0	High Level
19	DMA1	High Level
20	DMA2	High Level
21	DMA3	High Level
22	DMA4	High Level
23	DMA5	High Level
24	IRC	High Level
25	SPI1	High Level
26	SDIO	High Level
27	TIMER2	High Level
28	TIMER3	High Level
29	Reserved	-
30	MPU	High Level
31	Reserved	High Level

9.5.2 Register List

The ATS2819 implements a controller to handle 32 interrupt request, the registers are listed below:

Table 9-12 Table Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address
InterruptController	0xC00B0000	0xC00B0000

Table 9-13 Interrupt Controller Registers

Offset	Register Name	Description
0x00000000	INTC_PD	Interrupt Pending register
0x00000004	INTC_MSK	Interrupt Mask register
0x00000008	INTC_CFG0	Interrupt Config register 0
0x0000000c	INTC_CFG1	Interrupt Config register 1
0x00000010	INTC_CFG2	Interrupt Config register 2

9.5.3 Register Description

9.5.3.1 INTC_PD

INTC_PD (Interrupt Pending Register, offset = 0x00000000)

Bit Number	Bit Mnemonic	Function	Access	Reset
31	Reserved	Reserved	R	0
30	MPU_IP	MPU interrupt pending bit	R	0
29	Reserved	Reserved	R	0
28	TIMER3_IP	TIMER3 interrupt pending bit	R	0
27	TIMER2_IP	TIMER2 interrupt pending bit	R	0
26	SDIO_IP	SDIO interrupt pending bit	R	0
25	SPI1_IP	SPI1 interrupt pending bit	R	0
24	IRC_IP	IRC interrupt pending bit	R	0
23	Reserved	Reserved	R	0
22	DMA4_IP	DMA4 controller interrupt pending bi	R	0
21	DMA3_IP	DMA3 controller interrupt pending bit	R	0
20	DMA2_IP	DMA2 controller interrupt pending bit	R	0
19	DMA1_IP	DMA1 controller interrupt pending bit	R	0
18	DMA0_IP	DMA0 controller interrupt pending bit	R	0
17	SD_IP	SD/MMC interrupt pending bit	R	0
16	UART1_IP	UART1 interrupt pending bit	R	0
15	ADC_IP	ADC interrupt pending bit	R	0
14	DAC_IIS_TX_IP	DAC or IIS-TX interrupt pending bit	R	0
13	VAD_IP	VAD interrupt pending bit	R	0
12	IIC1_IP	IIC1 interrupt pending bi	R	0
11	IIC0_IP	IIC0 interrupt pending bit	R	0
10	USB_IP	USB interrupt pending bit	R	0
9	SPI0_IP	SPI0 interrupt pending bit	R	0
8	I2S_IP	I2S interrupt pending bit	R	0
7	GPIO_IP	GPIO interrupt pending bit	R	0
6	UART0_IP	UART0 interrupt pending bit	R	0
5	RTC_IP	RTC interrupt pending bit	R	0
4	TIMER0_IP	TIMER0 interrupt pending bit	R	0
3	TIMER1_IP	TIMER1 interrupt pending bit	R	0

2	WD_IP	WatchDog interrupt pending bit	R	0
1	PMU_IP	PMU pending	R	0
0	BT_BASEBAND_IP	BT_Baseband pending	R	0

Note:

(1) Interrupt Pending bits can not be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.

(2) 0: no interrupt request; 1: interrupt request detected

9.5.3.2 INTC_MSK

INTC_MSK (Interrupt Mask Register, offset = 0x00000004)

Bit Number	Bit Mnemonic	Function	Access	Reset
31	Reserved	Reserved	R	0
30	MPU_IM	MPU interrupt mask bit	R/W	0
29	Reserved	Reserved	R/W	0
28	TIMER3_IM	TIMER3 interrupt mask bit	R/W	0
27	TIMER2_IM	TIMER2 interrupt mask bit	R/W	0
26	SDIO_IM	SDIO interrupt mask bit	R/W	0
25	SPI1_IM	SPI1 interrupt mask bit	R/W	0
24	IRC_IM	IRC interrupt mask bit	R/W	0
23	Reserved	Reserved	R	0
22	DMA4_IM	DMA4 controller interrupt mask bit	R/W	0
21	DMA3_IM	DMA3 controller interrupt mask bit	R/W	0
20	DMA2_IM	DMA2 controller interrupt mask bit	R/W	0
19	DMA1_IM	DMA1 controller interrupt mask bit	R/W	0
18	DMA0_IM	DMA0 controller interrupt mask bit	R/W	0
17	SD_IM	SD/MMC interrupt mask bit	R/W	0
16	UART1_IM	UART1 interrupt mask bit	R/W	0
15	ADC_IM	ADC interrupt mask bit	R/W	0
14	DAC_IIS_TX_IM	DAC or IIS-TX interrupt mask bit	R/W	0
13	VAD_IM	VAD interrupt mask bit	R/W	0
12	IIC1_IM	IIC1 interrupt mask bit	R/W	0
11	IIC0_IM	IIC0 interrupt mask bit	R/W	0
10	USB_IM	USB interrupt mask bit	R/W	0
9	SPI0_IM	SPI0 interrupt mask bit	R/W	0
8	I2S_IM	I2S interrupt mask bit	R/W	0
7	GPIO_IM	GPIO interrupt mask bit	R/W	0
6	UART0_IM	UART0 interrupt mask bit	R/W	0
5	RTC_IM	RTC interrupt mask bit	R/W	0
4	TIMER0_IM	TIMER0 interrupt mask bit	R/W	0
3	TIMER1_IM	TIMER1 interrupt mask bit	R/W	0
2	WD_IM	WatchDog interrupt mask bit	R/W	0
1	PMU_IM	PMU interrupt mask bit	R/W	0
0	BT_BASEBAND_IM	BT Baseband interrupt mask bit	R/W	0

Note:

0: Interrupt is masked. 1: Interrupt is unmasked.

9.5.3.3 INTC_CFG0

INTC_CFG0 (Interrupt Configuration Register 0, offset = 0x00000008)

Bit Number	Bit Mnemonic	Function	Access	Reset

31	Reserved	Reserved	R	0
30	MPU_CFG0	MPU interrupt configuration bit 0	R/W	0
29	Reserved	Reserved	R/W	0
28	TIMER3_CFG0	TIMER3 interrupt configuration bit 0	R/W	0
27	TIMER2_CFG0	TIMER2 interrupt configuration bit 0	R/W	0
26	SDIO_CFG0	SDIO interrupt configuration bit 0	R/W	0
25	SPI1_CFG0	SPI1 interrupt configuration bit 0	R/W	0
24	IRC_CFG0	IRC interrupt configuration bit 0	R/W	0
23	Reserved	Reserved	R	0
22	DMA4_CFG0	DMA4 controller interrupt configuration bit 0	R/W	0
21	DMA3_CFG0	DMA3 controller interrupt configuration bit 0	R/W	0
20	DMA2_CFG0	DMA2 controller interrupt configuration bit 0	R/W	0
19	DMA1_CFG0	DMA1 controller interrupt configuration bit 0	R/W	0
18	DMA0_CFG0	DMA0 controller interrupt configuration bit 0	R/W	0
17	SD_CFG0	SD/MMC interrupt configuration bit 0	R/W	0
16	UART1_CFG0	UART1 interrupt configuration bit 0	R/W	0
15	ADC_CFG0	ADC interrupt configuration bit 0	R/W	0
14	DAC_IIS_TX_CFG0	DAC or IIS-TX interrupt configuration bit 0	R/W	0
13	VAD_CFG0	VAD interrupt configuration bit 0	R/W	0
12	IIC1_CFG0	IIC1 interrupt configuration bit 0	R/W	0
11	IIC0_CFG0	IIC0 interrupt configuration bit 0	R/W	0
10	USB_CFG0	USB interrupt configuration bit 0	R/W	0
9	SPI0_CFG0	SPI0 interrupt configuration bit 0	R/W	0
8	I2S_CFG0	I2S interrupt configuration bit 0	R/W	0
7	GPIO_CFG0	GPIO interrupt configuration bit 0	R/W	0
6	UART0_CFG0	UART0 interrupt configuration bit 0	R/W	0
5	RTC_CFG0	RTC interrupt configuration bit 0	R/W	0
4	TIMER0_CFG0	TIMER0 interrupt configuration bit 0	R/W	0
3	TIMER1_CFG0	TIMER1 interrupt configuration bit 0	R/W	0
2	WD_CFG0	WatchDog interrupt configuration bit 0	R/W	0
1	PMU_CFG0	PMU interrupt configuration bit 0	R/W	0
0	BT_BASEBAND_CFG0	BT Baseband interrupt configuration bit 0	R/W	0

Interrupt Config Registers. CPU can assign anyone interrupt source to one of the five interrupt requests.

INTC_CFG2	0	0	0	0	1
INTC_CFG1	0	0	1	1	x
INTC_CFG0	0	1	0	1	x
The interrupt request be assigned	0	1	2	3	4

9.5.3.4 INTC_CFG1

INTC_CFG1 (Interrupt Configuration Register 1, offset = 0x0000000c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31	Reserved	Reserved	R	0
30	MPU_CFG1	MPU interrupt configuration bit 1	R/W	0
29	Reserved	Reserved	R/W	0
28	TIMER3_CFG1	TIMER3 interrupt configuration bit 1	R/W	0
27	TIMER2_CFG1	TIMER2 interrupt configuration bit 1	R/W	0
26	SDIO_CFG1	SDIO interrupt configuration bit 1	R/W	0

25	SPI1_CFG1	SPI1 interrupt configuration bit 1	R/W	0
24	IRC_CFG1	IRC interrupt configuration bit 1	R/W	0
23	Reserved	Reserved	R	0
22	DMA4_CFG1	DMA4 controller interrupt configuration bit 1	R/W	0
21	DMA3_CFG1	DMA3 controller interrupt configuration bit 1	R/W	0
20	DMA2_CFG1	DMA2 controller interrupt configuration bit 1	R/W	0
19	DMA1_CFG1	DMA1 controller interrupt configuration bit 1	R/W	0
18	DMA0_CFG1	DMA0 controller interrupt configuration bit 1	R/W	0
17	SD_CFG1	SD/MMC interrupt configuration bit 1	R/W	0
16	UART1_CFG1	UART1 interrupt configuration bit 1	R/W	0
15	ADC_CFG1	ADC interrupt configuration bit 1	R/W	0
14	DAC_IIS_TX_CFG1	DAC or IIS-TX interrupt configuration bit 1	R/W	0
13	VAD_CFG1	VAD interrupt configuration bit 1	R/W	0
12	IIC1_CFG1	IIC1 interrupt configuration bit 1	R/W	0
11	IIC0_CFG1	IIC0 interrupt configuration bit 1	R/W	0
10	USB_CFG1	USB interrupt configuration bit 1	R/W	0
9	SPI0_CFG1	SPI0 interrupt configuration bit 1	R/W	0
8	I2S_CFG1	I2S interrupt configuration bit 1	R/W	0
7	GPIO_CFG1	GPIO interrupt configuration bit 1	R/W	0
6	UART0_CFG1	UART0 interrupt configuration bit 1	R/W	0
5	RTC_CFG1	RTC interrupt configuration bit 1	R/W	0
4	TIMER0_CFG1	TIMER0 interrupt configuration bit 1	R/W	0
3	TIMER1_CFG1	TIMER1 interrupt configuration bit 1	R/W	0
2	WD_CFG1	WatchDog interrupt configuration bit 1	R/W	0
1	PMU_CFG1	PMU interrupt configuration bit 1	R/W	0
0	BT_BASEBAND_CFG1	BT Baseband interrupt configuration bit 1	R/W	0

9.5.3.5 INTC_CFG2

INTC_CFG2 (Interrupt Configuration Register 2, offset = 0x00000010)

Bit Number	Bit Mnemonic	Function	Access	Reset
31	Reserved	Reserved	R	0
30	MPU_CFG2	MPU interrupt configuration bit 2	R/W	0
29	Reserved	Reserved	R/W	0
28	TIMER3_CFG2	TIMER3 interrupt configuration bit 2	R/W	0
27	TIMER2_CFG2	TIMER2 interrupt configuration bit 2	R/W	0
26	SDIO_CFG2	SDIO interrupt configuration bit 2	R/W	0
25	SPI1_CFG2	SPI1 interrupt configuration bit 2	R/W	0
24	IRC_CFG2	IRC interrupt configuration bit 2	R/W	0
23	Reserved	Reserved	R	0
22	DMA4_CFG2	DMA4 controller interrupt configuration bit 2	R/W	0
21	DMA3_CFG2	DMA3 controller interrupt configuration bit 2	R/W	0
20	DMA2_CFG2	DMA2 controller interrupt configuration bit 2	R/W	0
19	DMA1_CFG2	DMA1 controller interrupt configuration bit 2	R/W	0
18	DMA0_CFG2	DMA0 controller interrupt configuration bit 2	R/W	0
17	SD_CFG2	SD/MMC interrupt configuration bit 2	R/W	0
16	UART1_CFG2	UART1 interrupt configuration bit 2	R/W	0
15	ADC_CFG2	ADC interrupt configuration bit 2	R/W	0

14	DAC_IIS_TX_CFG2	DAC or IIS-TX interrupt configuration bit 2	R/W	0
13	VAD_CFG2	VAD interrupt configuration bit 2	R/W	0
12	IIC1_CFG2	IIC1 interrupt configuration bit 2	R/W	0
11	IIC0_CFG2	IIC0 interrupt configuration bit 2	R/W	0
10	USB_CFG2	USB interrupt configuration bit 2	R/W	0
9	SPI0_CFG2	SPI0 interrupt configuration bit 2	R/W	0
8	I2S_CFG2	I2S interrupt configuration bit 2	R/W	0
7	GPIO_CFG2	GPIO interrupt configuration bit 2	R/W	0
6	UART0_CFG2	UART0 interrupt configuration bit 2	R/W	0
5	RTC_CFG2	RTC interrupt configuration bit 2	R/W	0
4	TIMER0_CFG2	TIMER0 interrupt configuration bit 2	R/W	0
3	TIMER1_CFG2	TIMER1 interrupt configuration bit 2	R/W	0
2	WD_CFG2	WatchDog interrupt configuration bit 2	R/W	0
1	PMU_CFG2	PMU interrupt configuration bit 2	R/W	0
0	BT_BASEBAND_CFG2	BT Baseband interrupt configuration bit 2	R/W	0

10 Storage

SD/MMC Card Controller Features

- Two SD/MMC Card Controller.
- compliant with MMC Specification 4.0
- compliant with SD card Specification 2.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.
- Integrated Pull up resistance (value 51Komh) for Data and CMD line.
- Integrated CRC calculate and check circuit.
- Support 3.1V CLK/CMD/DATA PAD voltage.
- Maximal SD interface Clock: 50MHz
- SD0 Support SD 1line bus.
- SD1 Support SD 1/4line bus.
- Band Width: SD0:6.25, SD1:25MByte/S (max)

11 Transfer and Communication

11.1 USB

11.1.1 Features

- Complies with the USB1.1 Specification
- Supports point-to-point communication with one full-speed device in Host mode(no HUB support).
- Supports full-speed in peripheral mode.
- Supports 2 IN endpoint and 1 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup for Device Mode.

11.2 TWI

11.2.1 Features

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Both master and slave supports DMA mode
- Only 7-bit address mode support
- Two TWI modules
- 8 Bit x8 TX FIFO and 8Bit x8 RX FIFO
- Supports general call

11.2.2 Function Description

Two wire interfaces (TWI) bus is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.
TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

Note:

1. *The TWI module is in Slave mode by default.*
2. *Generate the IRQ while the bus status changes.*
   - *A byte transfer complete, include transmit and receive data or address*
   - *A stop bit detected*
3. *Release the bus by software after receiving data or address.*

11.2.3 Register List

Table 11-3 TWI Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
TWI0	0xc0130000	0xc0130000
TWI1	0xc0150000	0xc0150000

Table 11-4 TWI Registers Offset Address

Offset	Register Name	Description
0x00	TWI x_CTL	TWI Control Register
0x04	TWI x_CLKDIV	TWI Clock Divide Register
0x08	TWIx_STAT	TWI Status Register
0x0c	TWIx_ADDR	TWI Address Register
0x10	TWIx_TXDAT	TWI TX Data Register
0x14	TWIx_RXDAT	TWI RX Data Register
0x18	TWIx_CMD	TWI Command Register
0x1c	TWIx_FIFOCTL	TWI FIFO control Register
0x20	TWIx_FIFOSTAT	TWI FIFO status Register
0x24	TWIx_DATCNT	TWI Data transmit counter
0x28	TWIx_RCNT	TWI Data transmit remain counter

11.2.4 Register Description

11.2.4.1 TWIx_CTL

TWI DMA mode Control Register
Offset=0x00

Bits	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	IRQC	TWI IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode	RW	0x0
9:7	-	Resreved	RW	0x0
6	IRQE	IRQ Enable. 0: Disable 1: Enable	RW	0x0
5	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0x0
4	-	Reserved	RW	0x0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	RW	0x0

1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0x0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0x0

11.2.4.2 TWIx_CLKDIV

TWI Clock Divide Control Register
Offset=0x04

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	CLKDIV	Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=HOSC/(CLKDIV*16)	RW	0x0

11.2.4.3 TWIx_STAT

TWI Status Register
Offset=0x08

Bits	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0x0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0x0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0x0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it.	RW	0x0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0x0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0x0

4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0x0
3	-	Reserved	RW	0x0
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1. transfer complete 2. detect normal stop bit (no bus error) 3. arbit fail Clear condition: Writing 1 to this bit will clear it.	RW	0x0
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write “1” to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.	RW	0x0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0x0

11.2.4.4 TWIx_ADDR

TWI Address Register
Offset=0x0c

Bits	Name	Description	R/W	Reset
31：8	-	Reserved	R	0x0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	RW	0x0
0	-	Reserved.	R	0x0

11.2.4.5 TWIx_TXDAT

TWI Data Register
Offset=0x10

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0

7:0	DA	The registers of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit. 8 level FIFO, 8 x 8bit	W	0x0

11.2.4.6 TWIx_RXDAT

TWI Data Register
Offset=0x14

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	DA	The Receive data Register 8 level FIFO, 8 x 8bit	R	0x0

11.2.4.7 TWIx_CMD

TWI Data Register
Offset=0x18

Bits	Name	Description	R/W	Reset
31: 16	-	Reserved	R	0x0
15	SECL	Start to execute the command list 0: not execute 1: execute command	RW	0x0
14:13	-	Reserved	R	0x0
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	RW	0x0
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	RW	0x0
10	SE	Stop enable 0: disable 1: enable	RW	0x0
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	RW	0x0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT register.	RW	0x0
7:5	SAS	Second address select	RW	0x0

		000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address		
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	RW	0x0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address include slave address and slave internal memory address.	RW	0x0
0	SBE	Start bit enable 0: not send start bit 1: send start bit	RW	0x0

11.2.4.8 TWIx_FIFOCTL

TWI Counter Register
Offset=0x1c

Bits	Name	Description	R/W	Reset
31:3	-	Reserved	R	0x0
2	TFR	TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	RW	0x0
1	RFR	RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	RW	0x0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute, generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	RW	0x0

11.2.4.9 TWIx_FIFOSTAT

TWI Counter Register
Offset=0x20

Bits	Name	Description	R/W	Reset

31:16	-	Reserved	R	0x0
15:12	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0x0
11:8	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0x0
7	-	Reserved	R	0x0
6	WRS	Write or read status bit when acts as slave, used only in FIFO mode 0: master write to slave 1: master read from slave	R	0x0
5	TFF	TX FIFO full bit 0: not full 1: full	R	0x0
4	TFE	TX FIFO empty bit 0: empty 1: not empty	R	0x0
3	RFF	RX FIFO full bit 0: not full 1: full	R	0x0
2	RFE	RX FIFO empty bit 0: empty 1: not empty	R	0x0
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data Write 1 to clear this bit	RW	0x0
0	CECB	Command Execute Complete bit 0: not complete 1: complete	R	0x1

11.2.4.10 TWIx_DATCNT

TWI Counter Register
Offset=0x24

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Data Transmit counter	RW	0x0

11.2.4.11 TWIx_RCNT

TWI remain Counter Register
Offset=0x28

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	The counter of data remain, which have not transmitted.	R	0x0

11.3 UART

11.3.1 Features

ATS2819 support one UART interface, the UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- Add UART RX DMA counter for valid data in RAM

11.3.2 Operation Manual

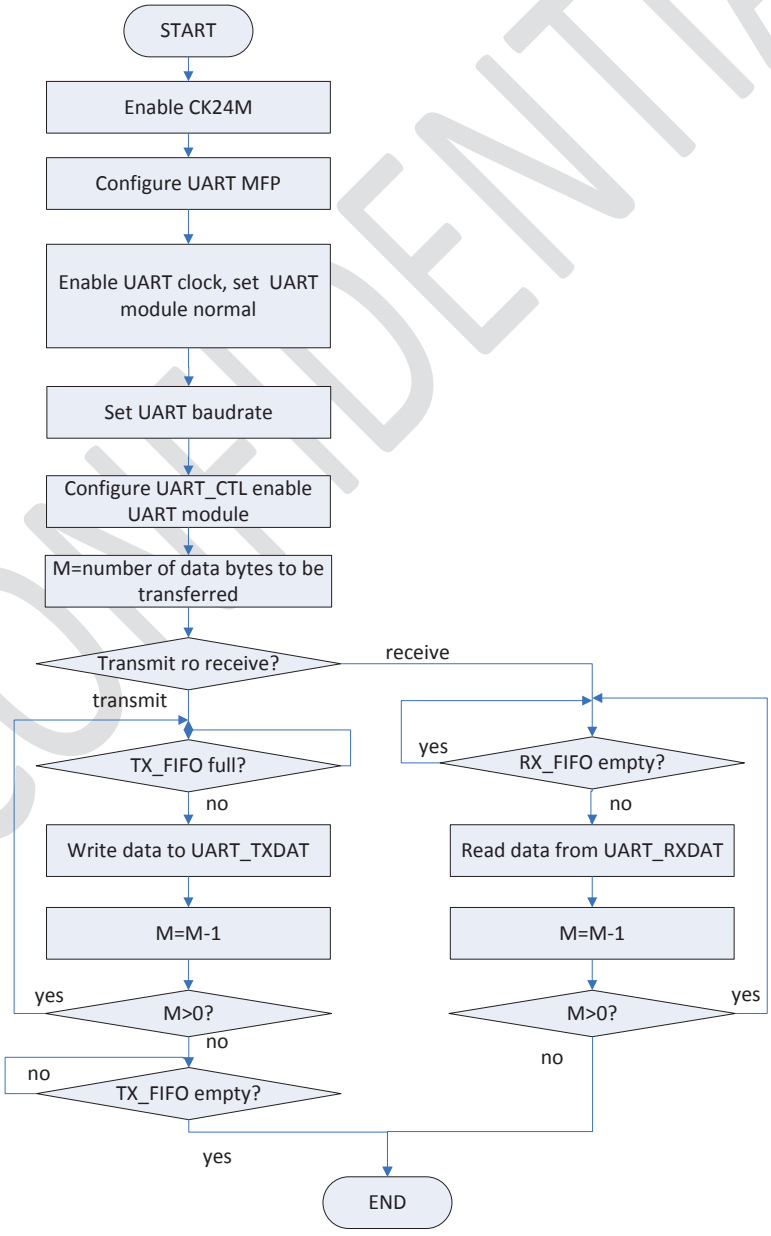


Figure 11-1 UART operation flow

11.3.3 Register List

Table 11-5 UART Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART0	0xC01A0000	0xC01A0000
UART1	0xC01B0000	0xC01B0000

Table 11-6 UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000C	UARTx_STA	UART Status Register
0x0010	UARTx_BR	BAUDRATE divider register

11.3.4 Register Description

11.3.4.1 UARTx_CTL

UART Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31	RXENABLE	UART RX disable 1: normal 0: disable	R/W	0x0
30	TXENABLE	UART TX disable 1: normal 0: disable	R/W	0x0
29:26	Reserved	Reserved	R	X
25:24	DBGSEL	UART debug select control.	R/W	0x0
23	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	R/W	0x0
22	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	R/W	0x0
21	TXAHB_DMA_SEL	UART TX FIFO Clock Select 0: AHB Clock 1:DMA Clock	R/W	0x0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the output will be presented on the input. And if we enable AFE, UART_RST's output will be presented on UART_CTS. 0: Disable 1: Enable	R/W	0x0
19	TXIE	UART TX IRQ Enable. 0: Disable	R/W	0x0

		1: Enable		
18	RXIE	UART RX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
17	TXDE	UART TX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART RX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
15	EN	UART Enable. 0:disable 1: enable	R/W	0x0
14	RXAHB_DMA_SEL	UART RX FIFO Clock Select 0: AHB Clock 1:DMA Clock	R/W	0x0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: request to send data 1: no request	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00,01 because at lease 8 bytes necessary.	R/W	0x0
9:8	TDIC	UART TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00,01 because at lease 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable. If this bit is 1, the transmitter checks CTS- before sending the next data byte. Note: This bit has no effect if Autoflow enable bit is set. 0: do not checks CTS- before sending 1: checks CTS- before sending	R/W	0x0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd	R/W	0x0

		1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0		
3	Reserved	Reserved	R	X
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit 1: 2 stop bit	R/W	0x0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

11.3.4.2 UARTx_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	Reserved	Reserved	R	X
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	X

11.3.4.3 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	Reserved	Reserved	R	X
7:0	TXDAT	Transmitted Data. The depth of FIFO is 8bit×16 levels	W	0x0

11.3.4.4 UARTx_STA

UART Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:24	Reserved	Reserved	R	X
23	PAER	Parity Status. 0: Parity OK 1: Parity error. Writing 1 to the bit will clear the bit. When parity error.	R/W	0x0
22	STER	Stop Status. 0: Stop OK 1: Stop error. Writing 1 to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out	R	0x0

		1:busy		
20:16	TXFL	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	0x1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	X
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	0x1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When clock error.	R/W	0x0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	R/W	0x0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	R/W	0x0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	R/W	0x0

11.3.4.5 UARTx_BR

UART BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:28	Reserved	Reserved	R	X
27:16	TXBRDIV	UART TX BAUDRATE divider BaudRate= Colck_source/BaudRate divider Clock_source=HOSC or CK24M, selected by CMU_UARTCLK[0]	R/W	0x028

15:12	Reserved	Reserved	R	X
11:0	RXBRDIV	UART RX BAUDRATE divider BaudRate= Colck_source/BaudRate divider Clock_source=HOSC or CK24M, selected by CMU_UARTCLK[0]	R/W	0x028

11.4 SPI0

11.4.1 Features

SPI0 is a combination module which includes conventional SPI and SPI_Cache interface.

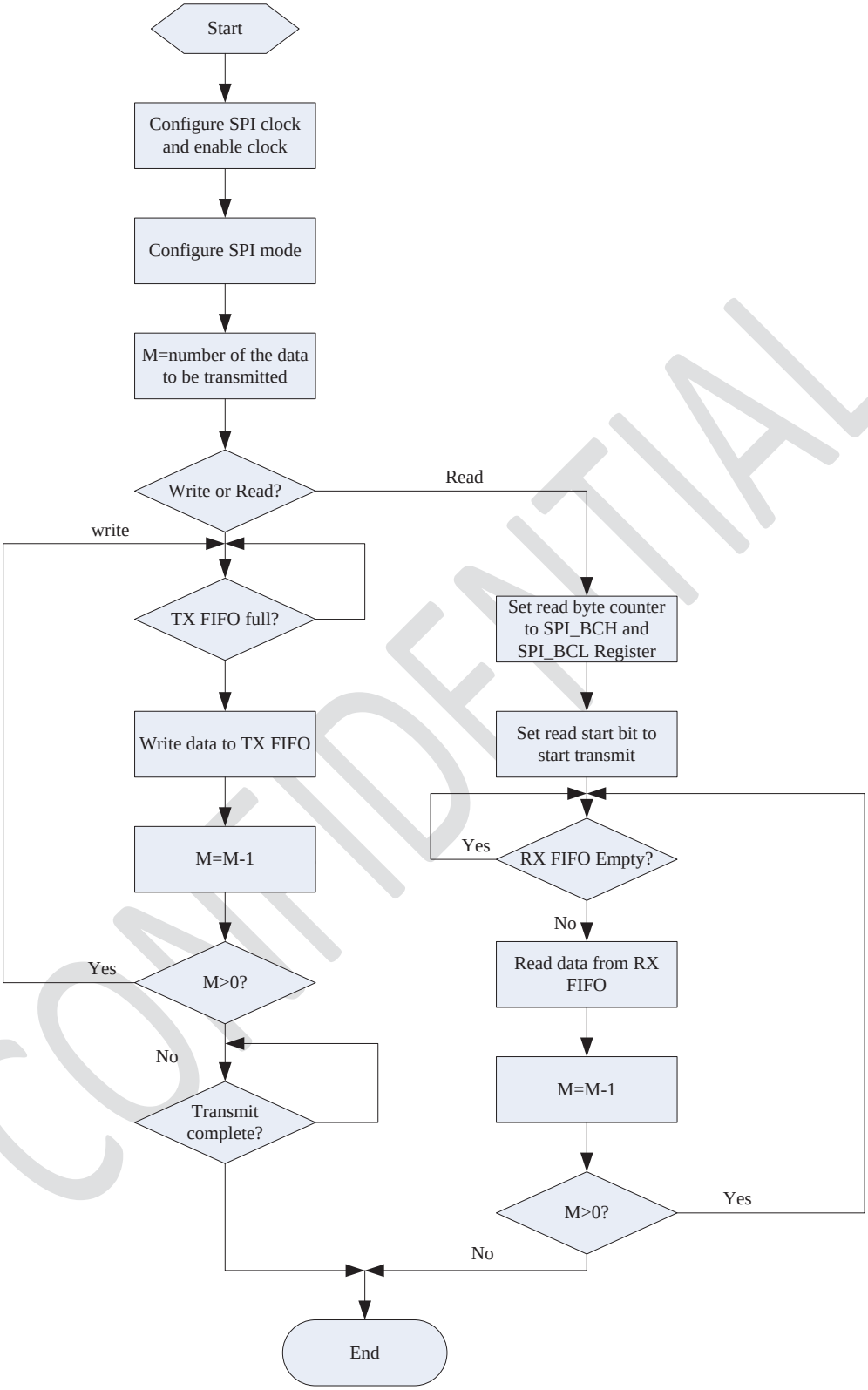
- Only support master mode
- Support mode0 and mode3
- Support AHB and Cache access SPI and DMA interface
- Only Support 8bit transfer mode
- Support 32 bit seed 8bit randomize
- Support 3wire
- Support 16 level delay chain, 1ns/step
- Support 1x/2x/dual/4x/quad access SPI NOR
- Support 16bit CRC only when Cache access fifo, not support CRC when AHB access fifo
- Support cache abort
- Support 100MHz spi_clk as highest speed
- Let R = spi_clk/cpu_clk. In 1x mode, R < 160; In 2x/dual mode, R < 80; In 4x/quad mode, R < 40

11.5 SPI1

11.5.1 Features

- A Support SPI normal mode: mode 0\1\2\3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data

11.5.2 Operation Manual



SPI operation flow

Figure 11-2 SPI1 operation flow

11.5.3 Register List

Table 11-7 SPI1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI1	0xC00F0000	0xC00F0000

Table 11-8 SPI1 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI1_CTL	SPI Control Register
0x0004	SPI1_STA	SPI Status Register
0x0008	SPI1_TXDAT	SPI Transmit FIFO Data Register
0x000C	SPI1_RXDAT	SPI Receive FIFO Data Register
0x0010	SPI1_BC	SPI Byte Counter Low Register

11.5.4 Register Description

11.5.4.1 SPI1_CTL

SPI1 Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27:23	-	Reserved	R/W	0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0
20	RX_WRITE_SEL	SPI Rx Write Select Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns	R/W	0000

		0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns 1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns		
15:12	-	Reserved	R/W	0
11	SPI_TDRQ_EN	SPI TX DRQ Enable Trigger DRQ when SPI TX FIFO at least 1 level empty; When DMA remain counter < 4, trigger DRQ until all data transfer completely; 0: disable 1: enable	R/W	0
10	SPI_RDRQ_EN	SPI RX DRQ Enable Trigger DRQ when SPI RX FIFO at least 1 level full.; When DMA remain counter < 4, trigger DRQ until all data received completely; 0: disable 1: enable	R/W	0
9	SPI_TIRQ_EN	SPI TX IRQ Enable Trigger SPI TX IRQ when SPI TX FIFO at least 2 level empty 0: disable 1: enable	R/W	0
8	SPI_RIRQ_EN	SPI RX IRQ Enable Trigger SPI RX IRQ when SPI RX FIFO is not empty. 0: disable 1: enable	R/W	0
7:6	-	Reserved	R/W	0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable	R/W	00

		01: Read only 10: Write only 11: Read and Write		

11.5.4.2 SPI1_STA

SPI Status Register
Offset=0x0004

Bits	Name	Description	R/W	Reset
31:12	Reserved	Reserved	R	x
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
10	Reserved	Reserved	R	x
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
7	SPI_RXFU	SPI RX FIFO Full 0: not full 1: full	R	0
6	SPI_RXEM	SPI RX FIFO Empty 0: not empty 1: empty	R	1
5	SPI_TXFU	SPI TX FIFO Full 0: not full 1: full	R	0
4	SPI_TXEM	SPI TX FIFO Empty 0: not empty 1: empty	R	1
3	SPI_TIRQ_PD	SPI TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0
2	SPI_RIRQ_PD	SPI RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0
1	Reserved	Reserved	R	x
0	SPI_BUSY	SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0

11.5.4.3 SPI1_TXDAT

SPI Transmit FIFO Data Register
Offset=0x008

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_TXDAT	SPI TX FIFO,32bitx4 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx16levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0

11.5.4.4 SPI1_RXDAT

SPI Receive FIFO Data Register
Offset=0x00c

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_RXDAT	SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx16levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx4 levels	R	0

11.5.4.5 SPI1_BC

SPI Bytes Count Register, this register is used for setting SPI bytes counter bits in the SPI read mode only.
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:13	Reserved	Reserved	R	0
12:0	SPI_BC	Bytes Counter [12: 0]	R/W	0

11.6 IRC

11.6.1 Features

- Support de-bounce function
- Support IRC(infrared remote control) Inputs
- Support RC5\RC6\9012\NEC(8bit) protocol, compatible 36kHz, 38kHz, 40kHz carrier.
- Need to connect an IR receiver when use.

11.6.2 Operation Manual

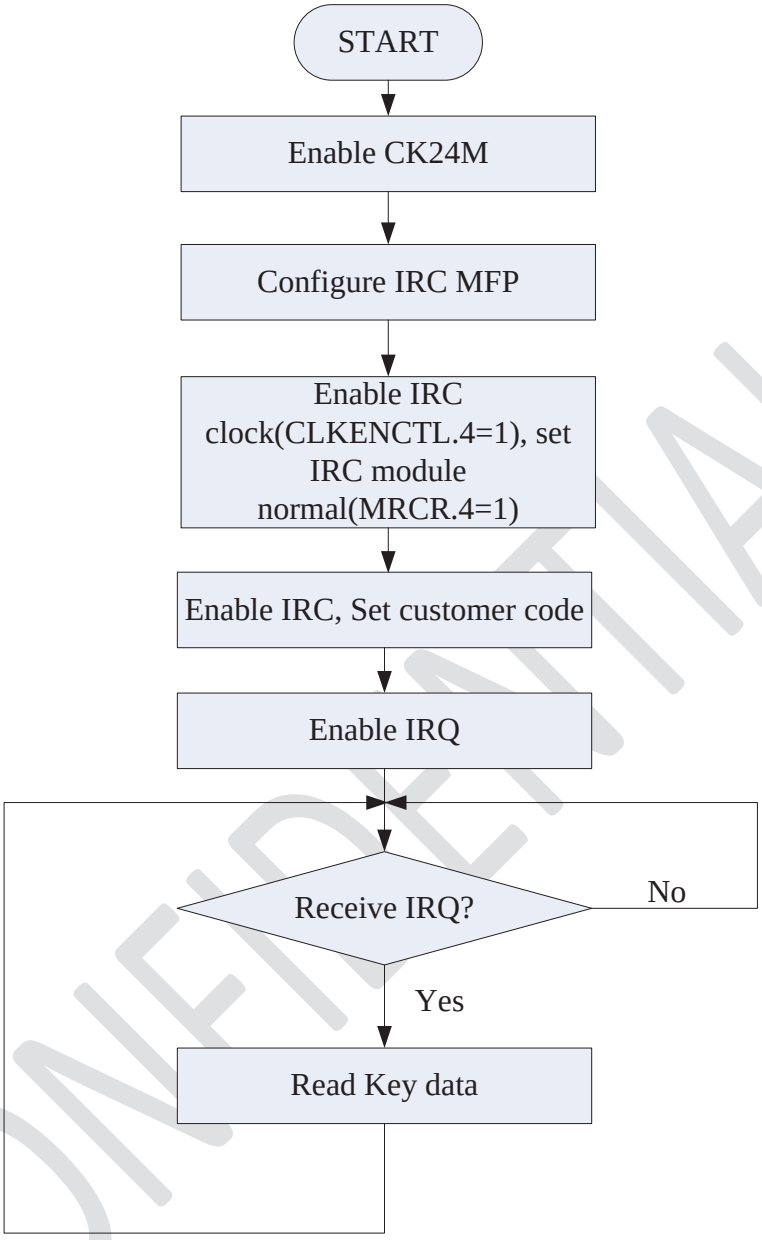


Figure 11-3 IRC operation flow

11.6.3 Register List

Table 11-9 IRC Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
IRC	0xc01c0000	0xc01c0000

Table 11-10 IRC Registers Offset Address

Offset	Register Name	Description
0x0050	IRC_CTL	Infrared remote control(IRC) interface control register
0x0054	IRC_STA	IRC status register
0x0058	IRC_CC	IRC customer code register

0x005C	IRC_KDC	IRC key data code register

11.6.4 Register Description

11.6.4.1 IRC_CTL

infrared remote control register
Offset=0x0050

Bits	Name	Description	R/W	Reset
31:17	Reserved		R	0
16	DBB_EN	Debounce Bypass enable 0: bypass disable 1:bypass enable	RW	0x0
15:4	DBC	Debounce counter, 1 counter=1/200KHz Default counter=40=200us	RW	0x028
3	IRE	IRC enable 0: disable 1:enable	RW	0
2	IIE	IRC IRQ enable 0:disable 1:enable	RW	0
1:0	ICMS	IRC coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11: RC6 code	RW	0

11.6.4.2 IRC_STA

Infrared remote status register
Offset=0x0054

Bits	Name	Description	R/W	Reset
31:7	Reserved		R	0
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:user code match 1:user code don't match	RW	0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:key data code match 1:key data code don't match	RW	0
4	RCD	Repeated code detected, Write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	RW	0
3	Reserved		R	0
2	IIP	IRC IRQ pending bit. write 1 to this bit will clear it 0:no IRQ pending 1: IRQ pending	RW	0

1	Reserved		R	0
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0

11.6.4.3 IRC_CC

Infrared remote control customer code register.
Offset=0x0058

Bits	Name	Description	R/W	Reset
31:16	CCRCV	customer code received In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R	0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	RW	0

11.6.4.4 IRC_KDC

Infrared remote control KEY data code register.
Offset=0x005C

Bits	Name	Description	R/W	Reset
31:16	Reserved		R	0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data	R	0

11.7 PWM

11.7.1 Features

PWM is multiplexing with GPIO, features of PWM are listed below:

- Support 9 PWM output
- Frequency ranges from 0.015625Hz~80K, adjustable. Under normal mode, PWM can output 256 kinds of duty cycles
- Breath mode PWM supports various frequency breathing lights.

11.7.2 Operation Manual

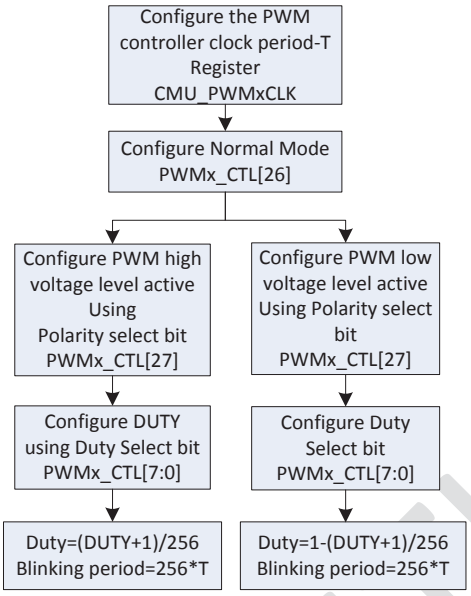


Figure 11-4 PWM Configuration

For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

11.7.3 Register List

Table 11-11 PWM Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
PWM	0xC00D0000	0xC00D0000

Table 11-12 PWM Registers Offset Address

Offset	Register Name	Description
0x00	PWM0_CTL	PWM0 Output Control
0x04	PWM1_CTL	PWM1 Output Control
0x08	PWM2_CTL	PWM2 Output Control
0x0C	PWM3_CTL	PWM3 Output Control
0x10	PWM4_CTL	PWM4 Output Control
0x14	PWM5_CTL	PWM5 Output Control
0x18	PWM6_CTL	PWM6 Output Control
0x1C	PWM7_CTL	PWM7 Output Control
0x20	PWM8_CTL	PWM8 Output Control

11.7.4 Register Description

11.7.4.1 PWM0_CTL

PWM0 Output Control Register

Offset=0x00

Bit(s)	Name	Description	R/W	Reset

31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.2 PWM1_CTL

PWM1 Output Control Register
Offset=0x04

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256	RW	0x0

		Only Active in Normal Mode		

11.7.4.3 PWM2_CTL

PWM2 Output Control Register
Offset=0x08

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.4 PWM3_CTL

PWM3 Output Control Register
Offset=0x0C

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32:	RW	0x0

		Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM		
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.5 PWM4_CTL

PWM4 Output Control Register
Offset=0x10

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.6 PWM5_CTL

PWM5 Output Control Register
Offset=0x14

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable	RW	0x0

		1: enable		
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.7 PWM6_CTL

PWM6 Output Control Register
Offset=0x18

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.8 PWM7_CTL

PWM7 Output Control Register
Offset=0x1C

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.7.4.9 PWM8_CTL

PWM8 Output Control Register
Offset=0x20

Bit(s)	Name	Description	R/W	Reset
31:29	Reserved	Reserved	R	0x0
28	PWM_EN	PWM enable: 0: disable 1: enable	RW	0x0
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Rising and falling time T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0

15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

12 GPIO and I/O Multiplexer

12.1 Features

GPIO (General Purpose Input /Output) MFP:

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADs are limited, so MFP module is designed for multiplexing these PADs. Features of GPIO are listed below:

- 22 Programmable GPIOs, and 10 analog IOs can also config as GPIOs.
- All PADs have internal pull down resistors (100KOhm) or pull up resistors (100 KOhm/50 KOhm/10KOhm)
- Driving strength adjustable
- Automatically switching PAD function
- All PADs have external Interrupts function

WIO (Wake up I/O) MFP:

- 1 wake up I/O can wake up SOC externally, and these I/O can be config as Special I/O. The Maximum work frequency should no more than 10KHz.

Settings in actual practice please consult our engineers. The multiplexing relationship can be found in *Pin Description list.*

12.2 Operation Manual

12.2.1 Block Diagram

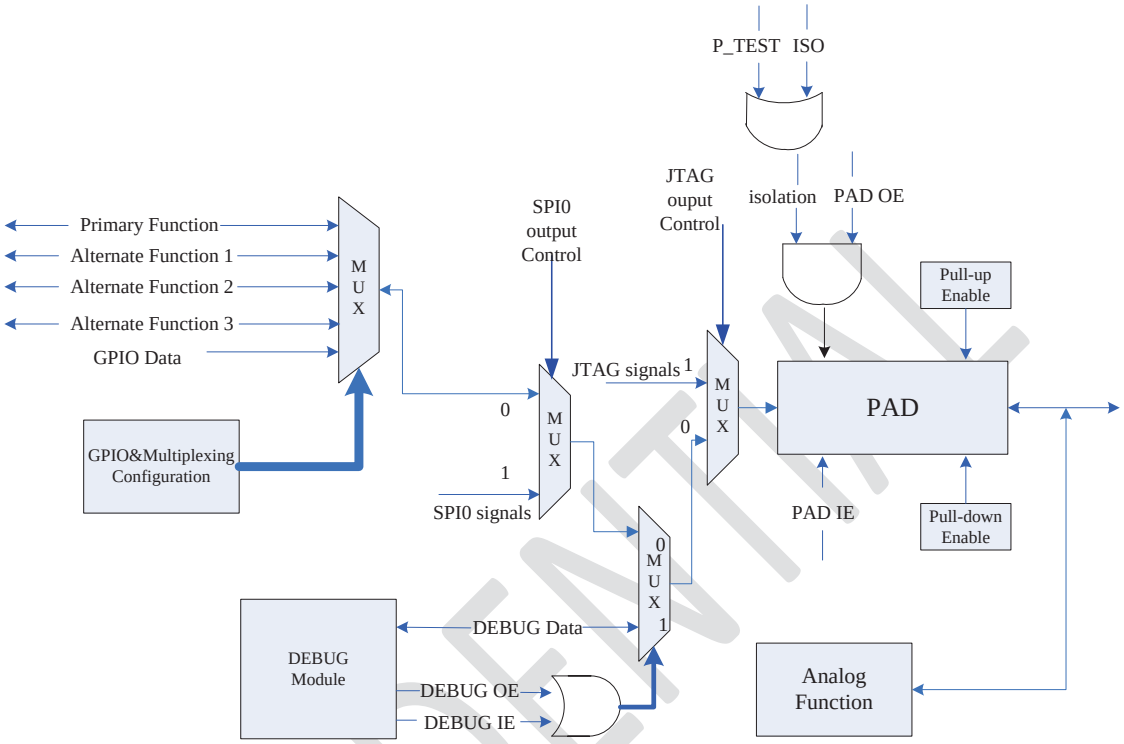


Figure 12-1 Block Diagram of GPIO controller

12.2.2 Multi-function Switch Operation

1. Some pin can be multiplexed as three kinds of functions: module function (MFP), GPIO function, Analog function, which can be configured by setting registers of MFP, GPIOINEN / GPIOOUTEN, and AD_SELECT.
2. The function priority of some multiplexed pin are Analog function > GPIO function & MFP function. GPIO and MFP are digital functions.
3. Some pin can be multiplexed as analog function and digital function. If the pin is used as digital function, analog function must be disabled firstly by setting AD_SELECT register.
4. Some MFP modules have their own pull-up and pull-down resistors, referring the chapter Pad PU control register and Pad PD control register; when the pin is multiplexed as MFP module function, the modules pull-up/pull-down resistors will be enabled automatically and the pull-up/pull-down resistors of GPIOs must be DISABLED, or the voltage level and functions will be abnormal.
5. The multiplexing register is AD_SELECT.

12.2.3 GPIO Output

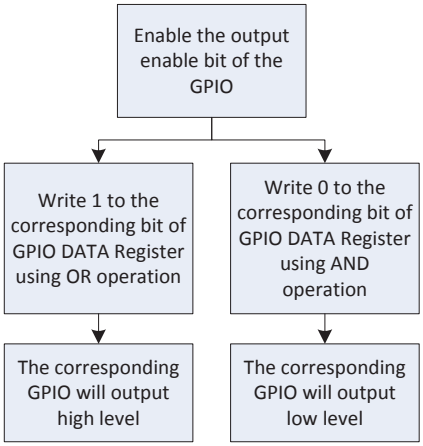


Figure 12-2 GPIO Output Configuration

12.2.4 GPIO Input

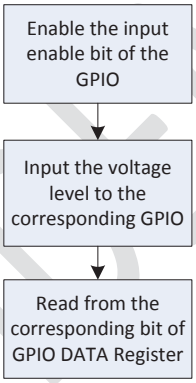


Figure 12-3 GPIO Input Configuration

12.2.5 GPIO Output/Input Loop Test

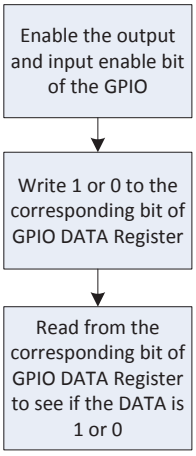


Figure 12-4 GPIO In/Out Loop Test

12.3 Register List

Table 12-1 Table GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP	0xc0090000	0xc0090000

Table 12-2 GPIO&MFP Controller Registers

Offset	Register Name	Description	Voltage
GPIO Register			
0x000C	GPIO0_CTL	GPIO0 control Register	VDD
0x0010	GPIO1_CTL	GPIO1 control Register	VDD
0x0014	GPIO2_CTL	GPIO2 control Register	VDD
0x0018	GPIO3_CTL	GPIO3 control Register	VDD
0x001C	GPIO4_CTL	GPIO4 control Register	VDD
0x0020	GPIO5_CTL	GPIO5 control Register	VDD
0x0024	GPIO6_CTL	GPIO6 control Register	VDD
0x0028	GPIO7_CTL	GPIO7 control Register	VDD
0x002C	GPIO8_CTL	GPIO8 control Register	VDD
0x0030	GPIO9_CTL	GPIO9 control Register	VDD
0x0034	GPIO10_CTL	GPIO10 control Register	VDD
0x0038	GPIO11_CTL	GPIO11 control Register	VDD
0x003C	GPIO12_CTL	GPIO12 control Register	VDD
0x0040	GPIO13_CTL	GPIO13 control Register	VDD
0x0058	GPIO19_CTL	GPIO19 control Register	VDD
0x005C	GPIO20_CTL	GPIO20 control Register	VDD
0x0060	GPIO21_CTL	GPIO21 control Register	VDD
0x0064	GPIO22_CTL	GPIO22 control Register	VDD
0x0068	GPIO23_CTL	GPIO23 control Register	VDD
0x006C	GPIO24_CTL	GPIO24 control Register	VDD
0x0070	GPIO25_CTL	GPIO25 control Register	VDD
0x0074	GPIO26_CTL	GPIO26 control Register	VDD
0x00A4	GPIO38_CTL	GPIO38 control Register(GPIO38 work in VCC domain)	VDD
0x00A8	GPIO39_CTL	GPIO39 control Register(GPIO39 work in VCC domain)	VDD
0x00AC	GPIO40_CTL	GPIO40 control Register(GPIO40 work in AVCC domain)	VDD
0x00B0	GPIO41_CTL	GPIO41 control Register(GPIO41 work in AVCC domain)	VDD
0x00B4	GPIO42_CTL	GPIO42 control Register(GPIO42 work in VCC domain)	VDD
0x00B8	GPIO43_CTL	GPIO43 control Register(GPIO43 work in VCC domain)	VDD
0x00BC	GPIO44_CTL	GPIO44 control Register(GPIO44 work in AVCC domain)	VDD
0x00C0	GPIO45_CTL	GPIO45 control Register(GPIO45 work in AVCC domain)	VDD
0x00C4	GPIO46_CTL	GPIO46 control Register(GPIO46 work in AVCC domain)	VDD
0x00C8	GPIO47_CTL	GPIO47 control Register(GPIO47 work in AVCC domain)	VDD
0x0100	GPIO_ODAT0	GPIO Output Data register 0	VDD

0x0104	GPIO_ODAT1	GPIO Output Data register 1	VDD
0x0108	GPIO_BSR0	GPIO Output Data bit set register 0	VDD
0x010C	GPIO_BSR1	GPIO Output Data bit set register 1	VDD
0x0110	GPIO_BRR0	GPIO Output Data bit reset register 0	VDD
0x0114	GPIO_BRR1	GPIO Output Data bit reset register 1	VDD
0x0118	GPIO_IDAT0	GPIO Input Data register 0	VDD
0x011C	GPIO_IDAT1	GPIO Input Data register 1	VDD
0x0120	GPIO_PD0	GPIO IRQ Pending register 0;	VDD
0x0124	GPIO_PD1	GPIO IRQ Pending register 1;	VDD
0x0140	WIO0_CTL	Wake up IO0/SIO0 control Register(WIO0 work in SVCC domain)	RTCVDD

12.4 GPIO Register Description

12.4.1 GPIO0_CTL

GPIO0 control Register
Offset=0x0C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA	R/W	0x1

		010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA		
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: SD0_CMD 0x1: GPIO0 0x2: UART0_CTS 0x3: FMCLKOUT 0x4: SPI1_SS 0x5: PWM0 0x6: I2STX_BCLK 0x7: I2SRX_BCLK Others: Reserved;	R/W	0x0

12.4.2 GPIO1_CTL

GPIO1 control Register
Offset=0x10

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode	R/W	0x0

		000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x3
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: SD0_CLK 0x1: GPIO1 0x2: UART0_RTS 0x3: UART0_RX 0x4: SPI1_CLK 0x5: PWM1 0x6: I2STX_LRCLK 0x7: I2SRX_LRCLK	R/W	0x0

		Others: Reserved;		

12.4.3 GPIO2_CTL

GPIO2 control Register
Offset=0x14

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0

6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: SD0_DAT 0x1: GPIO2 0x2: UART0_TX 0x3: TWI0_SDA 0x4: SPI1_MOSI 0x5: IR_RX 0x6: I2STX_MCLK 0x7: I2SRX_MCLK Others: Reserved;	R/W	0x0

12.4.4 GPIO3_CTL

GPIO3 control Register
Offset=0x18

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA	R/W	0x1

		101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA		
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC9) Note: There is only one GPIO can be set as LRADC9. When this GPIO is set as LRADC9, other can't be set as LRADC9.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: TWI0_SCL 0x1: GPIO3 0x2: UART0_CTS 0x3: PWM2 0x4: SPI1_MISO 0x5: Reserved 0x6: I2STX_DOUT 0x7: I2SRX_DI 0x8: LCD_SEG16 0x9: SPI0_IO2 Others: Reserved	R/W	0x1

12.4.5 GPIO4_CTL

GPIO4 control Register
Offset=0x1C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0

24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC10) Note: There is only one GPIO can be set as LRADC10. When this GPIO is set as LRADC10, other can't be set as LRADC10.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: FMCLKOUT	R/W	0x1

		0x1: GPIO4 0x2: UART0_RTS 0x3: PWM3 0x4: Reserved 0x5: UART0_TX 0x6: IR_RX 0x7: TIMER2_CAPIN 0x8: LCD_SEG17 0x9: CK802_TRST 0xA: SPI0_IO3 Others: Reserved		

12.4.6 GPIO5_CTL

GPIO5 control Register
Offset=0x20

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AVCC)	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: UART0_RX 0x1: GPIO5 0x2: CK802_TCK 0x3: TWI0_SDA 0x4: IR_RX 0x5: PWM4 0x6: I2STX_BCLK 0x7: TWI1_SDA 0x8: LCD_SEG20 0x9: SPI0_SS Others: Reserved	R/W	0x1

12.4.7 GPIO6_CTL

GPIO6 control Register
Offset=0x24

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable.	R/W	0x0

		0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AVCC)	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: UART0_TX 0x1: GPIO6 0x2: CK802_TMS 0x3: TWI0_SCL 0x4: Reserved 0x5: PWM5 0x6: I2STX_LRCLK 0x7: TWI1_SCL 0x8: LCD_SEG21 0x9: SPI0_CLK Others: Reserved	R/W	0x1

12.4.8 GPIO7_CTL

GPIO7 control Register
Offset=0x28

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0

5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: GPIO7 1:Analog Function(LRADC1)	R/W	0x0
3:0	Reserved	Reserved	R	0x0

12.4.9 GPIO8_CTL

GPIO8 control Register
Offset=0x2C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0

8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: UART1_TX 0x1: GPIO8 0x2: I2STX_MCLK 0x3: TWI0_SDA 0x4: SPI1_MISO 0x5: PWM6 0x6: LCD_SEG15 0x7: DMIC_CK 0x8: LCD_SEG18 0x9: SPI0_MOSI Others: Reserved	R/W	0x1

12.4.10 GPIO9_CTL

GPIO9 control Register
Offset=0x30

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when	R/W	0x0

		GPIO_INTC_MSK is '1'.		
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: UART1_RX 0x1: GPIO9 0x2: I2STX_DOUT 0x3: TWI0_SCL 0x4: SPI1_MOSI 0x5: PWM7 0x6: SPI0_MISO 0x7: DMIC_DAT 0x8: LCD_SEG19 Others: Reserved	R/W	0x1

12.4.11 GPIO10_CTL

GPIO10 control Register
Offset=0x34

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x4
11	1P5KPUEN	GPIO 1.5K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO15KPDEN	GPIO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO150KPUEN	GPIO 150K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: DM 0x1: GPIO10 0x2: UART1_CTS	R/W	0x0

		0x3: UART0_CTS 0x4: I2SRX_DI 0x5: PWM8 Others: Reserved		

12.4.12 GPIO11_CTL

GPIO11 control Register
Offset=0x38

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x4
11	1P5KPUEN	GPIO 1.5K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO15KPDEN	GPIO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO150KPUEN	GPIO 150K PU Enable. 0: Disable 1: Enable	R/W	0x0

7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0x0: DP 0x1: GPIO11 0x2: UART1_RTS 0x3: UART0_RTS 0x4: I2SRX_MCLK 0x5: PWM0 Others: Reserved	R/W	0x0

12.4.13 GPIO12_CTL

GPIO12 control Register
Offset=0x3C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA	R/W	0x7

		100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA		
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC2) Note: There is only one GPIO can be set as LRADC2. When this GPIO is set as LRADC2, other can't be set as LRADC2.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: SPI0_IO2 0x1: GPIO12 0x2: UART0_TX 0x3: TWI1_SDA 0x4: SPI1_SS 0x5: PWM8 0x6: I2SRX_BCLK 0x7: UART1_CTS 0x8: TIMER3_CAPIN Others: Reserved	R/W	0x0

12.4.14 GPIO13_CTL

GPIO13 control Register
Offset=0x40

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0

24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x7
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC3) Note: There is only one GPIO can be set as LRADC3. When this GPIO is set as LRADC3, other can't be set as LRADC3.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: SPI0_IO3	R/W	0x0

		0x1: GPIO13 0x2: UART0_RX 0x3: TWI1_SCL 0x4: SPI1_CLK 0x5: IR_RX 0x6: I2SRX_LRCLK 0x7: UART1_RTS 0x8: PWM0 0x9: LED_SEG7 Others: Reserved There is only one GPIO can be set as LED_SEG7. When this GPIO is set as LED_SEG7, other can't be set as LED_SEG7.		

12.4.15 GPIO19_CTL

GPIO19 control Register
Offset=0x58

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable.	R/W	0x0

		0: Disable 1: Enable		
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC3) Note: There is only one GPIO can be set as LRADC3. When this GPIO is set as LRADC3, other can't be set as LRADC3.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_COM5 0x1: GPIO19 0x2: LCD_SEG23 0x3: IR_RX 0x4: EM_CEB2 0x5: PWM8 0x6: TIMER3_CAPIN 0x7: SD1_CLK 0x8: CK802_TMS Others: Reserved	R/W	0x1

12.4.16 GPIO20_CTL

GPIO20 control Register
Offset=0x5C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge	R/W	0x0

		011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC4) Note: There is only one GPIO can be set as LRADC4. When this GPIO is set as LRADC4, other can't be set as LRADC4.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG0 0x1: GPIO20 0x2: LED_SEG0 0x3: LCD_D0 0x4: EM_D0 0x5: PWM1	R/W	0x1

		0x6: I2STX_BCLK 0x7: SD1_CMD 0x8: SPI1_SS Others: Reserved		

12.4.17 GPIO21_CTL

GPIO21 control Register
Offset=0x60

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0

7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC5) Note: There is only one GPIO can be set as LRADC5. When this GPIO is set as LRADC5, other can't be set as LRADC5.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG1 0x1: GPIO21 0x2: LED_SEG1 0x3: LCD_D1 0x4: EM_D1 0x5: PWM2 0x6: I2STX_LRCLK 0x7: SD1_CLK 0x8: SPI1_CLK Others: Reserved	R/W	0x1

12.4.18 GPIO22_CTL

GPIO22 control Register
Offset=0x64

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger	R/W	0x0

		event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC6) Note: There is only one GPIO can be set as LRADC6. When this GPIO is set as LRADC6, other can't be set as LRADC6.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG2 0x1: GPIO22 0x2: LED_SEG2 0x3: LCD_D2 0x4: EM_D2 0x5: PWM3 0x6: I2STX_MCLK 0x7: SD1_DAT0 0x8: SPI1_MOSI Others: Reserved	R/W	0x1

12.4.19 GPIO23_CTL

GPIO23 control Register

Offset=0x68

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0

4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC7) Note: There is only one GPIO can be set as LRADC7 When this GPIO is set as LRADC7, other can't be set as LRADC7.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG3 0x1: GPIO23 0x2: LED_SEG3 0x3: LCD_D3 0x4: EM_D3 0x5: PWM4 0x6: I2STX_DOUT 0x7: SD1_DAT1 0x8: SPI1_MISO Others: Reserved	R/W	0x1

12.4.20 GPIO24_CTL

GPIO24 control Register
Offset=0x6C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA	R/W	0x1

		101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA		
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC8) Note: There is only one GPIO can be set as LRADC8. When this GPIO is set as LRADC8, other can't be set as LRADC8.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG4 0x1: GPIO24 0x2: LED_SEG4 0x3: LCD_D4 0x4: EM_D4 0x5: PWM5 0x6: I2SRX_DI 0x7: SD1_DAT2 0x8: UART0_TX Others: Reserved	R/W	0x1

12.4.21 GPIO25_CTL

GPIO25 control Register
Offset=0x70

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0

23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC9) Note: There is only one GPIO can be set as LRADC9. When this GPIO is set as LRADC9, other can't be set as LRADC9.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG5 0x1: GPIO25	R/W	0x1

		0x2: LED_SEG5 0x3: LCD_D5 0x4: EM_D5 0x5: PWM6 0x6: I2SRX_MCLK 0x7: SD1_DAT3 0x8: UART0_RX Others: Reserved		

12.4.22 GPIO26_CTL

GPIO26 control Register
Offset=0x74

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC, when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable	R/W	0x0

		1: Enable		
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: disable 1: enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(LRADC10) Note: There is only one GPIO can be set as LRADC10. When this GPIO is set as LRADC10, other can't be set as LRADC10.	R/W	0x0
3:0	MFP	Multi-Function of GPIO 0x0: LCD_SEG6 0x1: GPIO26 0x2: LED_SEG6 0x3: LCD_D6 0x4: EM_D6 0x5: PWM7 0x6: Reserved 0x7: IR_RX 0x8: UART1_TX Others: Reserved	R/W	0x1

12.4.23 GPIO38_CTL

GPIO38 control Register(GPIO38 work in VCC domain)
Offset=0xA4

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable	R/W	0x0

		1: Enable		
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO38 1: Analog Function(VRO)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.24 GPIO39_CTL

GPIO39 control Register(GPIO39 work in VCC domain)
Offset=0xA8

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO39 1: Analog Function(VRO_S)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.25 GPIO40_CTL

GPIO40 control Register(GPIO40 work in AVCC domain)

Offset=0xAC

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO40 1: Analog Function(AUX0L)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.26 GPIO41_CTL

GPIO41 control Register(GPIO41 work in AVCC domain)
Offset=0xB0

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable.	R/W	0x0

		0: Disable 1: Enable		
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO41 1: Analog Function(AUX0R)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.27 GPIO42_CTL

GPIO42 control Register(GPIO42 work in VCC domain)
Offset=0xB4

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO42 1: Analog Function(AOUTL)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.28 GPIO43_CTL

GPIO43 control Register(GPIO43 work in VCC domain)
Offset=0xB8

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO43 1: Analog Function(AOUTR)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.29 GPIO44_CTL

GPIO44 control Register(GPIO44 work in AVCC domain)
Offset=0xBC

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable.	R/W	0x0

		0: Disable 1: Enable		
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO44 1: Analog Function(AUX1L)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.30 GPIO45_CTL

GPIO45 control Register(GPIO45 work in AVCC domain)
Offset=0xC0

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO45 1: Analog Function(AUX1R)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.31 GPIO46_CTL

GPIO46 control Register(GPIO46 work in AVCC domain)
Offset=0xC4

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO46 1: Analog Function(MIC0)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.32 GPIO47_CTL

GPIO47 control Register(GPIO47 work in AVCC domain)
Offset=0xC8

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x1
11:10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable.	R/W	0x0

		0: Disable 1: Enable		
8	GPIO100KPUEN	GPIO 100K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0:GPIO47 1: Analog Function(MIC1)	R/W	0x1
3:0	Reserved	Reserved	R	0x0

12.4.33 GPIO_ODAT0

GPIO Output Data register 0;
Offset = 0x100

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_ODAT	GPIO[31:0] Output Data.	R/W	0x0

12.4.34 GPIO_ODAT1

GPIO Output Data register 1;
Offset = 0x104

Bit(s)	Name	Description	R/W	Reset
31:20	Reserved	Reserved	R	0x0
19:0	GPIO_ODAT	GPIO[51:32] Output Data.	R/W	0x0

12.4.35 GPIO_BSR0

GPIO Output Data bit set register 0;
Offset = 0x108

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BSR	GPIO[31:0] Output Data bit set register 0: Not care; 1: Set the opposite bit of GPIO_ODAT0 as '1' and Set the GPIO to high level; Write this bit to '1', then will be clear automatically	R/W	0x0

12.4.36 GPIO_BSR1

GPIO Output Data bit set register 1;

Offset = 0x10C

Bit(s)	Name	Description	R/W	Reset
31:20	Reserved	Reserved	R	0x0
19:0	GPIO_BSR	GPIO[51:32] Output Data bit set register 0: Not care; 1: Set the opposite bit of GPIO_ODAT0 as '1' and Set the GPIO to high level; Write this bit to '1', then will be clear automatically	R/W	0x0

12.4.37 GPIO_BRR0

GPIO Output Data bit reset register 0;
Offset = 0x110

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BRR	GPIO[31:0] Output Data bit reset register 0: Not care; 1: Set the opposite bit of GPIO_ODAT0 as '0' and Set the GPIO to low level; Write this bit to '1', then will be clear automatically	R/W	0x0

12.4.38 GPIO_BRR1

GPIO Output Data bit reset register 1;
Offset = 0x114

Bit(s)	Name	Description	R/W	Reset
31:20	Reserved	Reserved	R	0x0
19:0	GPIO_BRR	GPIO[51:32] Output Data bit reset register 0: Not care; 1: Set the opposite bit of GPIO_ODAT0 as '0' and Set the GPIO to low level; Write this bit to '1', then will be clear automatically	R/W	0x0

12.4.39 GPIO_IDAT0

GPIO Input Data register 0;
Offset = 0x118

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_IDAT	GPIO[31:0] Input Data.	R	0x0

12.4.40 GPIO_IDAT1

GPIO Input Data register 1;
Offset = 0x11C

Bit(s)	Name	Description	R/W	Reset

31:20	Reserved	Reserved	R	0x0
19:0	GPIO_IDAT	GPIO[51:32] Input Data.	R	0x0

12.4.41 GPIO_PD0

GPIO IRQ Pending register 0;
Offset = 0x120

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_PD	GPIO[31:0] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it.	R/W	0x0

12.4.42 GPIO_PD1

GPIO IRQ Pending register 1;
Offset = 0x124

Bit(s)	Name	Description	R/W	Reset
31:20	Reserved	Reserved	R	0x0
19:16	GPIO_PD1	GPIO[51:48] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it.	R/W	0x0
15:6	Reserved	Reserved	R	0x0
5:0	GPIO_PD0	GPIO[37:32] IRQ Pending register. '0': No IRQ '1': IRQ Writing 1 to the bit is clear it.	R/W	0x0

12.4.43 WIO0_CTL

Wake up IO0/SIO0 control Register(This register is work in RTCVDD domain, WIO0 work in SVCC domain)
Offset=0x140

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	R	0x0
16	SIODAT	SIO Input/Output Data.	R/W	0x0
15	Reserved	Reserved	R	0x0
14:12	PADDRV	SIO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	R/W	0x0
11:10	Reserved	Reserved	R	0x0
9	SIO500KPDEN	SIO 500K PD Enable.	R/W	0x0

		0: Disable 1: Enable		
8	SIO500KPUEN	SIO 500K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	SIOINEN	SIOInput Enable. (When used as WIO, this bit should also be enable) 0: Disable 1: Enable	R/W	0x0
6	SIOOUTEN	SIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5:0	Reserved	Reserved	R	0x0

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Table 13-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	-10	70	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	4000	-	V
Supply Voltage	BAT	3.0	5	V
	VCC/AVCC/VDDIF/VDDRF/VDDLO/VDDDAC/SVCC	2.7	3.6	V
	ADC12	0.8	1.5	V
Input Voltage	ONOFF	-	5	V
	3.3V IO	2.7	VCC+0.2	V

Note:
Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

13.2 Recommended PWR Supply

Table 13-2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.3	3.8	4.5	V
VCC/VDDIF/VDDRF/VDDLO/VDDDAC/SVCC	2.7	3.1	3.4	V
AVCC	2.4	2.95	3.25	V
ADC12	1.08	-	1.45	V

13.3 DC Characteristics

Table 13-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.1V

High-level input voltage	VIH	2.0	-	V	Tamb = -10 to 70 °C
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 13-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.1V Tamb = -10 to 70 °C
Schmitt trigger negative-going threshold	VT-	1.2	-	V	

13.4 PWR Consumption

Table 13-5 PWR Consumption Table

VDD = 1.2V @ 25°C unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby	Is	Vbat = 3.8V;	-	45	60	uA

13.5 Bluetooth Characteristics

13.5.1 Transmitter

Table 13-6 Transmitter characteristics

VDD = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	4		dBm
RF PWR Control Range	-	-	16	-	dB

13.5.2 Receiver

Table 13-7 Receiver Performance

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity(when packet Type is 2-DH5)	0.1% BER	-	-86	-	dBm

13.5.3 Harmonic

Table 13-8 Harmonic

Parameter	2402MHz	2440MHz	2480MHz	Unit
2nd harmonic typical	-	-50	-	dBm
3rd harmonic typical	-	-50	-	dBm

Note:

A π -type matching or a Low Pass Filter(LPF) or Band Pass Filter(BPF) is needed to suppress the 2nd and 3rd harmonic energy, follow Actions design guide.

13.6 Stereo Audio ADC

Table 13-9 Audio ADC Parameters

Pre-Amplifier						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1%		-	-	2.8	Vpp
Analogue gain	AUX OP	-	-12	-	7.5	dB
	MIC OP	Single Ended	0	-	39	dB
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR (ADC+DAC+PA path)	fin = 1kHz@Full Scale Input Voltage, B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output		-	89	-	dB
			A-Weighting	91		
Dynamic Range (ADC+DAC+PA path)	fin = 1kHz@-40dBFS Input Voltage, B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output		-	88	-	dB
			A-Weighting	90		
THD+N (ADC+DAC+PA path)	fin = 1kHz(input=1.6Vpp), B/W = 22Hz~22kHz, Fs=48kHz & PA 1.6VPP output		-	-	-82	dB
			A-Weighting		-84	
Digital gain	-		0	-	45	dB

13.7 Stereo DAC

Table 13-10 Stereo DAC Parameters

Digital to Analogue Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	-			-	-	16	Bits
Output Sample Rate	-			8	-	48	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz	2.8VPP output@Load=10kΩ	-	-	94	-	dB
			A-Weighting		97		
		1.6VPP output@Load=16.5Ω	-	-	93	-	dB
			A-Weighting		96		
Dynamic Range	fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz	2.8VPP output@Load=10kΩ	-	-	90	-	dB
			A-Weighting		92		
		1.6VPP output@Load=16.5Ω	-	-	89	-	dB
			A-Weighting		91		
THD+N	fin = 1kHz@0dBFS input B/W =	2.8VPP output@Load=10kΩ	-	-	-81	-	dB
			A-Weighting		-83		

	22Hz~22kHz Fs=48kHz	1.6VPP output@Load=16.5Ω			-83		
			A-Weighting		-85		
Digital gain	-				-		-
Stereo crosstalk	fin = 1kHz@0dBFS input		-	-	-87	-	dB
PWR Amplifier							
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz	2.8VPP output@Load=10kΩ	Single Ended Output	-	-	945	mVrms
				-	-	-	mW
	fin = 1kHz@0dBFS input Fs=48kHz	1.6VPP output@Load=16.5Ω	Single Ended Output	-	-	550	mVrms
				-	-	18.3	mW

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	Acoustic Echo Cancellers
ADC	Analog-to-Digital-Converter
CP0	Control Coprocessor 0
DAC	Digital-to-Analog-Converter
dBFS	dB Full Scale
DMA	Direct Memory Access
GPIO	General Purpose Input Output
HOSC	High Frequency OSC
INTC	Interrupt Controller
IRQ	Interrupt Request
MIC	Microphone
MMU	Memory Management Unit
MFP	Multiple Function PAD
OSC	Oscillator

Actions (Zhuhai) Technology Co., Limited
Address:No. 1 / C, Ke Ji Si Road, Hi-Tech Zone, Tangjia, Zhuhai
Tel:+86-756-3392353
Fax:+86-756-3392251
Post Code:519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com