7-1. Circuit Composition and Operation Theory

The basic explanation for the circuit composition FRS-1000 consists mainly of the one board controlling the analog circuit parts and the digital circuit parts for the other control.

7-2. Receiver

FRS-1000 transmission parts is composed in the double conversion system, which has the 1st IF frequency of double 21.7 MHz and the 2nd IF frequency of 450 KHz. With the RF fronted which has an excellent band characteristics and skirt characteristics, the 2 pole MCF used in the 1st IF, and the 3 pole ceramic filter in the 2nd IF, the reception interrupting factors such as the image and the sensitivity repression are reduced for the more stable reception.

7-2-1. RF Front-end

The signal received by the antenna will be transmitted to the band pass filter through the antenna switching circuit consisted of L607, C613, D601. The front RF amplifier transistor Q1 consists of the C2, C3, C4, input band pass filter and SAW1 output band pass filter, primarily diminishes the other signal rather than the 1st IF image and other signal within the reception band and amplifier only the necessary signal within the RF

7-2-2. 1st Mixer

The receiver which has been amplifier in the RF front-end is provided to the base of the 1st mixer Q2. The 1st L/O signal provide from the VCO is supplied to the emitter of Q2 and Converted to the 1st IF 21.7 MHz

7-2-3. 1st IF Filter and 1st IF Amplifier

The signal covered by Q2 to 21.7 MHz, the 1st frequency, change its impedance through C17, L7 and then is infused to the fundamental MCF which has the center frequency of 21.7 MHz and the width of +/- 3.75 KHz.
Here, the signal reduces the image and other unwanted signal for the 2nd IF , and changes its impedance again through the R11. Then the signal is infused to the Q5, the 1st IF amplifier. The signal infused to the Q3 is amplifier approximately by 20 dB in other to acquire the required reception sensitivity, and infused to the IC1 which functions as the 2nd mixer, the 2nd IF amplifier, and the FM detector.

7-2-4. 2nd Mixer, and IF, FM Detector (IC1)

The receiver IF signal of 21.7 MHz, which has been infused to IC1 is mixed with the 2nd L/O converted to 450 KHz, the 2nd IF frequency. The receiver signal converted to the 2nd IF signal frequency passed through the CF2, the ceramic filter of 450 KHz again. After the limiting inside the IC1 and the FM demodulating by the quadrature detector inside the IC1, the signal offers the output through the 9th pin of IC1.
The squelch circuit is composed to detect the noises from the received signal demodulate in the 9th pin of the IC1. For this purpose, the noise filter is using the OP amplifier inside the IC1.

7-2-5. Audio Power Amplifier (IC9)

The receiver audio signal, which has been adjusted to the appropriate volume by IC4 supplied to the 2nd pin of the IC9 and amplified approximately by 20 dB.
Then, it turns up the speaker with the maximum output of 0.5 watts.
The 6th pin of IC9 is the audio mute terminal. If a voltage supply to the 6th pin of the IC2 is not supplied to this terminal, the IC9 stops functioning as the audio power amplifier regardless of the signal supplied to the 2nd pin of the IC9, and there is no sound emitter from the speaker.

7-3. Transmitter

The transmitter parts of the FRS-1000 is designed to amplify the RF signal oscillated and modulated by the synthesizer to approximately 0.5W by the power transistor of Q603,604,605.

7-3-1. Pre-emphasis (IC66)

The voice signal input from the microphone is pre-emphasized at the IC66B. The signal which comes out of the IC66A is limited to a certain amplitude for the voice signal not to exceed the allowable band width assigned for transmission.

7-3-2. Tx Power (Q603,604,605)

The transmitted signal of approximately 7 mW, combined at the driver TR is supplied to the base of the Q603,604,605 amplifiers. The transmitted signal amplifier to 0.5W here passes the TX LPF of the 2nd characteristics of the L608 and L609 and RX/TX switching takes place by the D601. After this, The signal is provided to the antenna the TX LPF of the 1st characteristics consisted of the L611.

7-4. "FRS" Frequency Synthesizer

7-4-1. Voltage Control Oscillator (VCO)

The VCO of oscillates 462.5625 MHz to 462.7125 MHz under the transmission condition and 467.5625 MHz to 467.7125 MHz under the reception condition. The VCO consist of the clip oscillator of the Q15 and contains the oscillator frequency of approximately 21.7 MHz during the transmission/reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared to transmission, the D5 is biased by the Q12.
Therefore as a result, the C89 is added in parallel to the resonance circuit of the VCO to oscillate a low frequency. During transmission, a relatively high frequency should be oscillate compared to reception. Therefore, the D5 is adversely biased by the Q12, and as a result , The C90 which is added unparalleled to the circuit of the VCO is removed to oscillate the desired transmission frequency.
The VCO is controlled by the IC3 PLL IC in order to oscillate accurate frequency. The output frequency of the VCO is supplied to the IC3 PLL IC immediately. At the IC3, TCXO(21.25MHz) is compared to the output frequency of the VCO.

The VCO is controlled the loop filter consisted of the R42, R43, R45 and the C72, C73, C74 in order to oscillate the stable frequency wanted for the radio.
The VCO controlled voltage which as passed the loop filter is supplies to the D6 varactor diode, and the VCO an oscillate the PLL programmed frequency by the capacity variance in the D6. In addition, the L12 on the VCO circuit function as frequency for the VCO to be properly controlled by the IC3 PLL IC.

7-4-2. RX/TX Buffer Amplifier (Q5,Q601)

The RF signal oscillate at the VCO is provide to the Q2 RX 1st mixer through the Q13 during the reception, and is provide to the Q603,604,605 power driver amplifier through the Q601 during the transmission.

7-4-3. PLL Frequency Synthesizer (IC3)

The PLL synthesizer of the signal loop PLL circuit with the reference of 6.25 KHz. The IC3 PLL IC includes all the function such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider. At the reference oscillator, the 21.25 MHz TCXO is connected to the pin 11 of the IC3 to oscillate the frequency of 21.25 MHz. The TCXO (21.25 MHz) is the temperature compensation circuit to maintain the frequency within the allowable error rang even under a low temperature of -30° C. The phase detector send out the output power to the loop filter through 3rd pin of the IC3. If the oscillation frequency of the VCO is low compared to the reference frequency, the phase detector send out output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector send out can maintain the frequency set. The programmable divider maintains the desired frequency with control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below :

N = VCO oscillation frequency / reference frequency

If the desired frequency is 462.5625 MHz

a) TX : N = 462.5625 MHz / 0.00625 MHz = 74010

b) RX : N = [462.5625 MHz – 21.7 MHz] / 0.00625 MHz = 70538

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