Fibocom
PERFECT WIRELESS EXPERIENCE

MG661-EU/LA

Hardware Guide

V1.0

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Contact Information

Website: https://www.fibocom.com

Address: 10/F-14/F, Block A, Building 6, Shenzhen International Innovation Valley, Dashi First Road, Xili Community, Xili Subdistrict, Nanshan District, Shenzhen

Tel: 0755-26733555

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Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Contents

Applicable Model

No.	Applicable Model	Description
1	MG661-EU/LA-19	Support LTE FDD

Change History

V1.0 (2023-06-04)	Initial version.

1 Product Overview

1.1 Product Introduction

The MG661 module is a broadband wireless terminal product applicable to multiple bands for FDD. The following table lists the sub-models of the MG661 product.

Table 1. Sub-models of the MG661 module

Item	MG661-EU-19	MG661-LA-19
LTE FDD	Band 1/3/5/7/8/20/28	Band 2/3/4/5/7/8/28/66
ANT	Main	Main
Memory	4MB Flash+8MB RAM	4MB Flash+8MB RAM

Main indicates that the main antenna use a common circuit and work in a time-sharing manner.

1.2 Product Specifications

The product hardware has the following characteristics.

Table 2. Basic configuration

Category	Description
Controller	500MHz
Memory	4MB Flash+8MB RAM

Table 3. Baseband characteristics

Category	Description
Function interface	USB × 1: USB 2.0, can be used for AT communication, capturing log and upgrading software version; I2C × 3: Support standard mode 100KHz and fast mode 400KHz, and the internal software of the module is pulled up by default SPI × 3: Two dedicated SPI interfaces (SPI CAM and SPI LCD) and one dedicated SPI FLASH interface ADC × 2: Supports 12-bit ADC, voltage range 0 to VBAT UART × 2: Used for sending AT commands or data transmission, the baud rate defaults to 115200bps, and the main serial port UART1 can support RTS and CTS hardware flow control GPIOs KEYs DEBUG_UART × 1: Debug serial port for AP log output, and the baud rate is 2M
Peripheral interface	SIM × 2: Support 1.8 V and 3V cards, support hardware two SIM card interfaces, but whether to support dual cards is mainly distinguished by software LCD × 1 CAM × 1 PCM/I2S: For external audio Codec

Table 4. RF characteristics

Category	Description
Antenna interface	Main antenna × 1

- The above supported interface description is based on the default definition of MG661 pins. Some pins in the OPEN version can be reused for other functions. For details, see the GPIO reuse table.
- The DEBUG_UART function corresponds to pins pin 38 and 39. By default, the function is UART4 and can be used to capture AP logs.
- Module pin 7, 58 can be reused as UART2 function, which is used to output CP log with baud rate of 8M.
- Two groups of USIM interfaces are supported by the hardware, but whether the module supports dual cards is mainly distinguished by software. The single card only supports SIM1 function of pin 11, 12, 13 and 14 by default.

1.3 Hardware Block Diagram

The MG661 product hardware consists of the following parts:

- Baseband part: CPU, memory, 26M
- RF part: RF Transceiver, RF PA, RF filter antenna

The following figure shows the internal structural block diagram.

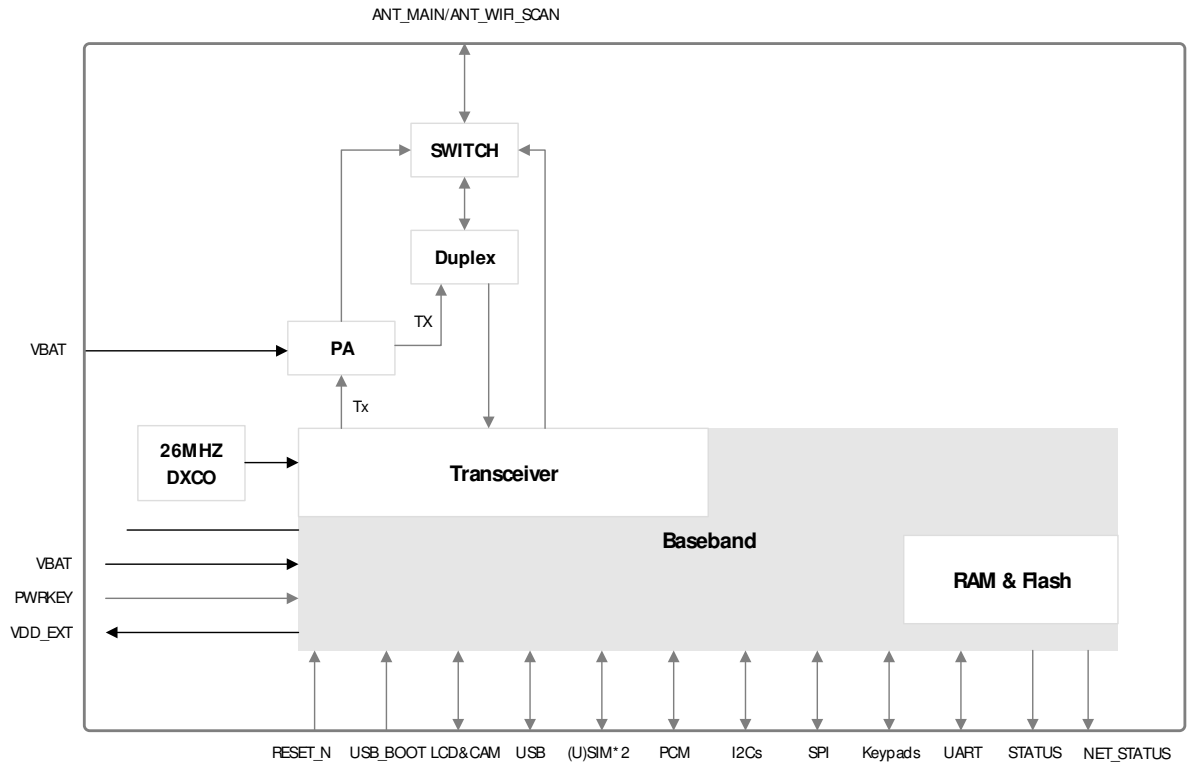


Figure 1. Hardware block diagram

1.4 Description of Development Board

To help customers develop MG661 modules, Fibocom provides MG661development boards (shared with MC981 series) for controlling or testing modules. For more details, see *Fibocom_MC981-CN_ADP User Guide*.

2 Pin Definition

2.1 Pin Attributes

The following attributes are used to describe pins.

Table 5. Pin attributes

Attribute	Description
No.	Pin No.
Name	Pin Name
I/O	Direction of pin signal PI: Power Input PO: Power Output DI: Digital Input DO: Digital Output DIO: Digital Input and Output AI: Analog input AO: Analog Output AIO: Analog Input and Output OD: Open Drain G: Ground
Voltage	Power domain of the interface
Description	Specific meaning of the pin and processing method when it is not used

2.2 Pin Distribution

The MG661 module is designed with LGA package and available with a total of 109 pins.

The distribution of pins is shown in the following figure.

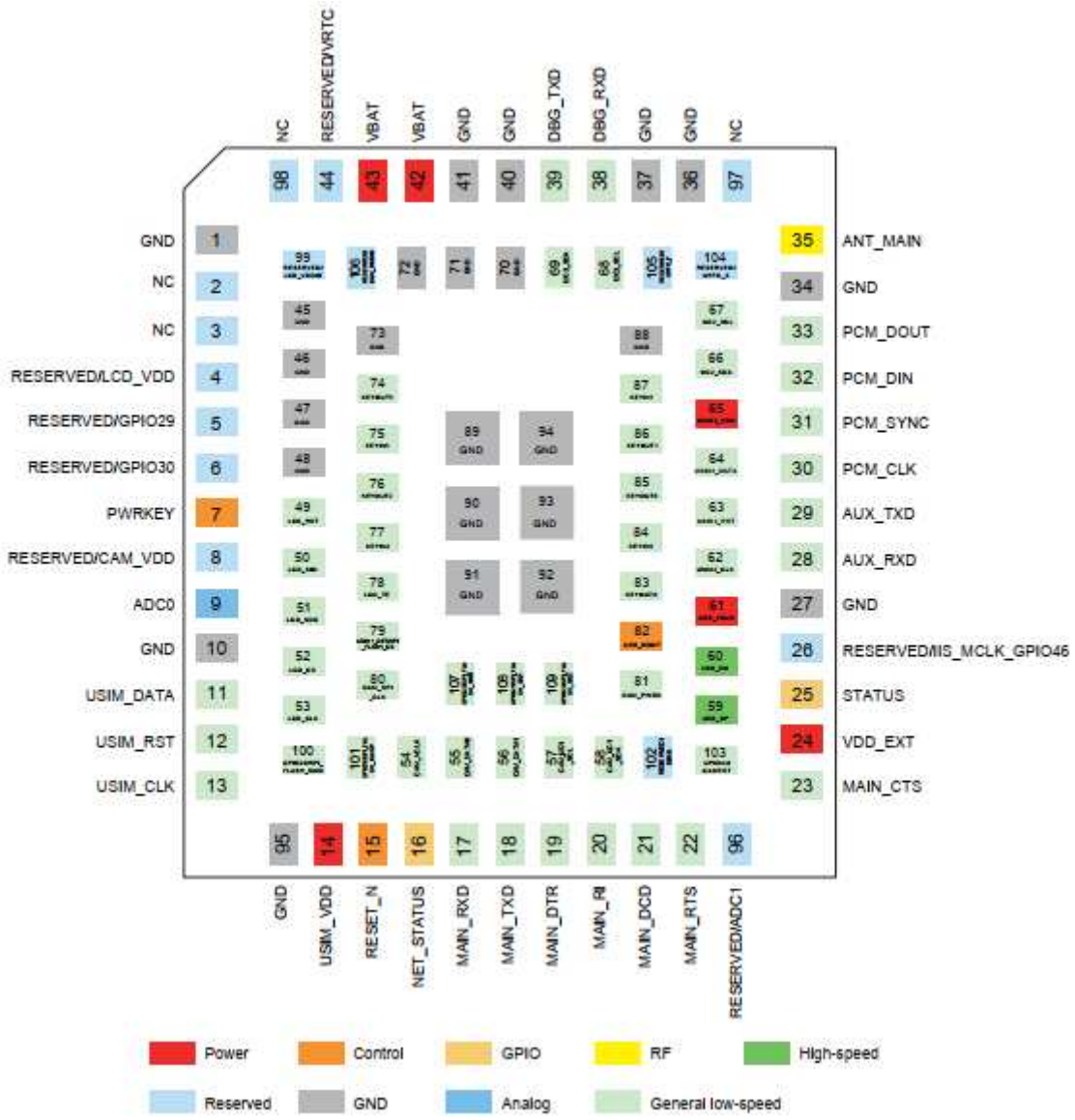


Figure 2. Pin distribution

- Keep the NC pin unconnected.
- Connect all GND pins to the ground network.
- The functions of reserved pins 4, 5, 6, 8, 26, 44, 96, 99, 102, 104, 105 and 106 in the figure have been debugged OK. For details, see the next section.

- Pin79 can be reused as USIM1_DET and SPI_FLASH_CS functions. When using external FLASH, SIM hot plug can be implemented by using other GPIO.
- If the USB_BOOT/KEYIN0 pin is pulled low or high before starting up, or the key combined with KEYOUT0 is pressed, the module will enter the download mode. Please be careful not to trigger it by mistake during design. It is recommended to pull down USB_BOOT to enter the download mode.
- KEYIN1 and KEYIN2 cannot be pulled low before starting up, otherwise it will enter the abnormal download mode.
- The power output of pin 99 LCD_VDDIO is the power domain voltage of the relevant pin of LCD. The default voltage of LCD_VDDIO is 1.8 V, that is, the voltage of LCD related pins 49, 50, 51, 52, 53 and 78 is 1.8 V.
- The reserved function LCD_VDD of pin 3 is occupied internally and has power-off control for sleep and flight modes. Therefore, it is not recommended for external use. If you must use it, check whether the current and timing of each application scenario meet the requirements.
- Reserve pin 38/39 for the AP and pin 57/58 for the CP LOG. The pin is not anti-backflow. When using, please note that after the module pin is powered off (shutdown or in PSM mode), there shall be no external high level or pull-up.
- If pin 57/58 is occupied, other pins that can be reused for UART2 function can be reserved as CP log port.
- To avoid interference, wiring is prohibited on the surface of the bottom plate below the module.

2.3 Pin Details

Unused pins are left unconnected.

Pins with * indicate that there are notes at the end of the section.

Table 6. Power interfaces

Pin No.	Pin Name	I/O	Power domain	Description
42, 43	VBAT	PI	3.4V–4.5V	Baseband/RF power input (3.4–4.5V) 3.8 V is recommended
24	VDD_EXT	PO	1.8V	Digital level, 1.8V output, with the maximum current of 100mA

Table 7. Control interface

Pin No.	Pin Name	I/O	Power Domain	Description
15	RESET_N	DI	VBAT	When the module is working, pull down RESET_N 100 ms or longer, and then release it. The module resets. Pins are internally pulled up to VBAT, and no external pull up is required.
7	PWRKEY	DI	VBAT	In power-off state, pull down PWRKEY for a long time, and the module automatically powers on. In power-off state, pull the PWRKEY for 2s or longer, and then release it, the module powers on. In power-on state, pull the PWRKEY for 3.1s or longer, and then release it, the module powers off.

Pin No.	Pin Name	I/O	Power Domain	Description
				Pins are internally pulled up to VBAT, and no external pull up is required.
82	USB_BOOT/KEYIN0	DI	1.8V	If USB_BOOT is pulled down to ground or up to 1.8V, the module will enter the download mode if it is powered on or reset. It is recommended to pull down USB_BOOT to enter the download mode.

Table 8. Baseband interface

Pin No.	Pin Name	RESET VALUE	I/O	Power Domain	Description
5	GPIO29	PU	DIO	1.8V	GPIO pin
6	GPIO30	PU	DIO	1.8V	GPIO pin
44	VRTC*	- -	PI	3.0V	RTC power input, not recommended, can be suspended
102	ISINK	- -	PI	- -	Current source input pin, can be connected to the cathode of the backlight, by adjusting the ISINK current to adjust the brightness of the backlight
1, 10, 27, 34, 36-37, 40-41, 45-48, 70-73, 88-95	GND	- -	G	- -	Ground

Pin No.	Pin Name	RESET VALUE	I/O	Power Domain	Description
2, 3, 97, 98	NC	- -	- -	- -	Suspended

Table 9. RF interface

Pin No.	Pin Name	I/O	Power Domain	Description
35	ANT_MAIN	- -	- -	Main antenna
104	GRFC_6*	DO	1.8V	RF control signal, not recommended
105	GRFC_7*	DO	1.8V	RF control signal, not recommended

Table 10. LPG interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
16	NET_STATUS	DO	PD	1.8V	Network status indication
25	STATUS	DO	PU	1.8V	Operating status indication

Table 11. USB interface

Pin No.	Pin Name	I/O	Power Domain	Description
61	USB_VBUS	PI	5.0V	USB insertion detection, typical value: 5 V
60	USB_DM	IO	3.3V	USB differential data signal (–), ensure 90Ω differential impedance
59	USB_DP	IO	3.3V	USB differential data signal (+), ensure 90Ω differential impedance

Table 12. SPI interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
101	SPI_FLASH_CLK	DO	PD	1.8V	SPI clock signal
100	SPI_ FLASH_SIO0	DIO	PD	1.8V	SPI data transmission
107	SPI_ FLASH_SIO3	DIO	PD	1.8V	SPI data transmission
108	SPI_ FLASH_SIO1	DIO	PD	1.8V	SPI data transmission
109	SPI_ FLASH_SIO2	DIO	PD	1.8V	SPI data transmission
79	SPI_ FLASH_CS	DO	PD	1.8V	SPI chip selection

Table 13. I2C interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
67	I2C2_SCL	OD	PU	1.8V	I2C clock signal, internal software pull-up, external 1.8V hardware pull-up can be reserved, can be suspended when not in use
66	I2C2_SDA	OD	PU	1.8V	I2C data signal, internal software pull-up, external 1.8V hardware pull-up can be reserved, can be suspended when not in use
68	I2C3_SCL	OD	PU	1.8V	I2C clock signal, internal software pull-up, external 1.8V

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
					hardware pull-up can be reserved, can be suspended when not in use
69	I2C3_SDA	OD	PU	1.8V	I2C data signal, internal software pull-up, external 1.8V hardware pull-up can be reserved, can be suspended when not in use

Table 14. Debug interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
39	DBG_TXD	DO	PU	1.8V	Debug serial port transmitting
38	DBG_RXD	DI	PU	1.8V	Debug serial port data receiving

Table 15. USIM interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
11	USIM_DATA	DIO	--	1.8V/3V	(U)SIM data signal line, SIM_DATA has internal pull-up, external pull-up can be reserved to SIM_VDD, keep NC first
12	USIM_RST	DO	--	1.8V/3V	(U)SIM reset signal line
13	USIM_CLK	DO	--	1.8V/3V	(U)SIM clock signal line

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
14	USIM1_VDD	PO	--	1.8V/3V	(U)SIM power supply, the module automatically identifies 1.8V or 3.0V (U)SIM card
79	USIM1_DET	DI	PD	1.8V	SIM 1 detection
64	USIM2_DATA	DIO	PD	1.8V/3V	(U)SIM data signal line, SIM_DATA has internal pull-up, external pull-up can be reserved to SIM_VDD, keep NC first
63	USIM2_RST	DO	PD	1.8V/3V	(U)SIM reset signal line
62	USIM2_CLK	DO	PD	1.8V/3V	(U)SIM clock signal line
65	USIM2_VDD	PO	--	1.8V/3V	(U)SIM power supply, the module automatically identifies 1.8V or 3.0V (U)SIM card

Table 16. UART interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
22	MAIN_RTS	DO	PU	1.8V	Main serial port UART1 transmitting request
23	MAIN_CTS	DI	PU	1.8V	Main serial port UART1 clears to send
20	MAIN_RI	DO	PD	1.8V	Ring prompt

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
21	MAIN_DCD	DO	PD	1.8V	Carrier detection
19	MAIN_DTR	DI	PD	1.8V	Data ready
18	MAIN_TXD	DO	PU	1.8V	Main serial port UART1 data transmitting
17	MAIN_RXD	DI	PU	1.8V	Main serial port UART1 data receiving
29	AUX_TXD	DO	PD	1.8V	UART1 data transmitting
28	AUX_RXD	DI	PD	1.8V	UART6 data receiving

Table 17. ADC interface

Pin No.	Pin Name	I/O	Power Domain	Description
9	ADC0	AI	VBAT	Analog-to-digital conversion 0
96	ADC1	AI	VBAT	Analog-to-digital conversion 1

Table 18. CAM interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
54	CAM_MCLK	DO	PD	1.8V	CAMERA clock signal
57	CAM_I2C1_SCL	OD	PU	1.8V	CAMERA I2C clock signal, internal software pull-up, external 1.8V hardware pull-up can be reserved, can be suspended when not in use
58	CAM_I2C1_SDA	OD	PU	1.8V	CAMERA I2C data signal, internal software pull-up, external 1.8V

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
					hardware pull-up can be reserved, can be suspended when not in use
80	CAM_SPI_CLK	DO	PD	1.8V	CAMERA SPI clock signal
55	CAM_DATA0	DIO	PD	1.8V	CAMERA MIPI data D0
56	CAM_DATA1	DIO	--	1.8V	CAMERA MIPI data D1
81	CAM_PWDN	DO	PD	1.8V	CAMERA POWER DOWN signal
8	CAM_VDD	PO	--	2.8V	CAMERA power supply with a maximum current of 100mA
106	CAM_VDDIO	PO	--	1.8V	CAMERA IO port power supply with a maximum current of 100mA
103	CAM_RST	DO	PD	1.8V	CAMERA reset signal

Table 19. LCD interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
50	LCD_SIO	DIO	PD	LCD_VDDIO (1.8V)	LCD SPI bus data bit
49	LCD_RST	DO	PD	LCD_VDDIO (1.8V)	LCD SPI bus reset signal
51	LCD_SDC	DO	PD	LCD_VDDIO (1.8V)	LCD SPI bus data address switching signal
53	LCD_CLK	DO	PD	LCD_VDDIO （1.8V）	LCD bus clock signal
52	LCD_CS	DO	PD	LCD_VDDIO	LCD bus chip selection

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
				(1.8V)	
4	LCD_VDD	PO	--	2.8 V	LCD analog power supply, with a maximum current of 100mA, shared with module internal switch, can not be enabled or disabled separately
99	LCD_VDDIO	PO	--	1.8V-3.2V	LCD IO interface power supply with a maximum current of 200mA Voltage ranges from 1.8V to 3.2V can be configured, after this power supply voltage changes, LCD pins (PIN 49-53, 78) voltage will change The default voltage is 1.8V
78	LCD_TE	DIO	PD	LCD_VDDIO (1.8V)	LCD synchronization signal

Table 20. KEY interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
83	KEYOUT0	DO	PD	1.8V	KEY output 0
76	KEYOUT2	DO	PD	1.8V	KEY output 2

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
77	KEYIN2	DI	PU	1.8V	KEY input 2, cannot be pulled down externally before boot, otherwise the module will enter abnormal download mode
85	KEYOUT6	DO	PD	1.8V	KEY output 6
84	KEYIN6	DI	PD	1.8V	KEY input 6
86	KEYOUT1	DO	PD	1.8V	KEY output 1
87	KEYIN1	DI	PU	1.8V	KEY input 1 and cannot be pulled down before boot, otherwise the module will enter the abnormal download mode
74	KEYOUT5	DO	PD	1.8V	KEY output 5
75	KEYIN5	DI	PD	1.8V	KEY input 5

Table 21. PCM/I2S interface

Pin No.	Pin Name	I/O	RESET VALUE	Power Domain	Description
30	PCM_CLK	DO	PD	1.8V	PCM clock
31	PCM_SYNC	DO	PD	1.8V	PCM data synchronization signal
32	PCM_DIN	DI	PD	1.8V	PCM data input
33	PCM_DOUT	DO	PD	1.8V	PCM data output
6	I2S_MCLK	DO	PD	1.8V	I2S main clock output signal

- The PIN44 VRTC pin is input by an external battery to maintain the voltage value after the module is powered down If it is necessary to use VRTC to maintain the reference clock in the module power-off state, it is not possible to use the PWRKEY automatic power-on design, otherwise it will lead to the failure of secondary power-on after shutdown. In addition, if the VRTC pin is used, the module must go through the normal shutdown process, and the module VBAT cannot be powered down directly, otherwise the clock will not be saved.

- PIN104/105 GRFC_6/7: RF tuning antenna control interface. If it is necessary to use it, please confirm with Fibocom.
- All RESET VALUEs in the table refer to the corresponding state of the pin of the module at RESET instant (during the duration of RESET low level) (at this time, the pin corresponds to the Function 0 in the GPIO multiplexing table), PU represents high level, and PD represents low level. For detailed GPIO state, please refer to the GPIO multiplexing table. Especially when enabling electro-acoustic devices, or controlling motors, relays and other devices, please refer to the GPIO multiplexing table to select the appropriate GPIO.

3 Application Interfaces

3.1 Power Interfaces

3.1.1 Electrical Indicators

Table 22. Electrical indicators

Indicator		Minimum Value	Typical Value	Maximum Value	Unit
Power supply voltage	VBAT power supply	3.4	3.8	4.5	V
Logic level	Digital input high level	1.6	--	--	V
	Digital input low level	--	--	0.3	V
	Digital output high level	1.2	--	--	V
	Digital output low level	–0.3	--	0.5	V

Table 23. Limit voltage indicator

Indicator		Minimum Value	Maximum Value	Unit
Power supply voltage	VBAT power supply	–0.3	4.6	V
USB_VBUS	USB insertion detection	–0.3	5.2	V

Indicator		Minimum Value	Maximum Value	Unit
GPIO	Level power supply voltage of digital I/O	–0.3	2.0	V

3.1.2 Power Input

Background

The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. If the power supply capacity is insufficient and the power supply voltage instantaneous drops, the module may be powered off or restarted.

The following figure shows the power supply limit.

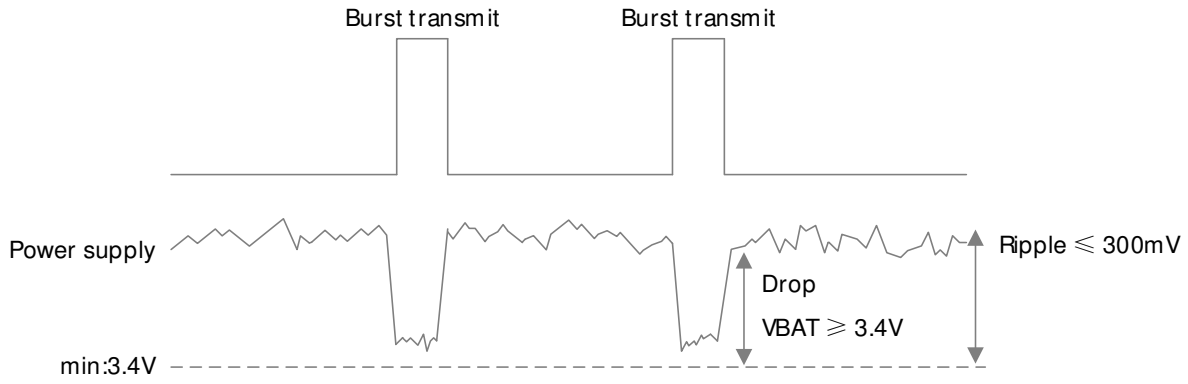


Figure 3. Power supply limit

The ripple of the power supply should be lower than 300 mV, and the line ESR (equivalent series resistance) should be < 150 mΩ. When the module is working, it is necessary to ensure that the DC power supply voltage is between 3.4V and 4.5V, including voltage sag, ripple and spike. The module power supply is far away from interference sources such as antennas.

Schematic Diagram Design

VBAT is the power pin of the module.

The reference design is shown in the following figure.

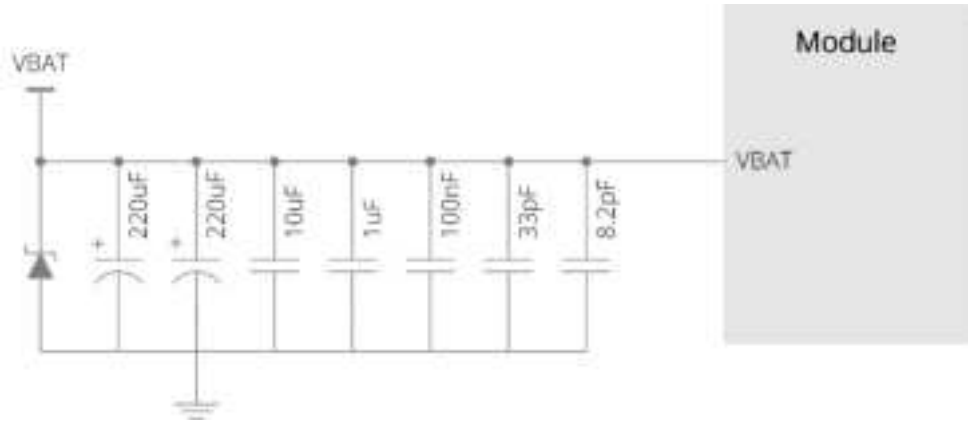


Figure 4. Reference power supply design

Design Description

Table 24. Design description

Design Consideration	Mode	Recommended Parameter
To reduce power fluctuations during module operation	Regulating capacitor	Use a capacitor with low ESR 220uF x 2, 10uF, 22uF LDO or DCDC power supply requires capacitor with a capacitance of no less than 440uF. Battery power supply requires capacitance of 100uF to 220uF.
Filter out interference caused by clock and digital signals.	Filter capacitor	1uF, 100nF
Eliminate low-frequency and intermediate-frequency RF interference.	Decoupling capacitor	33pF, 8pF

It is recommended to reserve the TVS tube position for the VBAT power supply. Recommended model: ESDH4V5P1/ESD5651N.

PCB Design

To reduce the equivalent impedance of the VBAT routing, the routing from the external power supply to VBAT is required to be as short and wide as possible (it is recommended that the routing width of VBAT should be at least 2 mm/2A to ensure sufficient power supply capacity). The capacitors with a small capacitance should be placed close to the module, and the ground plane of the power supply part should be as complete as possible.

Power supply layout and routing are far away from interference sources such as antennas.

3.1.3 Power Output

The power output interface of the module is described in the following table.

Table 25. Module power interface

Pin No.	Pin Name	I/O	Description	DC Parameter		
				Minimum Value (V)	Typical Value (V)	Maximum Value (V)
24	VDD_EXT	PO	Digital level 1.8V, 100mA	1.74	1.8	1.85

3.2 Control Interfaces

3.2.1 Power-on

Schematic Diagram Design

The startup sequence of the module is shown in the following figure.

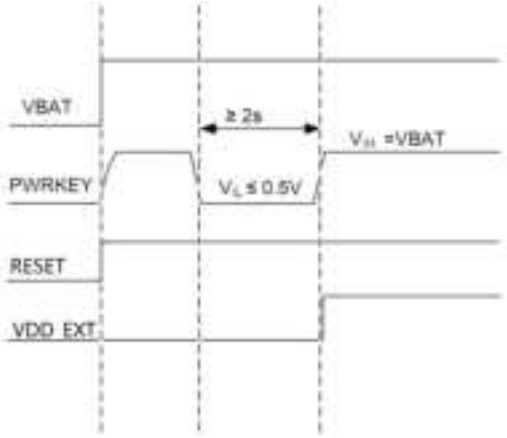


Figure 5. Power-on sequence

Before pulling down the PWRKEY pin, make sure that the VBAT voltage is stable. It is recommended that the time interval between VBAT power-on and pulling PWRKEY pin down be no less than 30ms, and the time for pulling PWRKEY pin down is recommended to last for 2 s (the minimum time for pulling PWRKEY down is 700ms).

One way is to use an OC/OD drive circuit to control the PWRKEY pin. The reference circuit is shown in the following figure.

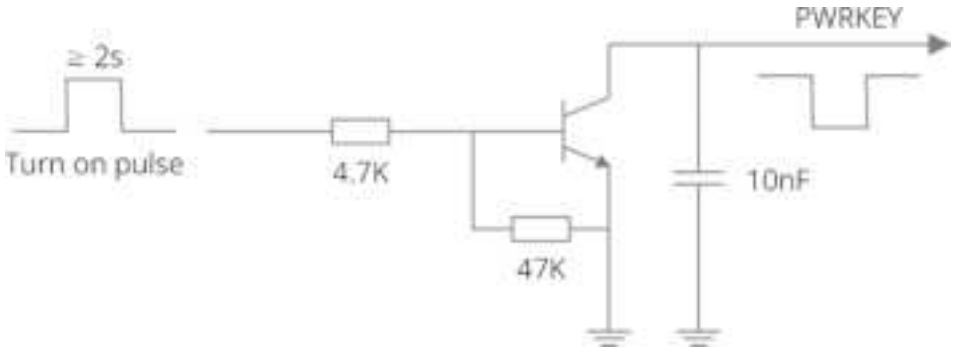


Figure 6. OC/OD drive reference circuit

The other way is to use a button switch. A TVS (ESD9X5VL-2/TR is recommended) should be located close to the button to implement ESD protection. The reference circuit is shown in the following figure.

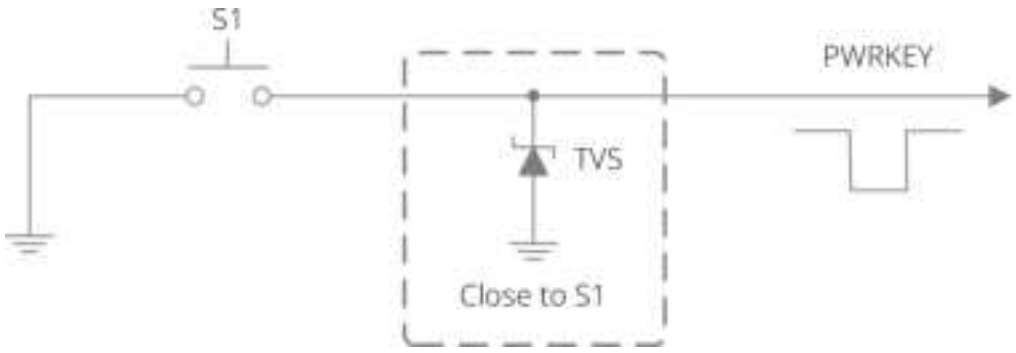


Figure 7. Button control reference circuit

Automatic power-on design: If the module needs to be powered on automatically, the PWRKEY pin can be connected in series with the resistor to ground (recommended resistance value is 1KΩ or 0Ω). In this way, the module sleep current will increase by about 0.2mA, and the module can only be directly powered off when it is powered down.

In addition, if you use the automatic power-on design, ensure that the battery/power supply voltage is not lower than the module automatic power-off voltage, otherwise you need to re-power up and down again or plug and remove the USB to power on normally.

Before pulling down the PWRKEY pin, make sure that the VBAT voltage is stable. It is recommended to control the interval from power-up by VBAT to PWRKEY pin pull-down no less than 30ms.

It is not recommended to design pull-down resistor larger than 1K for automatic power-on, otherwise it cannot guarantee that PWRKEY voltage is within the range of effective low level, which will lead to probability failure of boot.

3.2.2 Power-off

Background

The module can be powered off through the following ways:

- Low voltage power-off: The module is powered off when the power supply voltage is lower than the rated minimum operating voltage. The module does not log out from a base station.

- Hardware power-off: The module is powered off when the PWRKEY pin is pulled down for at least 3.1s.
- Software power-off: The module is powered off through the AT+CPWROFF command. This mode applies only to non-main control modules.

When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal flash and causing data loss. It is strongly recommended to power off the module by a normal way before cutting off the power supply.

When using the software to power off the module, ensure that the PWRKEY pin is always at the high level after the power-off command is executed. Otherwise, the module will automatically power on again.

Software command shutdown cannot be realized during automatic power-on design.

Avoid the low voltage power-off scenario when designing automatic power-on, otherwise it may lead to the failure of secondary power-on.

The hardware power-off sequence is follows.

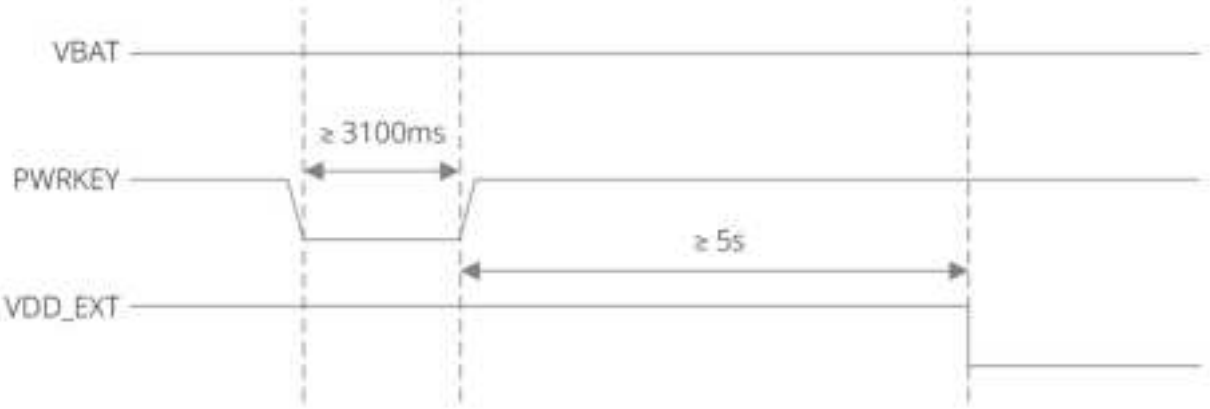


Figure 8. Hardware power-off sequence

After the PWRKEY signal is released, the next power-on trigger can be performed at least 5 seconds later. This interval is reserved for the module to perform the shutdown process and release the power of the peripheral circuit connecting with module interface.

3.2.3 Reset

Background

When the module needs to be restored to its initial state, it can be reset.

The module supports hardware reset and software reset.

- Hardware reset

The hardware reset timing sequence is as follows.

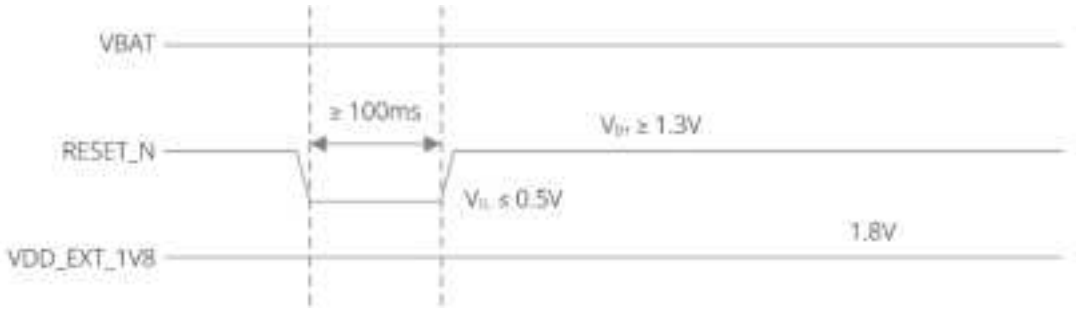


Figure 9. Hardware reset sequence

Set RESET_N to low level and hold for at least 100ms, then release. Similar to the power on/off control circuit, the reset reference circuit is shown in the following figure, and the RESET_N pin can be controlled using the OC/OD driver circuit or the button.

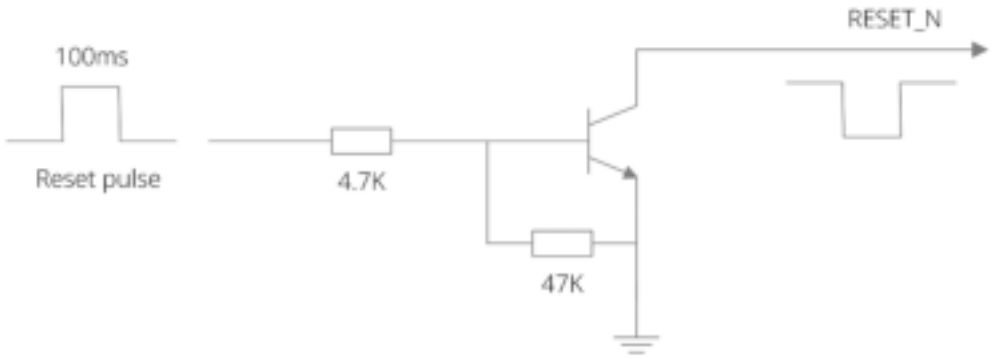


Figure 10. OC/OD drive reset reference circuit

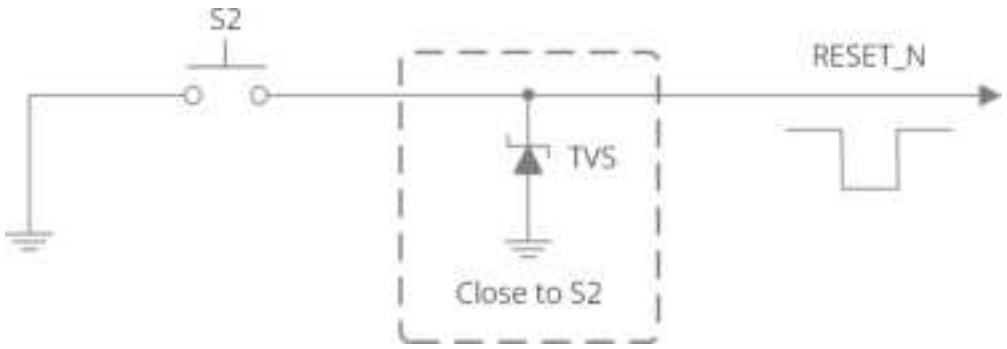


Figure 11. Button control bit reference circuit

Reset signal is a sensitive signal, so it is recommended to add a debounce capacitor (< 10 nf) close to the module.

- Software reset

AT+CFUN=15

PCB Design

RESET_N is a sensitive signal. During PCB layout, keep this signal far away from RF interference.

PCB routes must be protected using GND and kept away from edges of PCBs to avoid module reset due to ESD problems.

3.2.4 Download

The MG661 module supports USB download function. To enter the download mode, it is necessary to pull down USB_BOOT to ground or pull up to VDD_EXT, and then power on or reset the module. The module will enter the download mode. It is recommended to pull down USB_BOOT to ground to enter the download mode.

In the download mode, the module can be upgraded by the software through the USB interface. The following figure shows the reference circuit.

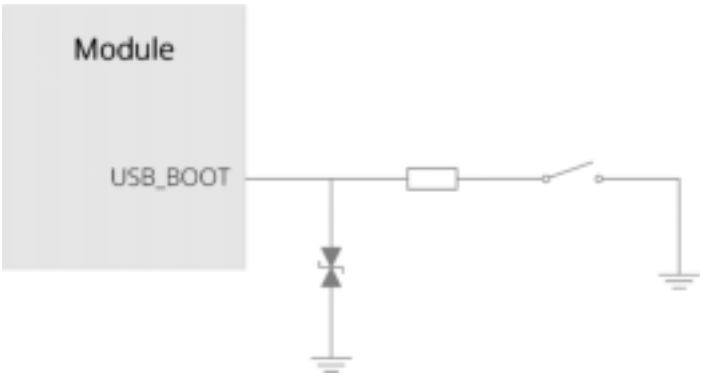


Figure 12. Reference circuit for entering the download mode

It is recommended to add 1k resistor and TVS tube near the module.

3.3 Baseband Interface

For details about how to use the GPIO multiplexing function of MG661 Open models, see *Fibocom_MG661_GPIO Function Multiplexing Table*.

3.3.1 USB 2.0

Background

USB (Universal Serial Bus) is an external bus standard used to regulate the connection and communication between computers and external devices. It is the interface technology applied in PC field. USB is generally used for debugging, or for software upgrades.

Schematic Diagram Design

The interface circuit design is shown in the following figure.

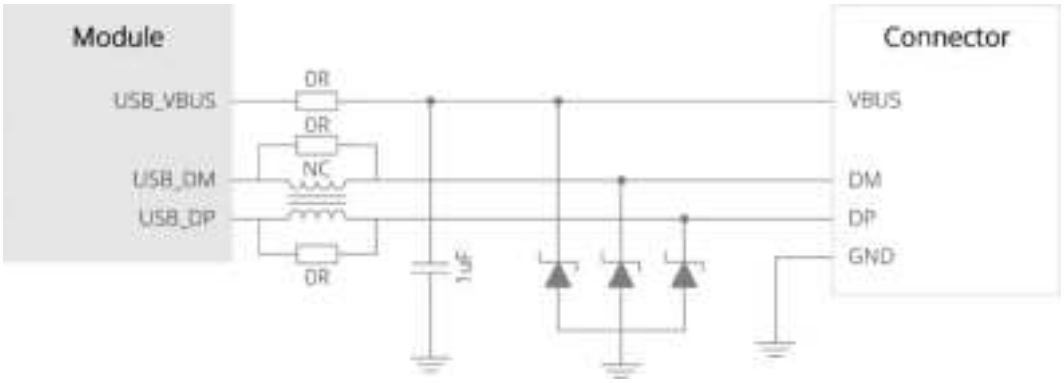


Figure 13. Interface circuit design

Since the module supports USB 2.0 High-Speed, it is recommended to use TVS with a capacitance of 0.5 pF on the USB_DM/DP differential signal line. It is recommended to connect a 0-ohm resistor on each USB_DM/DP differential line to facilitate debugging. USB enumeration requires an additional voltage to USB_VBUS. Otherwise, USB cannot be enumerated normally. The voltage range is 3.5V to 5.5V.

PCB Design

USB_DP and USB_DM are high-speed differential signal lines that should be equal in length and parallel to avoid right-angle route. The difference of cabling length is controlled within ≤ 2 mm, and the differential impedance is controlled at 90Ω±15%.

The USB data cable cannot be routed under the crystal, oscillator, magnetic device, or RF signal. It is recommended to take an inner differential cable that is wrapped with copper connected to the ground at all directions.

The ESD protector for the USB data cable must be placed close to the USB interface. The parasitic capacitance of the ESD protector must not exceed 1 pF, and a TVS with a capacitance of 0.5pF is recommended.

USB 2.0 differential signal cable should be laid on the signal layer nearest to the ground.

If the USB function is not used, you are advised to reserve test points for easy log capture and software upgrade.

3.3.2 UART

Background

UART is a Universal Asynchronous Receiver/Transmitter. It converts a parallel input signal into a serial output signal. UART is generally used to communicate with PCs, including monitoring debuggers and other devices, such as EEPROM.

Schematic Diagram Design

The module has main serial ports MAIN_UART and AUX_UART, and debugging serial port DEBUG_UART.

- MAIN_UART supports baud rates of 1200bps, 2400bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 1000000bps, 1500000bps and 2000000bps. The default baud rate is 115200 bps, used for data transmission and AT command exchange. Sleep and wakeup are supported.
- AUX_UART is a set of auxiliary serial ports that can be configured as UART6 or UART3. It supports baud rates of 1200bps, 2400bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 1000000bps, 1500000bps and 2000000bps. The default baud rate is 115200 bps.
- The debugging serial port DEBUG_UART supports 2000000bps baud rate for module AP log output. The baud rate is 2M.

The serial port level of the MG661 module is 1.8V. If the level of the customer host system is 3.3V or others, it is necessary to add a level converter in the serial port connection between the module and the host. The following figures show the design of reference circuit of the serial port level conversion chip. You can design the input and output circuits of the dashed line part by referring to the solid line part in the figure 15, but pay attention to the connection direction.

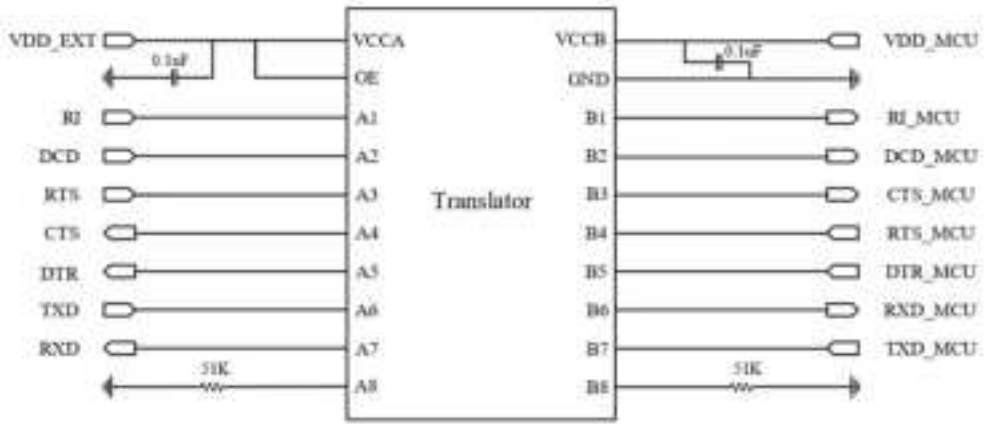


Figure 14. Reference circuit 1 for serial port level conversion

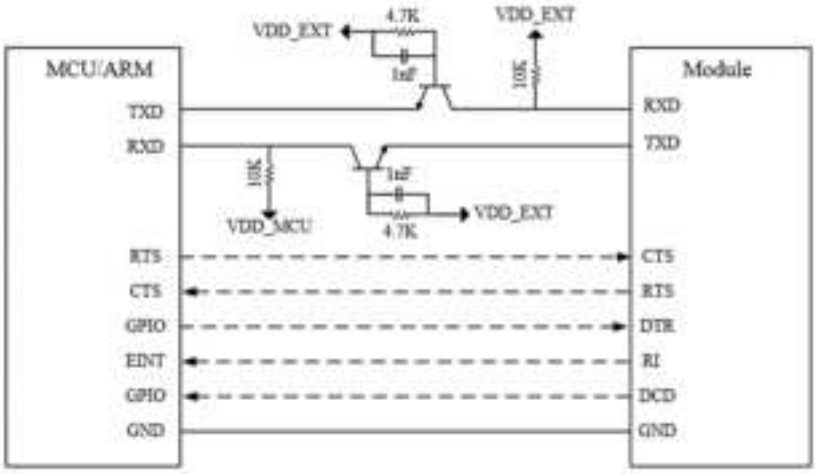


Figure 15. Reference circuit 2 for serial port level conversion

The level conversion circuits do not apply to applications whose baud rate exceeds 460Kbps.

Pay attention to TX/RX and CTS/RTS connection.

The pull-up resistor of the serial port level conversion circuit of triode or MOS tube is recommended to be 10K.

3.3.3 I2C

Background

The I2C bus is a simple, bidirectional two-wire synchronous serial bus. It only requires a data line and a clock line to transfer information between devices connected to the bus. It is mainly used in the communication between multiple integrated circuits (ICs) in the system.

Schematic Diagram Design

The module I2C interface has been pulled up by software by default, and external hardware pull-up is required to be reserved.

When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address. When some peripherals need to occupy I2C bus frequently, it is not recommended to share it with other devices.

The I2C supports standard mode 100Kbps and fast mode 400Kbps communication rates.

PCB Design

I2C PCB traces and peripherals require protection from interference.

3.3.4 PCM/I2S

The MG661 module enables external codec.

Table 26. PCM/I2S interface description

Pin No.	Pin Name	I/O	Power Domain	Description
30	PCM_CLK	DO	1.8V	PCM clock
31	PCM_SYNC	DO	1.8V	PCM data synchronization signal
32	PCM_DIN	DI	1.8V	PCM data input
33	PCM_DOUT	DO	1.8V	PCM data output
6	I2S_MCLK	DO	1.8V	I2S main clock output signal

Background

The module digital voice interface supports I2S and PCM transmission standards.

Schematic Diagram Design

According to the corresponding connection of the reference design of the codec chip used, the power supply and IO level are required to meet the requirements of the codec chip and match the module.

When the customer uses the external codec and audio power amplifier of the module interface, it is recommended that the control signal such as the enable of the audio power amplifier or I2C is also connected to the module to facilitate the debugging of the timing sequence and solve the audio problems such as pop sound.

It is recommended to use an independent power supply for chip power supply or ensure that the power supply is clean and noiseless.

RC (0Ω/33pF) filtering is recommended for I2S signals.

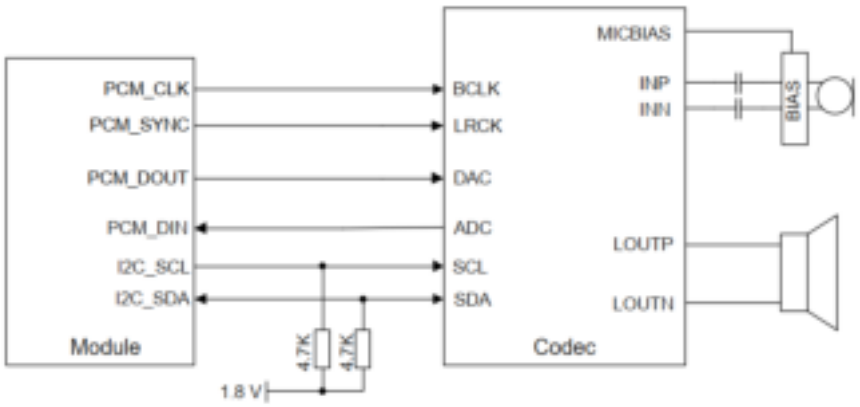


Figure 16. Schematic diagram of LCD reference circuit

PCB Design

The audio is partially protected or divided to ensure that the grounding is clean. Keep away from other interference sources.

Audio signal design requires filtering isolation and packet protection.

I2S_MCLK signal has a high speed, so it must be isolated from other high-frequency or

sensitive signals to avoid interference.

3.3.5 SIM

Background

The module can be connected to the network only after the SIM card is inserted. The module supports 1.8 V and 3 V SIM cards.

Schematic Diagram Design

There are the following scenarios:

- SIM card slot with detection signal: supports detection of SIM card insertion and removal, including normally opened card slot and normally closed card slot. It is used together with the hot plug function. The (U)SIM card with hot plug detection function is recommended.
- SIM card slot without detection signal: does not support detection of SIM card insertion and removal.

Refer to the following design for the normally closed SIM card slot.

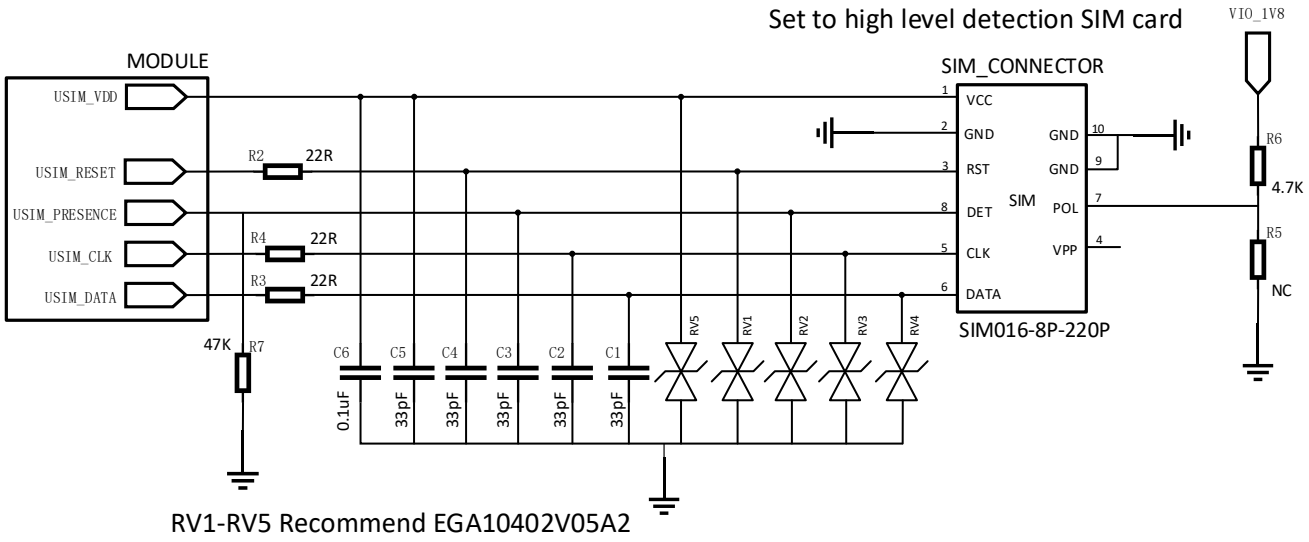


Figure 17. Normally closed SIM card slot

Refer to the following design for the normally opened SIM card slot.

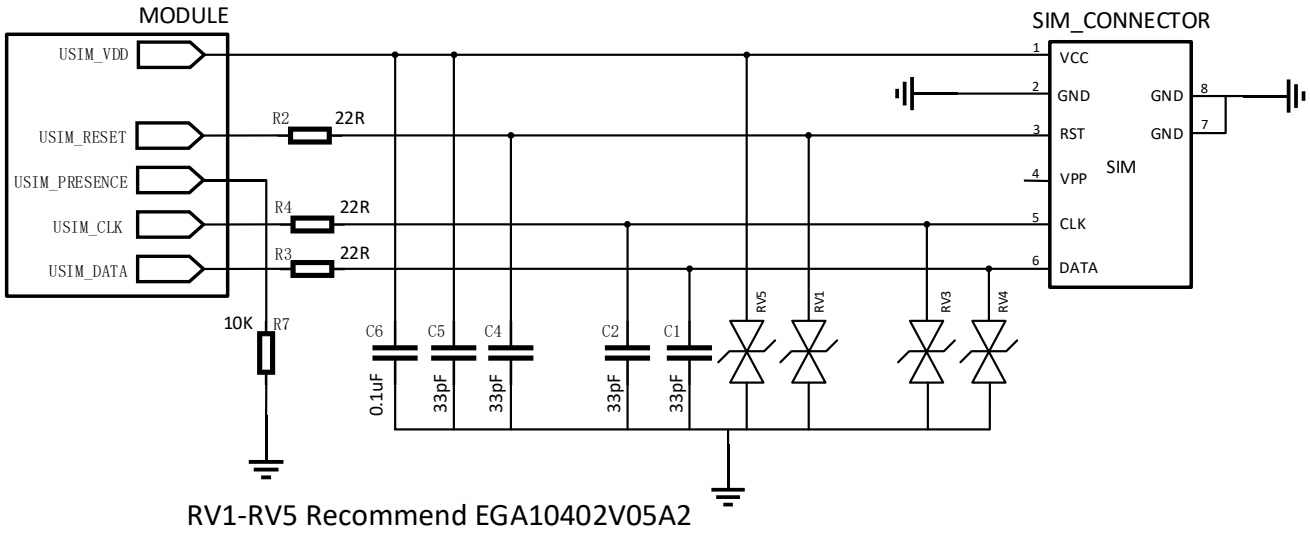


Figure 18. Normally opened SIM card slot

USIM_DATA has internal pull-up inside the module, and external pull-up can be reserved to keep NC. The recommended model for RV1 to RV5 is EGA10402V05A2.

For SIM card slot with no card detection, the USIM_PRESENCE pin of the module is suspended or connected in series with 10K resistor to ground.

The hot plug function is disabled by software default.

PCB Design

Layout key points:

- Reserve capacitor filter for SIM signal line to prevent interference from high frequency signal.
- SIM card and routing should be away from EMI interference source, such as power circuit, RF circuit, antenna, and high-speed digital signal circuit.
- ESD components of SIM card should be close to SIM card slot interface.
- When routing antenna feeder line, please keep the line away from power device, and avoid the line paralleling to antenna copper foil.

- The filter capacitor and ESD device of SIM signal cable are placed close to the SIM card slot. Less than 11pF capacitor is recommended for ESD device.

Routing points:

- To reduce EMC problem, keep SIM signal line away from RF cable, power line, clock line and high-speed data line.
- Do not route the adjacent cables with the SIM signal line; otherwise, the cabling poses an EMI risk. Design the other cables and SIM signal line to be perpendicular with each other to reduce risk.
- Ensure the ground connectivity and integrity of PCB environment and the connectivity and integrity of SIM_GND. The nearest path connects to a clean system ground. To avoid mutual interference, please separately ground SIM_CLK and SIM_DATA. If conditions do not permit, at least the SIM signal must be grounded as a set.
- The SIM signal line should be routed along the inner layer.
- SIM card connector is covered by metal shield shell to improve EMS.
- To ensure the integrity of signal, the cabling length from the module to SIM card should not exceed 100mm. Longer cable will reduce signal quality.
- It is recommended to make a clearance design for the PCB directly under the shrapnel of the SIM card connector to avoid the green oil on the surface of the PCB being worn down when the shrapnel is pressed down, resulting in a short circuit between the SIM card signal line and the ground.

Hot Plug

The MG661 module supports (U)SIM card hot-plug function. The module determines whether (U)SIM card is in place by detecting the status of USIM_PRESENCE pin. (U)SIM card hot-plug function is disabled by default and needs to be enabled before use. When the USIM_PRESENCE is at a high level, the module initializes the (U)SIM card after detecting that the (U)SIM card is inserted, and registers the network after reading the (U)SIM card

information. When the USIM_PRESENCE is at a low level, the module determines that the (U)SIM card is removed and does not read it.

The SIM card hot plug function can be configured by running the AT+MSMPD command. The AT commands are described as follows.

- AT+MSMPD=1, enable hot plug.
- AT+MSMPD=0, disable hot plug.
- AT+SIMPHASE=1, set high level detection.
- AT+SIMPHASE=0, set low level detection.

RF Interference Handling

In practice, RF interference is quite normal. Here are some solutions.

- Antenna coupling interference

Reason:

  - When antenna transmits with high power, it causes direct interference to the SIM signal.
  - When antenna transmits with high power, it is coupled to the ground, reducing the stability of the whole system and causing indirect interference to the SIM signal.

Solutions:

  - Adjust the filter capacitance value the of SIM signal.
  - Use a longer antenna and keep it far away from the SIM card.
  - Shield the interference signal to protect the SIM card.
  - Pay attention to the design of the ground, especially the connectivity of SIM card, module and the system ground.
  - Fully ground each layer of PCB and increase holes to enhance the EMC performance of the system.

- RF coupling will cause interference to GND. Adjust the capacitance values of capacitor and ESD components or even remove the capacitor (if it is necessary) to avoid the interference.

- PCB crosstalk:

Reason:

- Other signal line on the main board has crosstalk with the SIM signal through the PCB routing.
- Antenna interrupted signal has crosstalk with the SIM signal through the PCB routing.
- Fluctuations of power has crosstalk with the SIM signal through the PCB routing.

Solutions:

- Adjust the filter capacitance value the of SIM signal.
- Find out the interference source, and change the board specifically.

3.3.6 ADC

Background

An analog-to-digital converter (ADC) converts analog signals into digital values for use in processing and control systems. It can be used for voltage detection and other external circuits.

Schematic Diagram Design

The module provides two ADC interfaces, send the AT+MMAD=<INDEX> command (INDEX is the ADC channel) can read the voltage value of the channel. The ADC voltage ranges from 0 to VBAT, with 12-bit resolution and sampling accuracy from 20mV to 50mV. When using the ADC function, it is recommended to connect a 1KΩ resistor in serial mode to enhance ESD protection.

PCB Design

It is recommended to ground ADC signal lines to improve ADC voltage measurement accuracy.

3.3.7 Status Indication

Background

Table 27. Status indication pin

Pin No.	Pin Name	I/O	Power Domain	Description
16	NET_STATUS	DO	1.8V	Network status indication
25	STATUS	DO	1.8V	Operating status indication

The PIN16 of the MG661 module is the network status indication signal interface. It is used to drive the status indicator. The following table describes the working status of the module network indicator.

Table 28. Working status of the network status indicator

Mode	Level Status of Network Indicator Pin (PIN16 NET_STATUS)	Description
1	Slow flash (200 ms high/1800 ms low)	No SIM card SIM pin Registering with the network (T < 15s) Failed to register with the network
2	Slow flash (1800 ms high/200 ms low)	Standby
3	Quick flash (120 ms high/120 ms low)	Establishing a data

4	High level	Sleep status

Schematic Diagram Design

The reference circuit of network status indicator is shown in the following figure.

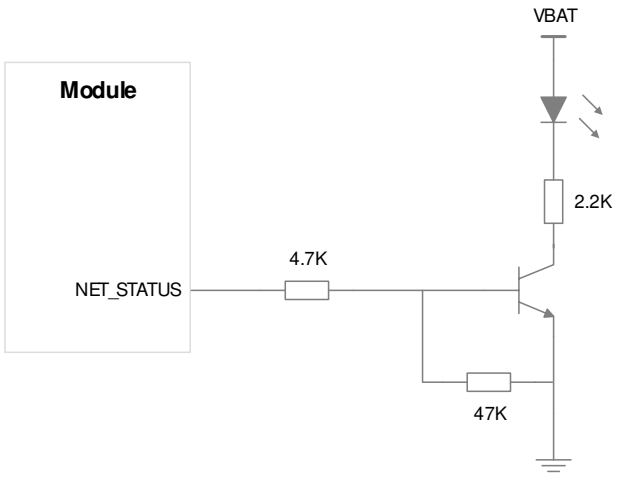


Figure 19. Network status indicator reference circuit

Please reserve the 4.7K and 47K positions for voltage division to ensure that the voltage of the triode V_{BE} is less than the starting voltage of the triode in startup, reset and wake up scenarios, and avoid power consumption increase caused by LED work. When the LED is required to work, the voltage of the V_{BE} is greater than the starting voltage of the triode.

STATUS indicates the operational status of the module. STATUS will output a high level when the module is powered on normally. The definition of the STATUS pin is described in the following table:

Table 29. STATUS operating status

Pin	I/O	Description	Note
STATUS (PIN25)	DO	Operating status indication	1.8V voltage domain Keep unsuspended when not in use

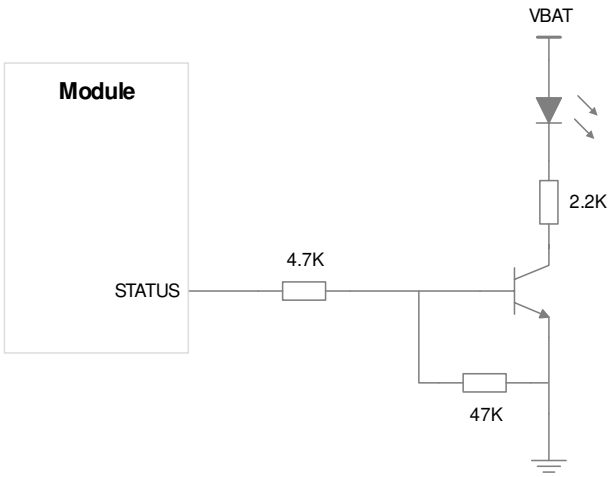


Figure 20. Reference circuit of STATUS operating status

3.3.8 LCD Interface

The MG661 module provides a set of LCD interface. The LCD interface supports a module with the maximum resolution of 240×320 (QVGA) @30fps LCD display and support 3-wire 9bits and 4-wire 8 bits SPI mode data transmission.

Refer to the reference design for the LCD peripheral circuit design.

3.3.9 Camera Interface

The MG661 module provides a set of CAMERA interface. The camera interface supports up to 30 W@15fps pixel sensor and supports 1-bit or 2-bit SPI interface.

See the reference design for the design of CAM peripheral circuits.

3.4 Operating Mode

The module supports the following operating modes.

Table 30. Operating modes

Operating Mode	Description
Standby mode (IDEL)	The module is powered on, and it can be operated using the AT commands through the serial port. The module is registered with the network, there is no service processing in progress, and the module is ready for communication. This is the default operating mode after the module is powered on.
Shutdown mode	The PMU stops supplying power to the baseband and RF sections, the software stops working, and the serial port is disabled. However, the VBAT pin is still energized.
Transmission mode	The module is powered on and successfully registered with the network for service transmission. The module can be operated using the AT commands through the serial port. The module transmits data. When data transmission is completed, the module returns to the standby mode.
Sleep mode	The module is in light sleep state. It is connected to a network and can receive paging messages. In this mode, the module can switch to the standby mode.
Flight Mode	The wireless communication of the module is turned off.

3.4.1 Flight Mode

Background

When it is necessary to turn off the transmission and reception of wireless signals to avoid interference to the surrounding area, the flight mode can be enabled. When the module enters flight mode, the RF function is disabled.

Entering mode

- Hardware control:

Send AT+GTFMODE=1 to enable flight mode control.

When the W_DISABLE# pin is pulled high or suspended, the module is in the normal mode; when the pin is pulled low, the module enters the flight mode.

- Software control:

Run the AT+CFUN=4 command to enter flight mode.

Exiting mode

- Hardware control

Pull the pin high, and the module is in normal mode.

- Software control:

Run the AT+CFUN=1 command to exit flight mode.

Entering or exiting flight mode can be realized by using GPIO pins of modules and software settings, and customers can determine whether they need it according to the actual situation.

3.4.2 Sleep Mode

Background

The sleep mode is also called the low-power mode. To minimize battery loss, the module can be set to enter the sleep mode when it is idle to save power. The module in sleep mode can be awakened to the normal operating mode.

Entering mode

AT commands or WAKEUP_IN signal are used to set the module into sleep mode and wake-up mode.

- Hardware control

Send AT+GTLPMMODE=1, x to set the effective level of the WAKEUP_IN signal that sets the module into sleep or wake-up mode. The setting is effective after sending the AT+csclk=1

command.

x=0: Wake up the module by level. The module enters wake-up mode when WAKEUP_IN is pulled down and enters sleep mode at high level.

x=1: Wake up the module by level. The module enters wake-up mode when WAKEUP_IN is pulled up and enters sleep mode at low level.

- Software control:

Run ATS24 to make the module to enter sleep. The wakeup hold time is subject to the </value> in the ATS24 = [<value>] command. Send the ats24=2 command. The module enters sleep mode after 2s. The setting is not saved after the module power supply is disconnected.

Send AT command through the main serial port to wake up the module.

The hardware control module enters sleep or wake up mode through GPIO and software configuration. By default, it is implemented on WAKEUP_IN pin. Without WAKEUP_IN pin, DTR can also implement module sleep wakeup function. The OPEN version is optional for any GPIO implementation.

3.4.3 PSM Mode

PSM is a power saving mode. Characteristics of terminal during non-service period in this mode:

1. Deep sleep, not receiving downlink data;
2. Only when the terminal actively sends the uplink data, the downlink data cached by the IOT platform can be received.

The PSM feature needs to be configured on the network. After the module enters PSM mode, the power consumption can be reduced to 3μA.

To enter PSM, run the AT command AT+CPSMS=1. For details, see *Flibocom_MC66x_Application Guide_PSM*.

Exiting the PSM mode:

1. Wake up through the PSM_EXT_INT pin, and active at high level.

2. Wake up by a PWRKEY button.

3. Wake up by TAU.

"*" indicates that the PSM function of the MG661 module is being debugged.

PSM_EXT_INT is a PSM wake-up pin. The PSM_EXT_INT pin is not defined in MG661 separately. If PSM pin wake-up function is required, PSM_EXT_INT can be implemented on GPIO0-7 pin, such as DTR (PIN19) pin.

4 RF Interface

4.1 RF Indicators

Table 31. RF indicators

Indicator		Description
LTE system	Operating band	LTE FDD: B1/2/3/4/5/7/8/20/28/66
	Modulation	Uplink: QPSK/16QAM Downlink: QPSK/16QAM/64QAM
	Transmitting power	23±2dBm
	Peak rate	LTE FDD: 10.296Mbps DL/5.160Mbps UL (Cat 1)

Table 32. Transmitting power of each band

System	Band	Tx Power (dBm)	Description
LTE FDD	Band 1	23±2	10MHz Bandwidth, 1 RB
	Band 2	23±2	10MHz Bandwidth, 1 RB
	Band 3	23±2	10MHz Bandwidth, 1 RB
	Band 4	23±2	10MHz Bandwidth, 1 RB
	Band 5	23±2	10MHz Bandwidth, 1 RB
	Band 7	23±2	10MHz Bandwidth, 1 RB
	Band 8	23±2	10MHz Bandwidth, 1 RB
	Band 20	23±2	10MHz Bandwidth, 1 RB
	Band 28	23±2	10MHz Bandwidth, 1 RB
	Band 66	23±2	10MHz Bandwidth, 1 RB

Table 33. Receiving sensitivity at each band

System	Band	Sensitivity (dBm)	Description
LTE FDD	Band 1	-98.0	10MHz Bandwidth
	Band 2	-98.0	10MHz Bandwidth
	Band 3	-98.0	10MHz Bandwidth
	Band 4	-97.5	10MHz Bandwidth
	Band 5	-98.0	10MHz Bandwidth
	Band 7	-97.0	10MHz Bandwidth
	Band 8	-98.0	10MHz Bandwidth
	Band 20	-98.0	10MHz Bandwidth
	Band 28	-98.0	10MHz Bandwidth
	Band 66	-97.5	10MHz Bandwidth

Table 34. Power consumption

Parameter	Mode	Condition	Average Current (mA)
I_{off}	Static leakage	Power on but not boot	0.015
	Hardware power-off	The module is powered on, and then powered off by the power off button	0.005
	Software shutdown	The module is powered on, and then powered off by AT command	0.005
I_{sleep}	Airplane	AT+CFUN=4	1.0
	LTE FDD	Paging cycle #64 frames (remove USB)	1.9
	LTE FDD	Paging cycle #64 frames (USB suspend)	2.7

Parameter	Mode	Condition	Average Current (mA)
I_{IDLE}	LTE FDD	Paging cycle #128 frames (remove USB)	1.5
	LTE FDD	Paging cycle #128 frames (USB suspend)	2.2
	LTE FDD	Paging cycle #256 frames (remove USB)	1.2
	LTE FDD	Paging cycle #256 frames (USB suspend)	1.9
	LTE FDD	Paging cycle #64 frames (USB in place)	25
	LTE FDD	Paging cycle #64 frames (remove USB)	11
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data transfer Band 1 @+23.5dBm	660
	LTE FDD	LTE FDD Data transfer Band 2 @+23.5dBm	660
	LTE FDD	LTE FDD Data transfer Band 3 @+23.5dBm	630
	LTE FDD	LTE FDD Data transfer Band 4 @+23.5dBm	630
	LTE FDD	LTE FDD Data transfer Band 5 @+23.5dBm	600
	LTE FDD	LTE FDD Data transfer Band 7 @+23.5dBm	650
	LTE FDD	LTE FDD Data transfer Band 8 @+23.5dBm	600
	LTE FDD	LTE FDD Data transfer Band 20 @+23dBm	550
	LTE FDD	LTE FDD Data transfer Band 28 @+23dBm	620
	LTE FDD	LTE FDD Data transfer Band 66 @+23dBm	630

The above power consumption data is the measured average value, and the floating range within 10% is normal.

4.2 RF Antenna

4.2.1 Antenna Introduction

Antenna interface

The module only has RF antenna pad. The RF cable can be connected to the antenna after PCB design of the RF signal line.

Antenna classification

According to the transmitting and receiving functions, it mainly includes:

- Main antenna: The antenna is divided into built-in and external antenna, which is responsible for RF signal transmission and reception.

The antenna is a sensitive device and is easily affected by the external environment. For example, the position of the antenna, the occupied space, and the surrounding grounding may affect the performance of the antenna. In addition, the RF cable connected to the antenna and the fixed antenna position will also affect the antenna performance.

A shield or module antenna is placed away from the DCDC device on the customer mainboard to prevent RF signals from interfering with the DCDC device, resulting in out-of-specification ripple output.

4.2.2 Impedance Design Principles

For modules that do not have a RF connector, you need to route a RF cable to connect to the antenna feeding point or connector. It is recommended to use a microstrip line. The shorter the better. The insertion loss should be controlled less than 0.2 dB, and impedance should be controlled within 50Ω.

In general, the impedance of the RF signal route is determined by the dielectric constant of the material, the route width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually is

implemented in two ways: microstrip route and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide when the impedance line is at 50Ω.

- Microstrip cable complete structure

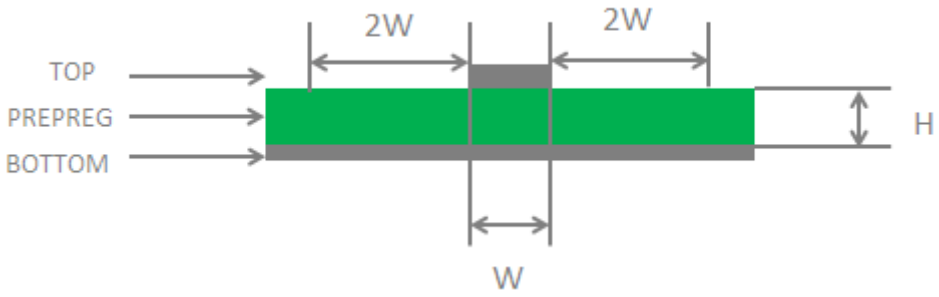


Figure 21. Two-layer PCB microstrip line structure

- Coplanar waveguide complete structure

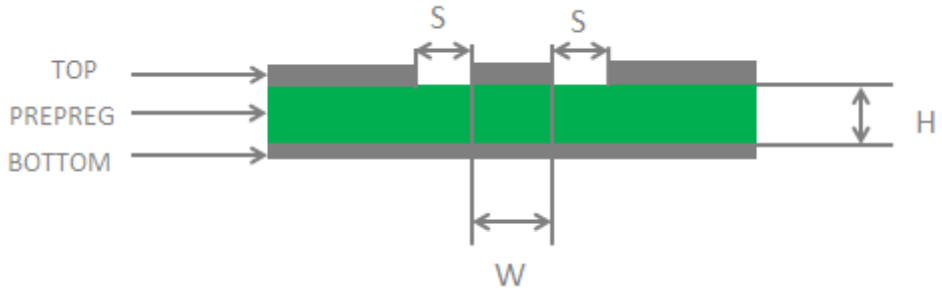


Figure 22. Two-layer PCB coplanar waveguide structure

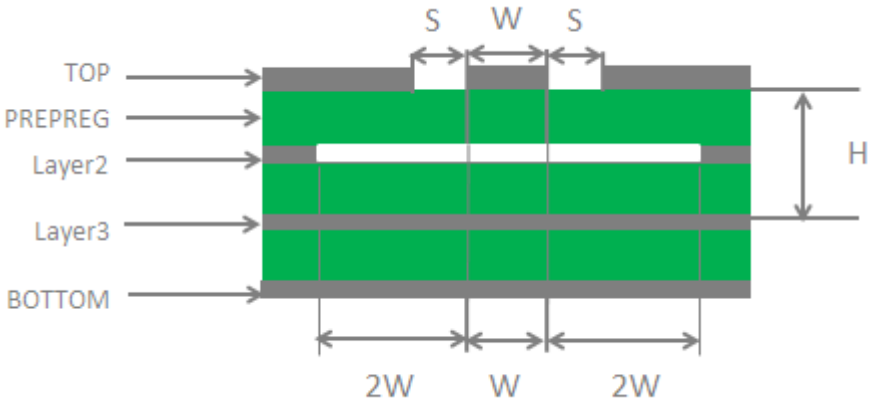


Figure 23. Four-layer PCB coplanar waveguide structure (see ground layer 3)

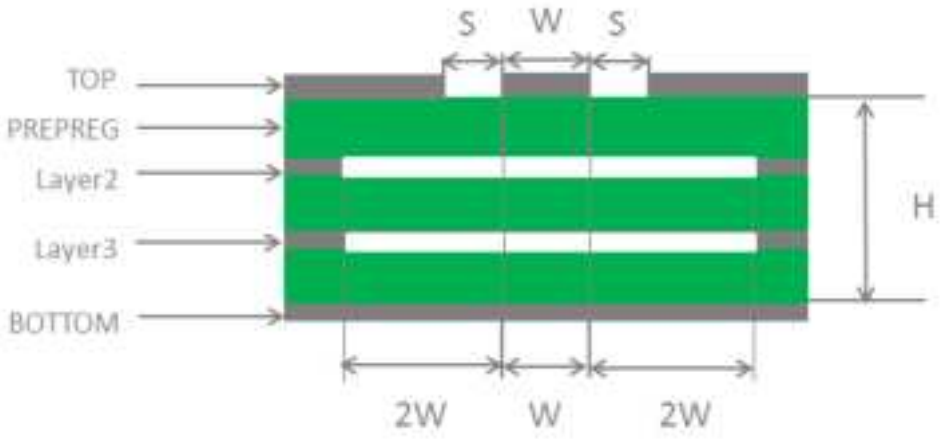


Figure 24. Four-layer PCB coplanar waveguide structure (see ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135°.
- Attention should be paid to the establishment of the connection component package and

the signal pin should be kept at a certain distance from the ground.

- The reference ground plane of the RF signal cable should be kept intact; adding a certain amount of ground holes around the signal and the reference ground can improve the RF performance; the distance between the ground hole and the signal cable should be at least 2 times the cable width (2*W).
- The equivalent capacitance of the TVS should be less than 0.5 pF.

Add a π-type circuit (two parallel component grounding pins are connected directly to the main GND) between the module and antenna connector (or feeding point) for antenna debugging. Two parallel components are directly connected across the RF cable, and the branch must not be pulled out.

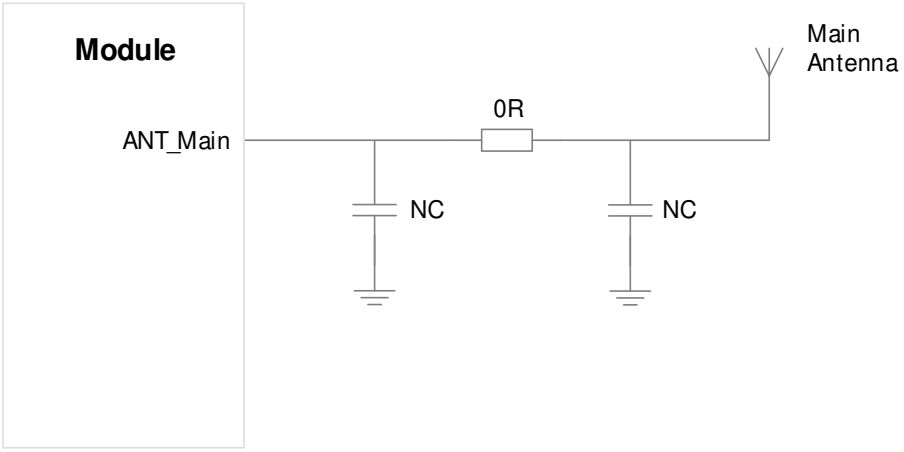


Figure 25. Antenna interface peripheral circuit

4.2.3 Antenna Passive Test

You will need: network analyzer and anechoic chamber.

The passive test evaluates the radiation performance of the device by focusing on the radiation parameters like gain, efficiency and antenna pattern. Although the test considers the environment (such as the device around the antenna, open and close lid) impact on the antenna performance, it cannot tell the final radiated transmitting power and receiving

sensitivity.

Figure 26. Network analyzer and anechoic chamber

You will need: Universal radio communication tester, spectrum analyzer and anechoic chamber.

Test items: TRP, TIS and directionality.

Antenna system is determined by the whole device, and the antenna is just an important part of the whole device. The antenna performance of the whole device must be concluded by the active test results.

The active test evaluates the radiation performance of the device by focusing on the transmitting power and receiving sensitivity. The test measures the transmitting power and receiving sensitivity of the device in all directions in 3D space in specific anechoic chamber, which can directly reflect the radiation performance of the whole device.

TRP

TRP (Total Radiated Power): the average value of the transmitting power of the entire radiation sphere. It reflects the transmitting power of the whole device, and it is related to the transmitting power and antenna radiation performance of the device in conductive state.

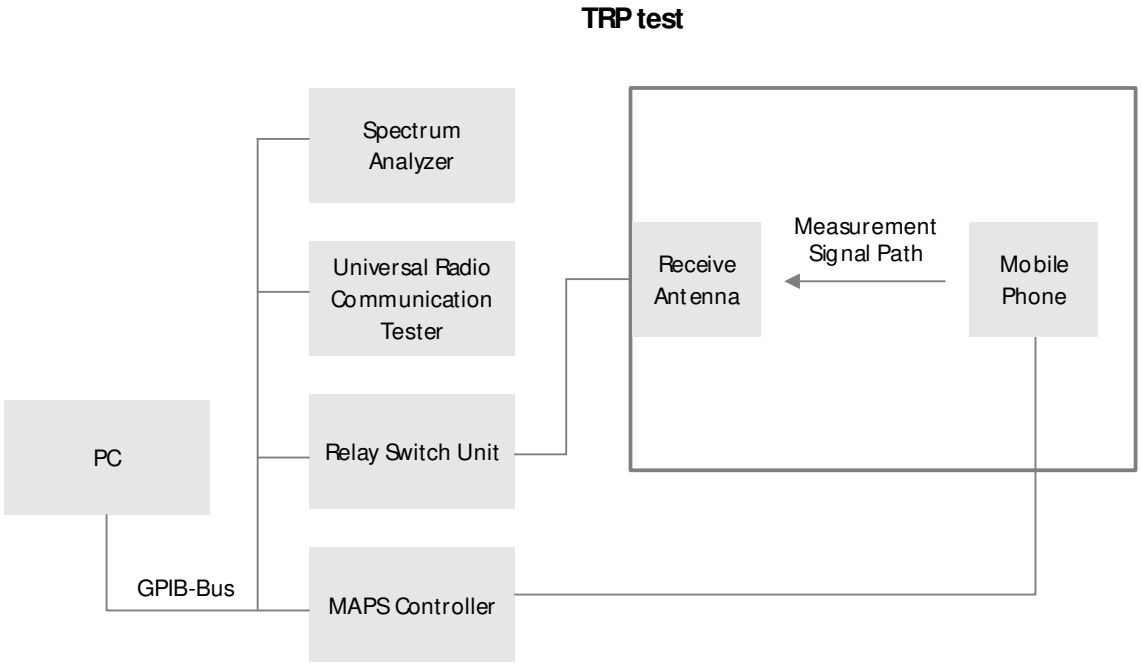


Figure 27. TRP test

TIS

TIS (Total Isotropic Sensitivity): reflects the receiving sensitivity of the entire radiation sphere. It reflects the reception of the whole device; it is related to the conductive sensitivity and radiation performance of the antenna.

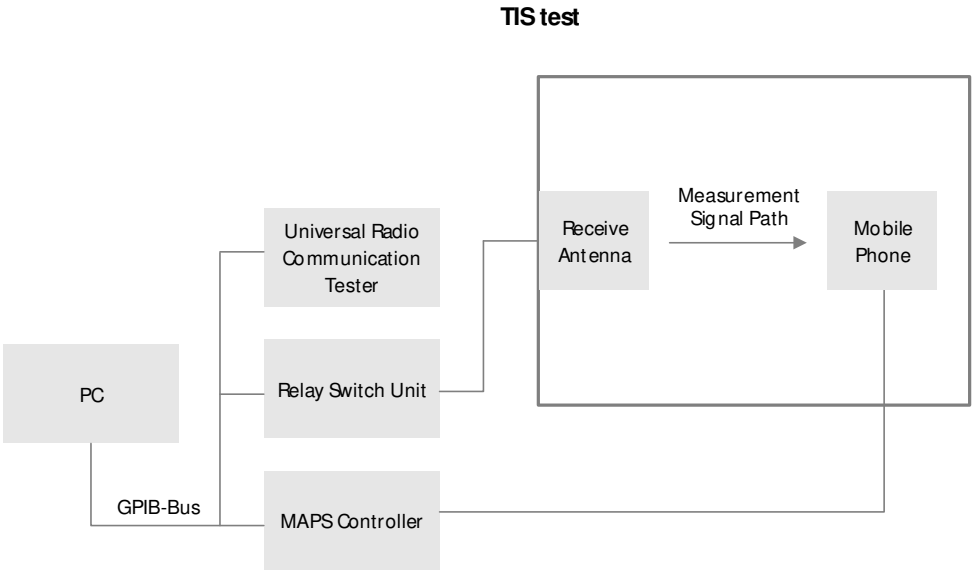


Figure 28. TIS test

5 Reliability

5.1 Temperature and Humidity Requirements

Table 35. Environment indicators

Indicator		Description
Temperature and Humidity Indicator	Operating temperature: –30℃ to +75℃	The module works normally within this temperature range, and the related performance meets the requirements of 3GPP standards.
	Extended temperature: -40℃ to +85℃	The module works normally within this temperature range, and the baseband RF function is normal. Some RF indicators may exceed the 3GPP standard. When the temperature returns to the normal working range of the module, all indicators will still meet the 3GPP standard.
	Storage temperature: -45℃ to +90℃	The module application terminal should be stored at a certain temperature. Beyond this range, the module may not work properly or be damaged.
	Humidity range: 0–95%RH	The module works normally within this humidity range, and the related performance meets the requirements of 3GPP standards.

In the extended operating temperature range, some RF indexes may exceed the standard. It is suggested that the temperature control measures should be considered in the application end under the harsh environment.

5.2 Reliability Indicators

The reliability test is conducted according to the industrial reliability test. The following are

the standard test items and test conditions.

Table 36. Industrial reliability test

Test Item	Test Condition
High temperature aging	85℃, 168H/504H/1008H
High temperature and humidity	85℃ , 85%RH, 168H/504H/1008H
Corner test	High and low temperature, high and low humidity, high and low voltage, six groups of combinations, and each combination runs for 24 hours
Temperature shock	90/-45℃, 200C
Random vibration	Frequency range: (200 to 2000)Hz, PSD = 0.04 g2/Hz, X/Y/Z axis for 1 hour
Monomer drop	1m, 6 sides and 2 wheels
Mechanical collision	Peak acceleration: 180m/s2 Pulse duration: 6ms Number of collisions: 1000
Low temperature boot	-40℃; 30 minutes Off/5 minutes Idle; 3 days
Condensation Test	3 days (3 cycles): • First and second cycle with cold cycle • Third cycle without cold cycle
Temperature cycle	85°C/-40°C; 10°C/min; 10min; 240 cycles
Sinusoidal vibration	Amplitude: 3.0G peak to peak; Frequency: 5 - 500Hz;

Test Item	Test Condition
	Sweep frequency: 0.5 Octave/min, linear; Each axis: 2H;
Salt spray	Neutral salt spray, 48H

5.3 ESD Indicators

The module is ESD sensitive component, and the ability to resist static electricity is weak. So ESD precautions that apply to ESD sensitive components should be strictly followed. Proper ESD procedures must be applied throughout the processing, delivery, assembly and operation.

The ESD allowable discharge range of the module is as follows (temperature: 25°C, relative humidity: 40 %):

Table 37. ESD indicators

Test Point	Air Discharge (kV)	Contact Discharge (kV)
Antenna ground	±15KV	±8
Antenna core	- -	±8

The data is tested based on the MG661 development board.

6 Thermal Design

6.1 Overview

The design guidelines provided in this document are general guidelines. There may be unavoidable differences between different products. When designing a specific interface circuit, please pay attention to the specific characteristics of the hardware and software of the module.

Before designing the hardware:

Refer to the Pin Definition section for details on the attributes of each pin in the module.

Prepare SCH component library and PCB package library.

6.2 Thermal Basis

Conductive heat dissipation

Conductive heat dissipation refers to the transfer of energy through kinetic energy between molecules of objects when they contact.

Heat sink/shell with larger surface area dissipates heat better.

The smaller distance between the cooling system and heat source is preferred.

Materials with high thermal conductivity are preferred, generally: solid > liquid > gas.

Thermal resistance

During two solid surfaces contact, the actual contact is only the area of some discrete parts due to limit of the material processing procedure. The gap between the non-contact surfaces is filled with air, and generates a large thermal resistance.

Methods of reducing the thermal resistance include increasing contact pressure and increasing materials (thermal conductive silicone) to fill the gap between the surfaces.

Thermal convection

Convective heat dissipation is an energy exchange in which a fluid flows over a solid surface. Heat sink/shell with larger surface area dissipates heat better.

6.3 Thermal Design

6.3.1 Main Board

Recommendations for main board design:

Increase PCB size, and keep the module away from other heat source devices.

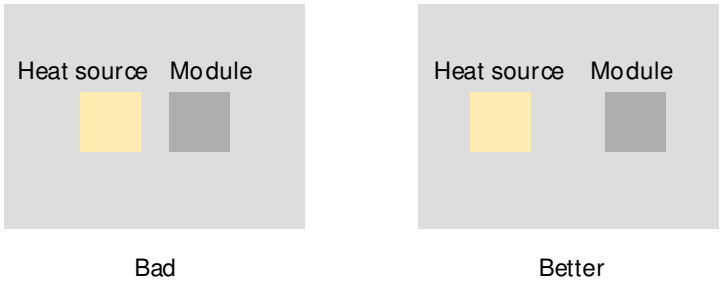


Figure 29.PCB layout

Increase PCB layers and the copper area at each layer.

Add adequate paths under and near the module. Plated holes boast better cooling effect than buried holes and blind holes. Vertically stacked paths boast better cooling effect than staggered paths.

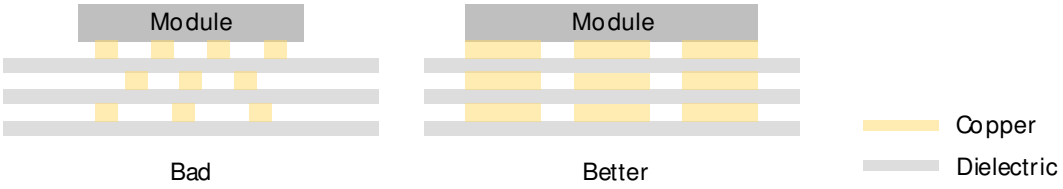


Figure 30. PCB stack

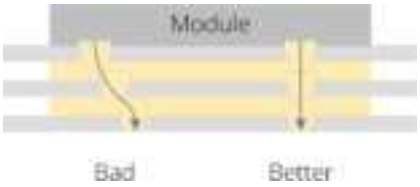


Figure 31. PCB hole comparison

6.3.2 Product Structure

Recommendations for structure design:

Reduce the distance between module and heat sink and shell. Thermal conductive material thickness should not exceed 3 mm.

The thermal conduction path is shown in the following figure.

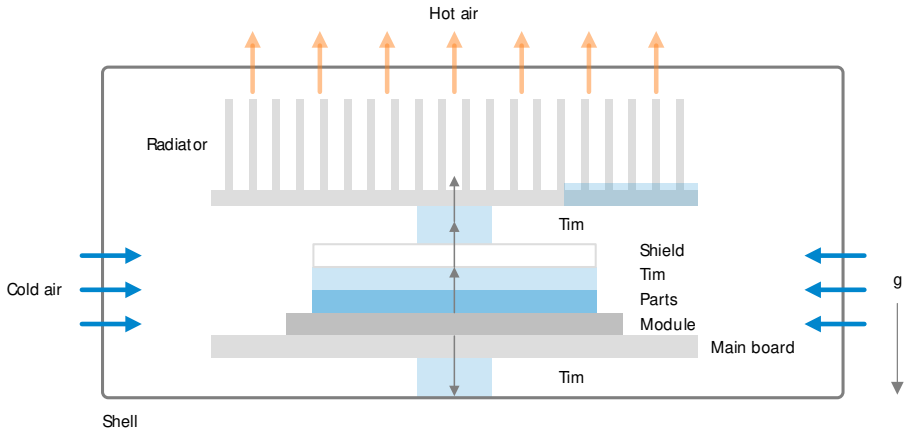


Figure 32. Thermal conduction path

Use shell material with better thermal conductivity to facilitate cooling. Thermal conductivity sequence: Al > Fe > Plastic.

Place the heat sink above the module.

Allow direct contact between the heat sink and thermal conductive material on the module if the heat sink can be exposed to the product surface.

Consider convection if the product has cooling holes.

7 Structure Specifications

7.1 Appearance

The schematic diagram of MG661 module is as follows:

Figure 33. TOP schematic diagram

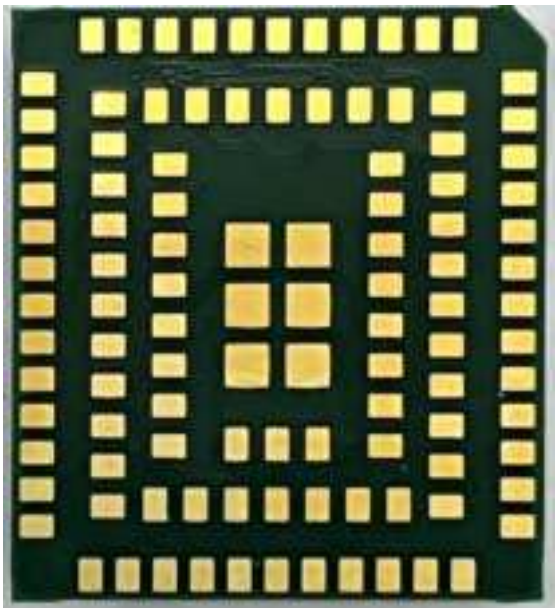


Figure 34. Bottom schematic diagram

7.2 Dimensions

Table 38. Packaging mode

Indicator	Description
Weight	1.2g
Package	LGA, with 109 pins in total
Appearance dimensions	(17.7±0.15) mm × (15.8±0.15) mm × (2.4±0.2) mm
Structure dimensions	See the following figure.

The following figure shows the structural dimensions.

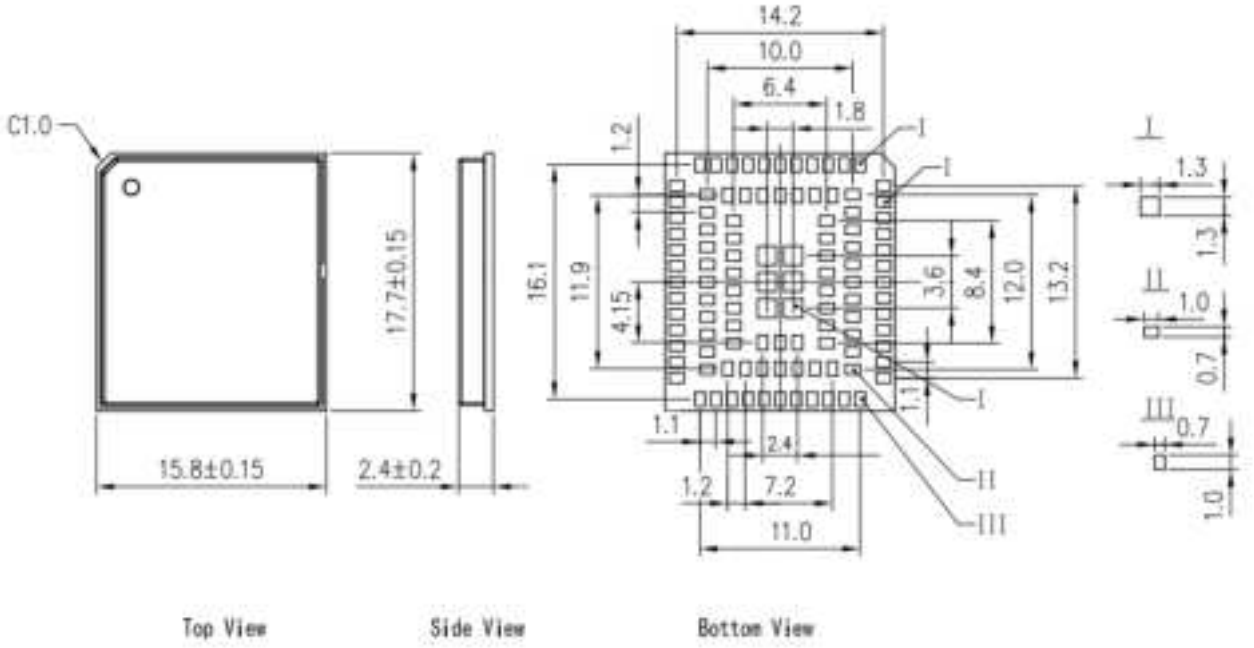


Figure 35. Structural dimensions (top view/side view/bottom view)

8 Packaging and Production

8.1 Packaging

The module adopts tape packaging, and the storage, transportation and the usage of module can be protected to the greatest extent. Please read the instructions carefully to avoid damaging the product.

The product packaging is divided into three layers:

- Outer packaging

Hard cartoon box

- Vacuum packaging

Anti-static sealed vacuum bag

- Inner packaging

Tape packaging

The module is a precise electronic product, and may be permanently damaged if you do not take correct ESD measures.

The module is moisture sensitive, please avoid moistening the product to prevent permanent damage.

Each roll is packed with 500 pcs, each box is packed with one roll, and each hard carton box is packed with 4 boxes.

Packaging process

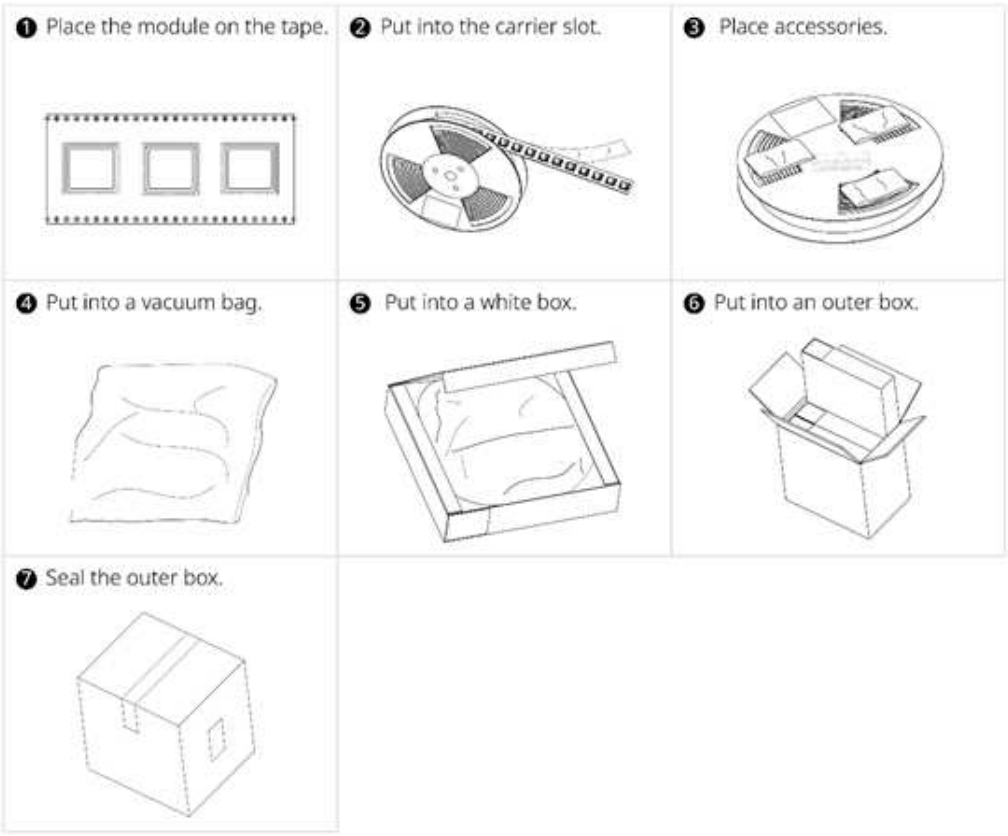


Figure 36. Tape packaging process

Description:

1. Place a module into the carrier tape slot in sequence according to the specified direction, and seal the heat sealing film.

2. Place the specified number of module tapes, as shown in the following figure.

3. Before vacuumizing, place 3 bags of drying agent and a humidity card above the tape, and paste the carrier tape label.

4. Put the whole into a vacuum bag and vacuumizing.

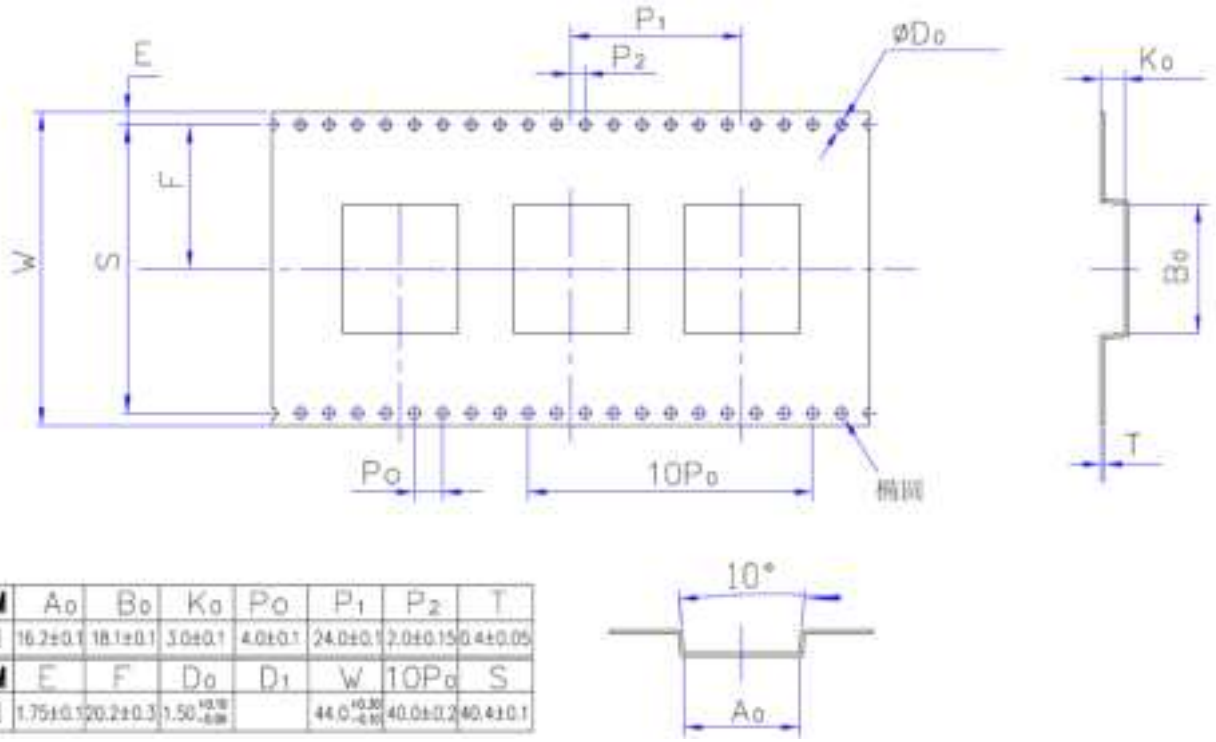
5. The vacuum electrostatic bag is put into a tape white box, and only one electrostatic bag is put into a single white box. Buckle the white box and paste a label.

6. Seal the bottom of the outer box, and put the 4 pcs white boxes into the outer box as shown in the figure.

7. Seal the top of the outer box in an I-shape, paste an outer box label in the rectangular frame on the side, and paste a box sealing label on the top and bottom parts of the outer box respectively.

Tape dimensions

- Tape dimensions:



ITEM	A0	B0	K0	P0	P1	P2	T
DIM	16.2±0.1	18.1±0.1	3.0±0.1	4.0±0.1	24.0±0.1	2.0±0.15	0.4±0.05
ITEM	E	F	D0	D1	W	10P0	S
DIM	1.75±0.1	20.2±0.3	1.50		44.0	40.0±0.2	40.4±0.1

Figure 37. Carrier tape dimensions

- Reel dimensions:

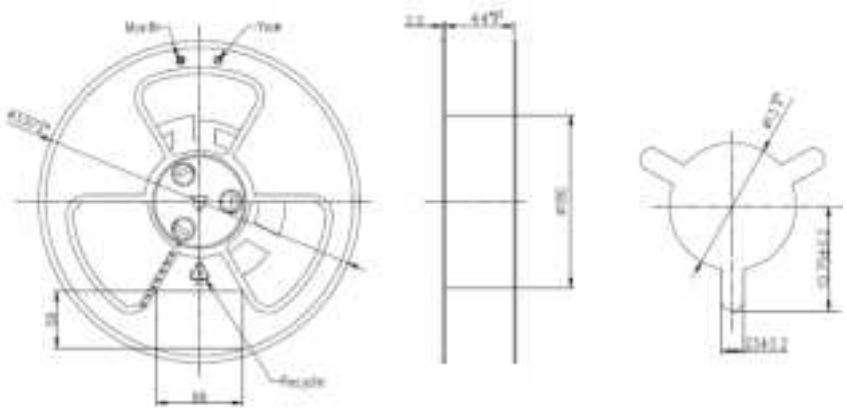


Figure 38. Reel dimensions

8.2 Storage

Storage conditions (recommended): temperature is 23±5°C; relative humidity is 35–70%.

Storage period (sealed vacuum packaging): 12 months under the recommended storage conditions.

8.3 SMT

For module stencils design, solder paste and oven temperature control, see *Fibocom_MG661_SMT Application Design*.

Appendix A Acronyms and Abbreviations

Acronym and Abbreviation	Description
ADC	Analog to Digital Converter
ADP	Application Development Platform
BT	Bluetooth
CPE	Customer Premises Equipment
DCDC	Direct Current to Direct Current
DDR	Double Data Rate
EDGE	Enhanced Data rate for GSM Evolution
ESD	Electronic Static Discharge
FDD	Frequency Division Duplexing
FEM	Front End Module
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
LDO	Low Dropout Regulator
LTE	Long Term Evolution
I2C	Inter Integrated Circuit
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PMU	Power Manager Unit
RF	Radio Frequency
RTC	Real Time Clock

RMII	Reduced Media Independent Interface
SDIO	Secure Digital Input and Output
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Appendix B Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

Appendix C Reference Documents

This product is designed by referring to the following documents:

- Fibocom_Design Guide_RF Antenna
- Fibocom_MC981_ADP_User Guide
- Fibocom_MC66x/MG66x_AT Commands User Manual
- Fibocom_MG661_SMT Application Design

FCC Conformance information

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the

instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a

window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID:ZMOMG661LA”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This

equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 15B requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter

rules) listed on the grant, and that the host product manufacturer is responsible for compliance to

any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also

contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that

the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the

OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Requirement per KDB996369 D03

2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.3

Explanation: This module meets the requirements of part 22, part 24, part 27

2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

Explanation: The EUT has a Rubber Duck Antenna, and the antenna use a replaceable antenna

2.4 Limited module procedures

If a modular transmitter is approved as a “limited module,” then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval.

This limited module procedure is also applicable for RF exposure evaluation when it is necessary to

demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

Explanation: The module is not a limited module.

2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects:

layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s),

dielectric constant, and impedance as applicable for each type of antenna);

b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency,

the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);

c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;

d) Appropriate parts by manufacturer and specifications;

e) Test procedures for design verification; and

f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

Explanation: Yes, The module with trace antenna designs, and This manual has been shown the layout

of trace design, antenna, connectors, and isolation requirements.

2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person's body); and (2) additional text

needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: ZMOMG661LA

2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, antenna gain etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)).

For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

Explanation: The EUT has a Rubber Duck Antenna, and allow maximum antenna gain as below:

LTE band 2	1.93 dBi
LTE band 4	2.86 dBi
LTE band 5	1.32 dBi
LTE band 7	1.07 dBi
LTE band 66	3.53 dBi

2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

Explanation: The host system using this module, should have label in a visible area indicated the

following texts: “Contains FCC ID: ZMOMG661LA”

2.9 Information on test modes and additional testing requirements5

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host.

Grantees can increase the utility of their modular transmitters by providing special means, modes, or

instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer’s determination that a module as installed in a host complies with FCC requirements.

Explanation: Top band can increase the utility of our modular transmitters by providing instructions

that simulates or characterizes a connection by enabling a transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer

The grantee should include a statement that the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Explanation: The module has evaluated by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.