3. THEORY OF OPERATION

3.1 PLL Block

Refer to Figure 3-1.

The Phase-Locked Loop (PLL) is comprised of a VCO circuit (QV02, QV03, QV04, QV05, and QV07), reference oscillator XP01, PLL IC QP01 and PLL loop filter. Oscillation from the VCO circuit is output from the collector of buffer amplifier QP07.

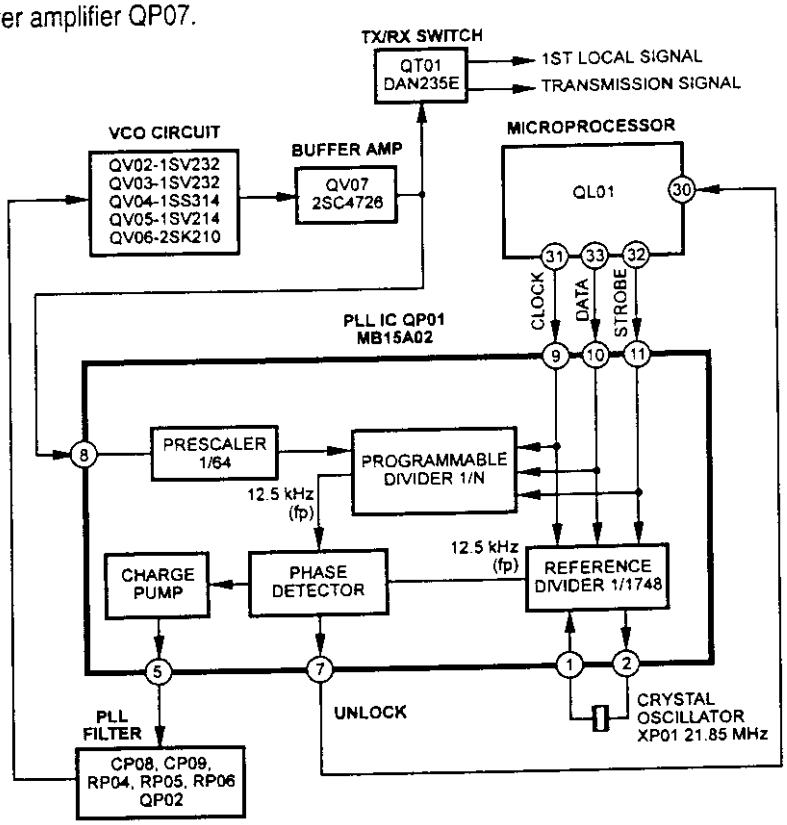

Figure 3-1

3.1.1 Programmable Divider

The microprocessor QL01 determines a divide-by number (N) which is sent to pins 9, 10 and 11 of PLL IC QP01. Inside QP01, the programmable divider divides the VCO frequency by the N number after being supplied to the divide-by-64 prescaler to produce a 12.5 kHz signal. Changing the operating frequency will cause the N number from microprocessor QL01 and the frequency from the prescaler to the programmable divider to change so that the programmable divider is consistently providing a 12.5 kHz signal to the phase detector inside QP01.

3.1.2 Phase Detector

The phase detector compares the phase relationship between the frequency from the programmable divider (fp) and the reference frequency (fr). Based on this phase difference, square wave signals are output from pin 5 of PLL IC QP01 and applied to the PLL filter.

3.1.3 Reference Divider

The 21.850 MHz frequency produced by the crystal oscillator XP01 passes through pin 1 of PLL IC QP01 and is applied to the reference divider inside QP01. The reference frequency (12.5 kHz) is produced by dividing the reference oscillator frequency by 1748. It is then applied to the phase detector in QP01.

3.1.4 PLL Filter

The PLL filter is compose a lag-lead filter and a lag-filter. The PLL filter converts the square wave signal output from pin 5 of QP01 to a DC voltage. This voltage is applied to varactors QV02 and QV03 in the VCO circuit.

3.1.5 Voltage-Controlled Oscillator (VCO)

The VCO circuit is comprised of QV02, QV03, QV04, QV05, and QV07. QV02 and QV03 are varactor diodes which change capacitance with different bias levels applied (determined by the error voltage from the PLL filter). The change in capacitance causes QV06 to change oscillation frequency. QV04 switches the VCO output between the first local signal during receive (LO = RX frequency -21.4 MHz) and the transmission frequency during transmit. QV05 in conjunction with CV05, LV02, and CV03 controls the deviation during transmit. QV07 is used as the output for the VCO circuit. During receive, pin 16 of microprocessor QL01 outputs a high voltage (5 V) which turns on RX switch QV08. When turned on, the 5V regulator circuit which is comprised of QM01 and QM02, supplies 5 V to the RX/TX switch circuit which is comprised of QV04, QV01 and QV08, allowing the first LO signal from buffer amplifier QV07 to be applied to first mixer QR02. During transmit, pin 15 of microprocessor QL01 outputs a low voltage (0 V) which turns on RX/TX switch QM03(2/2). When turned on, QM03(1/2) supplies 5 V to RX/TX switch QT01. The diode inside QT01, that is biased during receive, no longer has voltage applied to it and therefore is no longer active. The other diode inside QT01, which is now receiving 5V from QM03(2/2), is conducting. This allows the signal from buffer amplifier QV07 to be applied to the transmitter circuit for amplification. Also during transmit, audio from the microphone is supplied to microphone amplifier/low pass filter QA07, applied to potentiometer RA29 for deviation adjustment, then to varactor QV05 where the signal is frequency modulated. The modulated signal is applied to QV06 then output from buffer amplifier QV07.

3.1.6 Unlock Detector Circuit

The PLL circuit is locked or unlocked (operational/not operational) depending on the output of pin 7 of PLL IC QP01. When there is no phase difference between the reference and programmable frequencies in the phase detector of PLL IC QP01, the PLL is locked and a 5 V level is output from pin 7 of QP01. This voltage is applied to pin 30 of microprocessor PL01, which will stop supplying the N number to PLL IC QP01. When there is a phase difference between the reference and programmable frequencies in QP01, the PLL is unlocked and 0 V is output from pin 7 of PLL IC QP01. Then this low voltage is applied to pin 30 of microprocessor QL01 which will supply the N number to PLL IC QP01.

3.1.7 Weather Alert

Refer to Figure 3-2.

QA01 is a tone and frequency decoder. In order for QB01 to operate a weather channel needs to be present in the scan memory. This causes a low voltage (0 V) to be output from pin 18 of microprocessor QL01 (WA CONT). This voltage is applied to WA switch QB02 which turns it on and applies +5V to pin 4 of WA decode IC QB01. When the proper frequency (1050 Hz) is detected by WA decode IC QB01, a low voltage (0 V) is output from pin 8, and is then applied to pin 13 of microprocessor QL01. Microprocessor QL01 also outputs a low voltage from pin 27 (BEEP) which is applied to AF amplifier QA05. This causes a beep tone to be emitted from internal speaker EA01.

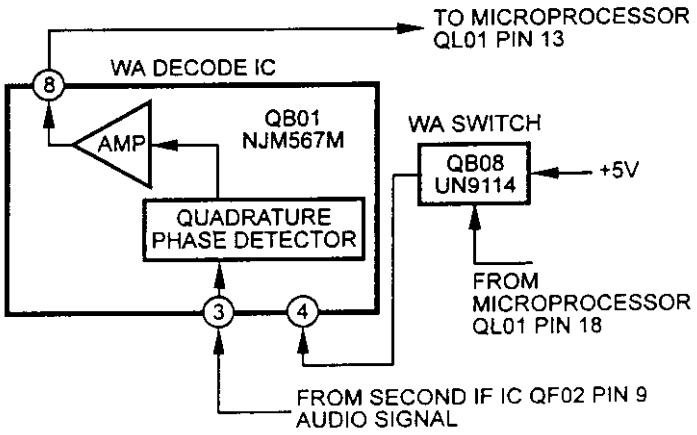

Figure 3-2

3.2 Receiver Block

Refer to Figure 3-3.

The receiver is a double-conversion super-heterodyne with a first intermediate frequency (IF) of 21.4 MHz and a second IF frequency of 450 kHz. The receiver consists of RF amplifier QR01, first mixer QR02, first IF amplifier QF01, second IF IC QF02, and AF power amplifier QA05

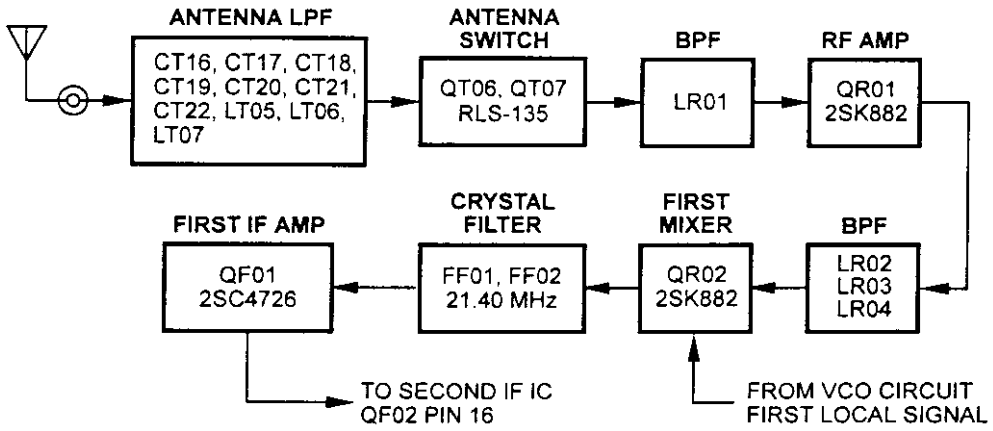

Figure 3-3

3.2.1 RF Amplifier Circuit

The incoming signal through the antenna socket JT01 passes through the low pass filter consisting of CT20, CT19, CT21, LT07, CT18, CT22, LT06, CT17, LT05, and CT16. It then passes through antenna switch QT07 and is applied to the band pass filter LR01. The signal from LR01 is applied to RF amplifier QR01 where it is amplified then applied to the first mixer QR02. The front end test point may be used to balance the band pass filters or used to check the RF amplifier and associated circuitry.

3.2.2 First Mixer Circuit

The first local signal is applied to the gate of first mixer QR02. The receive frequency and the first local signal are mixed in QR02 and produce four frequencies: the sum, the difference, receive, and first LO (the first LO is equal to the RX frequency minus 21.4 MHz.) These signals are applied to the crystal filter, comprised of FF01 and FF02, where the 21.4 MHz signal is filtered. The first IF signal of 21.4 MHz is then applied to first IF amplifier QF01.

3.2.3 First IF Amplifier Circuit

The 21.4 MHz first IF signal is amplified by QF01 and then applied to pin 16 of second IF IC QF02.

3.2.4 Second IF Circuit

Refer to Figure 3-4.

In the second mixer, the first IF (21.4 MHz) and second LO (21.850 MHz from XP01) are mixed to produce a 450 kHz second IF signal. The signal passes through pin 3 of QF02 and applied to ceramic filter FF03 to eliminate adjacent signals. It is then applied to pin 5 of QF02 where it is amplified by a second IF amplifier and fed to a quadrature detector where it is converted to audio and output from pin 9.

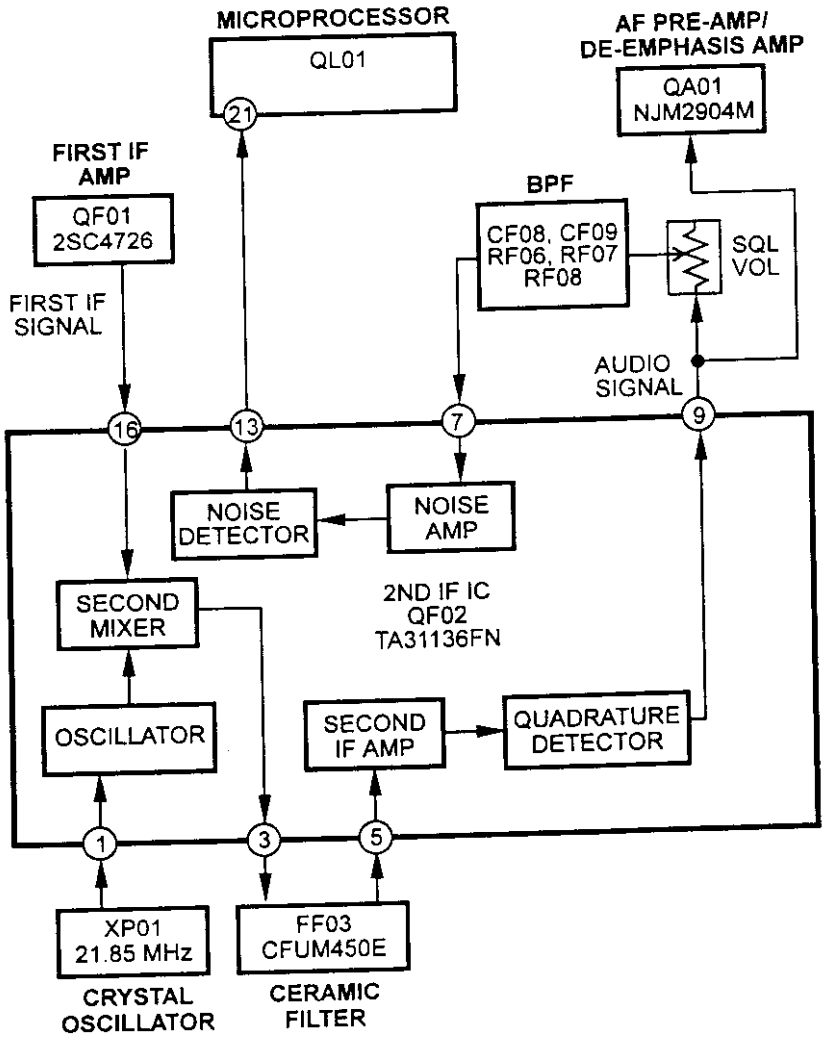

Figure 3-4

3.2.5 Audio Circuit

A portion of the audio signal output from second IF IC QF02 is applied to AF pre-amplifier QA01(1/2), and de-emphasis amp QA01(2/2) where the frequency of the audio signal is compensated and then applied to potentiometer RA10. The audio signal level is adjusted by potentiometer RA10, then input to pin 2 of AF power amplifier QA05. The amplified signal is output from pin 6 of QA05, passes through socket JA01 and drives internal speaker EA01.

3.2.6 Noise Squelch Circuit

A portion of the audio signal output from pin 09 of second IF IC QF02 is applied to potentiometer RA09. Then a band-pass filter consisting of CF08, CF09, RF06, RF07, and RF08. The audio signal is then applied to pin 7 of QF02. The noise component of the signal is output from pin 7 of QF02. It is rectified into a DC voltage in noise detector in IF IC QF02 to produce a squelch signal. The voltage of the squelch signal output pin 13 of IF IC QF02 ,and is applied to pin 21 of microprocessor QL01. The voltage is compared with the adjusted squelch level. Then be controlled pin 22(AF AMP SW) and pin 23(AF MUTE). When a low voltage(0V) output from pin 13 of IF IC QF02 is in operation (no sound is emitted from the transceiver.). When a high voltage(5V) output from pin 13 of IF IC QF02, squelch is off (noise is emitted from the transceiver.)

3.3 Transmitter Block

3.3.1 Microphone Amplifier

Refer to Figure 3-5.

When the push-to-talk switch (PTT) SL02 is pressed, it closes the microphone circuit which allows current to flow through microphone NA01 and also pulls the base of PTT on/off switch QL07 low (3.0 V). This turns on QL07 and 5 V is applied to pin 11 of microprocessor QL01 (PTT). When this happens, pin 15 of microprocessor Q601 (TX POWER B CONT) outputs a low voltage (0 V) which turns on RX/TX switch QM03 to supply TX B+ to the transmit circuits. Microphone audio is applied to the pre-emphasis circuit comprised of CA20 and RA27 then to pin 6 of microphone amplifier/LPF QA07. The amplified signal is output from pin 7 of QA07 and applied to QA06 for amplitude limiting. The limited signal is applied to pins 2 and 3 of MIC AMP/LPF QA07. QA07 contains a low pass filter that attenuates audio signals higher than 3 kHz by 18 dB/oct. The signal level is adjusted by Deviation Adjustment RA29 and applied to varactor QV05 to modulate the VCO.

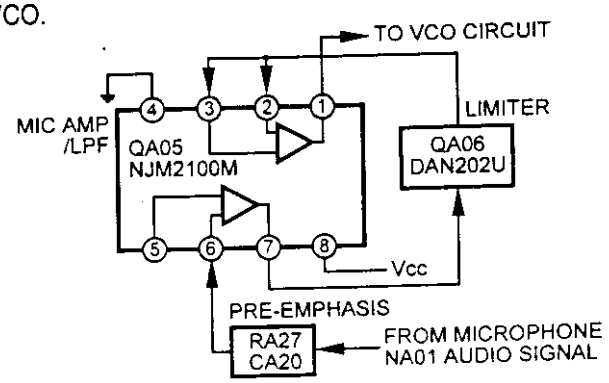

Figure 3-5

3.3.2 Buffer Amplifier

Refer to Figure 3-6.

The modulated transmit signal is output from QP06 of the VCO circuit and applied to buffer amplifier QP07. The amplified signal passes through TX/RX switch QT01 and is applied to a second buffer amplifier comprised of QT02 and QT03 which will amplify the signal from 1 mW to 50 mW. The amplified signal is then applied to the final power amplifier QT04.

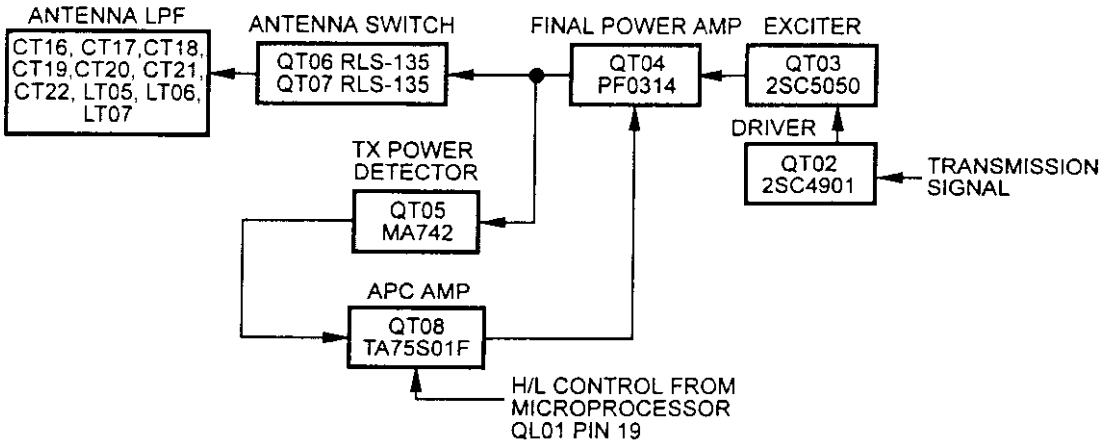

Figure 3-6

3.3.3 Final Power Amplifier

The transmit signal supplied by QT03 is further amplified to the desired level by final power amplifier QT04. The transmit signal output from QT04 passes through a low pass filter comprised of CT16 - CT22 and LT05 - LT07 to eliminate harmonics and spurious signals. The signal then passes through antenna socket JT01 and is output through the antenna.

3.3.4 High/Low Power

The RF power can be set to either 1 watt(LOW POWER) or 5 watts(HIGT POWER) by the H/L key on the front of the transceiver. If 1 watt is selected, a low voltage (0 V) is output from pin 19 of microprocessor QL01(HI/LO CONT), and applied to pin 1 of APC amp QT08 pass though QT09. This causes the automatic power control (APC) circuit to supply a lower signal level to the final amplifier QT04 so that the output is 1 watt. When 5 watts is selected, a high voltage (5 V) is output from pin 19 of microprocessor QL01(HI/LO CONT), and applied to pin 1 of APC amp QT08. This causes the APC circuit to stop operating and final amplifier Q304 will have an output of 5 watts.

3.3.5 APC (Automatic Power Control) Circuit

Refer to Figure 3-6.

When the transceiver is TX mode, a portion of the transmit signal output from final amplifier QT04 is applied to TX power detector QT05 which converts it to a DC voltage. The APC amp QT08 compare with an applied DC voltage from pin 19 of microprocessor QL01(HI/LO CONT) and an applied DC voltage from TX power detector QT05. Then the compare voltage output from pin 4 of APC amp QT08, and applied to pin 2 of the final amplifier QT04.

3.4 Control Circuit Block

3.4.1 Microprocessor

The microprocessor QL01 controls all the functions of the transceiver.

Microprocessor QL01

Table 3-1

Pin No.	I / O	Port name	Active	Initial	Pull up/Pull down	Function
1	O	NC	— —	— —	EXT UP	Not used
2	O	NC	— —	— —	EXT UP	Not used
3	— —	AVss	— —	— —	— —	Ground terminal
4	I	TEST	— —	— —	— —	Not used terminal (connected to ground)
5	I	Xin	— —	— —	— —	2MHz ceramic oscillator input
6	O	Xout	— —	— —	— —	2MHz ceramic oscillator output
7	I	RESET	— —	— —	EXT UP	Reset signal input
8	I	X1	— —	— —	EXT UP	Not used (connected to Vcc)
9	O	X2	— —	— —	— —	Not used(open)
10	— —	GND	— —	— —	— —	Ground terminal
11	I	PTT	H	L	EXT DN	PTT input terminal
12	I	LAMP	L	H	EXT UP	LAMP key input terminal
13	I	WA DET	L	H	EXT UP	WA detector input terminal
14	I	EXP SW	L	H	EXT UP	EXP CH setting mode on/off switching
15	O	TX B CONT	L	H	EXT UP	TX+B power supply control
16	O	RX B CONT	L	L	EXT UP	RX+B power supply control
17	O	LAMP CONT	L	H	EXT UP	LAMP on/off control
18	O	WA CONT	L	H	EXT UP	WA decoder IC power supply control
19	O	POWER CONT	L	L	EXT UP	power supply control
20	I	STOPC	L	H	EXT UP	STOP mode cancel control
21	I	POWER SW	L	H	EXT UP	POWER SW input
22	O	AF AMP SW	H	L	EXT DN	AF AMP power supply control
23	O	AF MUTE	L	L	INT UP	AF mute
24	O	BATT SAVE	H	L	EXT UP	Battery save output terminal
25	O	NC	— —	— —	— —	Not used
26	O	NC	— —	— —	— —	Not used
27	O	BEEP	— —	— —	INT UP	BEEP output terminal
28	O	NC	— —	— —	— —	Not used
29	O	NC	— —	— —	— —	Not used
30	I	UNLOCK	L	L	EXT DN	Lock : Hi Unlock : Lo
31	O	PLL CLK	— —	— —	INT UP	PLL CLK output terminal
32	O	PLL STB	— —	— —	INT UP	PLL STB output terminal
33	O	PLL DATA	— —	— —	INT UP	PLL DATA output terminal
34	I	EEPROM DO	— —	— —	EXT UP	Serial data input terminal
35	O	EEPROM DI	— —	— —	INT UP	Serial data output terminal
36	O	EEPROM SK	— —	— —	INT UP	Serial clock output terminal
37	O	EEPROM CS	— —	— —	EXT DN	Chip select output terminal
38	O	EVOL EN	— —	— —	INT UP	Electronic volume write enable output terminal
39	O	EVOL DATA	— —	— —	INT UP	Electronic volume clock output terminal
40	O	EVOL CLK	— —	— —	INT UP	Electronic volume data output terminal

Pin No.	I / O	Port name	Active	Initial	Pull up/Pull down	Function
41	O	NC	— —	— —	— —	Not used
42	O	SEG 0	— —	— —	— —	Segment 0 output terminal
43	O	SEG 1	— —	— —	— —	Segment 1 output terminal
44	O	SEG 2	— —	— —	— —	Segment 2 output terminal
45	O	SEG 3	— —	— —	— —	Segment 3 output terminal
46	O	SEG 4	— —	— —	— —	Segment 4 output terminal
47	O	SEG 5	— —	— —	— —	Segment 5 output terminal
48	O	SEG 6	— —	— —	— —	Segment 6 output terminal
49	O	SEG 7	— —	— —	— —	Segment 7 output terminal
50	O	SEG 8	— —	— —	— —	Segment 8 output terminal
51	O	SEG 9	— —	— —	— —	Segment 9 output terminal
52	O	SEG 10	— —	— —	— —	Segment 10 output terminal
53	O	SEG 11	— —	— —	— —	Segment 11 output terminal
54	O	SEG 12	— —	— —	— —	Segment 12 output terminal
55	O	SEG 13	— —	— —	— —	Segment 13 output terminal
56	O	SEG 14	— —	— —	— —	Segment 14 output terminal
57	O	SEG 15	— —	— —	— —	Segment 15 output terminal
58	O	SEG 16	— —	— —	— —	Segment 16 output terminal
59	O	SEG 17	— —	— —	— —	Segment 17 output terminal
60	O	SEG 18	— —	— —	— —	Segment 18 output terminal
61	O	SEG 19	— —	— —	— —	Segment 19 output terminal
62	O	SEG 20	— —	— —	— —	Segment 20 output terminal
63	O	SEG 21	— —	— —	— —	Segment 21 output terminal
64	O	SEG 22	— —	— —	— —	Segment 22 output terminal
65	O	SEG 23	— —	— —	— —	Segment 23 output terminal
66	O	COM 1	— —	— —	— —	Common 1 output terminal
67	O	COM 2	— —	— —	— —	Common 2 output terminal
68	O	COM 3	— —	— —	— —	Not used
69	O	COM 4	— —	— —	— —	Not used
70	— —	V 1	— —	— —	— —	LCD drive voltage (connected to Vcc)
71	— —	V 2	— —	— —	— —	Connected to V 3
72	— —	V 3	— —	— —	— —	Connected to V 2
73	— —	Vcc	— —	— —	— —	Power supply terminal
74	— —	AVcc	— —	— —	— —	A/D power supply terminal(connected to Vcc)
75	I	KEY 1	— —	— —	EXT UP	Front key input 1
76	I	KEY 2	— —	— —	EXT UP	Front key input 2
77	I	SQL	— —	— —	— —	SQL input
78	I	BATT_CHK	— —	— —	— —	Battery voltage input (+B / 2)
79	O	NC	— —	— —	EXT UP	Not used
80	O	NC	— —	— —	EXT UP	Not used

3.4.2 EEPROM

Refer to Figure 3-7.

EEPROM QL02 stores the data supplied by microprocessor QL01 that control channels placed into scan memory, the channel that the transceiver was set to when it was turned off, and expansion channels programmed into the transceiver's memory. And stores the initial data that is the TX H/L power data, the squelch level data, and the AF volume control level data. QL02 will store this data even when no voltage is supplied to it.

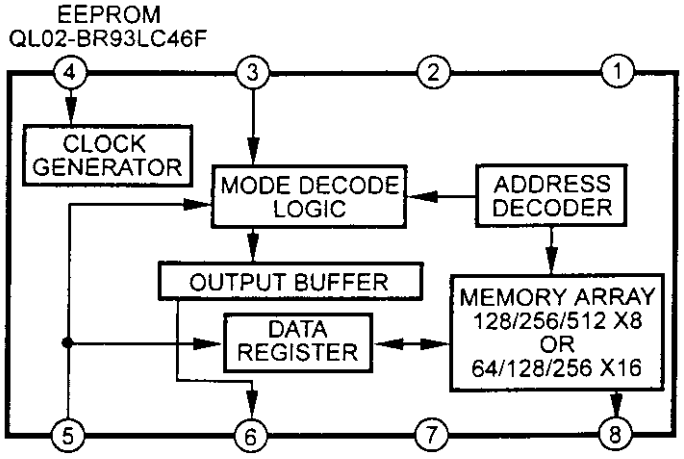

Figure 3-7

3.4.3 LAMP Control

When the LAMP/KEYLOCK key is pressed, a low voltage (0 V) is output from pin 17 of microprocessor QL01 (LAMP CONT). This causes lamp switch QL04 to turn on and the lamp to light. After 5 seconds, the output of pin 17 of microprocessor QL01 (LAMP CONT) will return to a high voltage level (5.0 V). This will cause lamp switch QL04 to turn off and the lamp will also turn off.