Circuit Description

1. Frequency Configuration

The receiver utilizes double conversion super heterodyne. The first IF is 45.05MHz and the second is 455KHz. The first local oscillator signal is supplied from PLL circuit. Frequency needed in the transmitter is supplied from PLL circuit. Figure 1 shows the frequency configuration.

Frequency range：TC2108U: 450MHz—470MHz

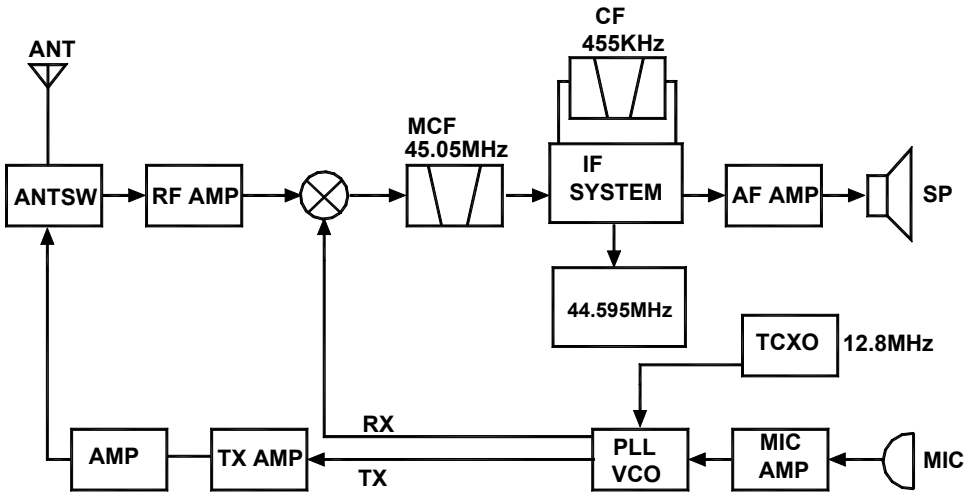

Figure 1. frequency configuration

2. Receiver

The receiver utilizes double conversion super heterodyne.

1) Front-end RF Amplifier

The input signal from antenna is amplified in RF amplifier (Q27) after passing through the receive/transmit circuit and a 3-stage LC band pass filter. The amplified signal is filtered by a band pass filter (a 3-stage LC BPF) to eliminate unwanted signal before passing to the first frequency mixer.

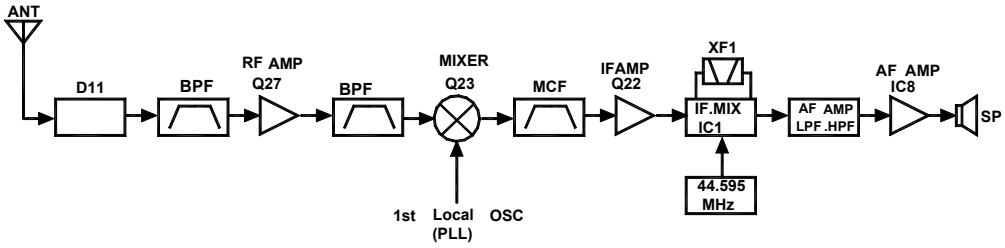

Figure 2. receiver section configuration

2) The First Mixer

The signal from RF amplifier is mixed with the first local oscillator signal from PLL frequency synthesizer in the first mixer (Q23) to generate a 45.05MHz first IF signal. The first IF signal is then fed through two monolithic crystal filters (XF1) to remove spurious signals from adjacent channels.

3) IF Amplifier

The first IF signal is amplified in Q22 and then enters the IF process chip IC1. The signal is mixed with the second local oscillator signal in IC1 to create a 455KHz second IF signal. The second IF signal is then fed to a 455KHz ceramics filter (CF1) to eliminate unwanted signals before it is amplified and FM detected in IC1.

4) AF Amplifier

The demodulated AF signal obtained from IC1 is amplified in IC7 (1/4), and then filtered by low pass filter Q19 and high pass filter Q20, and then de-emphasized by R130 and C156. The resulting AF signal passes through a volume control circuit and then is amplified to a sufficient level to drive the speaker by AF power amplifier (IC8).

5) Squelch

Part of the AF signal from IC1 enters IC1 again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level. The DC signal from IC1 goes to the analog port of the microprocessor (IC11). IC11 determines whether to output sounds from the speaker by detecting whether the input voltage is higher or lower than preset value.

To output sounds from the speaker, IC11 sends a high level signal to the MUTE and AFCO lines and turns IC8 on through Q12.

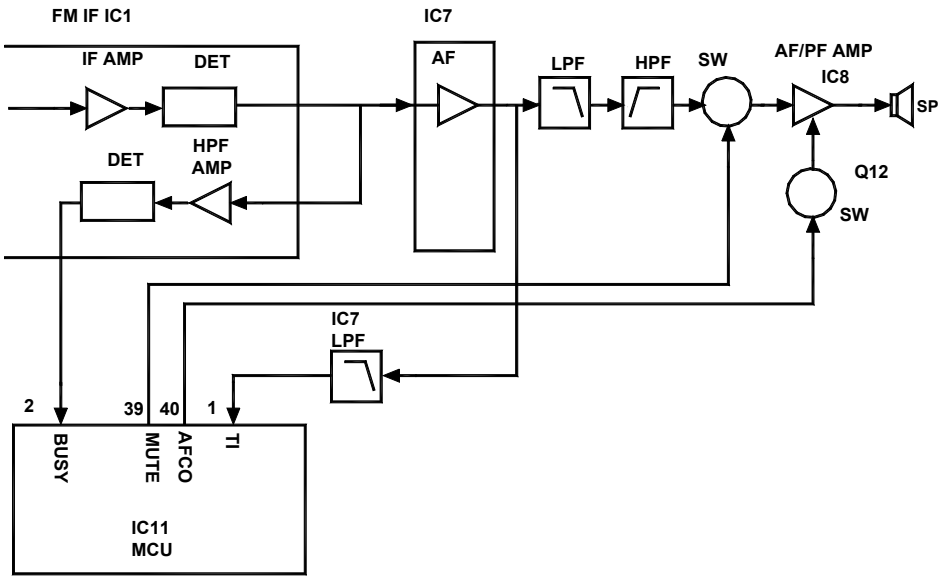

Figure 3. AF amplifier and squelch circuit

6) Receive signaling

CTCSS

Audio frequencies over 300Hz of the output signal from IC1 are cut off by a low-pass filter. The resulting signal enters the microprocessor IC11. IC11 determines whether the CTCSS matches the preset value and controls the MUTE and AFCO and the speaker sound output according to the squelch results.

3. PLL Frequency Synthesizer

PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

1) PLL Circuit

The frequency step of PLL circuit is 5KHz or 6.25KHz. A12.8MHz reference oscillator signal is divided at IC1 by a fixed counter to produce a 5KHz or 6.25KHz reference frequency. Output signal from voltage control oscillator (VCO) passes through buffer amplifier Q14 and is divided at IC2 by the dual-module programmable counter. The divided signal is compared in the phase comparator IC2 with the 5KHz or 6.25KHz reference signal. The output signal from phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency. (See figure 4)

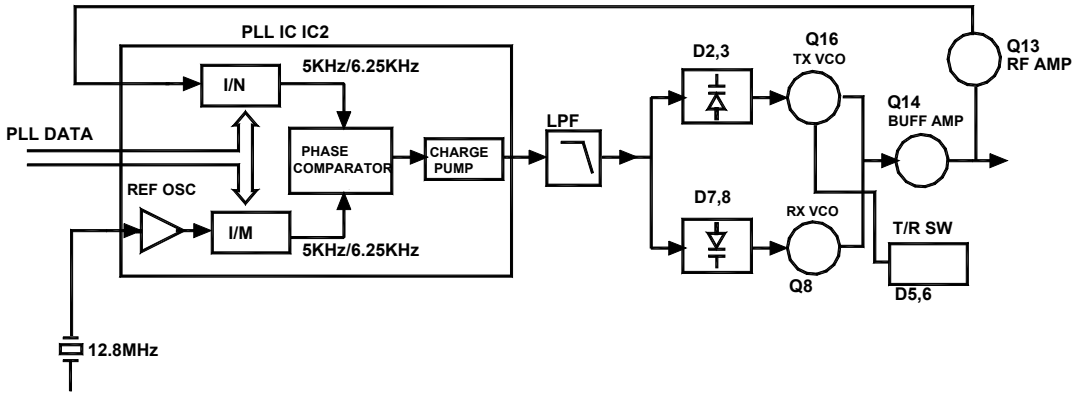

Figure 4. PLL circuit

2) VCO

The operating frequency is generated by Q16 in transmit mode and by Q8 in receive mode. The operation frequency generates a voltage through the phase comparator to control the varactor diodes, so as to keep the oscillator frequency consistent with the preset frequency in CPU (D2 and D3 in transmit mode and D7 and D8 in receive mode). T/R pin is set high in receive mode causing Q6 to turn off Q16 and turn Q7 on. The T/R pin is set low in transmit mode. The output from Q8 and Q16 is amplified by Q14 and sent to the buffer amplifier.

3) Unlock Detector

If low level appears at LD pin of IC2, unlock condition will occur, and DC voltage is obtained from D13 and R63, and the voltage supplied to the UL pin of microprocessor by IC2 goes low. When the microprocessor detects this condition, the transmitter is disabled, ignoring the push-to-talk switch input signal. (See figure 5)

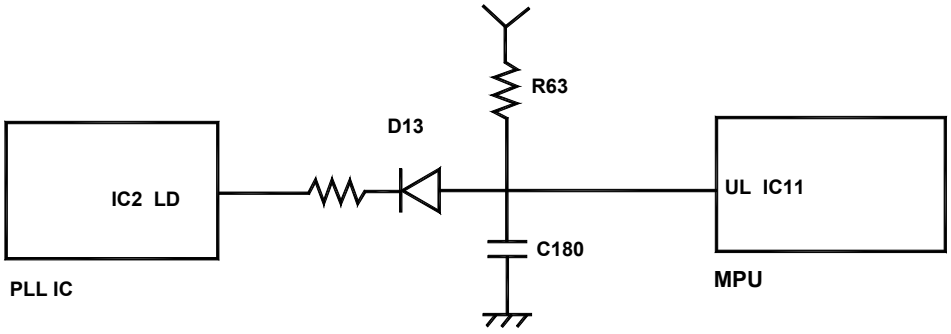

Figure 5. unlocked detect circuit

4. Transmitter

1) Transmit audio

The audio signal from microphone is amplified through IC3(1/2) ,and then pre-emphasized, and then filtered by another low-pass filter（separate filter）(Q25 and Q24) to eliminate the frequencies over 3KHz. The resulting signal enters the VCO for direct FM modulation. (See figure 6)

2) CTCSS Encoder

The necessary frequency for CTCSS encoder is generated by IC11 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is performed at the VCO side by adjusting the balance. (See figure 6)

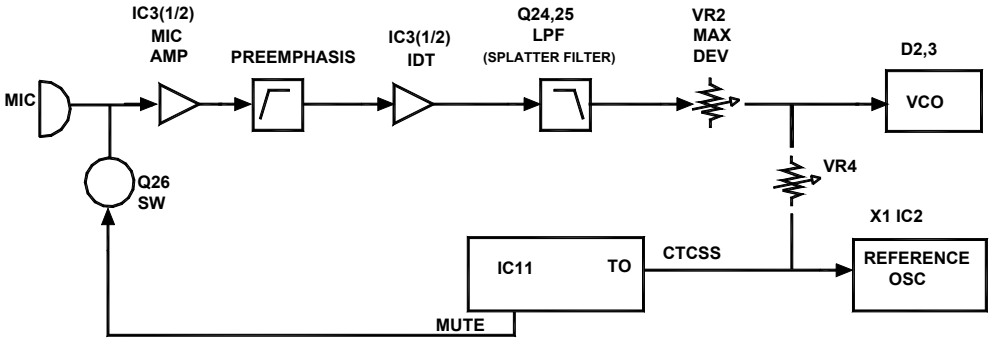

Figure 6. transmit CTCSS

3) VCO and RF amplifier

The transmit signal obtained from VCO buffer amplifier Q14 is amplified by Q15. This amplified signal is passed to power amplifier Q32 and Q31, which includes a 2-stage FET amplifier, and is capable of producing a 2.0W RF power.

4) Antenna Switch and LPF

The RF amplifier output signal is passed through a low-pass filter network and a transmit/receive circuit before it is passed to the antenna terminal. The transmit/receive switch circuit is comprised of D11 and D12. D11 and D12 is turned on in transmit mode and off in receive mode.

5. Power

The 5V reference power supply for the control circuit is derived from an internal battery. The reference power provides a 5V supply in transmit mode [T_V], a 5V supply in receive mode [R_V], and a 5V supply shared in both modes based the control signal from the microprocessor.

6. Control System

The IC11 CPU operates at 7.3728MHz.