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FIBOCOM AN958-NA Module Hardware User Guide

Version: 1.8

Date: 2022-04-19

Fibocom Auto Inc.

Applicability Model

No.	Product Model	Software Baseline	Applicable Customer	Description
1	AN958-NA	--	--	Support frequency bands in North Americas regions. See Table 2-1 for frequency band information.

Change History

Version	Date	Author	Reviewed by	Approved by	Change Description
1.0	2021-03-03	Deng Jie/Che Qingcheng	Dai Wenhui	Dai Wenhui	Initial version
1.1	2021-03-31	Deng Jie/Che Qingcheng	Dai Wenhui	Dai Wenhui	• Updated the recommended layout rules of RGMII and PCIe. • Updated the WCDMA features description. • Deleted section 1.2 "References." • Added the power supply current description of the module.
1.2	2021-06-16	Che Qingcheng	Dai Wenhui	Dai Wenhui	Updated the frequency band configuration, with n5 and n28 frequency bands added.
1.3	2021-07-26	Li Gao/Che Qingcheng	Dai Wenhui	Dai Wenhui	• Updated the GPIO name. • Updated the RF antenna interface configuration information.
1.4	2021-09-02	Li Gao/Che Qingcheng	Dai Wenhui	Dai Wenhui	• Modified the GSM frequency band information in NA version. • Updated the description of some pins.
1.5	2021-11-11	Che Qingcheng	Dai Wenhui	Dai Wenhui	Added the AN958 discrete solution.
1.6	2021-12-27	Qi Jianwen	Dai Wenhui	Dai Wenhui	Added the CA combinations in Chinese version and optimized the document format.
1.7	2022-02-09	Mo Wei	Dai Wenhui	Dai Wenhui	Updated pin distribution diagram and revised the function description of some pins.
1.8	2022-04-19	Che Qingcheng	Dai Wenhui	Dai Wenhui	• Normalized the AN958 series manuals. • Optimize related contents according to review results

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Notice

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Contents

1 About This Document

1.1 Description

This document describes information on the electrical characteristics, structural dimensions, application environment, and OTA interface as well as hardware interface of the AN958-NA series modules. With the help of this document and other related documents, customers can quickly apply AN958-NA series modules to customer applications.

1.2 Safety Instruction

Please observe the following safety instructions to ensure personal safety and protect the product and work environment from potential damages. The product manufacturer should communicate the following safety instructions to end users and incorporate the safety instructions into the User Manuals of end products. Fibocom Auto Inc. will not take any responsibility for the consequences made by users who do not follow the safety rules or use the product improperly.

	Road safety first! When you are driving, do not use a handheld mobile terminal, even if it has a hands-free function. Stop the car before making a call.
	Please turn off the mobile terminal before boarding. It is prohibited to turn on the wireless function of the mobile terminal on the aircraft to prevent interference with the communication system of the aircraft. Failure to follow this prompt may affect flight safety or even violate the law.
	When you are in a hospital or health care facility, please be aware of restrictions on the use of mobile terminals. RF interference may cause abnormal operation of medical devices. Therefore, it may be required to turn off the mobile terminals.
	The mobile terminal does not guarantee a valid connection under any circumstances, for example, when the mobile terminal is in arrears or the (U)SIM is invalid. In case of emergency in above situations, remember to use the emergency call, and make sure your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal will receive and transmit RF signals when it is turned on. When it is close to TV, radio, computer or other electronic equipment, RF interference will be generated.
	Keep the mobile terminal away from flammable gases. Please turn off the mobile terminal when it is near gas stations, oil depots, chemical plants or explosive workplaces. There are potential safety hazards caused by the operation of electronic devices in any area with potential explosion hazards.

2 Product Overview

2.1 General Description

AN958 series modules are highly integrated 5G automotive-grade modules, supporting 5G NR SUB6, LTE FDD, LTE TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE, GPRS, GSM, as well as Global Navigation Satellite System (GNSS) technology. AN958 series modules can be applied to the wireless communication networks of most mobile operators in the world. There are 357 LGA pins in total, and the package size is 48 mm × 48 mm × 2.7 mm. AN958 series modules can meet the needs of automotive-grade applications in all environments.

2.2 Product Specifications

2.2.1 RF Characteristics

Table 2–1 Operating bands of AN958-NA

Model	AN958-NA
5G NR	n2, n5, n7, n12, n14, n25, n28, n41, n48, n66, n71, n77, n78
LTE FDD	B2, B4, B5, B7, B12, B14, B17, B25, B26, B28, B29, B66, B71
LTE TDD	B41, B42
WCDMA	B2, B4, B5
GSM	850 MHz, 900 MHz, 1900 MHz
GNSS	L1

Table 2–2 Data Transmission of AN958-NA

Model	AN958-NA
NR Sub6 ENDC	DL peak rate 2.5 Gbps UL peak rate 625 Mbps DL 4 × 4 MIMO LTE/NR
NR Sub6 SA	DL peak rate 2.1 Gbps UL peak rate 525 Mbps DL 4 × 4 MIMO
LTE	DL peak rate 1.6 Gbps UL peak rate 200 Mbps DL 4 × 4 MIMO
WCDMA	DL peak rate 42 Mbps (CAT24) UL peak rate 5.76 Mbps (CAT6)
GSM	GPRS: DL peak rate 107 kbps UL peak rate 85.6 kbps EDGE: DL peak rate 296 kbps UL peak rate 236.8 kbps

Table 2–3 Modulation characteristics of AN958-NA

Model	AN958-NA

Model	AN958-NA
NR Sub6 ENDC	LTE modulation: Support DL 256 QAM, UL 64 QAM NR modulation: Support DL 256 QAM, UL 256 QAM
NR Sub6 SA	Support DL 256 QAM and UL 256 QAM Support RF bandwidth 5-100 MHz Support carrier interval: 15 kHz (FDD), 30 kHz (TDD)
LTE	Support 3GPP R15 Support 5DLCA maximally Support DL 256 QAM, UL 64 QAM Support bandwidth 1.4-20 MHz
WCDMA	Support 3GPP R9 DC-HSPA+ Support QPSK, 16-QAM and 64-QAM modulation
GSM	GPRS: Support GMSK EDGE: Support 8-PSK

2.2.2 Key Features

Table 2–4 Key features

Performance	Description
Power supply	DC: 3.4–4.2 V, typical voltage: 3.8 V
Processor	QUALCOMM SA515M, 7 nm process, ARM Cortex-A7, up to 1.5 GHz
Memory	8Gb LPDDR4X+8Gb Nand Flash
Operating system	Linux
Power class	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm ±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2.7dB) for LTE-FDD bands Class 3 (23dBm±2.7dB) for LTE-TDD bands Class 3 (23dBm2/-3dB) for NR Sub6 bands except N41/77/78 Class 2 (26dBm±1dB) for N41/77/78 bands
GNSS characteristics	Support GNSS L1 GPS/GLONASS/BeiDou/Galileo/QZSS
Antenna	WWAN Antenna x 4
	Support 4 × 4 MIMO
SMS	MO/MT SMS
Audio interface	Support I^2S digital audio interface
USB interface	USB3.0 Super-high Speed (SS) interface, with a data transmission rate of up to 5 Gbps, downward compatible with USB2.0 High-speed (HS) interface with a data transmission rate of up to 480 Mbps
PCIe interface	PCIe Gen 3 x 2 lanes
SIM interface	2 sets of SIM card interfaces (single channel) Support USIM/SIM: 1.8 V and 3 V

Performance	Description
	SIM1: USIM/SIM SIM2: USIM/SIM
SPI interface	2 sets of SPI interfaces. Maximum clock frequency at 50 MHz. Only the master mode is supported.
I^2C interface	2 sets of I^2C interfaces. High speed of up to 3.4 Mbps
UART interface	2 sets of UART interfaces (serial debugging interface × 1)
RGMII interface	Support 10/100/1000M PHY
SDIO interface	1 set, support 4-bit/8-bit mode
GPIOs	≥5
Physical characteristics	Dimensions: 48 mm × 48 mm × 2.7 mm Package: LGA Weight: about 15g
Temperature range	Operating temperature: –40℃ to 85℃[1] Extended temperature: –40℃ to 90℃[2] Storage temperature: –40℃ to 95℃ ECALL operating temperature: –40℃ to 95℃
Software update	Support FOTA update
RoHS	RoHS compliant, halogen free

Warning

1. When the temperature keeps in the specified range, the module can work properly. Module performance meets the 3GPP specifications.
2. When the temperature keeps in the specified range, the module performance may not meet the 3GPP specifications.

2.3 CA Combinations

2.3.1 CA Combinations Supported by AN958-NA

2CA Combination	3CA Combination	4CA Combination	5CA Combination
2A-2A	2A-2A-4A	2A-2A-4A-12A	2A-2A-5A-66A-66A
2A-4A	2A-2A-5A	2A-2A-4A-71A	2A-2A-5B-66A
2A-5A	2A-2A-12A	2A-2A-5A-66A	2A-2A-12A-66A-66A
2A-12A	2A-2A-14A	2A-2A-5B	2A-2A-14A-66A-66A
2A-14A	2A-2A-29A	2A-2A-12A-66A	2A-5B-66A-66A
2A-17A	2A-2A-66A	2A-2A-14A-66A	2A-14A-66A-66A-66A
2A-28A	2A-2A-71A	2A-2A-66A-66A	--
2A-29A	2A-4A-4A	2A-2A-66A-71A	--

2CA Combination	3CA Combination	4CA Combination	5CA Combination
2A-66A	2A-4A-5A	2A-2A-66C	--
2A-71A	2A-4A-12A	2A-4A-4A-12A	--
2C	2A-4A-28A	2A-5A-66A-66A	--
4A-4A	2A-4A-71A	2A-5B-66A	--
4A-5A	2A-5A-66A	2A-12A-66A-66A	--
4A-7A	2A-5B	2A-12A-66C	--
4A-12A	2A-12A-66A	2A-14A-66A-66A	--
4A-17A	2A-14A-66A	2A-66A-66A-66A	--
4A-28A	2A-29A-66A	2A-66A-66A-71A	--
4A-29A	2A-66A-66A	2A-66C-71A	--
4A-71A	2A-66A-71A	2C-66A-66A	--
5A-7A	2A-66C	5B-66A-66A	--
5A-12A	2C-66A	7C-66A-66A	--
5A-66A	4A-4A-12A	14A-66A-66A-66A	--
5B	4A-4A-71A	--	--
7A-28A	5A-7C	--	--
12A-66A	7A-66A-66A	--	--
14A-66A	7C-28A	--	--
29A-66A	12A-66A-66A	--	--
42A-42A	12A-66C	--	--
66A-66A	14A-66A-66A	--	--
66A-71A	66A-66A-71A	--	--
66B	66A-66C	--	--
66C	66C-71A	--	--

2.4 EN-DC Combinations

2.4.1 EN-DC Combinations Supported by AN958-NA

5G-NR	Combination Type	EN-DC Combination	4G DL	5G-NR	Combination Type	EN-DC Combination
TDD	1DL + FR1	DC_28A_n78A	--	n78A	28A	n78A
TDD	1DL + FR1	DC_7A_n78A	7A	n78A	7A	n78A
TDD	1DL + FR1	DC_5A_n78A	--	n78A	5A	n78A

5G-NR	Combination Type	EN-DC Combination	4G DL	5G-NR	Combination Type	EN-DC Combination
FDD	1DL + FR1	DC_12A_n2A	--	n2A	12A	n2A
FDD	1DL + FR1	DC_12A_n66A	--	n66A	12A	n66A
FDD	1DL + FR1	DC_5A_n66A	--	n66A	5A	n66A
FDD	1DL + FR1	DC_66A_n2A	--	n2A	66A	n2A
FDD	1DL + FR1	DC_66A_n71A	66A	--	66A	n71A
FDD	1DL + FR1	DC_71A_n2A	--	n2A	71A	n2A
FDD	1DL + FR1	DC_2A_n66A	--	n66A	2A	n66A
FDD	1DL + FR1	DC_2A_n71A	2A	--	2A	n71A
FDD	1DL + FR1	DC_5A_n2A	--	n2A	5A	n2A
FDD	1DL + FR1	DC_7A_n71A	7A	--	7A	n71A
FDD	1DL + FR1	DC_5A_n7A	--	n7A	5A	n7A
FDD	1DL + FR1	DC_12A_n7A	--	n7A	12A	n7A
FDD	1DL + FR1	DC_66A_n7A	--	n7A	66A	n7A
TDD	1DL + FR1	DC_66A_n78A	66A	n78A	66A	n78A
TDD	1DL + FR1	DC_2A_n78A	2A	n78A	2A	n78A
TDD	1DL + FR1	DC_12A_n78A	--	n78A	12A	n78A
FDD	1DL + FR1	DC_2A_n5A	2A	--	2A	n5A
FDD	1DL + FR1	DC_7A_n5A	7A	--	7A	n5A
FDD	1DL + FR1	DC_66A_n5A	66A	--	66A	n5A
FDD	1DL + FR1	DC_7A_n28A	7A	--	7A	n28A
TDD	1DL + FR1	DC_2A_n48A	2A	n48A	2A	n48A
TDD	1DL + FR1	DC_66A_n48A	66A	n48A	66A	n48A
FDD	2DL + FR1	DC_2A-2A_n5A	2A	--	2A	n5A
FDD	2DL + FR1	DC_2A-2A_n66A	--	n66A	2A	n66A
FDD	2DL + FR1	DC_2A-2A_n71A	2A	--	2A	n71A
FDD	2DL + FR1	DC_2A-5A_n2A	--	n2A	2A,5A	n2A
FDD	2DL + FR1	DC_2A-5A_n5A	2A	--	2A	n5A
FDD	2DL + FR1	DC_2A-5A_n66A	--	n66A	2A,5A	n66A
FDD	2DL + FR1	DC_2A-7A_n71A	2A	--	2A,7A	n71A
TDD	2DL + FR1	DC_2A-7A_n78A	--	n78A	2A,7A	n78A
FDD	2DL + FR1	DC_2A-12A_n2A	--	n2A	12A	n2A
FDD	2DL + FR1	DC_2A-12A_n66A	--	n66A	2A,12A	n66A

5G-NR	Combination Type	EN-DC Combination	4G DL	5G-NR	Combination Type	EN-DC Combination
FDD	2DL + FR1	DC_2A-66A_n5A	2A	--	2A	n5A
FDD	2DL + FR1	DC_2A-66A_n66A	--	n66A	2A	n66A
FDD	2DL + FR1	DC_2A-66A_n71A	2A	--	2A,66A	n71A
TDD	2DL + FR1	DC_2A-66A_n78A	--	n78A	2A,66A	n78A
FDD	2DL + FR1	DC_2C_n71A	2C	--	2C	n71A
TDD	2DL + FR1	DC_5A-7A_n78A	--	n78A	5A,7A	n78A
FDD	2DL + FR1	DC_5A-66A_n2A	--	n2A	5A	n2A
FDD	2DL + FR1	DC_5A-66A_n5A	66A	--	66A	n5A
FDD	2DL + FR1	DC_5A-66A_n66A	--	n66A	5A	n66A
TDD	2DL + FR1	DC_7A-7A_n78A	--	n78A	7A	n78A
TDD	2DL + FR1	DC_7A-28A_n78A	--	n78A	7A,28A	n78A
TDD	2DL + FR1	DC_7A-66A_n78A	--	n78A	7A,66A	n78A
TDD	2DL + FR1	DC_7C_n78A	--	n78A	7C	n78A
FDD	2DL + FR1	DC_7C_n5A	7C	--	7C	n5A
FDD	2DL + FR1	DC_7C_n28A	7C	--	7C	n28A
FDD	2DL + FR1	DC_12A-66A_n2A	--	n2A	12A,66A	n2A
FDD	2DL + FR1	DC_12A-66A_n25A	--	n25A	12A,66A	n25A
FDD	2DL + FR1	DC_12A-66A_n66A	--	n66A	12A	n66A
FDD	2DL + FR1	DC_66A-66A_n5A	66A	--	66A	n5A
FDD	2DL + FR1	DC_66A-66A_n71A	66A	--	66A	n71A
TDD	2DL + FR1	DC_66A-66A_n78A	--	n78A	66A	n78A
FDD	2DL + FR1	DC_66C_n71A	66C	--	66C	n71A
TDD	2DL + FR1	DC_2A-48A_n48A	--	n48A	2A	n48A
TDD	2DL + FR1	DC_48A-66A_n48A	--	n48A	66A	n48A
FDD	3DL + FR1	DC_2A-2A-5A_n66A	--	n66A	2A,5A	n66A
FDD	3DL + FR1	DC_2A-2A-12A_n66A	--	n66A	2A,12A	n66A
FDD	3DL + FR1	DC_2A-2A-66A_n5A	2A	--	2A,66A	n5A
FDD	3DL + FR1	DC_2A-2A-66A_n71A	2A	--	2A,66A	n71A
FDD	3DL + FR1	DC_2A-12A-	--	n2A	12A,66A	n2A

5G-NR	Combination Type	EN-DC Combination	4G DL	5G-NR	Combination Type	EN-DC Combination
		66A_n2A				
FDD	3DL + FR1	DC_2A-12A-66A_n66A	--	n66A	2A,12A	n66A
FDD	3DL + FR1	DC_2A-5A-66A_n5A	2A,66A	--	2A,66A	n5A
FDD	3DL + FR1	DC_2A-66A-66A_n5A	2A	--	2A,66A	n5A
FDD	3DL + FR1	DC_2A-66A-66A_n71A	2A,66A	--	2A,66A	n71A
FDD	3DL + FR1	DC_2A-66C_n71A	2A,66C	--	2A,66C	n71A
FDD	3DL + FR1	DC_2C-66A_n71A	--	--	2C,66A	n71A
FDD	3DL + FR1	DC_12A-66A-66A_n2A	--	n2A	12A	n2A
FDD	3DL + FR1	DC_66A-66A-66A_n5A	66A	--	66A	n5A
FDD	4DL + FR1	DC_2A-2A-66A-66A_n5A	66A	--	66A	n5A
FDD	4DL + FR1	DC_2A-12A-66A-66A_n2A	--	n2A	66A	n2A

2.5 Hardware Block Diagram

Figure 2-1 shows the main hardware functions of AN958-NA series modules, including baseband and RF functions.

The baseband functions include:

UMTS/LTE/NR Controller

PMU

NAND/LPDDR RAM

Application Interface

The RF functions include:

RF Transceiver

RF Power/PA

RF Front End

RF Filter

Antenna Connector

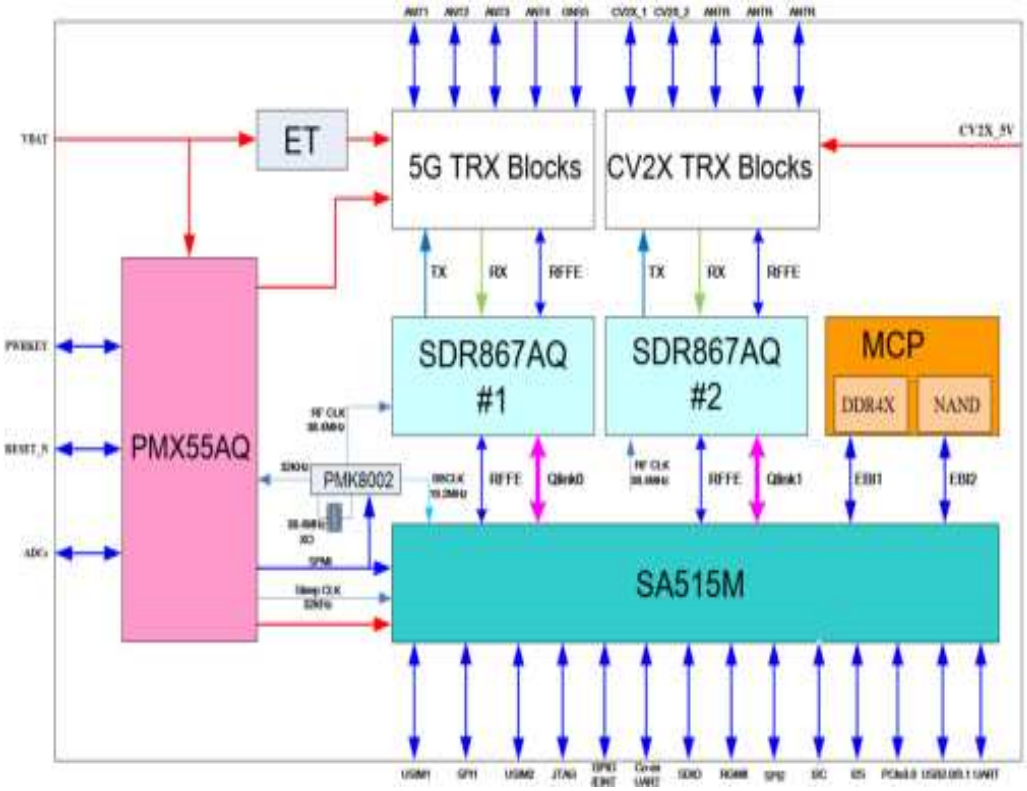

Figure 2-1 Hardware block diagram

3 Application Interfaces

3.1 LGA Interface

The AN958-NA module uses LGA interface with 357 pins in total.

3.1.1 Pin Distribution

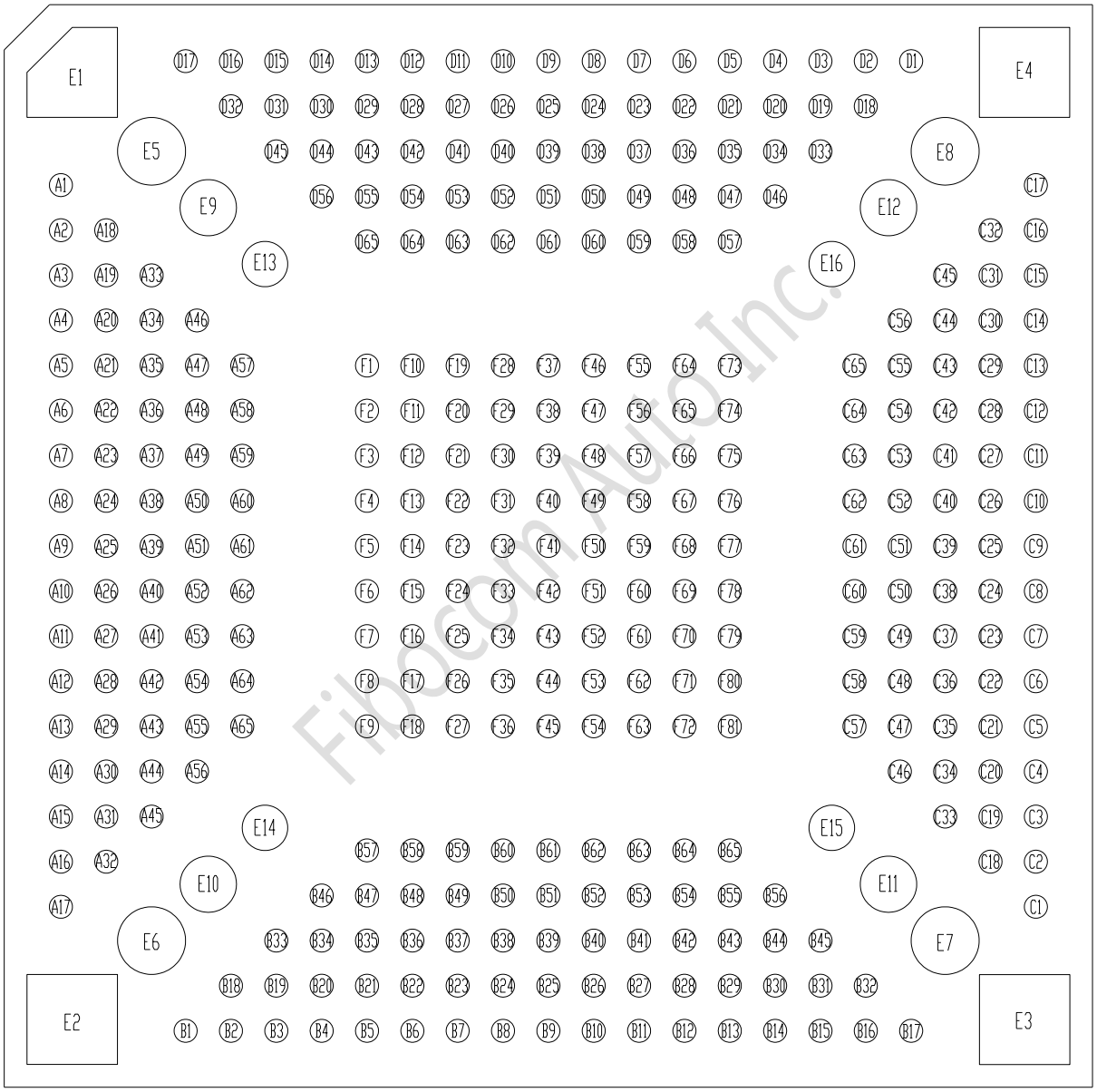

Figure 3-1 Pin distribution (top perspective)

3.1.2 Pin Definition

Table 3-1 I/O parameter definitions

Type	Description
IO	Input/Output

Type	Description
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain
Hi-Z	High resistance

The following table describes the AN958-NA module's pin functions and electrical characteristics.

Table 3-2 Pin description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
V2X_5V	A37 A38	PI	--	V2X 5V power input	This power supply needs to be controlled independently.
VPH_PWR	A7 A8 A23 A24	PI	--	Power supply : Input, 3.4–4.2V. Tyical value : 3.8V	--
VDD_EXT_1V8	A9	PO	--	IO power supply: 1.8 V	50mA
VREG_S2E_1P224	A25	PO	--	Wi-Fi power output. Default: 1.28 V	400mA
VREG_S3E_0P824	A50 A51	PO	--	Wi-Fi power output. Default: 0.88 V	1200mA
VREG_S4E_1P904	A39	PO	--	Wi-Fi power output. Default: 1.88 V	250 mA
RGMII					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
RGMII_VREG	A56	PI	--	RGMII power input	1.8/2.5 V (I_{PK}: 150 mA)
RGMII_VREG_EN	A43	DO	PD	RGMII_VREG power enable signal	--
RGMII_VREG_PWR_EN	A42	DO	PD	PHY power enable signal	--
RGMII_RESET	A17	DO	PD	RGMII reset output signal	--
RGMII_INT	A41	DI	PD	RGMII interrupt input signal	--
RGMII_MDIO	A45	DIO	PD	RGMII MDIO signal	--
RGMII_MDC	A44	DO	PD	RGMII MDC signal	--
RGMII_TX_CTL	A11	DO	PD	RGMII TX control signal	--
RGMII_TX_CLK	A12	DO	PD	RGMII TX clock signal	--
RGMII_TX_0	A13	DO	PD	RGMII TX bit 0 signal	--
RGMII_TX_1	A14	DO	PD	RGMII TX bit 1 signal	--
RGMII_TX_2	A15	DO	PD	RGMII TX bit 2 signal	--
RGMII_TX_3	A16	DO	PD	RGMII TX bit 3 signal	--
RGMII_RX_CTL	A27	DI	PD	RGMII RX control signal	--
RGMII_RX_CLK	A28	DI	PD	RGMII RX clock signal	--
RGMII_RX_0	A29	DI	PD	RGMII RX bit 0 signal	--
RGMII_RX_1	A30	DI	PD	RGMII RX bit 1 signal	--

RGMII_RX_2	A31	DI	PD	RGMII RX bit 2 signal	--
RGMII_RX_3	A32	DI	PD	RGMII RX bit 3 signal	--
PHY_WAKE_ OUT/ GPIO_61	D46	DIO	PD	Pin used to wake up Ethernet by module	Alternatively used for normal GPIO function
PHY_WAKE_IN/ GPIO_86	D47	DIO	PD	Pin used to wake up module by Ethernet	Alternatively used for normal GPIO function
ADC					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
ADC1	A53	AI	--	A/D conversion channel	Resolution: 15 bits
USIM					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
USIM1_VCC	A6	PI	--	SIM1 power supply input: 3V/1.8V	--
USIM1_DATA	A36	DIO	PD	SIM1 data signal	--
USIM1_CLK	A48	DO	PD	SIM1 clock signal	--
USIM1_RST	A22	DO	PD	SIM1 reset signal	--
USIM1_DET	A49	DI	PD	SIM1 detect signal	--
USIM2_VCC	A35	PI	--	SIM2 power supply input: 3V/1.8V	--
USIM2_RST	A34	DO	PD	SIM2 reset signal	--
USIM2_DATA	A46	DIO	PD	SIM2 data signal	--
USIM2_CLK	A47	DO	PD	SIM2 clock signal	--
USIM2_DET	A33	DI	PD	SIM2 detect signal	--
PCIe					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
PCIe_CLKREQ	B35	DIO	PU	PCIe clock request signal	--
PCIe_WAKE	B7	DIO	PU	PCIe wakeup signal	--
PCIe_RESET	B6	DIO	PD	PCIe reset signal	--
PCIe_REFCLK_P	B3	AIO	--	PCIe reference clock (+)	--
PCIe_REFCLK_M	B20	AIO	--	PCIe reference clock (-)	--
PCIe_TX0_P	B4	AO	--	PCIe data TX channel 0 signal (+)	--
PCIe_TX0_M	B21	AO	--	PCIe data TX channel 0 signal (-)	--
PCIe_TX1_P	B5	AO	--	PCIe data TX channel 1 signal (+)	--
PCIe_TX1_M	B22	AO	--	PCIe data TX channel 1 signal (-)	--
PCIe_RX0_P	B2	AI	--	PCIe data RX channel 0 signal(+)	--
PCIe_RX0_M	B19	AI	--	PCIe data RX channel 0 signal (-)	--
PCIe_RX1_P	B1	AI	--	PCIe data RX channel 1 signal(+)	--
PCIe_RX1_M	B18	AI	--	PCIe data RX channel 1 signal (-)	--
Bluetooth and Wi-Fi					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
WL_SW_CTRL	B49	DO	PD	Wi-Fi control signal	--

WL_PWR_CTRL1	B48	DO	PD	WLAN power control signal 1	--
WL_PWR_CTRL2	B47	DO	PD	WLAN power control signal 2	--
WL_RF_CLK3_WL	B34	AO	--	WLAN clock signal	--
RF_COEX_UART_TX	B24	DO	PD	RF_COEX_UART_TX	LTE/WLAN co-existence signal
RF_COEX_UART_RX	B23	DI	PD	RF_COEX_UART_RX	
WLAN_EN	B8	DO	PD	WLAN enable signal	--
WL_SLEEP_CLK	B33	AO	--	WLAN sleep clock	--
BT_EN	B46	DO	PD	Bluetooth enable signal, which can be configured as ADC	--
BT_INT_N/GPIO_93	B36	DI	PD	Bluetooth interrupt signal	Alternatively used to enable V2X_5V
BT_UART_RX/GPIO_64	B37	DI	PD	BT_UART RX signal	BT_UART_Reserved, alternatively used for normal GPIO function
BT_UART_TX/GPIO_63	B38	DO	PD	BT_UART TX signal	
BT_UART_RTS/GPIO_66	B40	DI	PD	BT_UART TX request signal	
BT_UART_CTS/GPIO65	B39	DI	PD	BT_UART RX ready signal	
Module Control					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
PWR_KEY	B55	DI	PU	Module button power control signal	The default voltage is 1.1 V upon power-on.
RESET_N	B56	DI	PU	Module reset control signal	--
USB_BOOT	C33	DI	--	Forced into USB download boot mode	Connect to VDD_EXT_1V8 pin, pull up to 1V8.
FASTBOOT	C11	DI	PD	Forced into fastboot mode	Connect to VDD_EXT_1V8 pin, pull up to 1V8.
PMX_GPIO					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
PMX_GPIO_03	B50	DIO	--	PMX_GPIO_03	--
PMX_GPIO_11	B51	DIO	--	PMX_GPIO_11, which can be configured as ADC	--
USB					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
USB_VBUS	B12	DI	--	USB VBUS insertion detection	--
USB_HS_DM	B27	AIO	--	USB high-speed differential signal (-)	--
USB_HS_DP	B11	AIO	--	USB high-speed differential signal (+)	--
USB_ID	B28	DI	PD	USB_ID	--
USB_SS_RX_M	B25	AI	--	USB super-speed receiver (-)	--
USB_SS_RX_P	B9	AI	--	USB super-speed receiver (+)	--
USB_SS_TX_M	B26	AO	--	USB super-speed transmitter (-)	--

USB_SS_TX_P	B10	AO	--	USB super-speed transmitter (+)	--
SDIO					
Pin Name	Pin No.	I/O	Reset Value	Pin Description	Remarks
SDC_RESET	B42	DO	PD	SD/EMMC reset signal	--
SDC_PWR_EN	B29	DO	PD	SD/EMMC power enable signal	--
SDC_PWR	B13	PI	--	SDC interface power input	1.8 V/2.95 V (I_{PK}: 10 mA)
SDC_CMD	B44	DIO	PD	SDC interface command signal	--
SDC_CLK	B45	DO	Hi-Z	SDC interface clock signal	--
SDC_DATA0	B14	DIO	PD	SDC interface DATA0 signal	--
SDC_DATA1	B15	DIO	PD	SDC interface DATA1 signal	--
SDC_DATA2	B16	DIO	PD	SDC interface DATA2 signal	--
SDC_DATA3	B17	DIO	PD	SDC interface DATA3 signal	--
SDC_DATA4	B30	DIO	PD	SDC interface DATA4 signal	--
SDC_DATA5	B31	DIO	PD	SDC interface DATA5 signal	--
SDC_DATA6	B32	DIO	PD	SDC interface DATA6 signal	--
SDC_DATA7	B43	DIO	PD	SDC interface DATA7 signal	--
UART					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
BLSP1_UART_TX	C5	DO	PD	UART TX signal	--
BLSP1_UART_RX	C6	DI	PD	UART RX signal	--
BLSP1_UART_CTS	C21	DI	PD	UART ready to RX signal	--
BLSP1_UART_RTS	C22	DO	PD	UART request TX signal	--
SPI					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
BLSP1_SPI_MISO	C23	DO	PD	SPI1 interface input signal	This set of SPI interfaces are used for communicating with the external MCU.
BLSP1_SPI_MOSI	C24	DI	PD	SPI1 interface output signal	
BLSP1_SPI_CLK	C7	DIO	PD	SPI1 interface clock signal	
BLSP1_SPI_CS_N	C8	DIO	PD	SPI1 interface chip select signal	
SPI_INT_OUT/GPIO_88	D48	DO	PD	SPI1 output interrupt signal (reserved)	
SPI_SLAVE_INT/GPIO_94	D36	DI	PD	SPI1 input interrupt signal (reserved)	

BLSP2_SPI_MISO	C49	DO	PD	SPI2 interface input signal	--
BLSP2_SPI_MOSI	C50	DI	PD	SPI2 interface output signal	--
BLSP2_SPI_CLK	C37	DIO	PD	SPI2 interface clock signal	--
BLSP2_SPI_CS_N	C38	DIO	PD	SPI2 interface chip select signal	--
CODEC					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
I2S_MCLK	C18	DO	PD	I^2S clock output signal	--
I2S_DIN	C19	DI	PD	I^2S data input signal	--
I2S_SCK	C1	DO	PD	I^2S data bit clock signal	--
I2S_DOUT	C3	DO	PD	I^2S data output signal	--
I2S_WS	C2	DO	PD	I^2S frame clock signal	--
CDC_RESET_N	C39	DO	PD	CODEC reset signal	--
PCM					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
PCM_CLK	C4	DO	PD	Reserved for BT	--
PCM_DOUT	C34	DO	PD	Reserved for BT	--
PCM_DIN	C46	DI	PD	Reserved for BT	--
PCM_SYNC	C20	DO	PD	Reserved for BT	--
I^2C					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
BLSP3_I2C_SDA	C35	DIO	PD	BLSP3_I2C_SDA	--
BLSP3_I2C_SCL	C36	DO	PD	BLSP3_I2C_SCL	
IMU_I2C_SDA	C47	DIO	PD	IMU_I2C data	--
IMU _I2C_SCL	C48	DO	PD	I^2C clock	
IMU _INT1	C40	DI	PD	IMU interrupt pin	--
IMU _INT2	C41	DI	PD	IMU interrupt pin	--
Control					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
WAKEUP_IN	C9	DI	PD	WAKEUP input signal	1.8 V level domain, configurable by software
WAKEUP_OUT	C10	DO	PD	WAKEUP output signal	1.8 V level domain, defined by customer
SUSPEND_STATUS	D34	DO	PD	Module suspend indication pin	L: The module is in suspended mode; H: The module is awakened.
STATUS	D49	DO	PD	Module boot indication pin	H: The module enters the Linux system.
DBG_UART_TX	C28	DO	PD	Debug UART output signal	--
DBG_UART_RX	C12	DI	PD	Debug UART input signal	--
EMAC_PPS0_OUT/Reserved	C25	DO	PD	EMAC_PPS0_OUT	Reserved
EMAC_PPS1_OUT/Reserved	C26	DO	PD	EMAC_PPS1_OUT	Reserved
NAV_DR_SYNC	C27	DO	PD	GPS 1PPS	--

JTAG					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
JTAG_TCK	C42	DI	PU	JTAG debugging interface, reserved	--
JTAG_TDO	C43	DO	Hi-Z	JTAG debugging interface, reserved	--
JTAG_TRST_N	C44	DI	PD	JTAG debugging interface, reserved	--
JTAG_PS_HOLD	C45	DI	Hi-Z	JTAG debugging interface, reserved	--
JTAG_TDI	C54	DI	PU	JTAG debugging interface, reserved	--
JTAG_TMS	C55	DI	PU	JTAG debugging interface, reserved	--
JTAG_SRST_N	C56	DI	PU	JTAG debugging interface, reserved	--
GPIO					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
GPIO_33	D33	DIO	PD	General GPIO	GPIO
GPIO_87	D35	DIO	PD	General GPIO	GPIO
GPIO_104	D37	DIO	PD	General GPIO, support wakeup	GPIO
GPIO_105	D50	DIO	PD	General GPIO	GPIO
GPIO_107	D38	DIO	PD	General GPIO	GPIO
GNSS_ELNA_EN					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
GNSS_ELNA_EN0	D45	DIO	PD	Reserved	--
GNSS_ELNA_EN1	D56	DIO	PD	Reserved	--
ANT Tuner Control					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
RFFE0_DATA	D54	DIO	PD	External Tuner MIPI control data pin	--
RFFE0_CLK	D42	DO	PD	External Tuner MIPI control clock pin	--
RFFE1_DATA	D53	DIO	PD	External Tuner MIPI control data pin	--
RFFE1_CLK	D41	DO	PD	External Tuner MIPI control clock pin	--
RFFE2_DATA	D52	DIO	PD	External Tuner MIPI control data pin	--
RFFE2_CLK	D40	DO	PD	External Tuner MIPI control clock pin	--
ANT					
Pin Name	**Pin No.**	**I/O**	**Reset Value**	**Pin Description**	**Remarks**
ANT-MAIN	C17	I/O	--	PRX (MIMO1)	--
ANT-DRX/AUX	D2	I/O	--	DRX (MIMO2)	--
ANT-MIMO3	D14	I/O	--	PRX (MIMO3)	--
ANT-MIMO4	D17	AI	--	DRX (MIMO4)	--

ANT-V2X	A4	I/O	--	CV2X TX, PRX	--
ANT-V2X	A1	I/O	--	CV2X TXD, DRX	--
ANT-GNSS	C14	AI	--	GNSS L1	--
ANT	D5	--	--	NC	--
ANT	D8	--	--	NC	--
ANT	D11	--	--	NC	--
RESERVED					
Pin Name	**Pin No.**				**Remarks**
RESERVED	A54, A55, A60, A61, B52, B53, B59 - B63, C52, C53, C59-C63, D39, D43, D44, D51, D55, D59-D63				Reserved, NC
GND					
Pin Name	**Pin No.**				**Remarks**
GND	A2, A3, A5, A10, A18-A21, A26, A40, A52, A57-A59, A62-A65, B41, B54, B57, B58, B64, B65, C13, C15-C16, C29-C32, C51, C57, C58, C64, C65, D1, D3, D4, D6, D7, D9, D10, D12, D13, D15, D16, D18-D32, D57, D58, D64, D65, E1-E16, F1-F81				GND

3.2 Power Supply

The power supply range of the AN958 module is 3.4–4.2 V, and the recommended value is 3.8 V. The stable power output capability is not lower than 3 A. The performance of the power supply, such as the load capacity and ripple , etc., will directly affect the performance and stability of the module.

3.2.1 Power Supply

The AN958 module provides power through the VPH_PWR pin.

Table 3-3 Power interfaces of the module

Pin Name	I/O	Pin No.	Description
VPH_PWR	I	A7, A8, A23, A24	Module power supply by VBAT_BB/VBAT_RF, 3.4–4.2 V, typical value of 3.8 V
V2X_5V	I	A37, A38	Power supply by external V2X PA, 4.75–5.25 V, typical value of 5.0 V
VREG_L6E_1P8	O	A9	Module digital level, 1.8 V output, Imax < 50 mA
GND	--	--	Grounding. All GND pins must be grounded.

Table 3-4 Module power supply parameters

Parameter	Minimum Value	Recommended Value	Maximum Value	Unit
VPH_PWR	3.4	3.8	4.2	V
V2X_5V	4.75	5	5.25	V

Power design is shown as follows:

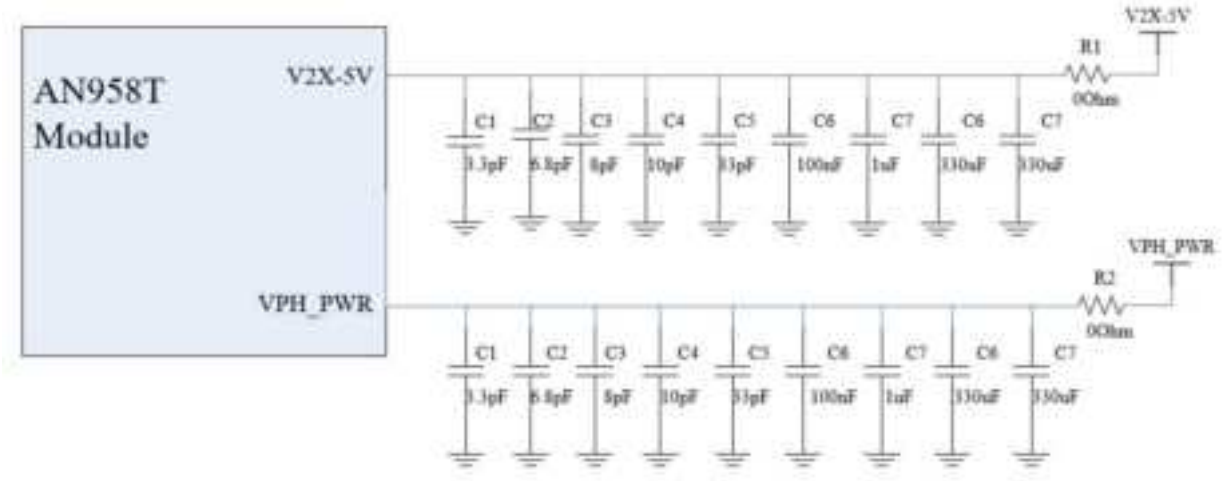

Figure 3-2 Power supply design

Warning

1. V2X_5V is used on AN958T series modules. It does not need to be connected on AN958-NA module.

The following table describes the filter capacitor design of power supply.

Table 3-5 Power supply filter capacitor design

Recommended Capacitor	Application	Description
330 uF x 2	Regulating capacitor	To reduce power fluctuations during module operation, low ESR capacitors are required. LDO or DCDC power supply requires a capacitor of no less than 680 uF. Battery power supply requires a capacitor of 100 uF to 330 uF.
1 uF, 100 nF	Digital signal noise	Filter out interference caused by clock and digital signals.
39 pF, 33 pF	700, 850/900 MHz band	Filter out the RF interference in low bands.
3.3 pF, 6.8 pF, 8 pF, 10 pF	1500/1700/1800/1900, 2100/2300, 2500/2600 MHz, 3500/3700 MHz, 5GHz frequency bands	Filter out the RF interference in medium and high-frequency bands.

The following figure shows the power voltage drop example.

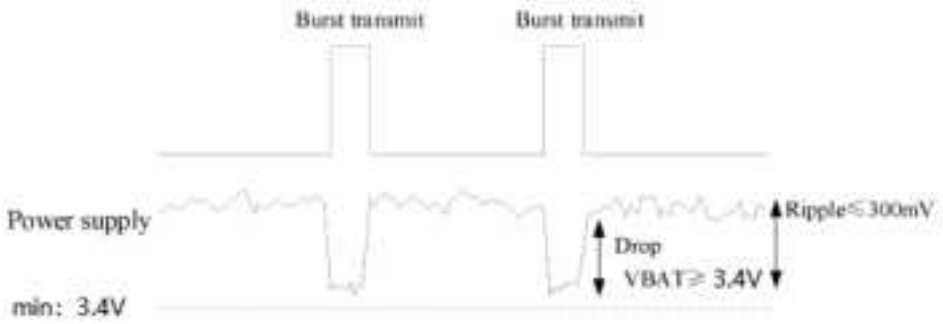

Figure 3-3 Power voltage drop example

To ensure that the power voltage is not less than 3.4V, it is recommended to connect two low ESR 330 uF tantalum

capacitors and 1 uF, 100 nF, 39 pF, and 33 pF filter capacitors in parallel connection near the power input of the module. It is recommended that the PCB wiring of the power supply be as short as possible and be as wide as possible. This aims to reduce the equivalent impedance of the power wire and ensure that no large voltage drops occur at high currents at maximum transmit power.

3.2.2 Power Output

The AN958 module has one reference power output used to pull up peripheral circuit; two SIM card power supplies are used to drive dual SIM cards.

Table 3-6 Power supply description

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VDD_EXT_1V8	--	1.8	50
USIM1_PWR	1.75 - 3.337	1.8/3	150
USIM2_PWR	1.75 - 3.337	1.8/3	150

3.2.3 Power Consumption

Table 3-7 Power consumption of the AN958-NA module

TBD

4 Antenna Interface

The AN958 module supports the 5-antenna scheme, of which 4 antennas are cell antennas and 1 antenna is a GNSS antenna. These antannas work at different frequency bands and frequency ranges.

The information of each antenna is describes as follows.

4.1 Cell Antenna Interface Configuration

The AN958-NA module provides four cell antenna interfaces. The antenna interfaces are defined in the following table.

Table 4-1 AN958-NA antenna interface definition

Antenna Interface	Pin	Description	Band	Frequency Range (MHz)
MAIN	C17	Main antenna interface	2/3/4/5G TX and RX	617–960 MHz 1427–2690 MHz 3300–5000 MHz
DRX/AUX	D2	MIMO2 antenna interface	3/4/5G diversity RX	617–960 MHz 1427–2690 MHz 3300–5000 MHz
MIMO3	D14	MIMO3 antenna interface	3/4/5G MIMO main RX	1427–2690 MHz 3300–5000 MHz
MIMO4	D17	MIMO4 antenna interface	3/4/5G MIMO diversity RX	1427–2690 MHz 3300–5000 MHz

4.1.1 Operating Bands

Table 4-1 Operating band and frequency range of AN958-NA

Band	Tx	Rx	Unit
GSM850	824 - 849	869 - 894	MHz
EGSM900	880 - 915	925 - 960	MHz
PCS1900	1850 - 1910	1930 - 1990	MHz
WCDMA B2	1850 - 1910	1930 - 1990	MHz
WCDMA B4	1710 - 1755	2110 - 2155	MHz
WCDMA B5	824 - 849	869 - 894	MHz
LTE-FDD B2	1850 - 1910	1930 - 1990	MHz
LTE-FDD B4	1710 - 1755	2110 - 2155	MHz
LTE-FDD B5	824 - 849	869 - 894	MHz
LTE-FDD B7	2500 - 2570	2620 - 2690	MHz
LTE-FDD B12	699 - 716	729 - 746	MHz
LTE-FDD B14	788 - 798	758 - 768	MHz

Band	Tx	Rx	Unit
LTE-FDD B17	704 - 716	734 - 746	MHz
LTE-FDD B25	1850 - 1915	1930 - 1995	MHz
LTE-FDD B26	814 - 849	859 - 894	MHz
LTE-FDD B28	703 – 748	758 - 803	MHz
LTE-FDD B29	--	717 - 728	MHz
LTE-FDD B66	1710 - 1780	2110 - 2200	MHz
LTE-FDD B71	663 - 698	617 - 652	MHz
LTE-TDD B41	2496 - 2690	2496 - 2690	MHz
LTE-TDD B42	3400 - 3600	3400 - 3600	MHz
5G NR n2	1850 - 1910	1930 - 1990	MHz
5G NR n5	824 - 849	869 - 894	MHz
5G NR n7	2500 - 2570	2620 - 2690	MHz
5G NR n12	699 - 716	729 - 746	MHz
5G NR n14	788 - 798	758 - 768	MHz
5G NR n25	1850 - 1915	1930 - 1995	MHz
5G NR n28	703 - 748	758 - 803	MHz
5G NR n41	2496 - 2690	2496 - 2690	MHz
5G NR n48	3550 - 3700	3550 - 3700	MHz
5G NR n66	1710 - 1780	2110 - 2200	MHz
5G NR n71	663 - 698	617 - 652	MHz
5G NR n77	3300 - 4200	3300 - 4200	MHz
5G NR n78	3300 - 3800	3300 - 3800	MHz

4.1.2 Reference Circuit Design

To achieve better RF performance, reserve a π-type matching circuit and place matching components as close to the antennas as possible. To improve the RX sensitivity, ensure that the isolation between the antennas is appropriate. The following figure shows the reference circuit for antenna connection.

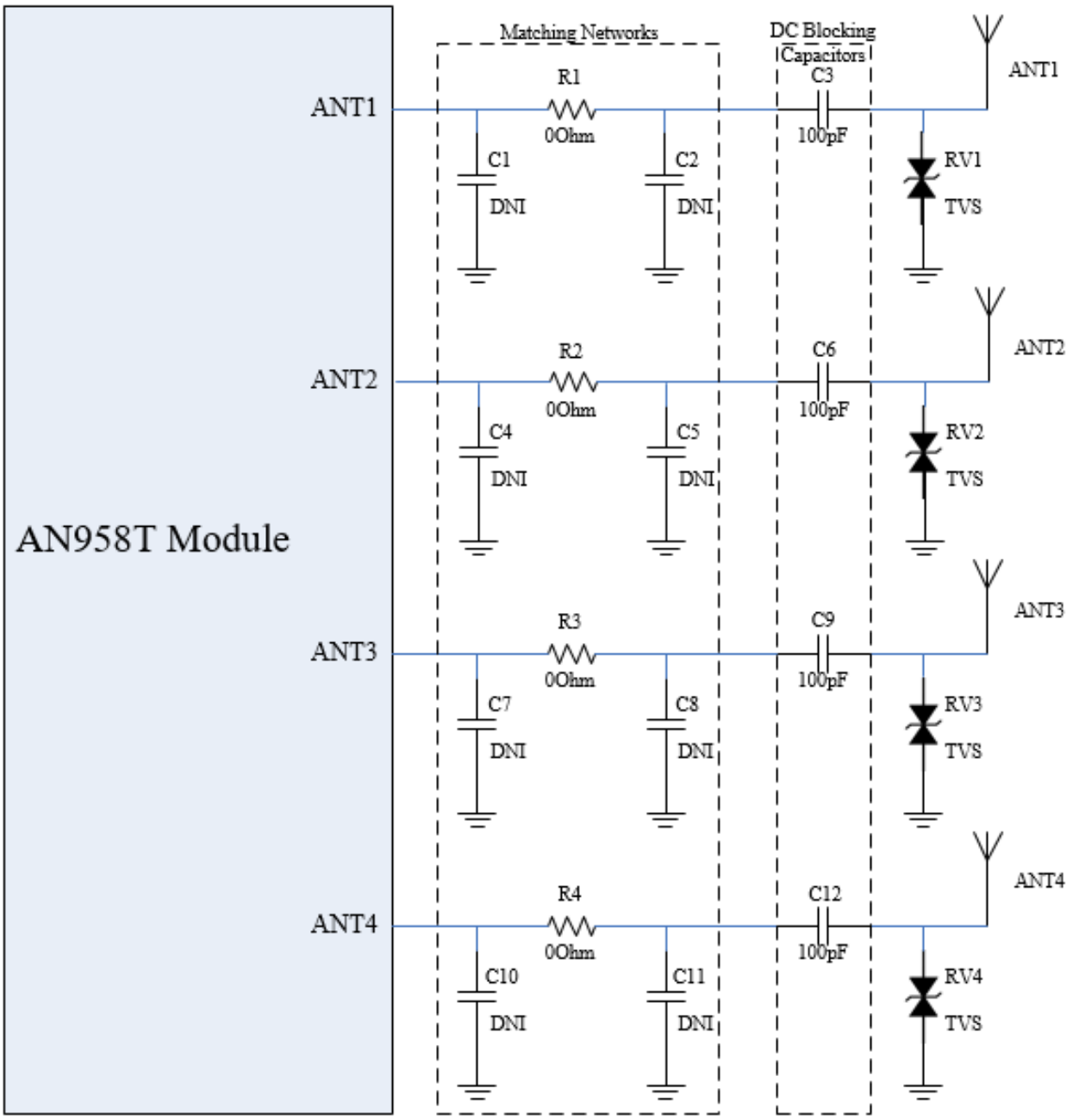

Figure 4-1 Reference circuit for antenna connection

4.2 GNSS Antenna Interface

This section describes GNSS related information. The module have not GPS internal LNA . The active antenna is recommended.

Table 4-1 GNSS antenna interface definition

Pin Name	Pin	Description	Frequency Range (MHz)	Remarks
ANT_GNSS	C14	GPS L1	L1 (1565-1610MHz)	--

4.2.1 Operating Bands

Table 4-2 GNSS operating bands

Mode	Center Frequency	Frequency Range	Unit
GPS L1	Center frequency (FC) = 1575.42	1574.4 - 1576.4	MHz
GLONASS G1	Center frequency (FC) = 1601.7	1597.5 - 1605.9	MHz
BeiDou B1	Center frequency (FC) = 1561	1559.1 - 1563.1	MHz
Galileo E1	Center frequency (FC) = 1575.42	1573.4 - 1577.5	MHz

4.2.2 Reference Circuit Design

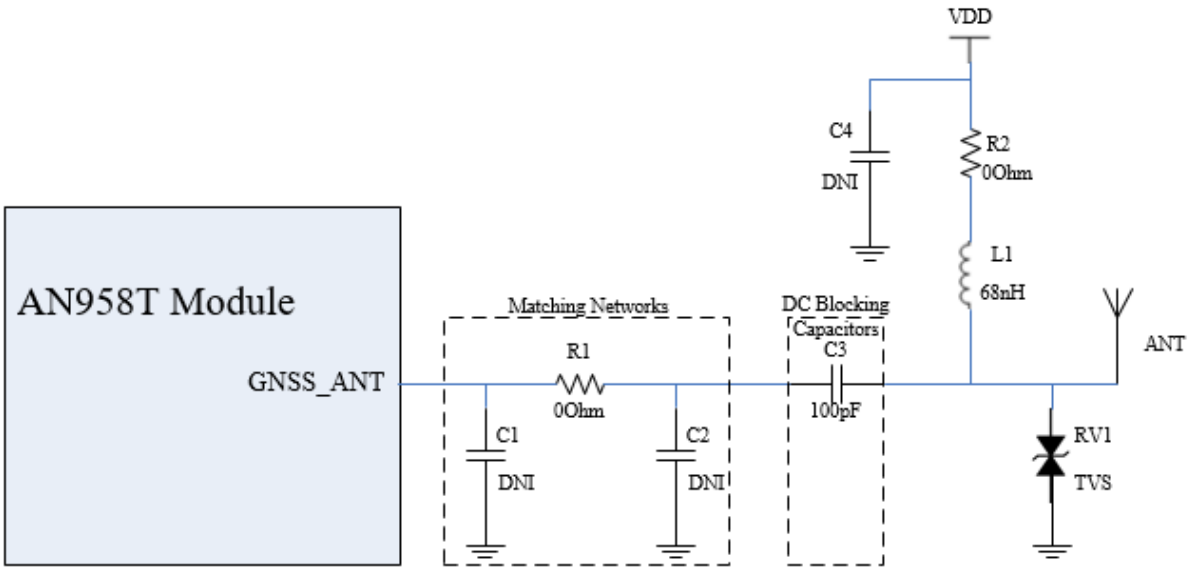

Figure 4-2 Reference circuit for GNSS antenna connectionAntenna RF Signal Cable Layout Requirements

4.2.3 Reference Layout of RF Signal Cable

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

1. The distance between the RF signal pin and the RF connector should be as short as possible.
2. When wiring RF cables, avoid right-angle wiring at the turning part, and use circular arc processing. The antenna led from RF module should be made into a microstrip line.
3. RF ground should be designed properly. The reference ground plane of the RF signal cable should be kept intact; adding a certain amount of ground vias around the signal and the reference ground can improve the RF performance; the distance between the ground via and the signal cable should be at least 2 times the cable width (2*W).
4. Precise 50 Ω impedance control of RF signal cables is required during PCB fabrication.

4.3 Antenna Requirements

AN958-NA module provides 6 RF transceiver antennas and 1 GNSS antenna interface. The antenna requirements are as follows:

Table 4-3 Antenna requirements

Antenna requirements of the AN958-NA module	
System	**Antenna Requirements**
GSM/WCDMA/LTE/NR	VSWR ≤ 2:1 Max input power (W): 2 Input impedance (Ω): 50 Antenna isolation belt (dB): > 25
GNSS (active antenna recommended)	Frequency range: L1: 1559 MHz to 1607 MHZ VSWR < 2:1 Built-in LNA Gain < 20 dB Antenna Gain > -2 dBi Total Gain < 18 dB

5 Other interfaces

5.1 Control Interface

Control signals are used to power on/off the module, reset the module, and set the Flight mode. The following table describes the pin definition.

Table 5-1 Control signals

Pin Name	I/O	Pin No.	Description
RESET_N	I	B56	When the module is operating, pull down the RESET_N pin for 700 ms-1s, and then pull up to reset the module.
PWRKEY	I	B55	In the power-off state, pull down the PWRKEY pin for 100 ms to 2s, and then pull it up to start up the module. In the power-on state, pull down the PWRKEY pin for 3s to 8s, and then pull it up to shut down the module.

5.1.1 Power-On/Off

5.1.1.1 Power-On

When the module is in power-off mode, pull down the PWRKEY for 100 ms to 2s to boot the module. It is recommended to use OC/OD driver circuit to control the PWRKEY pin. The OC drive reference circuit is shown as follows:

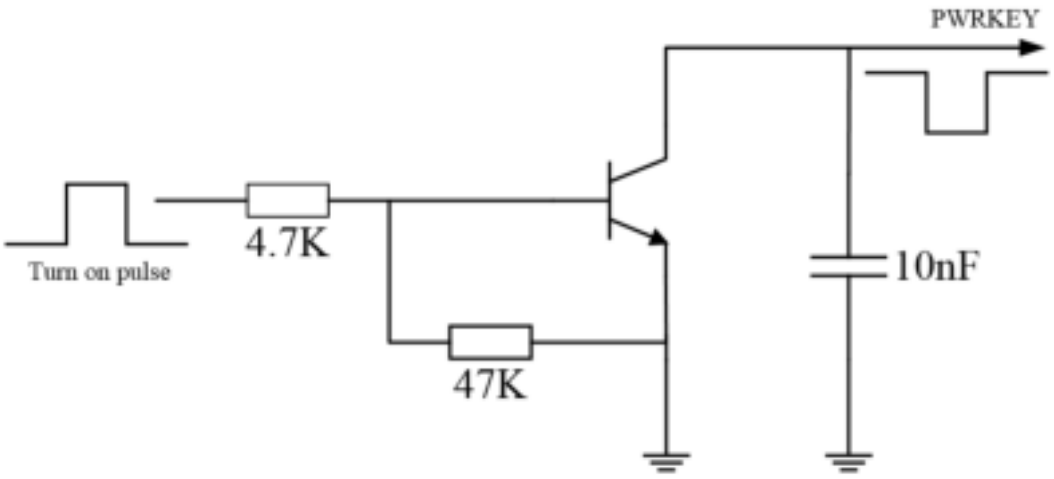

Figure 5-1 OC drive power-on reference circuit

Another way to control the PWRKEY pin is directly using a button switch. A TVS (ESD9X5VL-2/TR recommended) should be placed near the button for ESD protection in this way. The reference circuit is shown in Figure 5-2.

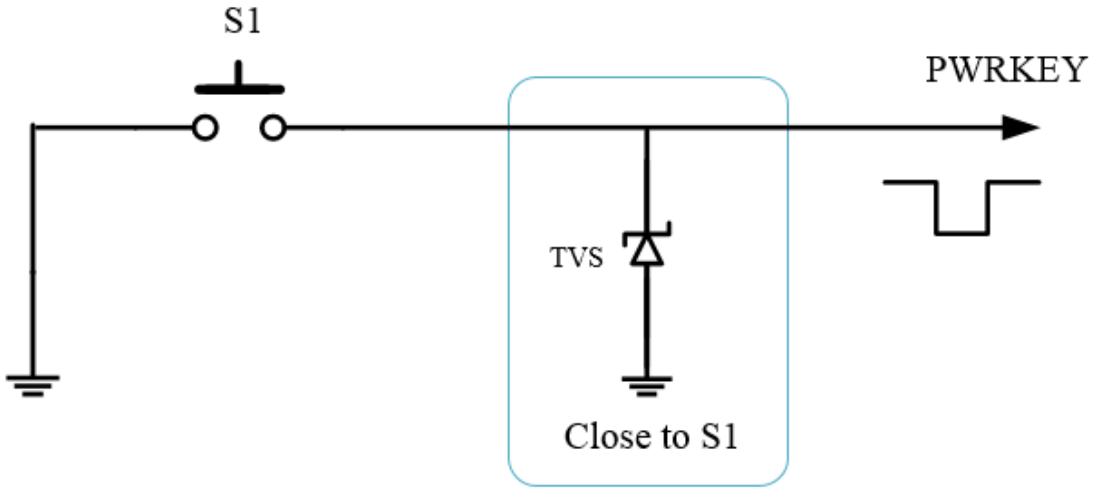

Figure 5-2 Button power-on reference circuit

The following figure shows the power-on timing sequence.

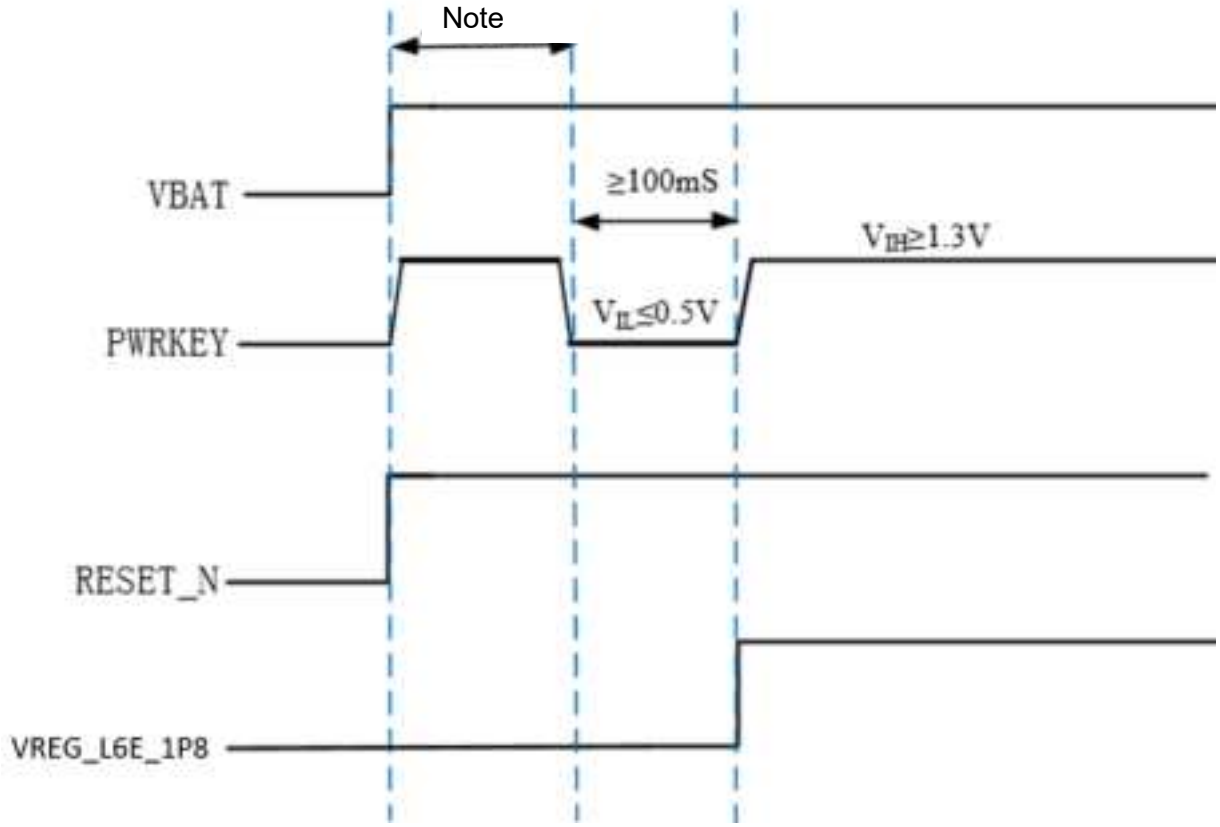

Figure 5-3 Power-on timing sequence

Note

1. Before pulling down the PWRKEY pin, make sure that the VBAT voltage is stable. It is recommended to control the interval from power-up of VBAT to pull-down of PWRKEY pin no less than 30 ms.

5.1.1.2 Power-Off

Table 5-2 Power-off modes supported by the module

Power-off Mode	Power-off Method	Applicable Scenario
Low-voltage power-off	When VBAT voltage is too low or power-down occurs, the module will power off.	The module does not log out from the base station.
Hardware	Pull down the PWRKEY pin for 3s to 8s.	Normal power-off

Note

1. When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal Flash. It is strongly recommended to power off the module by the PWRKEY pin or AT command before cutting off the power supply.
2. When using the AT command to power off the module, ensure that the PWRKEY pin is always at the high level after the power-off command is executed. Otherwise, the module will automatically power on again.

The following figure shows the power-off timing sequence.

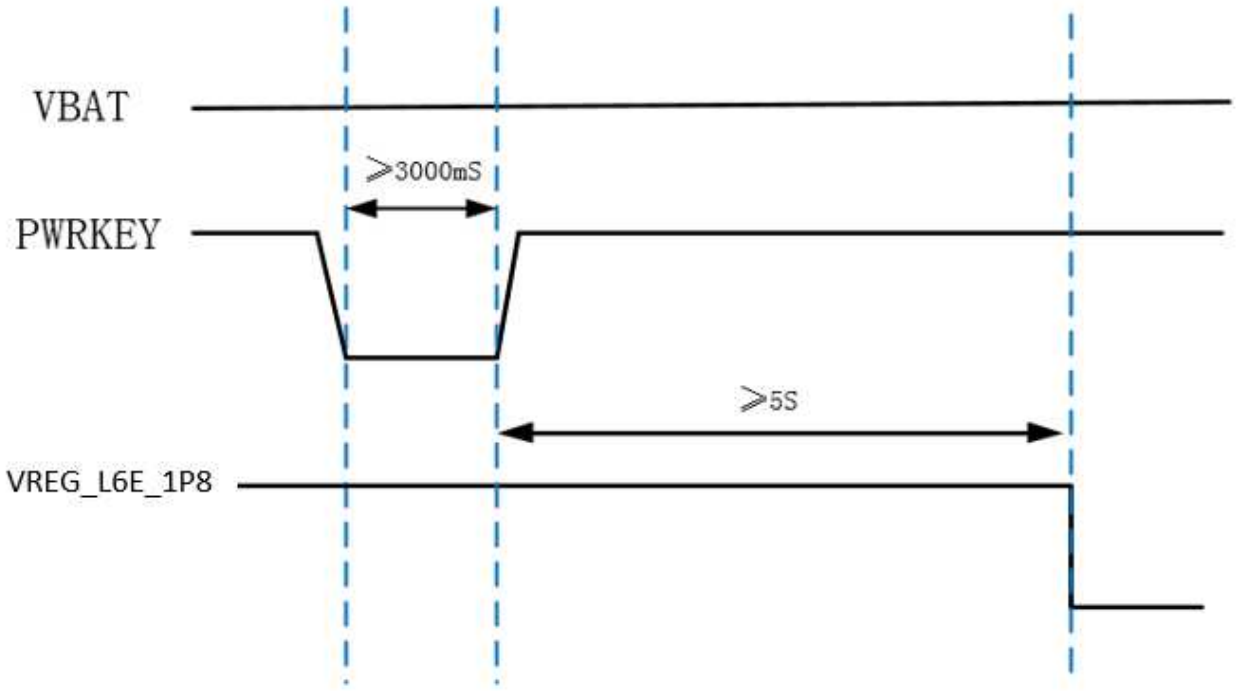

Figure 5-4 Power-off timing sequence

5.1.2 Reset

Table 5-3 Reset modes supported by the module

Reset Mode	Reset Method
Hardware reset	Pull down the RESET_N pin for 700 ms to 1s, and then pull it up to reset the module.
Software reset	Send the AT command **AT+RESET** to reset module.

Clients can control the RESET_N pin by OC/OD driver circuits and button switch.

Figure 5-5 and Figure 5-6 show the reference circuits respectively.

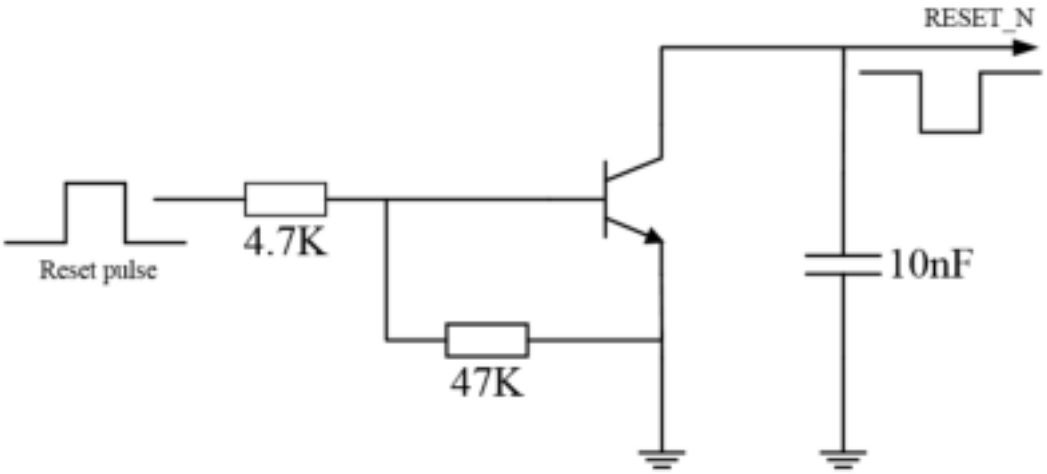

Figure 5-5 OC driver reset reference circuit

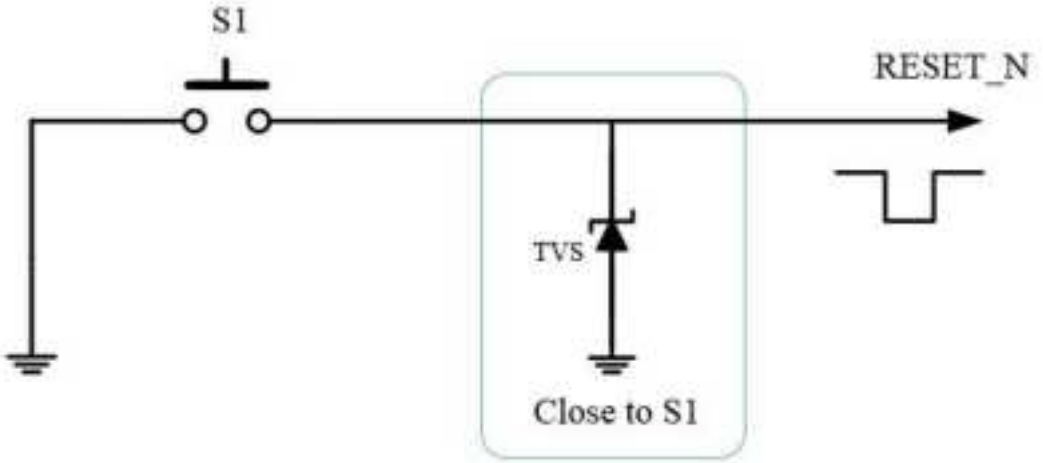

Figure 5-6 Button reset reference circuit

The following figure shows the RESET_N timing sequence.

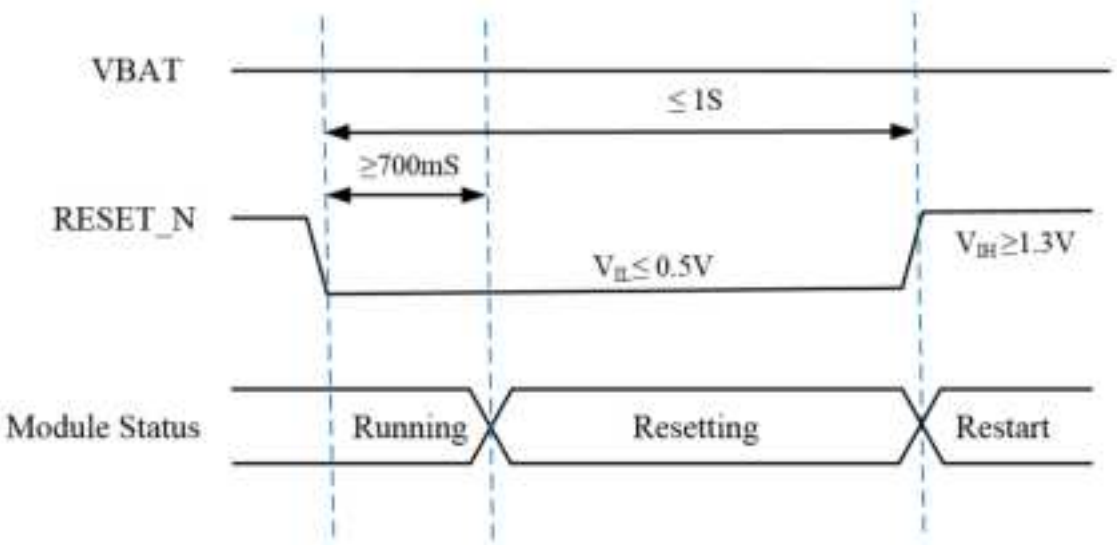

Figure 5-7 RESET_N reset timing sequence

5.2 (U)SIM Card Interface

The module has a built-in (U)SIM card interface, and supports 1.8 V and 3.0 V (U)SIM card.

5.2.1 (U)SIM Pin Definition

Table 5-4 (U)SIM pin definition

Pin Name	I/O	Pin No.	Description
USIM1_PRESENCE	I	A49	(U)SIM1 hot plug detect
USIM1_VDD	O	A6	(U)SIM1 power supply
USIM1_DATA	IO	A36	(U)SIM1 data signal
USIM1_CLK	O	A48	(U)SIM1 clock signal
USIM1_RESET	O	A22	(U)SIM1 reset signal
USIM2_PRESENCE	I	A33	(U)SIM2 hot plug detect
USIM2_VDD	O	A35	(U)SIM2 power supply
USIM2_DATA	IO	A46	(U)SIM2 data signal
USIM2_CLK	O	A47	(U)SIM1 clock signal
USIM2_RESET	O	A34	(U)SIM2 reset signal

5.2.2 (U)SIM Interface Circuit

5.2.2.1 (U)SIM Card Connector with Card Detection Signal

During (U)SIM design, you must select a (U)SIM card connector. A hot plug card connector (recommended wireless model: SIM016-8P-220P) with (U)SIM card detection function is recommended.

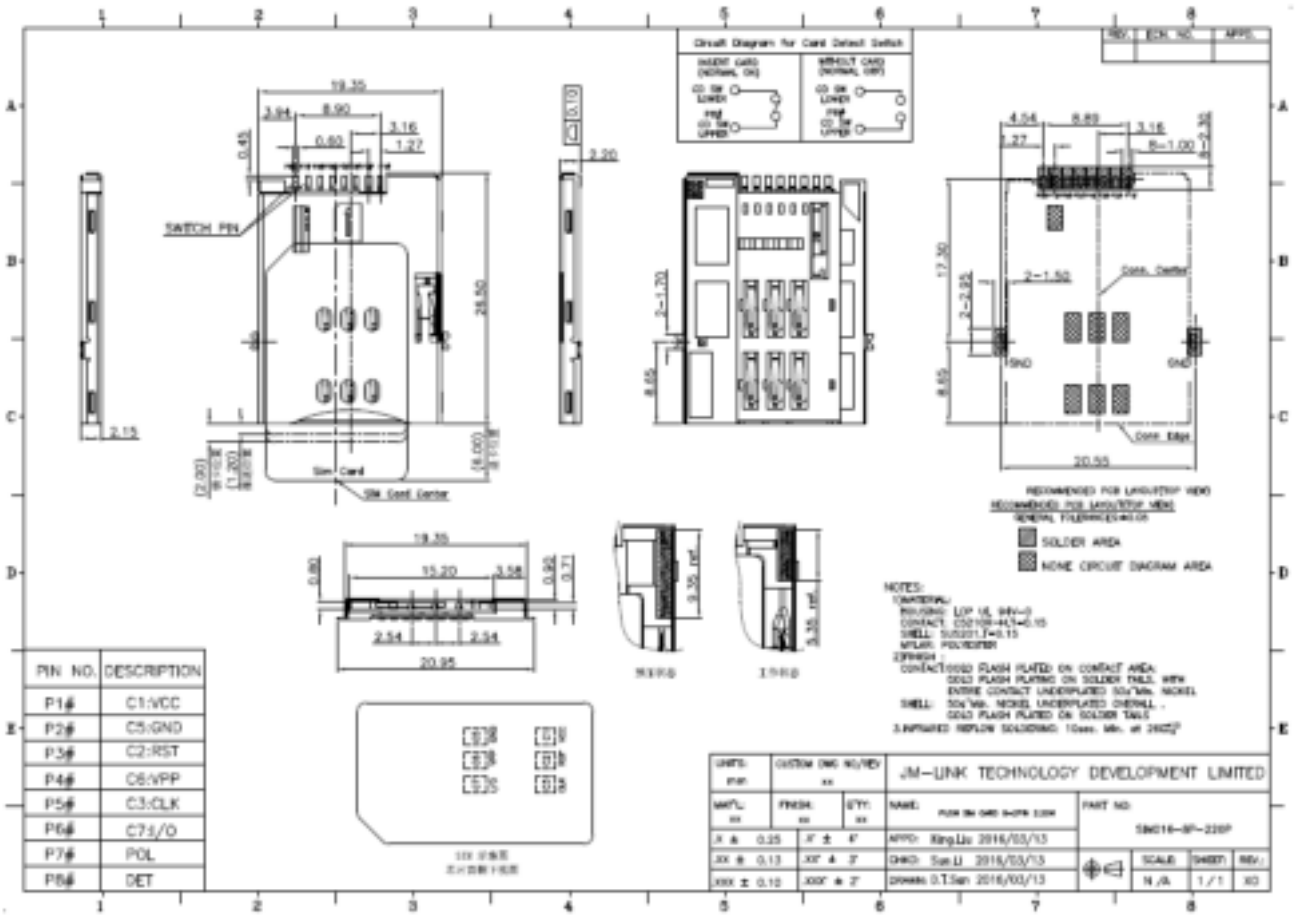

Figure 5-8 (U)SIM card connector (SIM016-8P-220P)

The principle of (U)SIM card connector with card detection signal is explained as follows:

When the (U)SIM card is inserted, USIM_PRESENCE pin is at a high level.

When the (U)SIM card is removed, USIM_PRESENCE pin is at a low level.

The following figure shows the reference circuit design of (U)SIM card connector with card detection signal.

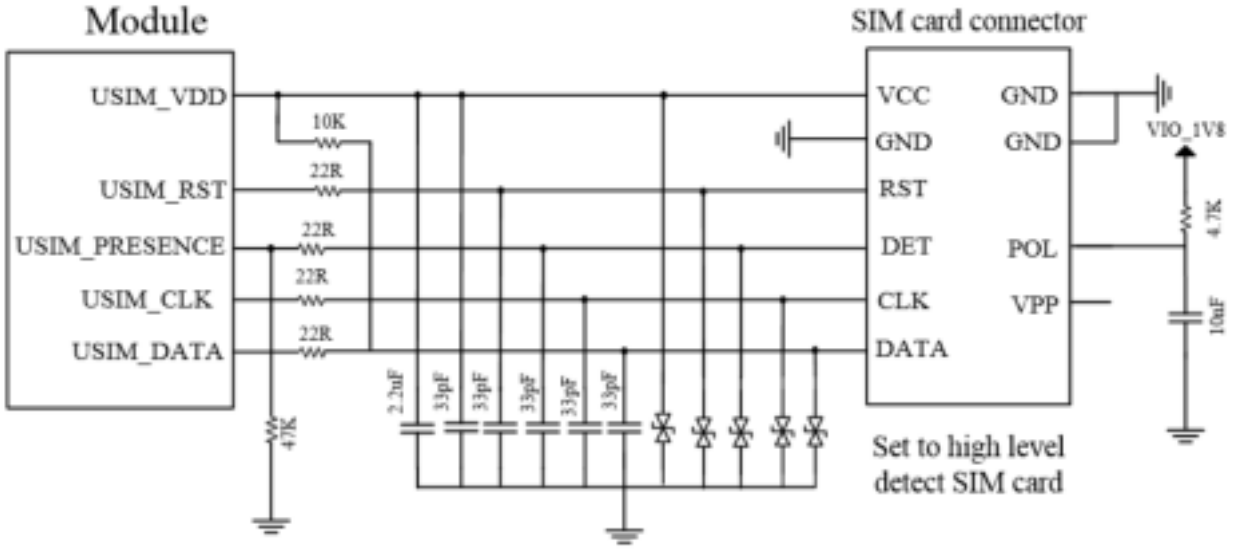

Figure 5-9 Reference circuit design of a (U)SIM card connector with card detection signals

5.2.2.2 (U)SIM Card Connector Without Card Detection Signals

When you use an (U)SIM card connector without detection signals, USIM_PRESENCE pin must be disconnected. The following figure shows the reference circuit.

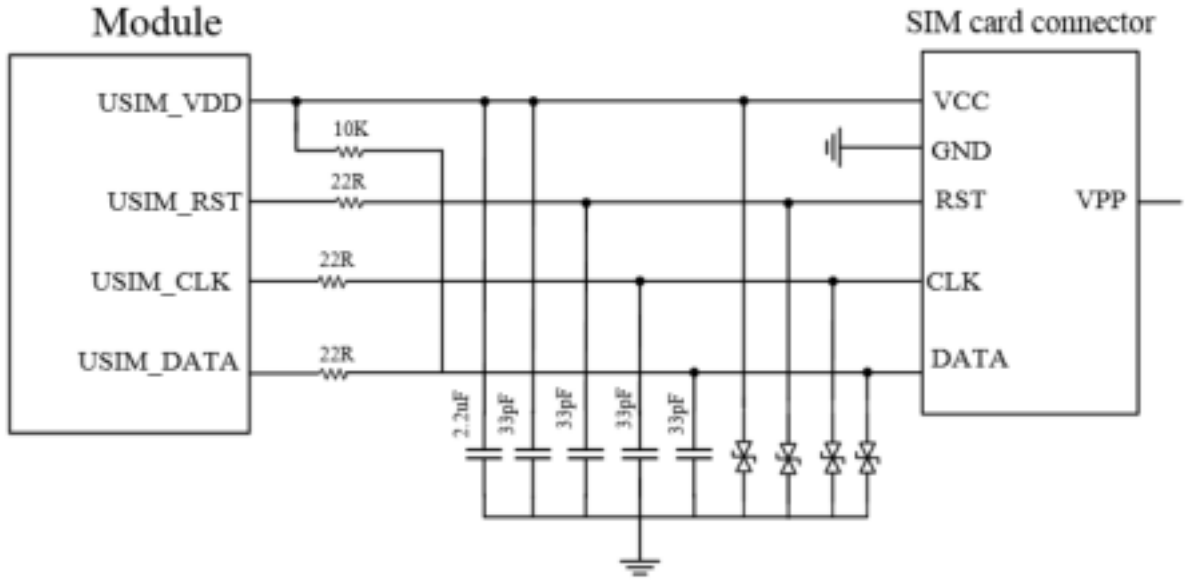

Figure 5-10 (U)SIM card connector without card detection signals

5.2.3 (U)SIM Hot Plug

The module supports (U)SIM card hot plug function, and determines whether the (U)SIM card is inserted or removed by detecting the pin status of USIM_PRESENCE.

5.2.4 (U)SIM Design Requirements

(U)SIM circuit design must meet EMC standards and ESD requirements, and at the same time, interference immunity capability must be improved to ensure that the SIM can work stably. The following principles must be strictly followed in the design:

- (U)SIM card connector should be laid as close to the module as possible, and kept away from the RF antenna, DCDC power, clock signal cables and other strong interference sources.
- (U)SIM card connector is covered by metal shield shell to improve interference immunity;
- The wiring length from the module to the (U)SIM card connector should not exceed 100mm. Longer wire will reduce signal quality;
- USIM_CLK and USIM_DATA signal wire should be surrounded by ground wire to aviod the interference. If it is difficult to do so, at least (U)SIM cardmust be surrounded by ground wire.
- The filter capacitor and ESD device of the (U)SIM card signal cable must be placed near the (U)SIM card connector. The equivalent capacitance of the ESD device must be 22 pF to 33 pF.
- . The connection between USIM_DATA and USM_VDD needs a 10K pull-up resistor

5.3 USB interface

The module supports USB 2.0/USB 3.0. For USB bus timing sequence and electrical specifications, see *Universal Serial Bus Specification 2.0* and *Universal Serial Bus Specification 3.0*.

5.3.1 USB Interface Definition

Table 5-5 Definition of USB interface

Pin Name	I/O	Pin No.	Description
USB_DP	AIO	B11	USB HS differential data signal+
USB_DM	AIO	B27	USB HS differential data signal–
USB_VBUS	PI	B12	USB plug detection
USB_ID	IO	B28	USB_ID
USB_SS_TX_P	AIO	B10	USB SS TX differential data signal+
USB_SS_TX_M	AIO	B26	USB SS TX differential data signal-
USB_SS_RX_P	AIO	B9	USB SS RX differential data signal+
USB_SS_RX_M	AIO	B25	USB SS RX differential data signal-

For more information about the USB 2.0/USB3.0 specifications, please visit http://www.usb.org/home

Warning

1. Since the module supports USB 2.0/USB 3.0, the TVS tube equivalent capacitance on the USB_DM/DP, USB_SS_TX_P/M, and USB_SS_RX_P/M differential signal cables must be less than 1 pF, and a 0.5 pF TVS is recommended.
2. It is recommended to connect a 0 Ω resistor in series to each differential cable of USB_DM/DP, USB_SS_TX_P/M, and USB_SS_RX_P/M.
3. USB_DM/DP, USB_SS_TX_P/M and USB_SS_RX_P/M are high speed differential signal cables. The following rules should be followed strictly in PCB layout:
   - The differential signal cable impedance of USB_DM and USB_DP, USB_SS_TX_P and USB_SS_TX_M, as well as USB_SS_RX_P and USB_SS_RX_M should be controlled at 90 Ω.
   - USB_DM and USB_DP, USB_SS_TX_P and USB_SS_TX_M, as well as USB_SS_RX_P and USB_SS_RX_M signal cables are required to be equal in length and parallel to avoid right-angle routing.
   - USB_DM and USB_DP, USB_SS_TX_P and USB_SS_TX_M, as well as USB_SS_RX_P and USB_SS_RX_M signal cables are laid in the signal layer nearest to the ground, and be surrounded by ground wire.

5.4 UART Interface

5.4.1 UART Interface Definition

The module has two serial ports: Main serial port and debugging serial port. The main serial port supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 380400 bps, 460800 bps, and 921600 bps. The default baud rate is 115200 bps, used for data transmission and AT command transmission. The debugging serial interface supports baud rate of 115200 bps for FIBOCOM internal debugging.

Table 5-6 and Table 5-7 describe the pins of the main serial port and debugging serial port.

Table 5-6 Pin definition of the main serial port

Pin Name	I/O	Pin No.	Description
CTS	I	C21	Clear to send
RTS	O	C22	Require to send
TXD	O	C5	Module TX data
RXD	I	C6	Module RX data

Table 5-7 Pin definition of the debugging serial port

Pin Name	I/O	Pin No.	Description
DBG_RXD	I	C12	Module RX data
DBG_TXD	O	C28	Module TX data

5.4.2 UART Interface Application

The serial port level of the module is 1.8 V. If the level of the host system is 3.3 V or others, a level translator is needed between the module and the host. The following figure shows the design of reference circuit of the serial port level translation chip.

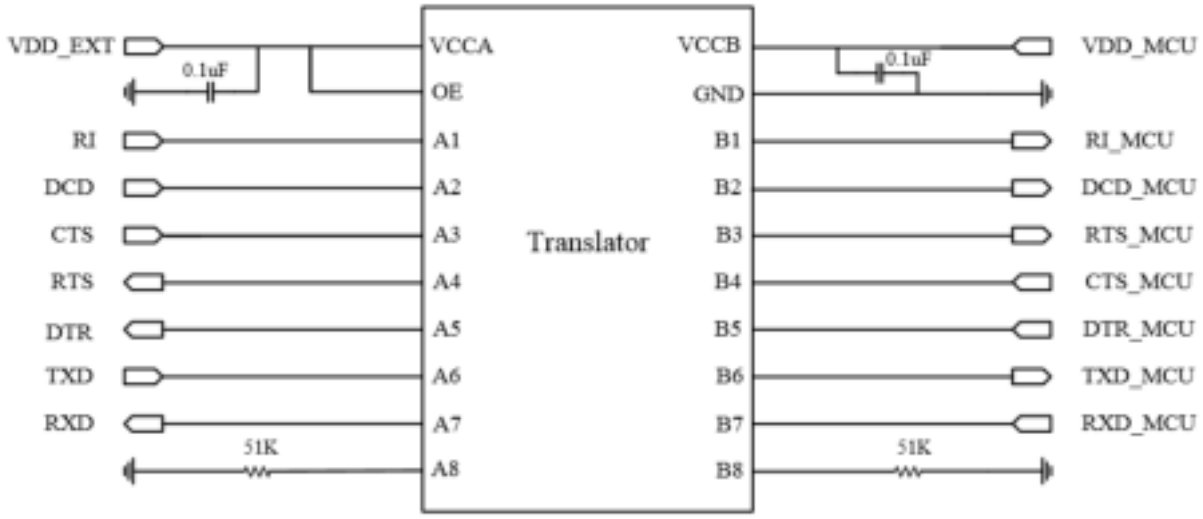

Figure 5-11 Reference circuit 1 for level translation

Figure 5-12 shows another level translation circuit. You can design the input and output circuit of the dashed line by referring to the solid line but pay attention to the connection direction.

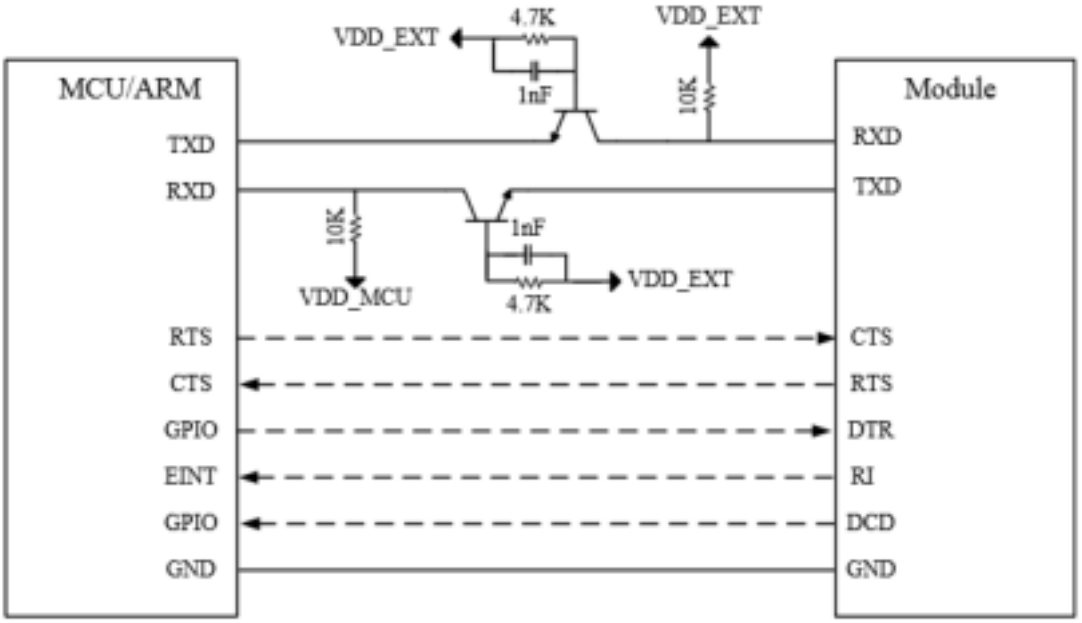

Figure 5-12 Reference circuit 2 for level translation

Warning

1. Level translation circuits cannot be used for serial ports whose baud rate exceeds 460 kbps.

5.5 ADC Interface

The module provides one analog-to-digital conversion interface. The ADC voltage range is 0.3 V to 1.875 V.

Table 5-8 Definition of ADC pin

Pin Name	I/O	Pin No.	Description
ADC1	I	A53	Analog-to-digital interface 1

Warning

1. It is recommended that ADC signal wires be surrounded by ground wire to improve ADC voltage measurement accuracy.
2. BT_EN/PMX_GPIO_11 can be extended to two ADCs.

5.6 Digital Audio

The module provides a digital audio interface (I^2S) for communication with external codec and other digital audio devices.

5.6.1 I2S Interface Definition

Table 5-9 Definition of I^2S interface

Pin Name	I/O	Pin No.	Description

I2S_MCLK	O	C18	I2S_MCLK
PRI_I2S_WS	I	C2	I2S word select
PRI_ I2S_DIN	IO	C19	I2S_DATA0
PRI_ I2S_DOUT	IO	C3	I2S_DATA1
PRI_I2S_SCK	IO	C1	I2S_CLK
CDC_RESET_N	DO	C39	CODEC reset signal (1.8 V level domain)

5.7 SDIO Interface

The module provides a set of SDIO interfaces that support the SD 3.0 protocol. The following table describes the SD card interface.

Table 5-10 Definition of SDIO interface

Pin Name	I/O	Pin No.	Description
SDC_DATA7/GPIO_101	IO	B43	SDIO bus DATA7
SDC_DATA6/GPIO_100	IO	B32	SDIO bus DATA6
SDC_DATA5/GPIO_99	IO	B31	SDIO bus DATA5
SDC_DATA4/GPIO_98	IO	B30	SDIO bus DATA4
SDC_DATA3	IO	B17	SDIO bus DATA3
SDC_DATA2	IO	B16	SDIO bus DATA2
SDC_DATA1	IO	B15	SDIO bus DATA1
SDC_DATA0	IO	B14	SDIO bus DATA0
SDC_CLK	O	B45	SDIO bus clock
SDC_CMD	IO	B44	SDIO bus command

The following figure shows the reference design of module and SDIO.

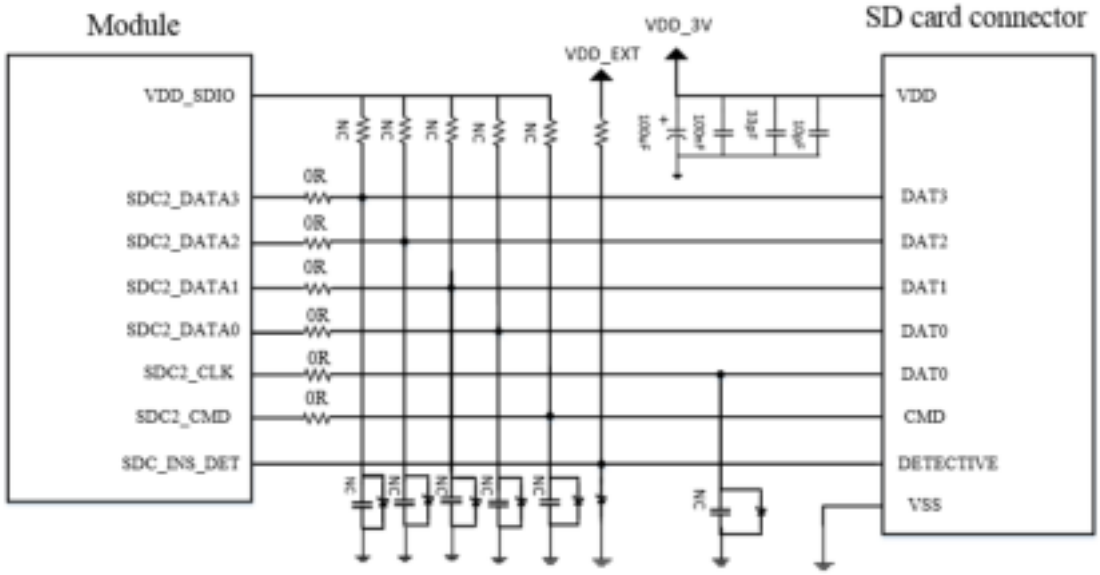

Figure 5-13 SD card reference circuit design

SD card circuit design should follow the following principles:

- The power supply VDD_3V voltage of the SD card ranges from 2.7 V to 3.6 V, and it needs to provide at least 800 mA current. SD card power supply should be provided from the external.

- In order to avoid bus jitter, it is necessary to reserve pull-up resistors to the SDIO signal. The resistance range is 10–100 kΩ, and the recommended value is 100 kΩ.
- In order to adjust the signal quality, a SDIO signal should be connected to 0 Ω resistor in series. Capacitors C1–C6 can be reserved, which are not placed by default. The resistance and capacitance should be placed close to the module side;
- In order to ensure good ESD performance, it is recommended to add TVs tube in SD pin;
- The load capacitance of SDIO bus needs to be less than 40 pF;
- SDIO signal needs to be surrounded by ground wire in upper and lower layers, and the impedance is controlled at 50 Ω ± 10%;
- Other sensitive signals such as RF signals and analog signals need to be far away from SDIO signals, and SDIO signals also need to be far away from noise signals such as clocks and DCDC;
- SD_CLK and SDC_DATA[0:3]/SDC_CMD need to be processed with equal length (the difference is less than 1 mm), and the total length should be less than 50 mm. Since the internal wiring length of the module is 15 mm, the external wiring length needs to be less than 35 mm.
- The distance between SDIO signal and other signals should be more than twice the line width, and the bus load should be less than 40 pF.

5.8 SPI Interface

The module provides 2 sets of SPI interfaces, and the maximum clock frequency is 50 MHz. Only the master mode is supported. The definition of SPI interface pin is described in the following table:

Table 5-11 SPI pin definition

Pin Name	I/O	Pin No.	Description
BLSP1_SPI_CS_N	O	C8	SPI1 chip select
BLSP1_SPI_MOSI	O	C24	SPI1 data output
BLSP1_SPI_MISO	I	C23	SPI1 data input
BLSP1_SPI_CLK	O	C7	SPI1 clock
SPI_INT_OUT/GPIO_88	O	D48	SPI1 output interrupt signal (reserved)
SPI_SLAVE_INT/GPIO_94	I	D36	SPI1 input interrupt signal (reserved)
BLSP2_SPI_CS_N	O	C38	SPI2 chip select
BLSP2_SPI_MOSI	O	C50	SPI2 data output
BLSP2_SPI_MISO	I	C49	SPI2 data input
BLSP2_SPI_CLK	O	C37	SPI2 clock

Warning

1. The SPI interface level of the module is 1.8 V. If the level of the host system is 3.3 V or others, a 50 MHz level translator is needed between the module and the host SPI.

5.9 RGMII Interface

The module provides a RGMII interface with embedded Ethernet MAC and a two-wire management interface. The pin

definitions are as follows:

Table 5-12 RGMII control interface

Pin Name	I/O	Pin No.	Description
RGMII_RX_CTL	DI	A27	RGMII RX control signal
RGMII_RX_CLK	DI	A28	RGMII RX clock signal
RGMII_RX_0	DI	A29	RGMII RX bit 0 signal
RGMII_RX_1	DI	A30	RGMII RX bit 1 signal
RGMII_RX_2	DI	A31	RGMII RX bit 2 signal
RGMII_RX_3	DI	A32	RGMII RX bit 3 signal
RGMII_INT	DI	A41	RGMII interrupt signal
RGMII_Reset	DO	A17	RGMII reset output signal
RGMII_TX_CTL	DO	A11	RGMII TX control signal
RGMII_TX_CLK	DO	A12	RGMII TX clock signal
RGMII_TX_0	DO	A13	RGMII TX bit 0 signal
RGMII_MDIO	DIO	A45	RGMII MDIO signal
RGMII_MDC	DO	A44	RGMII MDC signal
RGMII_TX_3	DO	A16	RGMII TX bit 3 signal
RGMII_TX_2	DO	A15	RGMII TX bit 2 signal
RGMII_TX_1	DO	A14	RGMII TX bit 1 signal
PHY_WAKE_ OUT	DO	D46	Wake up Ethernet by Module (reserved)
PHY_WAKE_IN	DI	D47	Wake up Module by Ethernet (reserved)

The RGMII interface of the module conforms to the following standards:

- Comply with IEEE802.3 standard
- Support 10M/100M/1000M working modes.
- Support 1.8V/2.5V voltage by management interface.
- Support the VLAN label.
- Connect to an external Ethernet PHY chip such as 88Q1010.

The RGMII signal design principles are as follows:

- RGMII data and control signals need to be kept away from sensitive signals, including radio frequency, analog signals, and noise signals such as clock and DCDC.
- The RGMII differential data signal impedance should be controlled at 50 Ω±10%, and the complete reference ground plane should be assured.
- RGMII has two groups of high-speed signals, TX and RX. Each group has 6 signals, TX_CLK/RX_CLK signal wiring needs to be separately surrounded by ground wire. The wiring length difference within the group is controlled to ≤ 2.5 mm, and the signal distance reference is as follows:

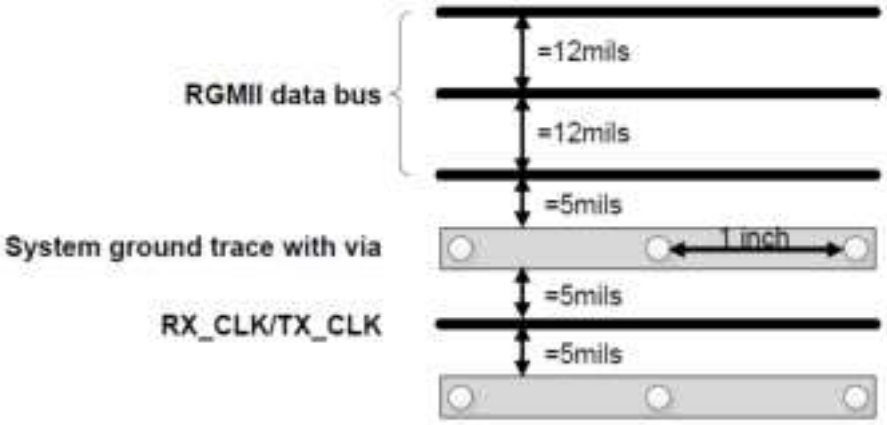

Figure 5-14 Reference signal distance of RGMII

5.10 PCIe Interface

The module provides a set of PCIe interfaces. The following table describes the pin definitions.

Table 5-13 PCIe pin definition

Pin Name	I/O	Pin No.	Description
PCIe_REFCLK_M	AIO	B20	PCIe reference clock (-)
PCIe_REFCLK_P	AIO	B3	PCIe reference clock (+)
PCIe_TX0_M	AO	B21	PCIe data TX channel 0 signal (-)
PCIe_TX0_P	AO	B4	PCIe data TX channel 0 signal (+)
PCIe_RX0_P	AI	B2	PCIe data RX channel 0 signal (+)
PCIe_RX0_M	AI	B19	PCIe data RX channel 0 signal (-)
PCIe_RX1_P	AI	B1	PCIe data RX channel 1 signal (+)
PCIe_RX1_M	AI	B18	PCIe data RX channel 1 signal (+)
PCIe_TX1_M	AO	B22	PCIe data TX channel 1 signal (-)
PCIe_TX1_P	AO	B5	PCIe data TX channel 1 signal (+)
PCIe_RESET	DO	B6	PCIe reset signal
PCIe_WAKE	DO	B7	PCIe wakeup signal
PCIe_CLKREQ	DO	B35	PCIe clock request signal

The module supports PCIe GEN 3.0x2 lanes. The PCIe signal is a differential signal, and the differential impedance is controlled at 85 Ω±10%, the wiring length difference within the differential pair is controlled at ≤ 0.7 mm, and the wiring length is controlled at ≤ 300 mm..

6 Electrical Characteristics and Reliability

6.1 Recommended Parameters

Table 6-1 Recommended parameters

Parameter	Minimum	Nominal	Maximum	Unit	Remarks
VBAT	3.4	3.8	4.2	V	--
VIL	-0.3	0	0.63	V	--
VIH	1.17	1.8	1.95	V	--
VOL	0	--	0.45	V	--
VOH	1.35	--	1.8	V	--
Operating Temperature	-40	25	85	℃	--
Storage Temperature	-40	25	95	℃	--

6.2 RF Transmit Power

The following table lists transmit power for each band of the AN958-NA module.

Table 6-1 RF transmit power of the AN958-NA module

System	Band	3GPP Requirement	Max Power Typical Value	Unit	Remarks	
GSM	GSM850	33+2/-2	33	dBm	--	
	GSM900	33+2/-2	33	dBm	--	
	DCS1900	30+2/-2	30	dBm	--	
WCDMA	Band 2	24+1.7/-3.7	23	dBm	--	
	Band 4	24+1.7/-3.7	23	dBm	--	
	Band 5	24+1.7/-3.7	23	dBm	--	
LTE FDD	Band 2	23±2.7	23	dBm	--	
	Band 4	23±2.7	23	dBm	--	
	Band 5	23±2.7	23	dBm	--	
	Band 7	23±2.7	23	dBm	--	
	Band 12	23±2.7	23	dBm	--	
	Band 14	23±2.7	23	dBm	--	
	Band 17	23±2.7	23	dBm	--	
	Band 25	23±2.7	23	dBm	--	
	Band 26	23±2.7	23	dBm	--	
	Band 28	23±2.7	23	dBm	--	
	Band 29	23±2.7	23	dBm	--	
	Band 66	23±2.7	23	dBm	--	
	Band 71	23±2.7	23	dBm	--	

System	Band	3GPP Requirement	**Max Power** Typical Value	Unit	Remarks	
LTE TDD	Band 41	23±2.7	23	dBm	--	
	Band 42	23±2.7	23	dBm	--	
5G NR	n2	23±2	23	dBm	--	
	n5	23±2	23	dBm	--	
	n7	23±2	23	dBm	--	
	n12	23±2	23	dBm	--	
	n14	23+2 /-2.5	23	dBm	--	
	n25	23±2	23	dBm	--	
	n28	23±2	23	dBm	--	
	n41	26+2 /-3	23	dBm	--	
	n48	23±2	23	dBm	--	
	n66	23±2	23	dBm	--	
	n71	23±2	26	dBm	--	
	n77	26+2 /-3	26	dBm	--	
	n78	26+2 /-3	26	dBm	--	

6.3 Dual-Antenna RX Sensitivity

The following table lists RX sensitivity with dual antennas for each band of the AN958-NA module.

Table 6-2 RF RX sensitivity of the AN958-NA module

TBD

6.4 Four-Antenna RX Sensitivity

Basically, AN958-NA module support 4 × 4 MIMO in medium and high-frequency band.

Table 6-3 RF RX sensitivity of the AN958-NA module

TBD

6.5 GNSS

The AN958-NA module adopts Qualcomm IZat™ engine，of which GEN 9 V4 supports five-satellite positioning, including GPS, GLONASS, BeiDou, Galileo, and QZSS. The module is embedded with LNA which can effectively improve the sensitivity of GNSS. Table 6-14 describes the performance indicators.

Table 6-2 GNSS performance indicators

Parameter	**Description**	**Data**	**Unit**	**Remarks**
Sensitivity	Positioning and capture	-144	dBm	--

Parameter	Description	Data	Unit	Remarks
	Positioning and tracking	-154.5	dBm	--
C/No	-130 dBm	37	dB-Hz	--
TTFF	Cold boot time	37	S	--
	Warm boot time	36	S	--
	Hot boot time	3	S	--
CEP	Static precision	1	m	--

6.6 Electrostatic Protection

In the application of the module, static electricity is generated by human body and friction between micro-electronics. The static electricity is discharged to the module through various channels and may cause damage to the module. Therefore, ESD protection should be taken seriously. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should be applied at the designed circuit interfaces and at the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

The following table lists the ESD performance parameters (temperature: 25°C, humidity: 45%).

Table 6-3 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
GND	±8	±15	kV
Antenna Interface	±8	±15	kV
Other interfaces	±8	±15	kV

Note

1. ESD is measured under the conditions of Fibocom EVK development kit.

7 Structural Specification

7.1 Product Appearance

The following figure shows the top view/bottom view of AN958 series modules.

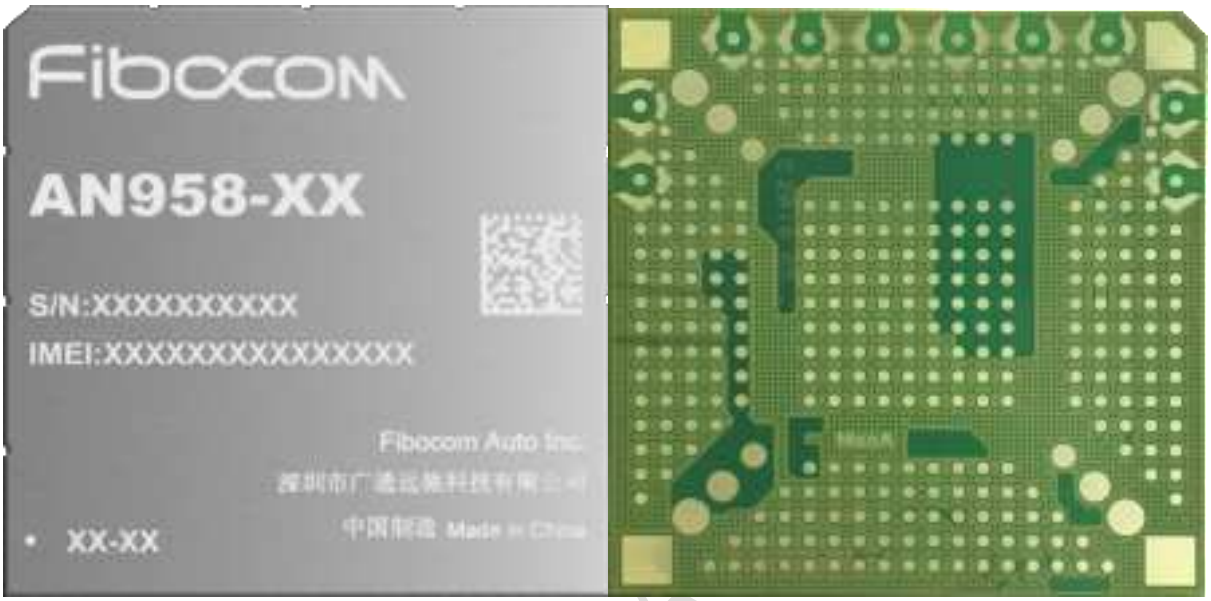

Figure 7-1 AN958 module appearance

7.2 Structural Dimensions

The following figure shows the structural dimensions of the AN958 series modules.

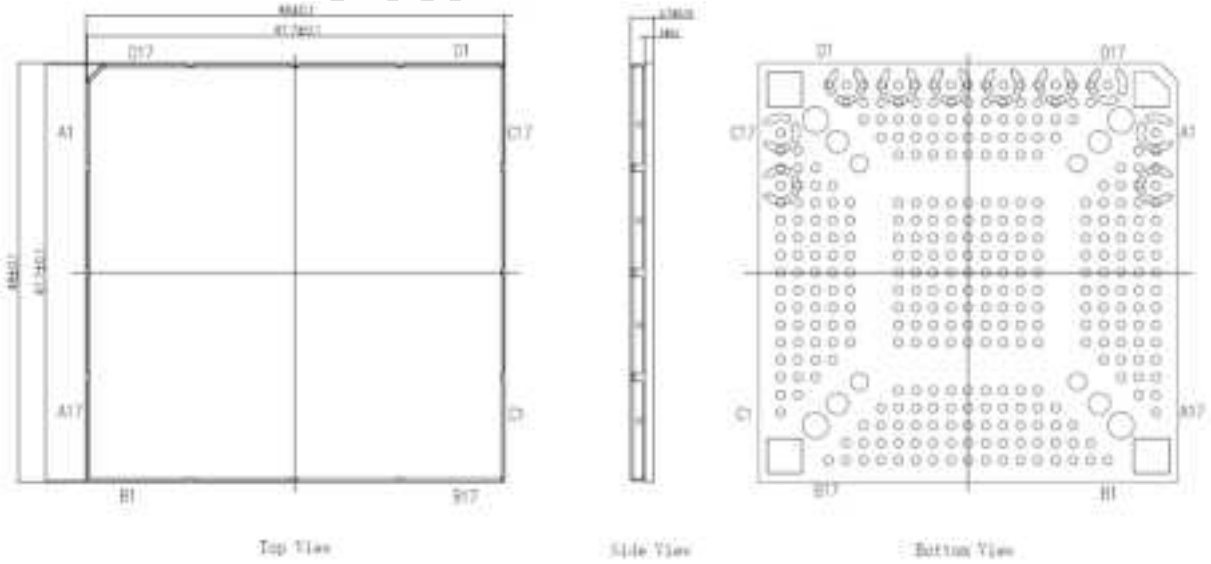

Figure 7-2 Structural dimensions of the AN958 series modules

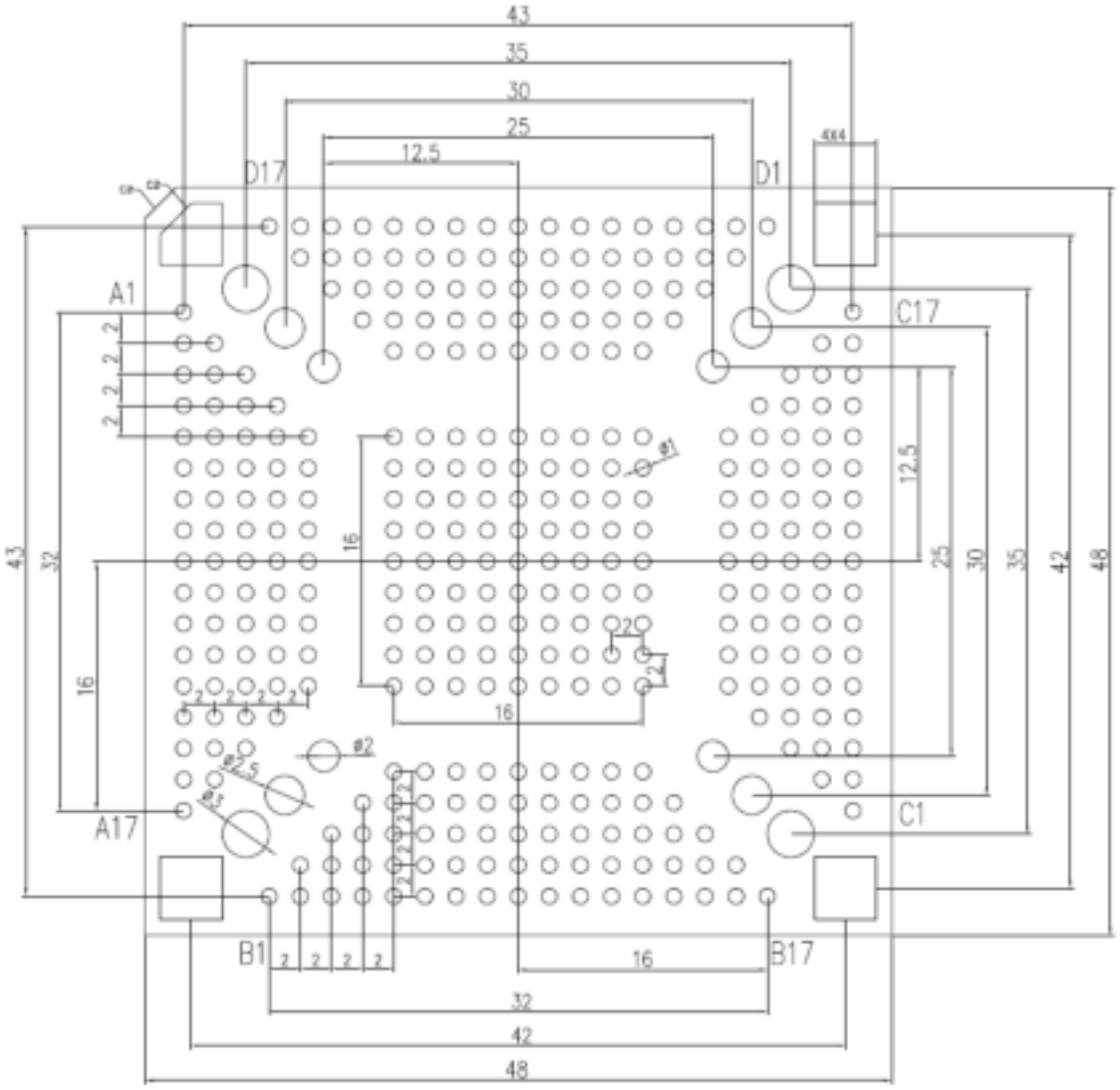

Figure 7-3 Structural dimension

Note

1. Unmarked dimensional tolerances are ±0.1 mm.

7.3 Storage

See *FIBOCOM AN958 Series SMT Design Guide.*

7.4 Packaging

See *FIBOCOM AN958 Series Product Packaging Specifications.*

8 Appendix A Abbreviations

Term	Description
AR	Augmented Reality
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Downlink
DLCA	Downlink Carrier Aggregation
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	Multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System

Term	Description
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
VR	Virtual Reality
WCDMA	Wideband Code Division Multiple Access

9 Appendix B Operating band and frequency range of 2G/3G/4G/5G NR Sub-6

Band	Mode	Tx (MHz)	Rx (MHz)
Band 1	NR/LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 2	NR/LTE FDD/WCDMA	1850 - 1910	1930 - 1990
Band 3	NR/LTE FDD/WCDMA/GSM	1710 - 1785	1805 - 1880
Band 4	LTE FDD/WCDMA	1710 - 1755	2110 - 2155
Band 5	NR/LTE FDD/WCDMA/GSM	824 - 849	869 - 894
Band 7	LTE FDD	2500-2570	2620-2690
Band 8	NR/LTE FDD/WCDMA/GSM	880 - 915	925 - 960
Band11	LTE FDD	1427.9 - 1447.9	1475.9 - 1495.9
Band12	LTE FDD	699 - 716	729 - 746
Band13	LTE FDD	777 - 787	746 - 756
Band14	LTE FDD	788 - 798	758 - 768
Band17	LTE FDD	704 - 716	734 - 746
Band18	LTE FDD	815 - 830	860 - 875
Band19	LTE FDD/WCDMA	830 - 845	875 - 890
Band20	NR/LTE FDD	832 - 862	791 - 821
Band21	LTE FDD	1447.9 - 1462.9	1495.9 - 1510.9
Band25	LTE FDD	1850 - 1915	1930 - 1995
Band26	LTE FDD	814 - 849	859 - 894
Band28	NR/LTE FDD	703 - 748	758 - 803
Band29	LTE FDD	NA	717 - 728
Band30	LTE FDD	2305 - 2315	2350 - 2360
Band32	LTE FDD	NA	1452 - 1496
Band 34	LTE TDD	2010-2025	2010-2025
Band 38	LTE TDD	2570 - 2620	2570 - 2620
Band 39	LTE TDD	1880 - 1920	1880 - 1920
Band 40	LTE TDD	2300 - 2400	2300 - 2400
Band 41	NR/LTE TDD	2496 - 2690	2496 - 2690
Band 42	LTE TDD	3400-3600	3400-3600
Band 47	LTE TDD	5855-5925	5855-5925
Band 48	LTE TDD	3550-3700	3550-3700
Band 66	NR/LTE FDD	1710 - 1780	2110 - 2200
Band 71	NR/LTE FDD	663 - 698	617 - 652
n77	NR	3300-4200	3300-4200
n78	NR	3300-3800	3300-3800
n79	NR	4400-5000	4400-5000

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain（dBi）
GSM 850	5.60
GSM 1900	1.00
WCDMA Band II	7.31
WCDMA Band IV	4.30
WCDMA Band V	8.72
LTE Band 2	7.30
LTE Band 4	4.30
LTE Band 5	8.71
LTE Band 7	7.30
LTE Band 12	8.00
LTE Band 14	8.53
LTE Band 17	8.04
LTE Band 25	7.30
LTE Band 26（814~824）	8.66
LTE Band 26（824~829）	8.71
LTE Band 41	7.30
LTE Band 42	4.30
LTE Band 66	4.30
LTE Band 71	7.78
NR Band n2	7.00
NR Band n5	8.42
NR Band n7	7.00
NR Band n12	7.71
NR Band n14	8.23
NR Band n25	7.00
NR Band n41	4.00
NR Band n48 (PC2)	-3.00
NR Band n66	4.00
NR Band n71	7.48
NR Band n77（3450~3550） (PC2)	1.00
NR Band n77（3700~3980） (PC2)	1.00
NR Band n78（3450~3550） (PC2)	1.00
NR Band n78（3700~3800） (PC2)	1.00