TECHNICAL SPECIFICATION FOR

SP-220-250

PORTABLE RADIO

ISSUE 1.0

LMR DIVISION

MAXON KOREA

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Introduction

The SP-220-250 is a small, lightweight handportable for applications where small size is the primary requirement. The SP-220-250 used a BCD Encoder SW and the current RF circuit of SP-210 and applied a new LMR ASIC in stead of Analog circuit, which is capable of Automatic Adjustment by a PC and test equipments.
Both the VHF and UHF models are controlled by PLL / microprocessor

Content

- Unit
- ANT
- Metal-Hydride Battery Pack(7.5V/1350mAh)
- Drop in Charger
- Adaptor

Features

- On/Off & Volume Switch
- PTT Switch
- Monitor Switch
- External One Jack
- 4/16 channels /with CTCSS and DCS
- 12.5 KHz /20 KHz/ 25KHz Programmable
- 1/5 Watts Switchable

Main Function

- Wideband
- Standard/Non-Standard CTCSS signaling
- Transmit Time-Out-timer/TX Inhibit
- Low Battery Indication
- Memory Protect
- Battery save Circuitry
- 4/16 Channels

Wideband

This software is made to work and control the wide band receiver/transmitter board.

Marked Idle Enable

If this function is enabled, the unit will transmit provided that the correct programmed CTCSS tone has been decoded. This function is essential for repeater operation.

Standard/Non-Standard CTCSS

When programming a channel with CTCSS, any frequency from 55 to 250 Hz can be selected in 0.1 Hz increments. The radio will be capable of encoding and decoding two non-standard CTCSS tones.

Transmit Time-Out-Timer (TOT)/TX Inhibit

The time-out-timer is system programmable for 10 seconds to 990 seconds, in 10 second increments and cans also be selected as disabled. The default value is 10 seconds. The addition to this feature is a programmable lock-out-timer that inhibits the radio transmitter for a specified time after the time-out-timer expires.

When the time-out-timer function is enabled,and the TX inhibit function is disabled, the radio will transmit after the time-out-timer has expired and the PTT button is released and again depressed. With the TOT and TX enabled, the radio will not transmit after the time-out-timer has expired, even if the PTT is released and depressed again. Transmission will not be allowed until the TX inhibit time has expired. Tx inhibit time is system programmable from 5 to 60 seconds in 5 second increments. The default value for the TX inhibit is 5 seconds. The radio will beep one time, 5 seconds before the TOT time expires. This will indicate to the user that the transmitter is about to be locked out.. If the PTT is released and depressed again anytime before the TOT has expired, the TOT time will be reset. If the beep tone enable /disable is set to disable , the one beep will not be issued. The radio will beep 4 times when the TOT time expires. After the TX inhibit time passes, the radio will beep one final time.

VCO Lock Time

The micro will allow more lock time for the VCO before the indication of out-of-lock beep.

Low Battery Indication

Low Battery Indication will be changed so that it does not inhibit RX and will allow one transmission after low cell is indicated. Low cell will not be indicated during transmit mode. If the battery goes below sepecified limits

during the TX mode, low cell will be indicated immediately after releasing the PTT button.

After the low cell indication is issued, the transmitter can only be used one time. When the PTT is pushed again and then released, the transmitter is locked out unit the unit is powered down and then powered back up.

Memory Protect

The software is such that if the radio is inadvertently put into program mode it will not lose the contents of the EEPROM memory. Date will only move in and out of the memory when the program mer is attached.

External Option Detect

An input to the microprocessor will be available that will indicate to the microprocessor that the external option has been selected. This input should be connected to the external option connector. External option should be selected for each channel. If a channel is selected during programming for external option, this input should be active when the channel is selected during opteration of the unit.

THEORY OF OPERATION

The VHF and UHF handheld radios are comprised of a RF PCB and a Digital PCB. The RF PCB containts the transmitter, receiver circiuts and the Digital PCB, control circuits respectively. The control circuits contain the micro controller, Asic(Audio sigmal precessor) and associated digital circuits.

DIGITAL CIRCUIT

ASIC
is comprised of Analog signal path, SAT signal path, miscellaneous signals and controller as follows

Analog signal path

A1： is a BUFFER AMP to generate discriminator audio from Pin9 to ASW1.
And its gain 1

A2：amplifies analog signal which was received from IN2(Mic input terminal) by 10dB. And then output signal goes ASW1.

ASW1 : is 2 way switch. It generates one of analog signals which was applied from A1 and A2. The control signal should be controlled by 1 bit signal. Default value is <0□and A1 is selected

INTRIM : compensates the deviation for the input analog signal sensitivity. The control range of the signal is +3.5/-4dB and is controlled by 16 steps. And the control signal is handled by 4 bit signal. Default value is □1000 □ and gain is 0dB.

HPF : was composed of the 8th order or more and the cut-off frequency is 300Hz. As for the attenuation characteristic of filter, the signal diggerence must at least over 30dB at the cut-off frequency 300Hz and the first 250Hz of attenuation bandwith.

ASW2 : is 4 way switch. It receives analog signals from HPF and its output goes one of De-Emphasys, RXVOL or AMP(with 6dB/oct Pre-Emphasys), AMP(without Pre-Emphasys)by the control instruction. The control signal must be controlled by 2 bit signal. Default value is <00□and De-Emphasys is selected.

DEMPHA : has a characteristic of +6dB/oct De-Emphasys. The gain for 1KHz Analog Signal which is appllied from ASW2 is 1.

PREMPHA : has a characteristic of +6dB/oct Pre-Emphasys. The gain for 1KHz Analog Signal which is appllied from ASW2 is 1.
RXVOL : controls the magnitude of input analog signal to generate to the speaker. The analog signal must be able to be controlled as 16 stages within the range of maximum 0dB to minimum -37.5dB.

AMP : is amplifier which generates analog signal is applied by ASW2 to Limitter. And it also has to have the characteristicof +6dB/oct Pre-Emphasys before the amplifing stage. And the minimum gain of the amplifier is +20dB at the minimum level of the control signal. The control instruction should be controlled as 8 stages from minimum+20dB to +41dB by 3bit signal

LIMITER : has the function of limiting the signal at the definite magnitude for modulation Limiter input level must be limited at 0dB(2800mVp-p)and Liniter output signal must be controlled at 4 stages from 0dB to -5.4dB by 2 bit signal. Also output signal of Limiter go to the LMOUT termimal.

ASW3 : is 2 way switch. It selects signal from either Limiter or SATRIM and its output goes VSLP.

VSLP : is low pass filter of at least 6th order or more and its cut-off frequency must be elected either 2.55KHz or 3KHz by 1 bit signal. Filter attenuation characteristics must be at least over 21dB/oct. But unlike VSCBPF, the cut-off frequency of VLPF should be changed by switching of device. That is to prevent reducting of S/N ratio due to the harmonic by the internal clock.

TXTRIM1 : to compensate deviation for the magnitude of analog input signal, within the Gain range of +3.5dB ti -4dB, TXTRIM1 controls as 16 stages by 4bit signal.

TXSUM : mixes the signal from TXTRIM1 with the other signal which is applied by TDIN 4 bit signal , or selects one of the signals. And it also must be able to mute two applied signal. When muting, attenuation factor must be at least ove 50dB.

ATTN : attenuates the signal applied from TXSUM by 6dB. This should be able to select the atteneation of 0dB or 6dB by 1 bit contro signal.

TXTRIM2/3 : control the deviation of final output signal for modulation, Within the range of +3.75 to -4dB. It can be controlled as 32 stages by 5 bit signal, respectevely.

A3/A4/INV : is the final output Buffer AMP of TX Analog signal and Gain is 0dB,
respectively. Output A3 and A4 is non-inveriting signal.INV inverts the phase of the TXTRIM3 output of TXTRIM3 is INV.

SAT Signal Path

SATRIM2 : is received DTMF or other tone signal and compensates the deviation of the input signal. The signal can be controlled by 4 bit control signal within the range of +2.5dB to -3dB and +13.5dB to +12dB.
ASW3 : Two way switch. selects one of the signals which is applied by RDIN and TDIN.
Both RDIN AND TDIN siganls is DCS or CTCSS , and all of the paths from TDIN to FLTOUT and COMPON to MODOUT1/2/3 must be DC couple.

VSCLPF : is the Variable Switched Capacitor Low Pass Filer , which is variable the applied signal from ASW4 by signal instruction, at cut-off frequency, from 50Hz to 300Hz. It is composed of the 7th order elliptic Low Pass Fiter or mor. To make the desition of cut-off frequency , the clock which is applied to VSCLPF oscillates at internal controller by controller instruction and it must be supplied to VSCLPF.

SATRIM : to compensate the deviation of input SAT signal, it controls the amplitude as 16 stages within the range of +3.5dB to -4dB by 4 bit signal.

COM : comparing external reference voltage(COMPP)with the applied SAT signal which is from FLTOUT to COMPIN and it goes to Logic High and Logic Low at this point. The reference voltage goes to Vref.

Miscellaneous signals and controller

ADC/ DAC : 8 bit Analog to Digital Converter/ 8 bit Digital to Analog Converter

CTRL : transfering its mutual data passing throug 3 pin to external controller by Serial Communication. And execute the relevant instructions
DATA : transferring all the instructions with exeternal controller. It operates as output terminal by READ instruction and it operates as input terminal by WRITE instruction.
CLOCK : is synchronous input terminal for communication with external controller. Clock is supplied from external controller and data transfer is moded at CLK down edge.
ENBL : In data communication , it determines effective timing. At Active Low, Data Read and Write can be effective.

AGND,DGND : Reference voltage of internal Analog paths. Classifed Digtal's Analog's GND.

CTCSS/ DCS Decoding Processing

Discriminator audio from pin 9 IC5 is applied to the 7th order elliptic Low Pass Filter through Pin 3 IC406 where the signal of the voice band affecting the processing of CTCSS or DCS decodig is diminished sufficiently. The deviation of the signal passed through the 7th order LPF is controlled by SATRIM2 and the applied signal which is from FLTOUT to COMPIN is compared with external reference voltage (COMPP) and then it goes to Logic High and Logic Low. The signal is output from Pin 21(IC406) and fed into IC403(micro) wher it is matched with a programmed frequency. If successful, a Decode occurs, which is shown by a green L.E.D on the top side of the VHF and UHF handheld and audio is heared. If valid Decode was not seen , the busy L.E.D.(Yellow) would be shown.

CTCSS Encoding Processing

During TX encode the tone squelch digital signal is produced as a 3bit parallel word at pins 48,49 and 50 of the micro controller (IC403). The 3bit digital signal is converted to an analog siginal by resistors R420, 421 and 423. The analog signal is fed into IC406 pin4 and filtered by 7th order elliptic LPF. The filtered signal is output on pin 23 (IC406) and fed into pin22 of IC406 . The filtered encode signal is mixed with the audio signal from TXTRIM1 by TXSUM. Via ATTN , the mixed signals applied to TXTRIM2/TXTRIM3, which control for modulation.

External Mic/PTT Control circuit

The external microphone is connected via 3.5mm stereo connector on the right side of the handheld. The internalmic and speaker are disable by SPK/MIC Jack.

LOW Battery Indicator Circuit

When the battery voltage drops below 5.6 VDC, D403 and Q405 turn on. The micro controller disables the transmitter and at the same time enables the red LER and sends an alert tone to warn the user. The battery should

be replaced or charged at this time (one tx allowed after low battery).

EEPROM

RX/TX channels, and CTCS/DCS as well as other data from the programmer are stored in the EEPROM. The data stored is retained without power supplied. This is a non-volatile memory. The EEPROM may have information re-programmed or erased. IC404 is an EEPROM with 25C32S capacity and data is written and read serially

Mute (squelch) Circuit

The mute circuit which is controlled by the output of IC403(micro) pin13(3837) is connected to Q415,414 via R446 which mutes the H8/3837IC on the Digital circuits.

Monitor

The unit contains a switch mounted on the PTT assembly for monitor function. This is enabled or disabled by programming software.

RF CIRCUITS

Transmitter

The transmitter is comprised of:
1. Buffer
2. Power AMP
3. Low Pass Filter
4. Antenna Switch
5. A.P.C Circuits

Buffer

VCO output level is 0dBm and amplified to +17dBm (UHF)/(VHF). The buffer consists of Q16, Q17 and Q3 for isolation and gain.

Power AMP

The P.A Module onsists of 2-stage amplifier and amplies the TX signal from +16dBm to +37dBm. The input and the output terminal of the P.A Module are matcued 50 OHM.

Low Pass Filter

L7, L8, L11, C73, C74, C75 and C76 are the 7th order Chebyshev low pass filter. Unwanted harmonic are reduced by -65 dBc.

Antenna Switch

When transmitting, the diodes D5 and D6 are forward biased enabling the RF signal passage to the antenna. D6 is shorted to ground inhibiting the RF signal to front-end. In receive the diodes D5 and D6 are reversed biased passing the signal from the antenna through L13 and C83 to the front-end without signal loss.

Automatic Power Control Circuit

The APC circuit consists of the R109, variable resistor RV1, IC3, and Transistor Q19, Q21, and Q22. The supply current is monitored by difference voltage on R109(0.1 Ohm) which is through for it. If the current is varied by RF power output or other reasons, it produces some bias voltage by IC3A and Q19. The differential signal at the output of IC3 is passed to Q21 and q22 that produces a constant power output to the antenna. RV1 is used to adjust the RF power level.

RFCIRCUITS PLL SYNTHESIZER

12.8 MHz TCXO

The TCXO contains the 2-stage thermistor network compensation and crystal oscillator and modulation ports. Compensation is +/-2.5 PPM or less from -30c to +60c.

PLL IC Dual Modules Prescaler

Input frequency of 12.8 MHz to IC2 MB15E03SL pin 1 is divided to 6.25 KHz or 5 KHz by the reference counter, and then supplied to comparator. RF signal input from VCO is divided to 1/64 at prescaler in IC2, Divided by A and N counter in IC2 to determine frequency steps, and then supplied to the comparator. PLL comparison frequencccy is 6.25/5KHz so that minimum programmable frequency step is 5/6.25 KHz. A and N counter is programmed to obtain the desired frequency by serial data in CPU. In comparator, the phase difference between reference and VCO signal is compared. When the phase of reference frequency is leading , Fv is output, but when VCO frequency is leading, Fr is the output. When Fv=Fr, phase detector out is very small 0v pulse. 64/65 modulus prescaler is comprised in IC2.

Level Shifter & Charge Pump

The charge pump is used for changing output signals Fr, Fv at PLL IC from 0-5v to 0-12v necessary for controlling vco.

Reference Frequency LPF

The Loop Filter contains R12, C21 and C22. LPF settling time is 12mS with 1 KHz frequency. This also reduces the residual side-band noise for the best signal-to-noise ratio.

DC to DC Converter

The DC to DC converter converts the 5v to 14-16v to supply the necessary voltage for wide range frequency in vco.

VCO

The VCO consist of one VCO. Is switched TX/RX by switching TR Q201. It is configured as colpits oscillator and connected to buffer as cascade bias in order to save power. The varicap diodes D201 and D202 are low-resistance elements and produce a change in frequency with a change in reverse bias voltage (2-11v). L203 and C220 are resonant coil and capacitor, which change the control voltage by the turning core and capacitor. D202 modulation diode, modulates the audio signal. C204 compensate for the non-linearity of the vco due to modulation diode, and maintain a constant modulation regardless of frequency .

RECEIVER

Front End

The receive signal is routed backward through the low pass filter, then onward to Pin 1 of the Hybrid Receiver Front End Module to a matchig circuit consisting of C603 through C601 ,L602 through L601 is coupled to the base of Q601 which serves as an RF amplifier. Diode D601 serves as protection from static RF overload from nearby transmitters. The output of Q601 is then coupled to a bandpass filter consisting of C604 through C615 and L603 through L607).The output of Pin 6 is then couples to the doubly balanced mixer D4. The receiver Front End module is factory pre-turned and requires no adjustment. Repair is effected by replacement of the entire module of

the proper banded module. These are VHF 138MHz to 162 MHz and UHF 440 MHz to 470 MHz. The receiver Front End module signal pins are as follows:

1. RF Input
2. Input Ground
3. N/A
4. Receive +5V
5. Ground
6. Output

First Mixer

D9, T1 and T2 are double balanced mixers which provide the 45.1 MHz intermediate frequency output. The filtered frequency from the Front End module is coupled to T1 . The 45.1 MHz IF output is matched to the input of the 2-pole monolithic filter by L14, L15, C93 and C92. The crystal filter provides a bandwidth of +/-7.2 KHz from the operating frequency providing a high degree of spurious and intermodulation protection. Additionally, a 90 MHz trap (XF1) is also placed at the filter output to provide additional attenuation of the second order IMD. The output of the filter is impedance matched by C90 and C43 to the base of the post of filter IF amplifier Q25.

Second Oscillator Mixer Limiter And FM Detector

The output of the post filter amplifier, Q25, is coupled, via C98 to the input of IC5 (TA31136FN). IC5 is a monolithic single conversion FM transceiver, containing a mixer, the second local oscillator, limiter and quadrature detector. Crystal X1 44.645 MHz is used to provide resultant 455KHz signal from the output of the second mixer. The mixer output is then routed to CF1 or CF2. These ceramic filters provide the adjacent channel selectivity of
25KHz or 12.5 KHz bandwidth .

Mute (squelch) Circuit

The mute circuit switches off the power amplifier when no audio signal is present. The squelch circuit consists of IC5 and RV2 (RV4) and thier associated components. The noise signal foom pin 9 of IC5 is amplified by internal amp of IC5 and then fed into RV2(RV4). RV2(RV4) is used to adjust the squelch circuit sensitivity and is normally adjusted to produc anoise squelch opening sensitivity of 10dB to 12dB SINAD

Speaker Audio Amplifier

After signal detection and audio filtering , Via VR5 on the RF board, the low level audio is returned to the digital board. This is then routed to Pin2 of IC408 to provide speaker audio. IC408 is enable by a logic low applied to Q415 which in turn enable Q414, appiying GND to pin 9 of IC408.