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Federal Communications Commission (Authorization and Evaluation Division) 7435 Oakland Mills Road Columbia, MD 21046

SUBJECT: Attestation of Model Difference

FCC: QOQGM210P

Models: BGM210P22A, BGM210P32A, MGM210P22A, MGM210P32A

We, Silicon Laboratories Finland Oy, hereby declare that the family of our Bluetooth Low Energy and ZigBee wireless radio modules, includes 4 models with names as listed above. These models are electrically and mechanically identical. The differences between models are described in the table below:

Model	MGM210P22A	MGM210P32A	BGM210P22A	BGM210P32A
Specification	Low-Power,	High-Power,	Low-Power, BLE	High-Power, BLE
	Zigbee and/or BLE	Zigbee and/or BLE		
Antenna Type	1. On-board ceramic chip antenna with 1.86dBi of gain			
	2. Reference external dipole antenna with the theoretical gain of 2.14dBi which can be optionally			
	connected to module's RF pin			
Hardware Note	The wireless chipset (System-on-Chip, SoC) is the same in all these modules, and it integrates a			
	PA subsystem and a RF switch to route the RF signal to two separate RF ports, one further routed			
	to the module's integral on-board ceramic chip antenna, and the other routed to a module's RF pin			
	for an optional external antenna. Both antennas can be used for a switched diversity			
	implementation with Zigbee-only. There cannot be simultaneous transmission out of the two RF			
	ports, and packets are transmitted only using one protocol at a time.			
RF max TX power	10dBm	20dBm	10dBm	20dBm

Differences: The $\underline{\mathsf{M}}\mathsf{GM}210\mathsf{P}$ modules are for Zigbee + BLE, while the $\underline{\mathsf{B}}\mathsf{GM}210\mathsf{P}$ modules are for BLE only. The Zigbee is disabled in the $\underline{\mathsf{B}}\mathsf{GM}210\mathsf{P}$ by a hardcoded software configuration in the SoC. The $\underline{\mathsf{2}}\mathsf{2}$ and $\underline{\mathsf{3}}\mathsf{2}$ in the model names indicate the power variant, $\underline{\mathsf{2}}\mathsf{2}$ referring to the low-power variants which are allowed to transmit at up to 10dBm, based on a purely hardcoded software limitation in the SoC, whereas the $\underline{\mathsf{3}}\mathsf{2}$ indicates the high-power variants for up to 20dBm. Hardware-wise, the two power variants only differ in their $\mathsf{50}\Omega$ matching networks which are optimized for the related max allowed output power.

Should you have any question, feel free to contact the undersigned directly.

Sincerely yours,

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