DESCRIPTION OF CIRCUIT FUNCTION

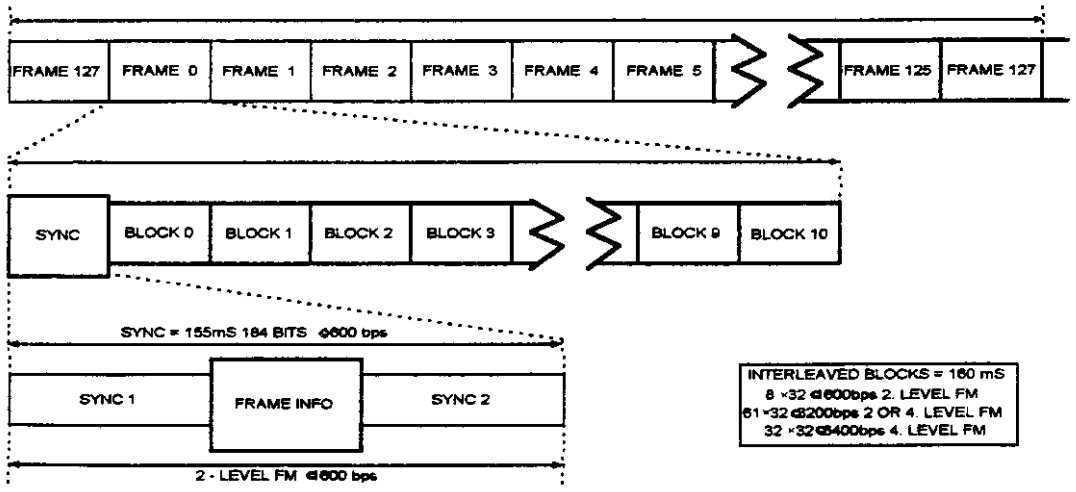
1. INTRODUCTION

The HANTEL FLEX numeric display pager uses a microcomputer to control radio frequency(RF) circuits and other customized decoding hardware to receive, decode, store, and display FLEX numeric pages. A page is received via the main RF carrier modulated with the proper base band sequence defined by the FLEX paging protocol. As FLEX is a multi-speed code, the base band signal is at a symbol rate of either 1600 or 3200 symbols per second (bps) with either 2 level or 4 level modulation. Note that 3200 symbols per second with 4 level modulation results in a maximum FLEX baud rate of 6400 bits per second (bps).

The circuitry in the receiver performs the RF to intermediate frequency (IF) conversion. The receiver then passes the frequency demodulated audio signal to the decoder, which contains the customized analog and digital circuitry necessary to decode the page information. Additionally, the decoder contains other support circuitry to capture switch closures to provide audio and visual alerts, and to display page and other user information on the LCD screen.

2. FLEX PAGING FORMAT, CODE, AND CODE CAPACITY

A FLEX cycle is defined as 128 frames (4minutes) with each frame numbered from 0 to 127. An hour is divided into 15 FLEX cycles numbered 0 through 14. The structure of a FLEX frame is shown the below. FLEX frames are transmitted at 32 frames per minute (1.875 seconds per frame). The Sync 1 portion of each frame is transmitted at 1600 bps providing means for obtaining frame timing, 1600 bps symbol timing, and an indication of the speed of the remainder of the frame. The frame information word carries the cycle number indications by time multiplex phase of low traffic (address field does not extend past Block 0), and a 4-bit check character to ensure quality of the received information.



3. GENERAL CIRCUIT DESCRIPTION

a. Power

Operating power for both the receiver and decoder boards is obtained from the battery. On the receiver board, a 1-volt regulator supplies the rf circuitry with power. The regulator is turned on and off from the decoder via the battery-saver strobe. The decoder board receives its power from the battery and generates 3 volts, which is supplied to the microcomputer/LCD driver and the code plug.

b. Standard receiver basic circuit description

The basic pager circuits consist of the following receiver board stages : antenna and amplifier/preselector to receive, amplify, and filter the RF paging signal. The mixer converts the RF signal to an intermediate frequency(IF). The crystal filter attenuates the signal above and below the RF carrier. The oscillator/multiplier supplies the appropriate injection signal to convert the RF paging signal to the correct IF. The IF demodulator amplifies, filters, and mixes with the first IF to produce a 455KHz second IF and demodulates the signal to recover the audio data.

The receiver board receives power from the main system battery. A 1 Volt regulator contained in the IF demodulator supplies the receiver circuits with power. Control lines turn this regulator on and off as well as to select the IF demodulator model of operation.

c. Decoder basic circuit description.

The basic decoder consists of the following functional module : Microcomputer module with LCD driver, LCD display module, user interface buttons, FLEX decoder. The FLEX decoder is a signal processing module which communicates with the host microcomputer, which contains FLEXstack software driver used to fully reconstruct a FLEX page. Two switches provide user interface for the pager.

The DC-DC converter contains the voltage management circuits that provide the main system voltage from the primary battery. The microcomputer controls the major functions involving data decoding and control of the alert circuitry and the LCD.

4. OPERATING MODES

There are two modes of operation for the decoder : power-up and page search.

a. Power-up

The power-up condition starts when the primary battery is inserted into the pager. the voltage management circuits in the DC/DC converter activate and begin to regulate the system voltage(nominal 3.0V).

b. Page search

When the pager powers up, the receiver is turned on and the decoder begins to search for a valid FLEX frame. When a valid FLEX frame is detected, the pager synchronizes to the channel and begins to operate at the desired collapse value continuously. If no frame is detected within 1 minutes, the pager enters a baud detect mode. While in this mode, the pager searches every 1.84 seconds to determine if there is any FLEX information on the channel. Once FLEX data rates are detected, the pager then searches for a valid frame as noted before.

The microcomputer searches for the pager's FLEX address once it synchronizes to the channel. If no address is present, the pager shuts off the receiver and data decoding circuits and enters a lower current consumption mode. While in this mode the pager waits until the next frame is due on the channel. If a matching address is detected, the microcomputer extracts the message data from the signal and stores it in the internal RAM.

The pager notifies the user by enabling the appropriate alert circuits dependent upon the user and code plug information. if the audio alert options is selected, the tranducer activates with the appropriate alert waveform. If the vibration mode is selected, the vibrator motor is enabled. The alerts are stopped by pressing any of the two buttons. The message is then read by pressing the READ button.

5. DETAILED CIRCUIT DESCRIPTION

a. Battery voltage, voltage multiplier, voltage regulator and battery-saver strobe circuits.

The negative side of the battery is connected to circuit common. The positive voltage from the battery is distributed throughout the decoder and receiver section. A voltage regulator on board the IF demodulator supplies 1.0 volt to sections of the receiver at discrete times, reducing current drain.

The battery voltage is applied to the decoder DC-DC converter IC(U06), where it is converted to 3.0V operating voltage. This higher voltage is applied to the microcomputer(U03), and FLEXchip.

b. FLEX receiver circuit descriptions.

(1) Battery voltage and DC-DC converter.

The negative side of the battery is connected to circuit common. Positive voltage from the battery, B+, is distributed throughout the decoder and receiver sections.

BATT is applied to the dc to dc converter(U06) where it is boosted to 3.0 volts. This higher voltage is applied to Microcomputer(U03), Reset IC(U05) and EEPROM(U04)

(2) Antenna and RF amplifier

The antenna system for the pager is the metal-looped type which resonates with the

capacitors C26, C28 and VC2 trimming capacitor. Matching the antenna impedance to the input of RF amplifier(Q4, Q5) is performed by the fixed capacitor C26. By tuning the VC2 capacitor, the antenna can be turned to the pager's operating frequency.

The RF signal is coupled by C26 to the input of the RF amplifier, cascoded pair Q4 and Q5. Resistors R11, R12 and R9 provide DC bias stability. DC supply decoupling were performed by C25. The output of the RF amplifier is coupled to the mixer Q3 via a SAW filter. The antenna circuitry, together with the SAW filter, provide image and spurious response protection.

(3) Two-pole crystal filter.

The two pole crystal filter is a very high Q bandpass filter, resonant at the IF frequency. The low-conversion output contained frequencies other than desire 21.4MHz. The very narrow bandpass filter out the signal above and below 21.4MHz.

(4) Low-conversion/Demodulation module.

The first IF signal from filter F2 couples to the second mixer at pin 24 of low conversion module U01. It mixes with the second oscillator frequency for an output of 455KHz.

The second oscillator is a crystal controlled unit X2. There are no peaking or tuning adjustments. Output of the second oscillator must be 455KHz below the first IF. Output of the second mixer(second IF) is routed through ceramic filter F1 and the two internal IF amplifier stages. This further reduces the unwanted signals and provide better adjacent channel selectivity. After the second IF amplifier, the signal is applied to the audio demodulator.

c. FLEX decoder circuit description

(1) Microprocessor module

The microcomputer(U03) module controls the overall operation of the decoder section. Each time the pager is turned on, the U03 reads the code-plug information and performs the necessary operations to produce a power-up alert(audio beeps). Basically, the U03 consists of a microprocessor and a read-only memory(ROM).

A program in the ROM instructs the U03 to decode the recovered data, store the data message, power the RF/IF circuits on and off, process display data, and interact with the user controls and switches.

The MC68HC05L32 is an 80 pin MCU with highly sophisticated on-chip peripheral functions. The memory map includes 24K bytes of user ROM and 768 bytes of RAM. The MCU has eight parallel ports A, B, C, D, E, F, G, and J. ports A, B, C, and E have 8 I/O pins, port D has 7 I/O pins, port J has 2 I/O pins, port F has 8 input-only pins, and port G has 8 output-only pins. The MC68HC05L32 includes 16-bit and 8-bit timers, a COP Watch dog timer, LCD drivers, an 8 channel ADC, and two channel

serial perpheral interface. The details features are as below.

. Low cost, HC05 core, 80 pin QFP package
. 24592 bytes of MASK ROM including 16 bytes of user vectors
. 768 bytes of on-chip RAM
. 41 bidirectional I/O lines, 8 input-only lines, 8 output-only lines
. 16 bit timer with 2 input capture and 2 output compare
. 8 bit event counter / Modulus clock divider (8 bit timer)
. COP Watch dog timer
. 2 channel serial perpheral interface (SPI)
. 8 bit 8 channel analog to digital converter
. LCD drivers (4 back plane drivers) X (39 front plane drivers)
. On chip time base circuits
. Dual oscillators and selectable system clock frequency
. Power saving STOP mode / wait mode
. Two IRQ inputs
. Key wake up interrupt with 8 bit input.

(2) Code plug module

The code plug module includes an electrically erasable programmable read only memory(EEPROM) integrated circuit. It is programmed with pager address codes, functions to which the pager will respond, and pager options.

(3) FLEX Decoder

It simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receiver IC's and any of several off-the-shelf host microcontroller/microprocessors. Its primary function is to process information received and demodulated from a FLEX radio paging channel, select messages addressed to the paging device and communicate the message information to the host. The host's function is the interpret the message information in an appropriate manner. The FLEXchip IC also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low power mode when monitoring a single channel for message information.