BreezeNet SA-PC PRO
Functional Description and Block Diagram Description

1. Functional Description.

The DUT is a Frequency Hopping Wireless LAN PCMCIA Adapter operating in the 2.4 to 2.4835 GHz frequency band.
The DUT has two options:

- SA-PCR with two integral retractable monopole antennas.
- SA-PCD with two non-standard connector interface and a dipole antenna.

2. Block Description.

The device is designed to operate under IEEE 802.11 standard.
The device includes 3 main areas:

- RF Section.
- Baseband Section.
- Digital Section.

The device consists of a single board that includes the following parts:

1. A Controller that handles the protocol and the PCMCIA port.
2. A Modem that handles the modulation/demodulation tasks.
3. A Radio Transceiver that transmits and receives the radio signals.

The block diagram of the system is shown in Fig. 1

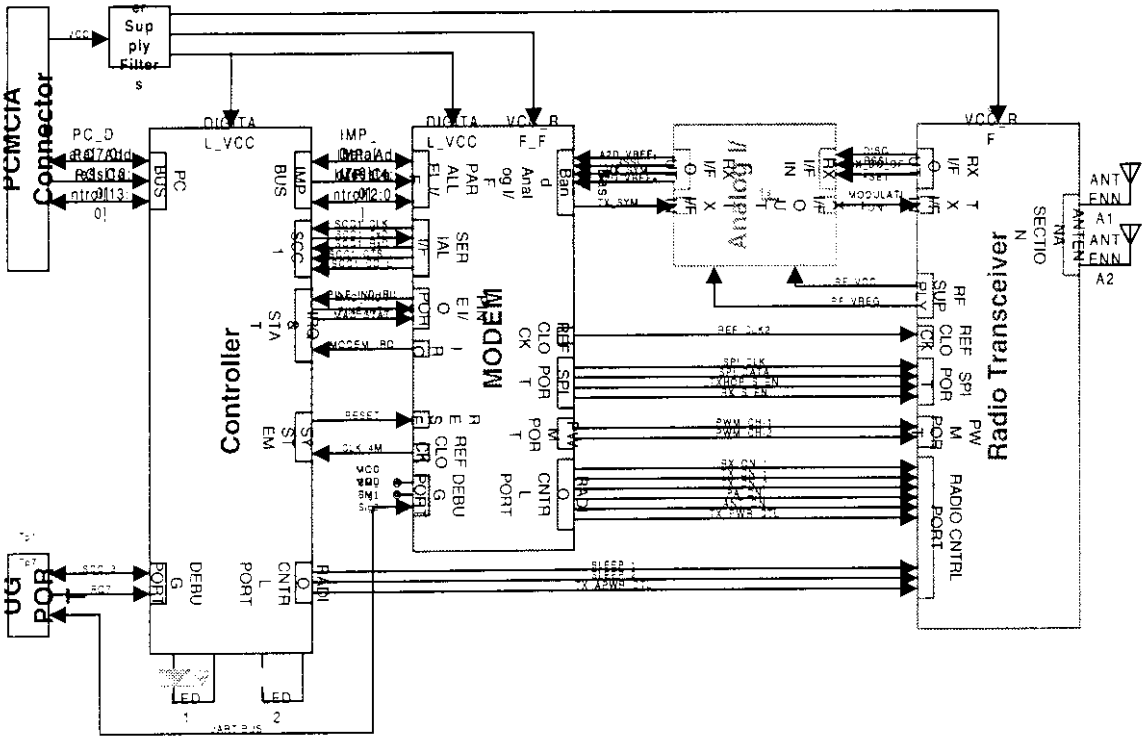

Figure 1

3. Block Diagram - RF Part.

3.1 Functions

The RF part has 2 main functions:

1. Modulate and transmit analog data.
2. Receive and demodulate the RF signals and forward these signals to the Baseband processor in analog form.

3.2 Oscillators.

There are three RF oscillators on the RF board:

1. Tx VCO (Modulator) which continuously operates at 880 MHz, In transmit mode the output of this modulator is divided by two.
2. Rx VCO serves as Local Oscillator for the second conversion, Operates at 463 MHz.
3. Hopping synthesizer, Operating in the frequency range of 1962 MHz to 2040 MHz, with step size of 1 MHz.

There is also a Reference Oscillator that operating at 40 MHz, Used as reference for all 3 VCOs. All 3 synthesizers are frequency locked by use of PLL.

3.3 Transmit Path.

The transmit path consists of a modulator operating at twice the IF frequency, Hopping VCO, Up converter, PA and Diversity switch.

In transmit mode the divider is operated and thus enabling the division of the modulator by 2. This signal is upconverted by mixing it with the hopping signal that operates as LO. The mixed signal that is now in the 2.4 GHz band is filtered and fed to the PA, filtered again and through the diversity switch feeds the antenna.

The modulating signal is a 2, 4 or 8 levels analog signal.

3.4 Receive Path.

The received signal is received in any of the antennas, selected by the diversity switch, filtered and transferred to the LNA, filtered again and down converted by mixing the received signal with the hoping synthesizer. The product has a 440 MHz IF where the signal is filtered and down converted to 23 MHz where it is demodulated into baseband signal. The baseband signal is filtered and transferred to the baseband processor (analog). The output signal is a 2, 4, or 8 levels analog signal with 500 kHz bandwidth.

The block diagram of the radio is shown in Fig. 2.

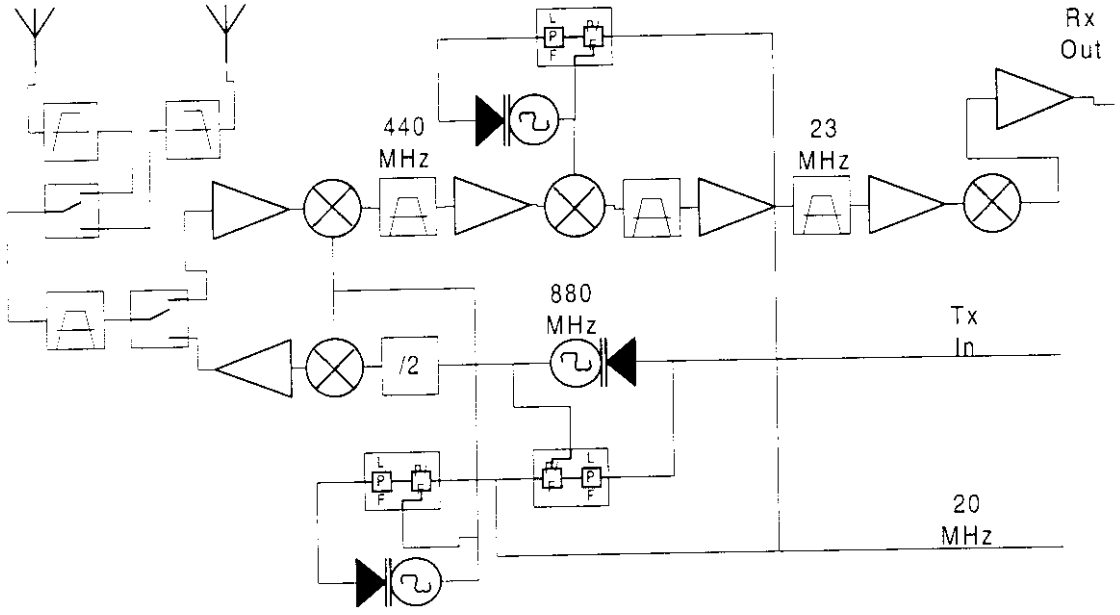

Figure 2

4. Block Diagram- Digital Section.

The Digital section consist of the following:

- 20Mhz CPU (683PM302) with internal PLL (external reference frequency 4MHz)
- 128Kx8 Flash memory
- 128Kx8 SRAM
- MODEM chip

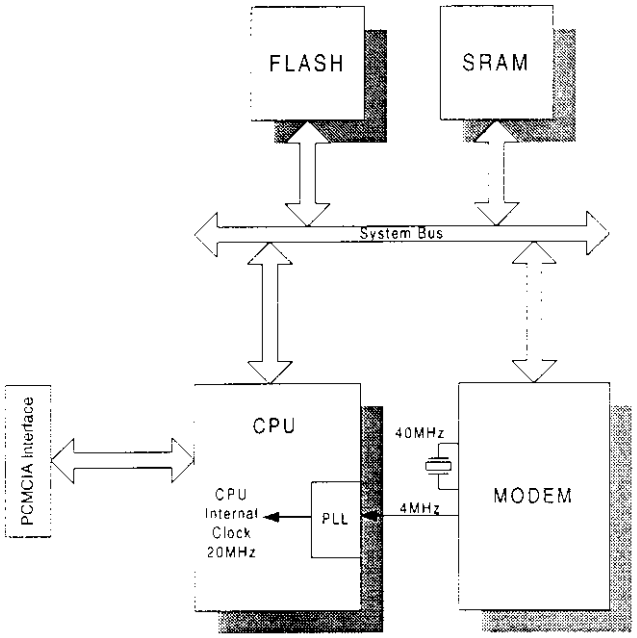

Figure 3

Clocking Method:

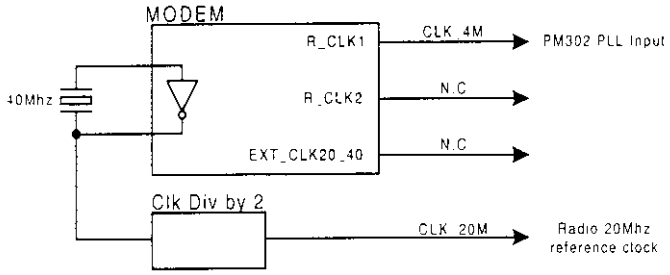

Figure 4

The MODEM chip is the system master clock, it is running from 40Mhz crystal (±10 / ±4 PPM tolerance / stability respectively). R_CLK1 default frequency is 4MHz witch is a division by 2.5 and 4 from the 40Mhz clock.