SARA-R5 series

Multi-band LTE-M / NB-IoT modules

System integration manual

Abstract

This document describes the features and the integration of the size-optimized SARA-R5 series cellular modules, based on the u-blox UBX-R5 cellular chipset. The modules are a size-optimized solution specifically designed for IoT, integrating an in-house developed cellular modem, end-to-end trusted domain security and u-blox's leading GNSS technology. The modules deliver high performance satellite positioning alongside data connectivity in the very small and compact SARA form factor.

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This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
SARA-R500S	SARA-R500S-00B-00	N.A.	N.A.	N.A.	Functional sample
SARA-R510S	SARA-R510S-00B-00	01.00	A00.01	UBX-20010454	Prototype
SARA-R510M8S	SARA-R510M8S-00B-00	01.00	A00.01	UBX-20010454	Prototype

Contents

1 System description

1.1 Overview

The SARA-R5 series LTE Cat M1 / NB2 modules are ideal solutions for IoT, in the miniature SARA LGA form factor (26.0 x 16.0 mm, 96-pin). They allow an easy integration into compact designs and a seamless drop-in migration from other u-blox cellular module families.

SARA-R5 series modules are form-factor compatible with u-blox LISA, LARA and TOBY cellular module families and are pin-to-pin compatible with u-blox SARA-N, SARA-G and SARA-U cellular module families. This facilitates migration from u-blox NB-IoT, GSM/GPRS, CDMA, UMTS/HSPA and other LTE modules, maximizes customer investments, simplifies logistics, and enables very short time-to-market. See Table 1 for a summary of the main features and interfaces.

Model	Region	RAT			Positioning				Interfaces							Features																Grade		
		3GPP Release Baseline	3GPP LTE category	LTE FDD bands	Integrated GNSS receiver	External GNSS control via modem	AssistNow software	CellLocate®	UART	USB	SPI	SDIO	DDC (I2C)	GPIOs	Digital audio (I2S)	Security services	Root of trust: secure element	Antenna dynamic tuning	CellTime®	Ultra-low power consumption in PSM	Embedded TCP/UDP stack	Embedded HTTP, FTP	Embedded TLS, DTLS	FW update via serial (FOAT)	u-blox Firmware update Over the Air (uFOTA)	LwM2M with dynamically loaded objects	Embedded MQTT, MQTT-SN	Embedded CoAP	Last gasp	Jamming detection	Antenna and SIM detection	Standard	Professional	Automotive
SARA-R500S	Multi Region	14	M1 NB2	*		•	•	•	•	•	○	○	•	•	○	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•		•	
SARA-R510S	Multi Region	14	M1 NB2	*		•	•	•	•	•	○	○	•	•	○	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	
SARA-R510M8S	Multi Region	14	M1 NB2	*	•		•	•	•	•	○	○	•	•	○	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•		•	

* = LTE Bands 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 26, 28 in M1 and NB2, LTE band 25 in M1-only, and LTE bands 66, 71, 85 in NB2-only

• = supported by all FW versions ○ = supported by future FW versions

Table 1: SARA-R5 series main features summary

☞ The “00” products version of the SARA-R5 series modules do not support LTE category NB2.

With a discrete, hardware-based secure element and a lightweight pre-shared key management system, u-blox offers state-of-the-art security that is ideal for IoT applications and includes data encryption and decryption, zero touch provisioning, anti-cloning, and secure chip-to-chip communication. SARA-R5 series modules are the optimal choice for LPWA applications with low to medium data throughput rates, as well as devices that require long battery lifetimes, such as used in smart metering, smart cities, telematics, and connected health.

The modules support handover capability and delivers the technology necessary for use in applications such as vehicle, asset and people tracking where mobility is a pre-requisite. Other applications where the modules are well-suited include and are not limited to: smart home, security systems, industrial monitoring and control.

The modules support multi-band data communication over an extended operating temperature range of –40 to +85 °C, with extremely low power consumption, and with coverage enhancement for deeper range into buildings and basements (and underground with NB2).

SARA-R5 series modules include the following variants / product versions:

- SARA-R500S LTE Cat M1 / NB2 module for multi-region use, cost effective solution for devices that do not need to reach ultra-low power consumption in deep-sleep power saving mode (PSM)
- SARA-R510S LTE Cat M1 / NB2 module for multi-region use, designed to achieve extremely low current consumption in deep-sleep power saving mode (PSM)
- SARA-R510M8S LTE Cat M1 / NB2 module for multi-region use, integrating the u-blox M8 GNSS receiver for global position acquisition

Table 2 summarizes cellular and GNSS characteristics of the modules.

Item	SARA-R500S	SARA-R510S	SARA-R510M8S
Cellular protocol stack	3GPP release 14	3GPP release 14	3GPP release 14
Cellular RAT	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex
Cellular LTE FDD bands	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) [1] Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) [2] Band 71 (600 MHz) [2] Band 85 (700 MHz) [2]	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) [1] Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) [2] Band 71 (600 MHz) [2] Band 85 (700 MHz) [2]	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) [1] Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) [2] Band 71 (600 MHz) [2] Band 85 (700 MHz) [2]
Cellular power class	LTE power class 3 (23 dBm)	LTE power class 3 (23 dBm)	LTE power class 3 (23 dBm)
Cellular data rate	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL
GNSS receiver	-	-	72-channel u-blox M8 engine GPS L1C/A, SBAS L1C/A, QZSS L1C/A, QZSS L1-SAIF, GLONASS L1OF, BeiDou B1I, Galileo E1B/C

Table 2: SARA-R5 series modules cellular and GNSS characteristics summary

☞ The "00" products version of the SARA-R5 series modules do not support LTE category NB2.

☞ See Table 39 for the detailed list of RATs and bands included in each certification approval of the SARA-R5 series modules product versions.

[1] Not supported in LTE category NB2
[2] Not supported in LTE category M1

1.2 Architecture

Figure 1, Figure 2 and Figure 3 summarize the internal architecture of the SARA-R500S modules, the one of the SARA-R510S modules, and the one of the SARA-R510M8S modules respectively.

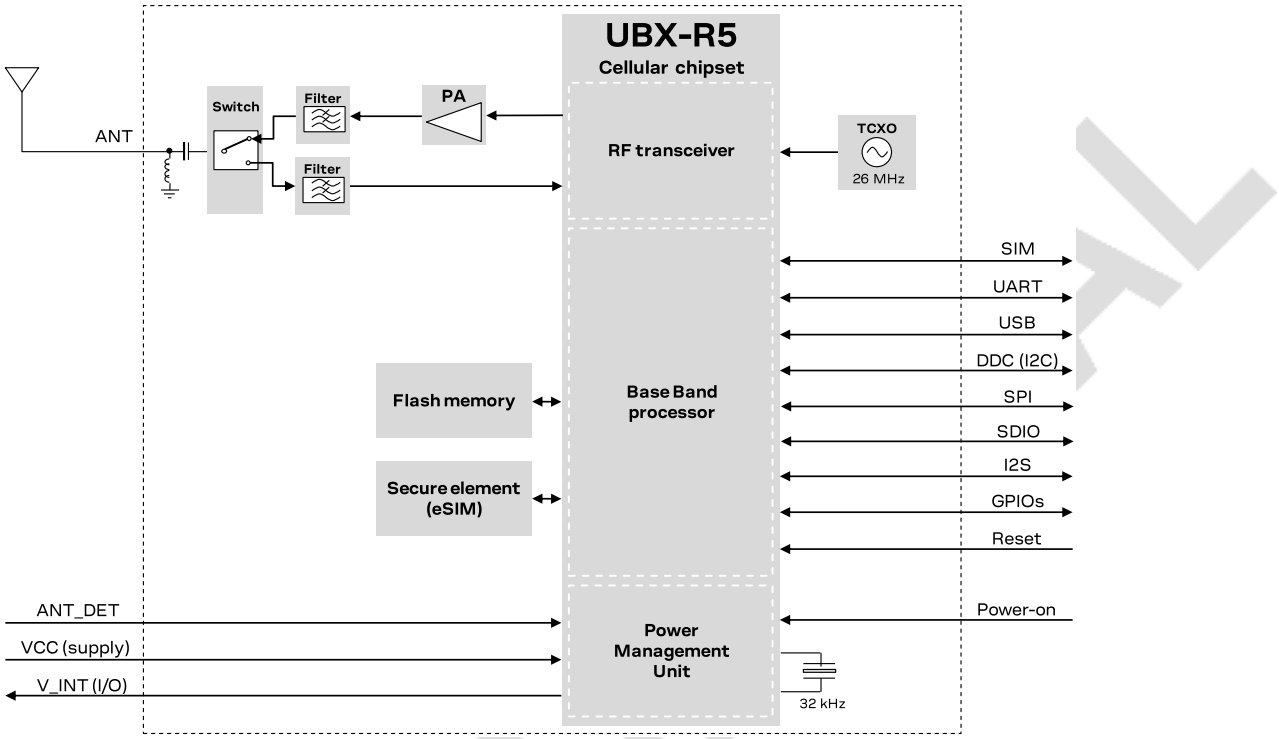

Figure 1: SARA-R500S block diagram

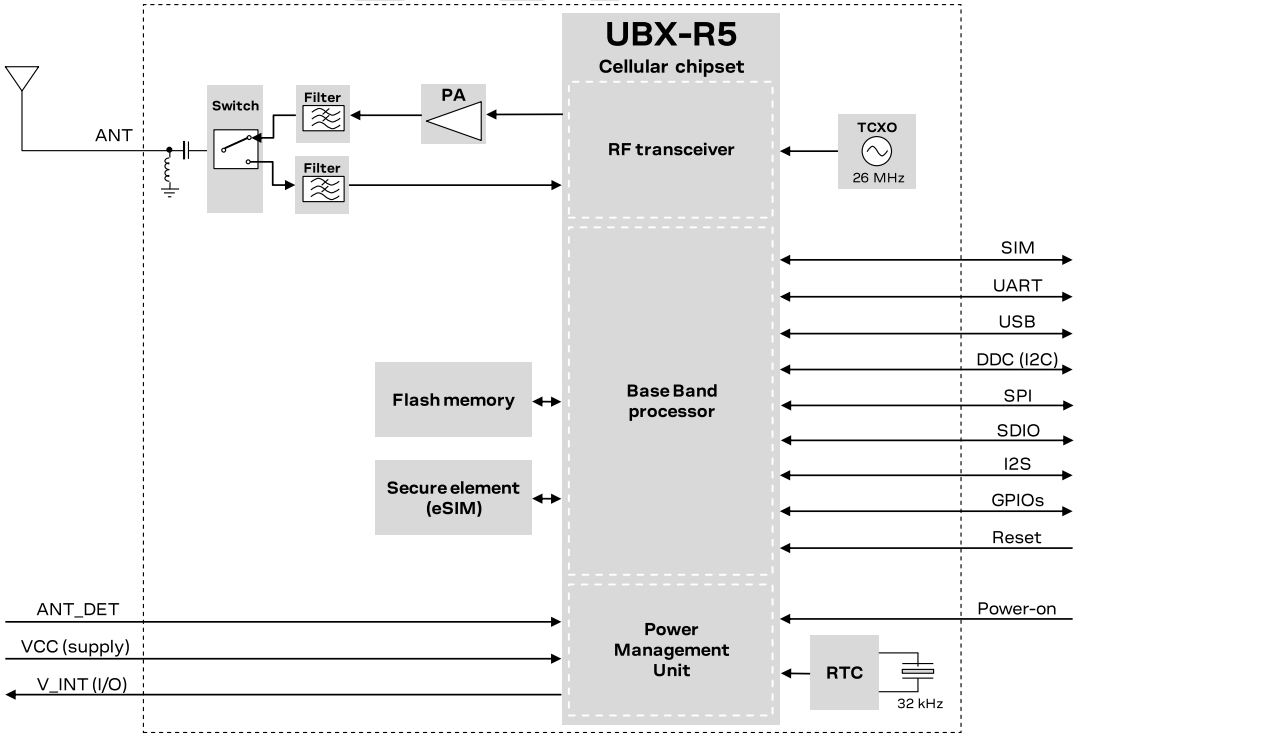

Figure 2: SARA-R510S block diagram

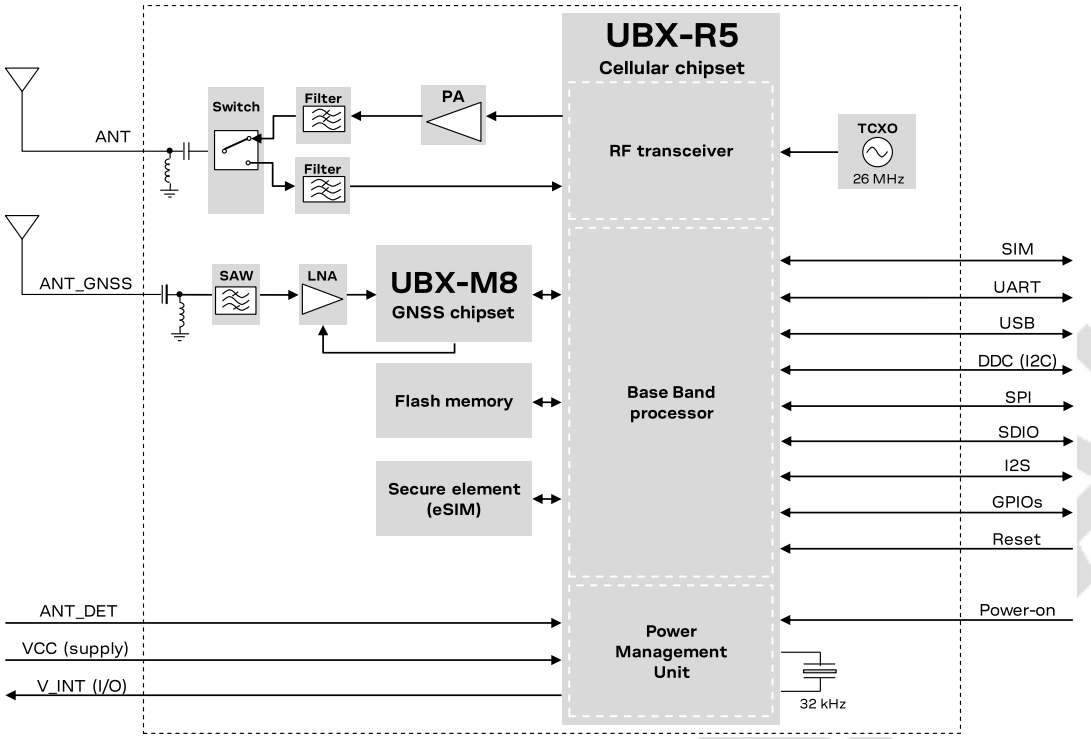

Figure 3: SARA-R510M8S block diagram

The "00" product version of the SARA-R5 series modules do not support the following interfaces, which should be left unconnected and should not be driven by external devices:

- SPI interface
- SDIO interface
- Digital audio (I2S) interface

SARA-R5 series modules internally consist of the following sections described herein with more details than the simplified block diagrams of Figure 1, Figure 2 and Figure 3.

RF section

The RF section is composed of the following main elements:

- RF switch connecting the antenna port (**ANT**) to the suitable RF Tx / Rx paths for LTE Cat M1 / NB2 Half-Duplex operations
- Power Amplifiers (PA) amplifying the Tx signal modulated and pre-amplified by the RF transceiver
- RF filters along the Tx and Rx signal paths providing RF filtering
- RF transceiver integrated in the u-blox UBX-R5 cellular chipset, performing modulation, up-conversion and pre-amplification of the baseband signals for LTE transmission, and performing down-conversion and demodulation of the RF signal for LTE reception
- 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) generating the reference clock signal for the RF transceiver, the Base-Band system and the GNSS system, when the related system is in active mode or connected mode.

Base-Band and Power Management section

The Base-Band and Power Management section, based on the u-blox UBX-R5 cellular chipset, is composed of the following main elements:

- On-chip modem processor, vector signal processor, with dedicated hardware assistance for signal processing and system timing
- On-chip modem processor, with interfaces control functions
- On-chip voltage regulators to derive all the internal or external (**V_SIM**, **V_INT**) supply voltages from the module supply input **VCC**
- On-chip cryptographic hardware acceleration with Root of Trust
- On-chip memory system, including pSRAM and secure boot ROM
- Dedicated flash memory IC
- Dedicated secure element
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle mode, which can be enabled using the +UPSV AT command, and in the PSM deep-sleep mode, which can be enabled using the +CPSMS in addition to the +UPSV AT command

GNSS section

The GNSS section, based on the u-blox UBX-M8 GNSS chipset, is composed of the following main elements illustrated in Figure 4:

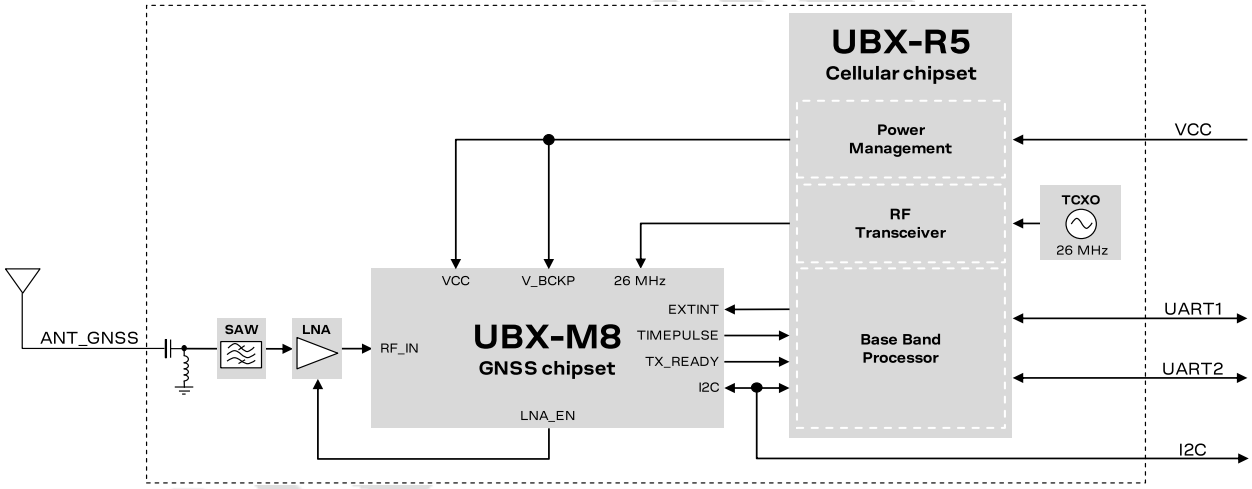

Figure 4: SARA-R510M8S modules GNSS section block diagram

1.3 Pin-out

Table 3 lists the pin-out of the SARA-R5 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	VCC	51, 52, 53	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	1, 3, 5, 14, 20-22, 30, 32, 43, 50, 54, 55, 57-61, 63-96	N/A	Ground	GND pins are internally connected to each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	4	O	Generic digital interfaces supply output	V_INT = 1.8 V (typical) generated by internal regulator when the module is switched on, outside the low power PSM deep-sleep mode. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in. Provide test point for diagnostic purposes.
System	PWR_ON	15	I	Power-on input	Internal active pull-up. See sections 1.6.1, 1.6.2 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for diagnostic purposes.
	RESET_N	18	I	External reset input	Internal active pull-up. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in. Provide test point for diagnostic purposes.
Antenna	ANT	56	I/O	Cellular antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4.2 for external circuit design-in.
	ANT_GNSS	31	I	GNSS antenna [3]	50 Ω nominal characteristic impedance. See section 1.7.2 for functional description / requirements. See section 2.4.3 for external circuit design-in.
	ANT_DET	62	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.3 for functional description. See section 2.4.4 for external circuit design-in.
SIM	VSIM	41	O	SIM supply output	VSIM = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM. Internal pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	Clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.

[3] Not supported by SARA-R500S and SARA-R510S modules

Function	Pin Name	Pin No	I/O	Description	Remarks
UART	RXD	13	O	UART data output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 104 (RxD) in ITU-T V.24, for AT, data, Mux, FOAT, FW update via u-blox EasyFlash tool. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	12	I	UART data input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 103 (TxD) in ITU-T V.24, for AT, data, Mux, FOAT, FW update via u-blox EasyFlash tool. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	11	O	UART clear to send output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART request to send input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O/I	UART data set ready output / AUX UART request to send input	USIO variant 0: Pin disabled USIO variant 1: Primary UART circuit 107 (DSR) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O	UART ring indicator output / AUX UART clear to send output	USIO variants 0 / 1: Primary UART circuit 125 (RI) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I	UART data terminal ready input / AUX UART data input	USIO variants 0 / 1: Primary UART circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up enabled. USIO variants 2 / 3 / 4: Auxiliary UART circuit 103 (TxD) in ITU-T V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	8	O	UART data carrier detect output / AUX UART data output	USIO variant 0: Pin disabled. USIO variant 1: Primary UART circuit 109 (DCD) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 104 (RxD) in ITU-T V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
USB	VUSB_DET	17	I	USB detect input	VBUS USB supply generated by the host must be connected to this input pin to enable the USB interface. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
	USB_D-	28	I/O	USB Data Line D-	USB interface for diagnostics. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors, as required by the USB 2.0 specification [4], are part of the USB pin driver and shall not be provided externally. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
	USB_D+	29	I/O	USB Data Line D+	USB interface for diagnostics. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors, as required by the USB 2.0 specification [4], are part of the USB pin driver and shall not be provided externally. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
SPI	SDIO_D0	47	I/O	SPI MOSI	SPI Master Output Slave Input, alternatively settable as SDIO. Not supported by “00” product version, except for diagnostics.
	SDIO_D1	49	I/O	SPI MISO	SPI Master Input Slave Output, alternatively settable as SDIO Not supported by “00” product version, except for diagnostics.
	SDIO_D2	44	I/O	SPI clock	SPI clock, alternatively configurable as SDIO. Not supported by “00” product version, except for diagnostics.
	SDIO_D3	48	I/O	SPI Chip Select	SPI Chip Select, alternatively configurable as SDIO. Not supported by “00” product version, except for diagnostics.
SDIO	SDIO_D0	47	I/O	SDIO serial data [0]	SDIO serial data [0], alternatively configurable as SPI MOSI. Not supported by “00” product version.
	SDIO_D1	49	I/O	SDIO serial data [1]	SDIO serial data [1], alternatively configurable as SPI MISO. Not supported by “00” product version.
	SDIO_D2	44	I/O	SDIO serial data [2]	SDIO serial data [2], alternatively configurable as SPI clock. Not supported by “00” product version.
	SDIO_D3	48	I/O	SDIO serial data [3]	SDIO serial data [3], alternatively settable as SPI Chip Select. Not supported by “00” product version.
	SDIO_CLK	45	O	SDIO serial clock	SDIO serial clock. Not supported by “00” product version.
	SDIO_CMD	46	I/O	SDIO command	SDIO command, alternatively configurable by AT+UGPIOC. Not supported by “00” product version.
DDC	SCL	27	O	I2C bus clock line	Fixed open drain, for communication with I2C-slave devices. Internal active pull-up: external pull-up is not required. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDA	26	I/O	I2C bus data line	Fixed open drain, for communication with I2C-slave devices. Internal active pull-up: external pull-up is not required. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
Audio	I2S_TXD	35	O	I2S transmit data	I2S transmit data. Not supported by “00” product version. Alternatively configurable by +UGPIOC AT command.
	I2S_RXD	37	I	I2S receive data	I2S receive data. Not supported by “00” product version.
	I2S_CLK	36	I/O	I2S clock	I2S clock. Not supported by “00” product version.
	I2S_WA	34	I/O	I2S word alignment	I2S word alignment. Not supported by “00” product version. Alternatively configurable by +UGPIOC AT command.
GPIO	GPIO1	16	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	23	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	24	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	25	I/O	GPIO / Time stamp output [4]	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO5	42	I/O	Pin for SIM card detection	See sections 1.8.2 and 1.11 for functional description. See sections 2.5 and 2.8 for external circuit design-in.
	GPIO6	19	I/O	GPIO / Time pulse output	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	I2S_TXD	35	O	Pin for antenna dynamic tuning	Configurable as output for antenna dynamic tuning. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	I2S_WA	34	O	Pin for antenna dynamic tuning	Configurable as output for antenna dynamic tuning. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	EXT_INT	33	I	External interrupt	Configurable as interrupt input triggering the generation of an URC time stamp. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	SDIO_CMD	46	I	External time pulse input [4]	Configurable as input for external GNSS time pulse. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
Reserved	RSVD	2	N/A	Reserved pin	Leave unconnected. See sections 1.12 and 2.9.

Table 3: SARA-R5 series modules pin definition, grouped by function

[4] Not supported by SARA-R510M8S modules

1.4 Operating modes

SARA-R5 series modules have several operating modes as defined in Table 4.

General Status	Operating Mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal operation	**Deep-sleep mode**	RTC runs with 32 kHz reference internally generated.
	Idle mode	Module processor runs with 32 kHz reference internally generated.
	Active mode	Module processor runs with 26 MHz reference internally generated.
	Connected mode	RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.

Table 4: SARA-R5 series modules operating modes definition

Figure 5 describes the transition between the different operating modes.

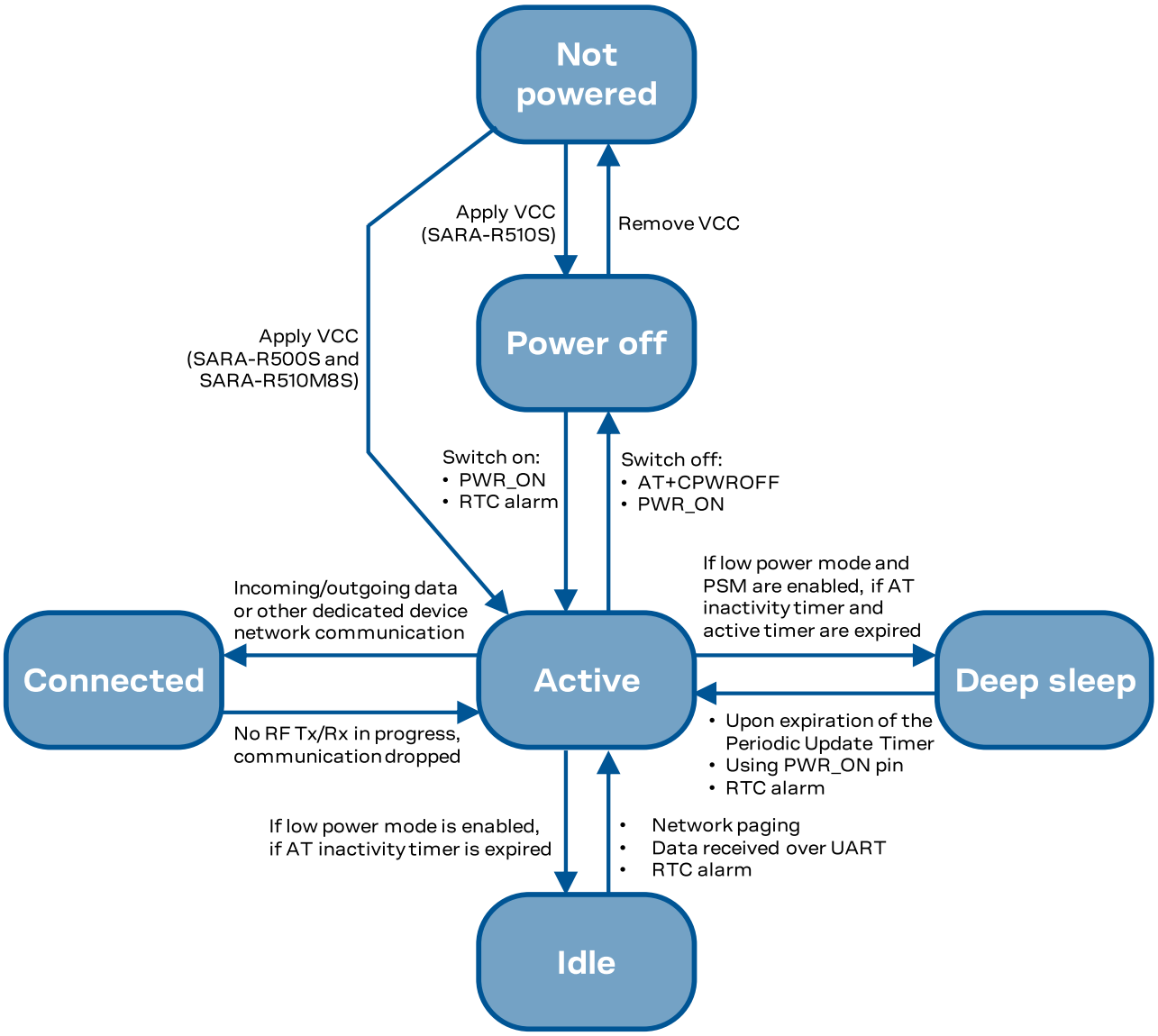

Figure 5: SARA-R5 series modules operating modes transitions

The initial operating mode of SARA-R5 series modules is the one with **VCC** supply not present or below the operating range: the modules are switched off in not-powered mode.

Once a valid **VCC** supply is applied to the SARA-R500S and the SARA-R510M8S modules, this event triggers the switch on routine of the modules that subsequently enter the active mode.

Instead, once a valid **VCC** supply is applied to the SARA-R510S modules, they remain switched off in power-off mode. Then the proper toggling of the **PWR_ON** input line is necessary to trigger the switch on routine of the modules that subsequently enter the active mode.

SARA-R5 series modules are fully ready to operate when in active mode: the available communication interfaces are completely functional and the module can accept and respond to any AT command, entering connected mode upon LTE signal reception / transmission.

The internal GNSS functionality can be concurrently enabled on the SARA-R510M8S modules by the dedicated +UGPS AT command, as well as the possible external GNSS functionality can be concurrently enabled using SARA-R500S or SARA-R510S modules by the dedicated +UGPS AT command.

Then, the SARA-R5 series modules switch from active mode to the low power idle mode whenever possible, if the low power configuration is enabled by the dedicated +UPSV AT command. The low power idle mode can last for different time periods according to the specific +UPSV AT command setting, according to the specific +CEDRXS / +CEDRXRDP AT commands setting, and according to the concurrent activities executed by the module, as for example according to the concurrent GNSS activities.

Then, after having enabled the low power configuration by the dedicated +UPSV AT command, according to the +CPSMS / +UCPSMS AT commands setting, and according to the concurrent activities executed by the module (for example according to the concurrent GNSS activities), whenever possible the SARA-R500S and SARA-R510M8S modules can enter the PSM deep-sleep mode and the SARA-R510S modules can enter the ultra-low power PSM deep-sleep mode.

Once the modules enter the PSM deep-sleep mode (SARA-R500S and SARA-R510M8S modules) or the ultra-low power PSM deep-sleep mode (SARA-R510S modules), the available communication interfaces are not functional: a wake up event, consisting in proper toggling of the **PWR_ON** input line, the expiration of the “Periodic Update Timer” set by the LTE network, or the expiration of an RTC alarm, is necessary to trigger the wake up routine of the modules that subsequently enter back into the active mode.

SARA-R5 series modules can be gracefully switched off by the dedicated +CPWROFF AT command, or by proper toggling of the **PWR_ON** input line.

☞ See the SARA-R5 series AT commands manual [2], +UPSV, +CEDRXS, +CEDRXRDP, +CPSMS, +UCPSMS, +UGPS, +CALA, +CPWROFF AT commands, for the possible configurations and settings of different operating modes.

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

Voltage must be stable, because during operation, the current drawn by the SARA-R5 series modules through the **VCC** pins may vary significantly, depending on the operating mode and state (as described in sections 1.5.1.2, 1.5.1.3, 1.5.1.4 and 1.5.1.5).

It is important that the supply source is able to withstand the average current consumption occurring during Tx / Rx call at maximum RF power level (see the SARA-R5 series data sheet [1]).

The 3 **VCC** pins of SARA-R5 series modules are internally connected each other to both the internal Power Amplifier and the internal baseband Power Management Unit.

Figure 6 provides a simplified block diagram of SARA-R5 series modules' internal VCC supply routing.

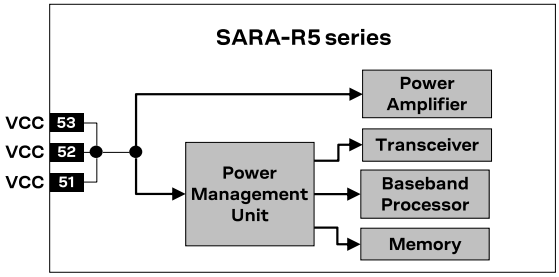

Figure 6: Block diagram of SARA-R5 series modules' internal VCC supply routing

1.5.1.1 VCC supply requirements

Table 5 summarizes the requirements for the VCC modules supply. See section 2.2.1 for suggestions to correctly design a **VCC** supply circuit compliant with the requirements listed in Table 5.

⚠ The supply circuit affects the RF compliance of the device integrating SARA-R5 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in the Table 5 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.3 V / 4.4 V	RF performance is guaranteed when **VCC** voltage is inside the normal operating range limits. RF performance may be affected when **VCC** voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.0 V / 4.5 V	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.

Item	Requirement	Remark
VCC current	Support with adequate margin the highest averaged **VCC** current consumption value during Tx conditions specified in the SARA-R5 series data sheet [1]	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Section 1.5.1.2 describes current consumption profiles in connected mode.
VCC voltage ripple	Noise in the supply pins must be minimized	High supply voltage ripple values during RF transmissions in connected mode directly affect the RF compliance with the applicable certification schemes.

Table 5: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in LTE connected mode

During an LTE connection, the SARA-R5 series modules transmit and receive in half duplex mode.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

Figure 7 shows an example of SARA-R5 series modules' current consumption profile versus time in connected mode: transmission is enabled for one sub-frame (1 ms) according to LTE Category M1 half-duplex connected mode.

Detailed current consumption values can be found in the SARA-R5 series data sheet [1].

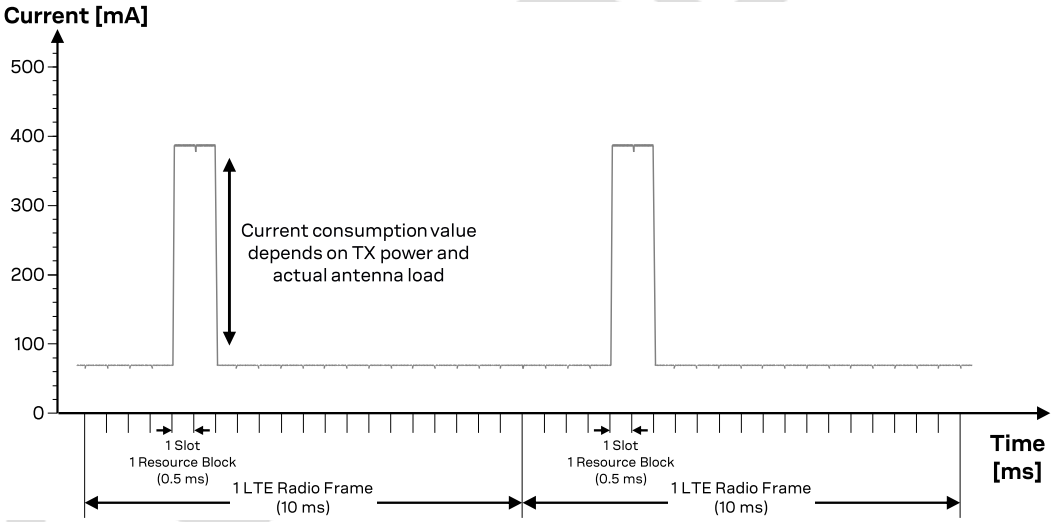

Figure 7: VCC current consumption profile versus time during LTE Cat M1 half-duplex connection

1.5.1.3 VCC consumption in deep-sleep mode (low power mode and PSM enabled)

The low power mode and the PSM configurations are by default disabled, but they can be enabled using the +UPSV and +CPSMS AT commands (see the SARA-R5 series AT commands manual [2]).

When low power mode and PSM are enabled, whenever possible the modules automatically enter the PSM deep-sleep mode (SARA-R500S and SARA-R510M8S modules) or the ultra-low power PSM deep-sleep mode (SARA-R510S), reducing current consumption down to the lowest steady value: only the RTC runs with internal 32 kHz reference clock frequency.

1.5.1.4 VCC current consumption in low power idle mode (low power mode enabled)

The low power mode configuration is by default disabled, but it can be enabled using the +UPSV AT command (see the SARA-R5 series AT commands manual [2]).

When low power mode is enabled, the module automatically enters the low power idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G / LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power mode. This is known as discontinuous reception (DRX) or extended discontinuous reception (eDRX).

1.5.1.5 VCC current consumption in active mode (low power mode and PSM disabled)

The active mode is the state where the module is switched on and ready to communicate with an external device by means of the application interfaces (as the UART serial interface). The module processor core is active and the 26 MHz reference clock frequency is used.

If low power mode configuration is disabled, as it is by default (see the SARA-R5 series AT commands manual [2], +UPSV AT commands for details), the module remains in active mode. Otherwise, if low power mode configuration is enabled, the module enters low power idle mode (and deep-sleep mode power saving mode, if enabled) whenever possible.

Figure 8 shows a typical example of the module current consumption profile when the module is in active mode. Here, the module is registered with the network and, while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception.

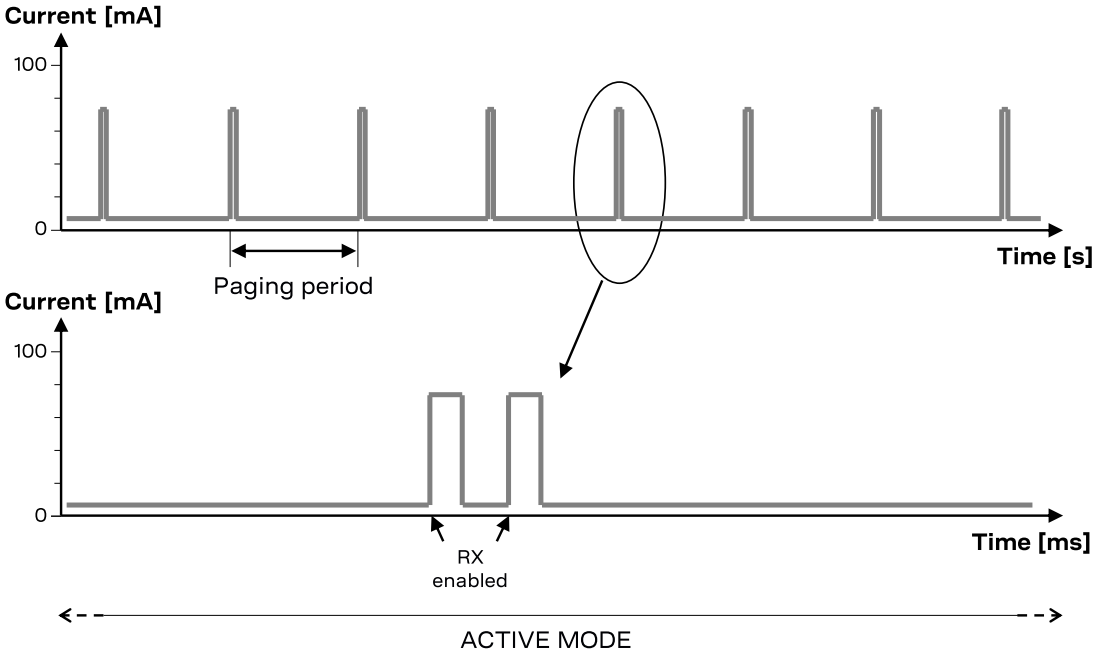

Figure 8: VCC current consumption profile with low power mode disabled and module registered with the network: active mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 Generic digital interfaces supply output (V_INT)

The same voltage domain internally used as supply for the generic digital interfaces of SARA-R5 series modules is also available on the **V_INT** output pin, as illustrated in Figure 9.

The internal regulator that generates the **V_INT** supply output is a switching (DC-DC) converter, which is directly supplied from the **VCC** main supply input of the module.

The **V_INT** voltage regulator output of SARA-R5 series modules is disabled (i.e. 0 V) when the module is switched off, and it can be used to monitor the operating mode of the module as follows:

- When the module is off, or in deep-sleep mode, the voltage level is low (i.e. 0 V)
- When the module is on, outside deep-sleep mode, the voltage level is high (i.e. 1.8 V)

The current capability is specified in the SARA-R5 series data sheet [1]. The **V_INT** voltage domain can be used in place of an external discrete regulator as a reference voltage rail for external components.

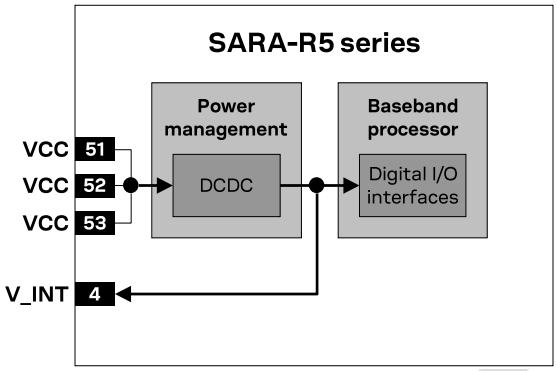

Figure 9: SARA-R5 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

1.6.1.1 Switch-on events

When the SARA-R500S and SARA-R510M8S modules are in the not-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch on routine can be triggered by:

- Applying a voltage at the **VCC** module supply input within the operating range (see SARA-R5 series data sheet [1]).

When the SARA-R510S modules are in the not-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch on routine can be triggered by:

- Applying a voltage at the **VCC** module supply input within the operating range (see SARA-R5 series data sheet [1]), and then forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period.

When the SARA-R5 series modules are in the power-off mode (i.e. switched off, but with a valid voltage present at the **VCC** module supply input) or in deep-sleep mode, they can be switched on or they can be woken up as following:

- Forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period.

As illustrated in Figure 10, the **PWR_ON** input pin is equipped with an internal pull-up resistor. Detailed electrical characteristics with voltages and timings are described in the SARA-R5 series data sheet [1].

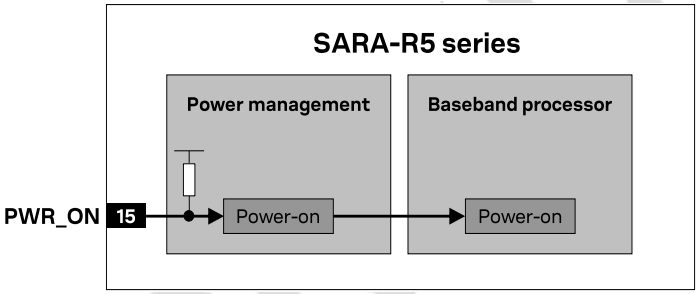

Figure 10: SARA-R5 series PWR_ON input equivalent circuit description

1.6.1.2 Switch-on sequence from not-powered mode

Figure 11 shows the SARA-R500S / SARA-R510M8S switch-on sequence from the not-powered mode:

- The external power supply is applied to the **VCC** module pins, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see SARA-R5 series AT commands manual [2])
- The module is fully ready to operate after all interfaces are configured.

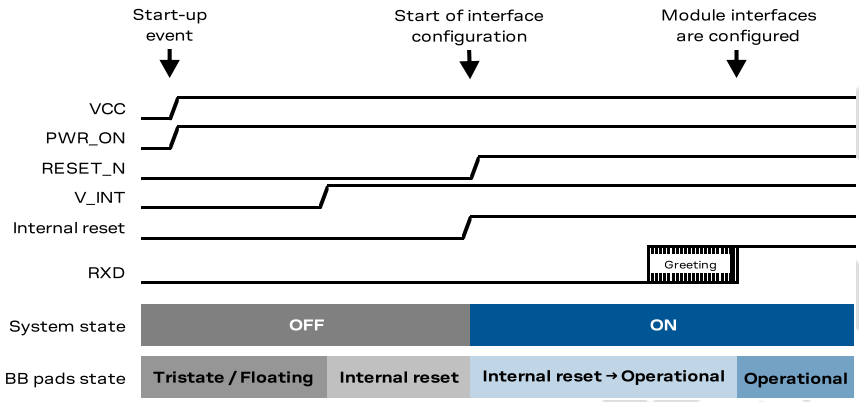

Figure 11: SARA-R500S / SARA-R510M8S switch-on sequence description from not-powered mode

Figure 12 shows the SARA-R510S modules switch-on sequence from the not-powered mode:

- The external power supply is applied to the **VCC** module pins
- The **PWR_ON** pin is held low for a valid time, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see SARA-R5 series AT commands manual [2])
- The module is fully ready to operate after all interfaces are configured.

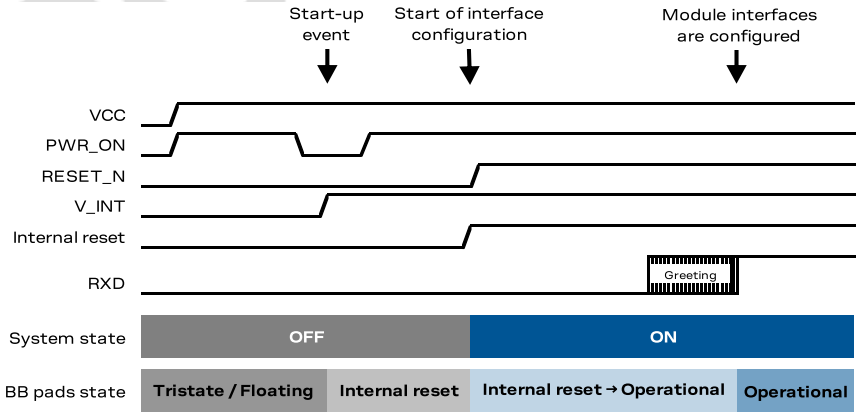

Figure 12: SARA-R510S switch-on sequence description from not-powered mode

1.6.1.3 Switch-on / wake-up sequence from power-off / deep-sleep mode

Figure 13 shows the SARA-R5 series modules switch-on or wake-up sequence from the power-off or deep-sleep mode:

- The external power supply is still applied to the VCC module pins, with the module being previously switched off (by means of the +CPWROFF AT command or by proper PWR_ON pin toggling), or with the module being previously entered deep-sleep mode.
- The PWR_ON pin is held low for a valid time, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (V_INT).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the RXD pin (for more details, see SARA-R5 series AT commands manual [2])
- The module is fully ready to operate after all interfaces are configured.

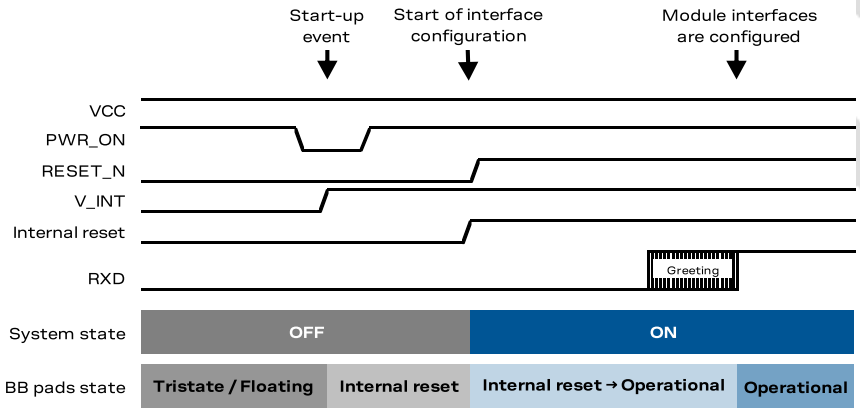

Figure 13: SARA-R5 series switch-on / wake-up sequence description from power-off / deep-sleep mode

1.6.1.4 General considerations for the switch-on procedure

If the greeting text is not used by the external application to detect that the module is ready to reply to AT commands, then the only way of checking it is polling: the external application can start sending "AT" after that the **CTS** line is set to the ON state (in case UART is used as AT interface with HW flow control enabled as default), but any AT command sent before the time when the module is ready to reply may be not buffered and may be lost.

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:

- the **V_INT** pin, to sense the start of the SARA-R5 series module switch-on sequence
- the **GPIO** pin configured to provide the module status indication or module operating mode indication (see SARA-R5 series AT commands manual [2], +UGPIOC), to sense when the module is ready to operate

☞ Before the switch-on of the generic digital interface supply (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ The duration of the SARA-R5 series modules' switch-on routine can vary depending on the application / network settings and the concurrent module activities.

1.6.2 Module power-off

1.6.2.1 Switch-off events

SARA-R5 series modules can be gracefully switched off, triggering the storage of the current parameter settings in the non-volatile memory of the module and performing a clean network detach procedure, by:

- +CPWROFF AT command (see SARA-R5 series AT commands manual [2]).
- Forcing a low pulse on the **PWR_ON** pin (normally high due to internal pull-up) for a valid time period (see the SARA-R5 series data sheet [1]).

A fast emergency shutdown procedure of the modules, without storage of the current parameter settings in the module's non-volatile memory and without proper network detach, can be triggered by:

- Toggling the GPIO input pin configured with fast emergency shutdown function (see section 1.11)

An abrupt under-voltage shutdown occurs on SARA-R5 series modules when the **VCC** supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-R5 series modules normal operations.

1.6.2.2 Switch-off sequence by +CPWROFF AT command

Figure 14 describes the switch-off sequence of the modules started by the +CPWROFF AT command, allowing storage of parameter settings in the non-volatile memory and a clean network detach:

- When the +CPWROFF AT command is sent the module starts the switch-off routine.
- Then the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch-on event does not occur (e.g. applying a low level to **PWR_ON**), or enters not-powered mode if the **VCC** supply is removed.

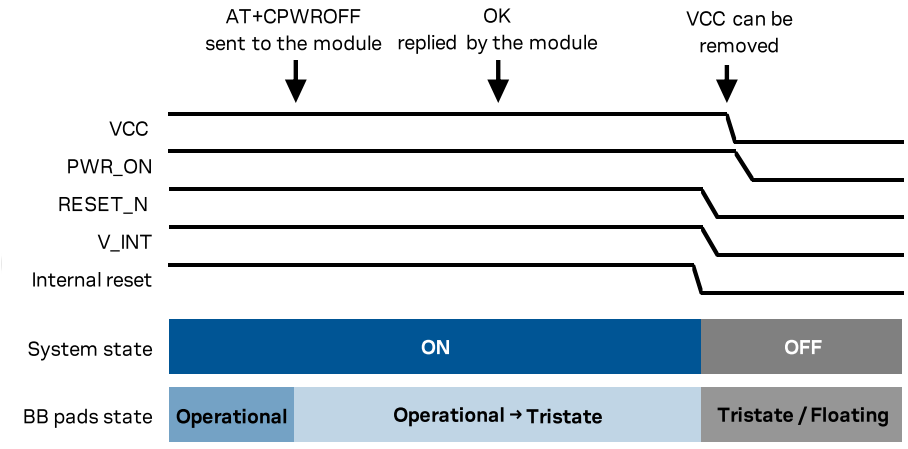

Figure 14: SARA-R5 series modules switch-off sequence by means of +CPWROFF AT command

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ The duration of each phase in the SARA-R5 series modules' switch-off routines can largely vary, depending on the application / network settings and the concurrent module activities.

1.6.2.3 Switch-off sequence by PWR_ON input pin

Figure 15 describes the switch-off sequence of the modules started by the **PWR_ON** input pin, allowing storage of parameter settings in the non-volatile memory and a clean network detach:

- When a low pulse with appropriate time duration is applied at the **PWR_ON** input pin (see the SARA-R5 series data sheet [1]), the module starts the switch-off routine.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch on event does not occur (e.g. applying a low level to **PWR_ON**), or enters not-powered mode if the **VCC** supply is removed.

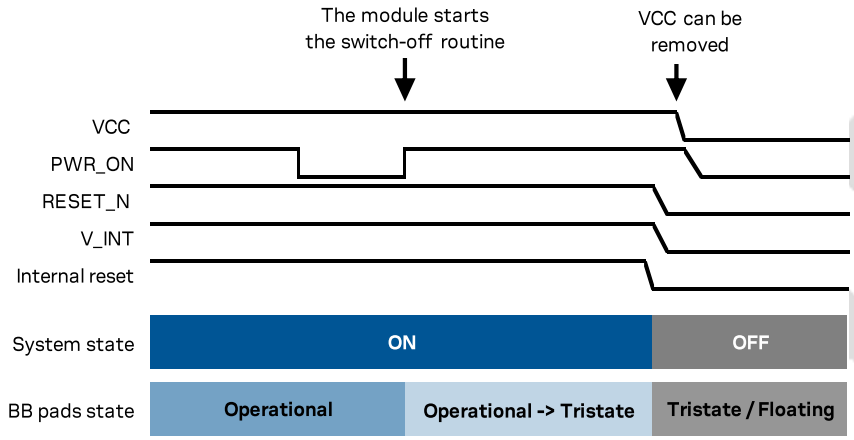

Figure 15: SARA-R5 series modules switch-off sequence by means of PWR_ON input pin

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ The duration of each phase in the SARA-R5 series modules' switch-off routines can largely vary, depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

SARA-R5 series modules can be gracefully reset (re-booted), triggering the storage of the current parameter settings in the non-volatile memory of the module and performing a clean network detach procedure, by:

- +CFUN AT command (see SARA-R5 series AT commands manual [2]).

An abrupt software reset of the modules, without storage of the current parameter in the module's non-volatile memory and without proper network detach, can be triggered by:

- Forcing a low pulse on the **RESET_N** pin (normally high due to internal pull-up) for a valid time period (see the SARA-R5 series data sheet [1]).

An abrupt emergency hardware reset of the modules, without storage of the current parameter in the module's non-volatile memory and without proper network detach, can be triggered by:

- Forcing a low pulse on the **PWR_ON** pin (normally high due to internal pull-up) for a valid time period (higher than the period for the graceful switch-off, see the SARA-R5 series data sheet [1]).

☞ It is highly recommended to avoid an abrupt emergency hardware reset during module normal operation: this should be used only if software reset (via AT commands or via **RESET_N** pin) or graceful switch-off (via AT commands or via **PWR_ON** pin) fails.

As described in Figure 16, the **RESET_N** input pin is directly connected to the processor core, with an integrated active pull-up, in order to perform an abrupt software reset when asserted, excluding the power management unit. Detailed electrical characteristics with voltages and timings are described in the SARA-R5 series data sheet [1].

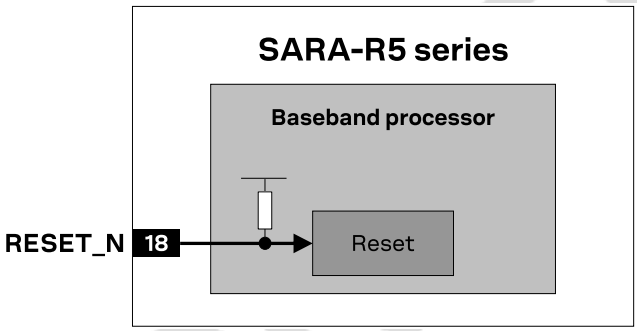

Figure 16: SARA-R5 series RESET_N input equivalent circuit description

1.7 Antenna interfaces

1.7.1 Cellular antenna RF interface (ANT)

SARA-R5 series modules provide an RF interface for connecting the external cellular antenna. The **ANT** pin represents the RF input/output for transmission and reception of LTE RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the Tx / Rx cellular antenna through a 50 Ω transmission line to allow proper RF transmission and reception.

1.7.1.1 Cellular antenna RF interface requirements

Table 6 summarizes the requirements for the cellular antenna RF interface. See section 2.4.2 for suggestions to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating SARA-R5 series modules with applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interface requirements summarized in Table 6 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency range	See the SARA-R5 series data sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits.
Input power	> 24 dBm (> 0.25 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 6: Summary of cellular antenna RF interface requirements

1.7.2 GNSS antenna RF interface (ANT_GNSS)

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

SARA-R510M8S modules provide an RF interface for connecting the external GNSS antenna. The **ANT_GNSS** pin represents the RF input reception of GNSS RF signals.

The **ANT_GNSS** pin has a nominal characteristic impedance of 50 Ω and must be connected to the Rx GNSS antenna through a 50 Ω transmission line to allow proper RF reception. As shown in Figure 4, the GNSS RF interface is designed with an internal DC block, and is suitable for both active and/or passive GNSS antennas due to the built-in SAW filter followed by an additional LNA in front of the integrated high performing u-blox M8 concurrent position engine.

1.7.2.1 GNSS antenna RF interface requirements

Table 7 summarizes the requirements for the GNSS antenna RF interface. See section 2.4.3 for suggestions to correctly design antennas circuits compliant with these requirements.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT_GNSS** port.
Frequency range	BeiDou 1561 MHz GPS / SBAS / QZSS / Galileo 1575 MHz GLONASS 1602 MHz	The required frequency range of the antenna connected to **ANT_GNSS** port depends on the selected GNSS constellations.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT_GNSS** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT_GNSS** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Gain (passive antenna)	> 4 dBic	The antenna gain defines how efficient the antenna is at receiving the signal. It is important providing good antenna visibility to the sky, using antennas with good radiation pattern in the sky direction, according to related antenna placement.
Gain (active antenna)	17 dB minimum, 30 dB maximum	The antenna gain defines how efficient the antenna is at receiving the signal. It is directly related to the overall C/No.
Noise figure (active antenna)	< 2 dB	Since GNSS signals are very weak, any amount of noise degrades all the sensitivity figures of the receiver: active antennas with LNA with a low noise figure are recommended.
Axial ratio	< 3 dB recommended	GNSS signals are circularly-polarized. The purity of the antenna circular polarization is stated in terms of axial ratio (AR), defined as the ratio of the vertical electric field to the horizontal electric field on polarization ellipse at zenith.

Table 7: Summary of GNSS antenna RF interface requirements

1.7.3 Cellular antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an analog to digital converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the SARA-R5 series AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the SARA-R5 series data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.4 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.7.4 Cellular and GNSS coexistence

Desensitization or receiver blocking is a form of electromagnetic interference where a radio receiver is unable to detect a weak signal that it might otherwise be able to receive when there is no interference (see Figure 17). Good blocking performance is particularly important in the scenarios where a number of radios of various forms are used in close proximity to each other. This is the case with SARA-R510M8S modules integrating both an LTE radio and a GNSS receiver.

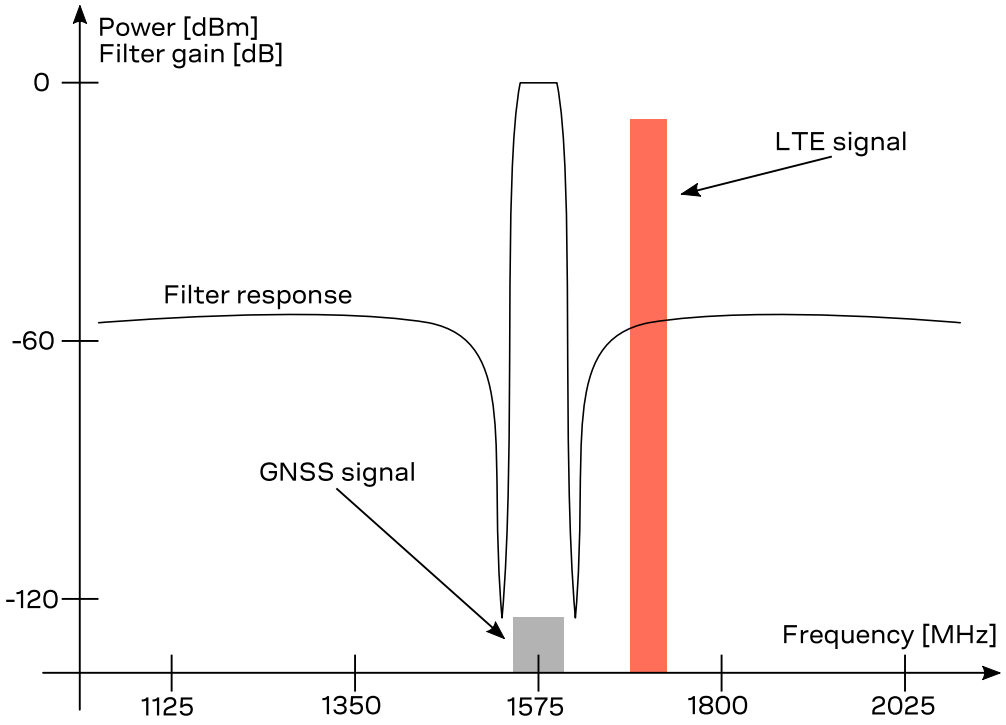

Figure 17: Interference signals due to LTE transmission. Low channels in LTE B3, B4 and B66 (1710 MHz) are close to GNSS frequencies (1561 to 1605 MHz). Harmonics due to transmission in LTE B13 and B18 may also fall into the GNSS bands.

Jamming signals come from in-band and out-band frequency sources. In-band jamming is caused by signals with frequencies within or close to the GNSS constellation frequency used, while out-band jamming is caused by very strong signals with frequencies different from the GNSS carrier, that is picked up at the input of the GNSS receiver and that can saturate the receiver front-end. if not properly taken into consideration those signals cause a reduction in the carrier-to-noise power density ratio (C/No) of the GNSS satellites.

In-band interference signals are typically caused by harmonics from displays, switching converters, micro-controllers and bus systems. Moreover, considering for example the LTE Band 13 high channel transmission frequency (787 MHz) and the GPS operating band (1575.42 MHz ± 1.023 MHz), the second harmonic of the cellular signal is exactly within the GPS operating band. Therefore, depending on the board layout and the transmit power, the highest channel of LTE Band 13 is the channel that has the greatest impact on the C/No reduction.

Countermeasures against in-band interference include:

- maintaining a good grounding concept in the design
- ensuring proper shielding of the different RF paths
- ensuring proper impedance matching of RF traces
- placing the GNSS antenna away from noise sources
- add a notch filter along the GNSS RF path, in front of SAW filter, at the frequency of the jammer (as for example, a notch filter at ~787 MHz improves the immunity to LTE Band 13 high channel)

Out-band interference is caused by signal frequencies that are different from the GNSS, the main sources being cellular, Wi-Fi, bluetooth transmitters, etc. For example, the lowest channels in LTE Band 3, 4 and 66 can compromise the good reception of the GLONASS satellites. Again, the effect can be explained by comparing the LTE frequencies (low channels transmission frequency is 1710 MHz) with the GLONASS operating band (1602 MHz ± 8 MHz). In this case the LTE signal is outside the useful GNSS band, but, provided that the power received by the GNSS subsystem at 1710 MHz is high enough, blocking effects may appear reducing once again the C/No.

Countermeasures against out-band interference include:

- maintaining a good grounding concept in the design
- keeping the GNSS and cellular antennas more than the quarter-wavelength (of the minimum Tx frequency) away from each other. If for layout or size reasons the aforementioned requirement cannot be met, then the antennas should be placed orthogonally to each other and/or on different side of the PCB.
- ensuring at least 15 – 20 dB isolation between antennas in the GNSS band
- adding a GNSS pass-band SAW filter along the GNSS RF line, providing very large attenuation in the cellular frequency bands (as for example Murata SAFFB1G56AC0F0A, or SAFFB1G56AC0F7F). It has to be noted that, as shown in Figure 3, a SAW filter and an LNA are already integrated in the GNSS RF path of the SARA-R510M8S: the addition of an external filter along the GNSS RF line has to be considered only if the conditions above cannot be met.
- adding a GNSS stop-band SAW filter along the cellular RF line, providing very low attenuation in the cellular frequency bands (as for example the Qualcomm B8636, or B8666). It has to be noted that the addition of an external filter along the cellular RF line has to be carefully evaluated as further countermeasure only if the conditions above cannot be met in different way, considering that an external filter may affect the cellular TRP and/or TIS RF performance figures.

As far as Tx power is concerned, SARA-R5 series modules maximum output power during LTE transmission is 23 dBm. High-power transmission occurs very infrequently: typical output power values are in the range of -3 to 0 dBm (see Figure 1 in the GSMA official document TS.09 [10]). Therefore, depending on the application, careful PCB layout and antenna placement should be sufficient to ensure accurate GNSS reception.

1.8 SIM interface

1.8.1 SIM card interface

SARA-R5 series modules provide on the **VSIM**, **SIM_IO**, **SIM_CLK** and **SIM_RST** pins a high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with automatic voltage switch from 1.8 V to 3 V are implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output provides internal short circuit protection to limit start-up current and protects the SIM to short circuits.

1.8.2 SIM card detection interface (GPIO5)

The **GPIO5** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if cleanly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented or not according to the application requirements.

For more details, see the SARA-R5 series AT commands manual [2], +UGPIOC, +CIND and +CMER AT commands.

1.9 Data communication interfaces

SARA-R5 series modules provide the following serial communication interfaces:

- UART interfaces, available for communications with host application processor. See section 1.9.1.
- USB 2.0 compliant interface, available for diagnostic only. See section 1.9.2.
- SPI interfaces, available for communications with external SPI devices and for diagnostic. See section 1.9.3.
- SDIO interface, available for communications with external SDIO devices. See section 1.9.4.
- DDC (I2C bus compatible) interface, available for communications with external I2C devices. See section 1.9.5.

1.9.1 UART interfaces

1.9.1.1 UART features

SARA-R5 series modules include 1.8 V unbalanced asynchronous serial interfaces (UART) for communications with external host application processor.

UART can be configured by dedicated AT command (see the SARA-R5 series AT commands manual [2], +USIO AT command) in the following variants:

- **Variant 0** (default configuration), consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **RI** pins, supporting:
  - AT commands
  - data communication
  - multiplexer protocol functionality (see 1.9.1.3)
  - FW update by means of FOAT
  - FW update by means of the u-blox EasyFlash tool

  The following lines are provided:
  - data lines (**RXD** as output, **TXD** as input)
  - hardware flow control lines (**CTS** as output, **RTS** as input)
  - modem status and control lines (**DTR** as input, **RI** as output)
- **Variant 1**, consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **DSR**, **DCD**, **RI** pins, supporting:
  - AT commands
  - data communication
  - multiplexer protocol functionality (see 1.9.1.3)
  - FW update by means of FOAT
  - FW update by means of the u-blox EasyFlash tool

  The following lines are provided:
  - data lines (**RXD** as output, **TXD** as input)
  - hardware flow control lines (**CTS** as output, **RTS** as input)
  - modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output)
- **Variants 2, 3 and 4**, consisting in two UART interfaces (first primary UART on **RXD**, **TXD**, **CTS**, **RTS** pins, and second auxiliary UART on **DCD**, **DTR**, **RI**, **DSR** pins) plus ring indication and DTR functions:
  - First primary UART interface supports:
    - AT commands
    - data communication
    - multiplexer protocol functionality (see 1.9.1.3)
    - FW update by means of FOAT
    - FW update by means of the u-blox EasyFlash tool

    The following lines are provided:
    - data lines (**RXD** as output, **TXD** as input)
    - hardware flow control lines (**CTS** as output, **RTS** as input)
  - Second auxiliary UART interface supports:
    - AT commands (variant 2 only)
    - data communication (variant 2 only)
    - FW update by means of FOAT (variant 2 only)
    - diagnostic trace log (variant 3 only)
    - GNSS tunneling (variant 4 only)

The following lines are provided:
  - data lines (**DCD** as data output, **DTR** as data input)
  - hardware flow control lines (**RI** as flow control output, **DSR** as flow control input)
- Ring indication function over the GPIO pin configured for this purpose (see section 1.11)
- DTR function, to control low power idle mode in case of +UPSV: 3 setting, over the GPIO pin configured for this purpose (see section 1.11)

UART general features, valid for all variants, are:

- Serial port with RS-232 functionality conforming to the ITU-T V.24 recommendation [5], with CMOS compatible levels (0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state)
- Hardware flow control (default value) or none flow control are supported
- UART power saving indication available on the hardware flow control output, if hardware flow control is enabled: the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- One-shot autobauding is supported and it is enabled by default: automatic baud rate detection is performed only once, at module start up. After the detection, the module works at the fixed baud rate (the detected one) and the baud rate can be changed via AT command
- The default frame format is 8N1 (8 data bits, no parity, 1 stop bit)

SARA-R5 series modules are designed to operate as cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 recommendation [5]. A host application processor connected to the module UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the cellular modules conform to the ITU-T V.24 recommendation [5]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

SARA-R5 series modules' UART interface is by default configured for AT commands: the module waits for AT command instructions and interprets all the characters received as commands to execute. All the functionalities supported by SARA-R5 series modules can be in general set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7], 3GPP TS 27.010 [8]
- u-blox AT commands (see the SARA-R5 series AT commands manual [2])

The UART interfaces settings can be suitably configured by AT commands (for more details, see the SARA-R5 series AT commands manual [2]).

Figure 18 describes the 8N1 frame format.

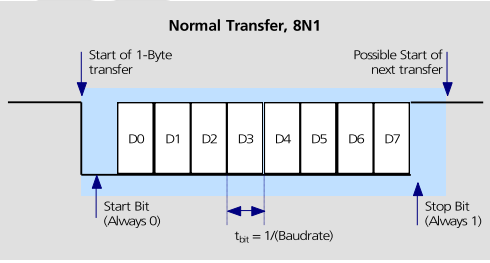

Figure 18: Description of UART default frame format (8N1 = 8 data bits, no parity, 1 stop bit), with fixed baud rate

1.9.1.2 UART signals behavior

At the end of the module boot sequence (see Figure 11, Figure 12, Figure 13), the module is by default in active mode, and the UART interface is initialized and enabled as AT commands interface.

The configuration and behavior of the UART signals after the boot sequence are described below:

- The module data output lines (**RXD** only if USIO variant 0 or 1 is set; **RXD** and **DCD** if USIO variant 2, 3 or 4 is set) are set by default to the OFF state (high level) at UART initialization. The module holds these lines in the OFF state until the module transmits some data.
- The module data input lines (**TXD** only if USIO variant 0 or 1 is set; **TXD** and **DTR** if USIO variant 2, 3 or 4 is set) are assumed to be controlled by the external host once UART is initialized. The data input lines have an internal active pull-up enabled.

1.9.1.3 UART multiplexer protocol

SARA-R5 series modules include multiplexer functionality as per 3GPP TS 27.010 [8], on the UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART).

When USIO variant 0 or 1 is set, the following virtual channels are defined:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 2 is set, AT commands and data communication are available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 2: AT commands / data communication
- Channel 3: GNSS tunneling

When USIO variant 3 is set, diagnostic trace log is available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 4 is set, GNSS tunneling is available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication

1.9.2 USB interface

SARA-R5 series modules include a high-speed USB 2.0 compliant interface with a maximum 480 Mbit/s data rate according to the Universal Serial Bus Revision 2.0 specification [4]. The module itself acts as a USB device and can be connected to any USB host equipped with compatible drivers.

The USB interface is available for diagnostic purpose only.

The **USB_D+** / **USB_D-** lines carry the USB data / signaling, while the **VUSB_DET** input pin represents the input to enable the USB interface by applying an external valid USB VBUS voltage (5 V typical).

1.9.3 SPI interfaces

☞ The SPI interface are not supported by the “00” product version of SARA-R5 series modules, except for diagnostic purpose.

SARA-R5 series modules include 1.8 V Serial Peripheral Interfaces available for communications with external SPI slave devices, or for diagnostic purpose with the module acting as SPI master.

1.9.4 SDIO interface

☞ The SDIO interface is not supported by the “00” product version of SARA-R5 series modules.

SARA-R5 series modules include a 1.8 V 4-bit Secure Digital Input Output interface over the **SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK** and **SDIO_CMD** pins, with the module acting as an SDIO host, available for communications with compatible external SDIO devices, and for diagnostic purpose.

1.9.5 DDC (I2C) interface

☞ Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

SARA-R5 series modules include a 1.8 V I2C-bus compatible DDC interface over the **SDA** and **SCL** pins, available to communicate with an external u-blox GNSS receiver and with external I2C devices as for example an audio codec: the SARA-R5 series module acts as an I2C master that can communicate with I2C slaves in accordance with the I2C bus specifications [9].

The same 1.8 V I2C-bus compatible DDC interface is internally connected to the u-blox M8 GNSS chipset integrated in SARA-R510M8S modules, as illustrated in Figure 4.

The **SDA** and **SCL** pins have internal active pull-up, so there is no need of additional pull-up resistors on the external application board.

1.10 Audio

☞ Audio is not supported by “00” product version of SARA-R5 series modules.

SARA-R5 series modules include a 1.8 V I2S digital audio interface over the **I2S_TXD**, **I2S_RXD**, **I2S_CLK** and **I2S_WA** pins for transferring digital audio data with an external compatible digital audio device.

1.11 General purpose input / output (GPIO)

SARA-R5 series modules include pins which can be configured as General Purpose Input/Output or to provide custom functions via u-blox AT commands (for more details see the SARA-R5 series AT commands manual [2], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 8.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Output indicating cellular network status: registered, data transmission, no service	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
External GNSS supply enable [5]	Output to enable/disable the supply of an external u-blox GNSS receiver connected to the cellular module by I2C	-	GPIO2 [5]
External GNSS data ready [5]	Input to sense when an external u-blox GNSS receiver connected to the module is ready for sending data over I2C	-	GPIO3 [5]
External GNSS RTC sharing [5]	Output providing RTC synchronization signal to an external u-blox GNSS receiver connected to cellular module by I2C	-	GPIO4 [5]
SIM card detection	Input for SIM card physical presence detection, to optionally enable / disable SIM interface upon detection of external SIM card physical insertion / removal	GPIO5	GPIO5
Module status indication	Output indicating module status: power-off or deep-sleep mode versus idle, active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Module operating mode indication	Output indicating module operating mode: power-off, deep-sleep or idle mode versus active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Ring indicator	Output providing events indicator	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
DTR	Input to control low power idle mode of the module in case of +UPSV: 3 and +USIO: 2/3/4 configuration	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Antenna dynamic tuning	Output for real time control of an antenna tuning IC according to the LTE band used by the module	-	I2S_TXD, I2S_WA
Last gasp	Input to trigger last gasp notification	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Fast shutdown	Input to trigger emergency fast shutdown of the module	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Time stamp output [5]	Output indicating the generation of an URC time stamp triggered via interrupt from an external GNSS system		GPIO4
Time pulse output	Output providing accurate time reference, as a sequence with 1 PPS or as single time pulse, based on the GNSS system, the LTE system, or CellLocate	-	GPIO6
External time stamp input	Input triggering via interrupt the generation of an URC time stamp over AT serial interface	-	EXT_INT
External time pulse input [5]	Input to receive an accurate time reference, as a sequence with 1 PPS from an external GNSS system		SDIO_CMD
General purpose input	Input to sense high or low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
General purpose output	Output to set the high or the low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6, I2S_TXD, I2S_WA, EXT_INT, SDIO_CMD	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6, I2S_TXD, I2S_WA, EXT_INT, SDIO_CMD

Table 8: SARA-R5 series modules GPIO custom functions configuration

1.12 Reserved pin (RSVD)

SARA-R5 series modules have a pin reserved for future use, marked as **RSVD**. This pin is to be left unconnected on the application board.

[5] SARA-R500S and SARA-R510S modules only.

2 Design-in

2.1 Overview

For an optimal integration of the SARA-R5 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be suitably designed to guarantee the correct functionality of the relative interface, but a number of points require particular attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antennas connection: **ANT**, **ANT_GNSS** [6] and **ANT_DET** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a SARA-R5 series module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for schematic and layout design.

2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a SARA-R5 series module with the applicable required certification schemes as well as the antenna circuits design. Very carefully follow the suggestions provided in the relative section 2.2.1 for schematic and layout design.

3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in relative section 2.5 for schematic and layout design.

4. System functions: **PWR_ON** and **RESET_N** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in relative section 2.3 for schematic and layout design.

5. Other digital interfaces: UART, USB, SPI, SDIO, I2C, I2S and GPIOs.
   Accurate design is required to guarantee correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6, 2.7 and 2.8 for schematic and layout design.

6. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to guarantee correct functionality. Follow the suggestions provided in the corresponding section 2.2.2 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

[6] Not supported by SARA-R500S and SARA-R510S modules

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-R5 series modules must be sourced through the **VCC** pins with a suitable DC power supply that should comply with the module **VCC** requirements summarized in Table 5.

The appropriate DC power supply can be selected according to the application requirements (see Figure 19) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

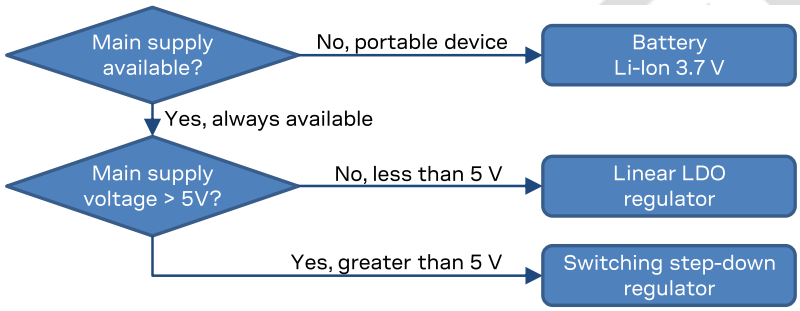

Figure 19: VCC supply concept selection

The switching step-down regulator is the typical choice when primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of SARA-R5 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case, the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for design-in.

If SARA-R5 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.6 and 2.2.1.7 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit, which is not included in the modules. The charger circuit needs to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements. A DC-DC switching charger is the typical choice when the charging source has a high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6 and 2.2.1.7 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in the SARA-R5 series data sheet [1] during connected mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin the highest averaged current consumption value specified in the SARA-R5 series data sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 5.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during transmissions at the maximum power, as specified in the SARA-R5 series data sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the active mode to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 20 and the components listed in Table 9 show an example of a power supply circuit for SARA-R5 series modules. In this example, the module **VCC** is supplied by a step-down switching regulator capable of delivering the maximum peak / pulse current specified for the LTE use-case, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

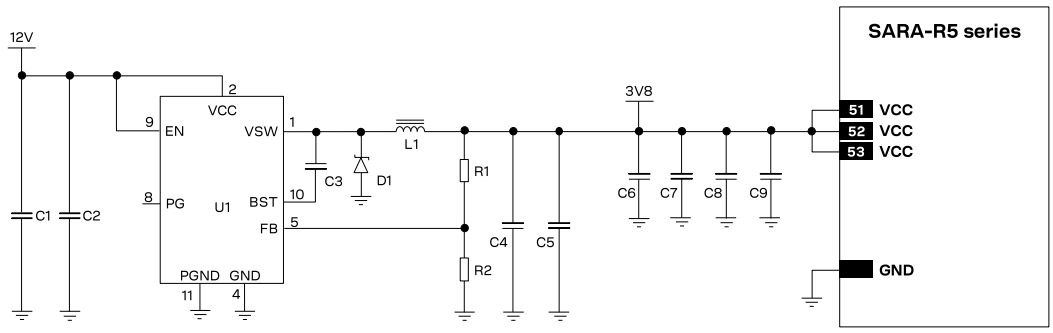

Figure 20: Example of VCC supply circuit for SARA-R5 series modules, using a step-down regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X7R 50 V	Generic manufacturer
C2	10 nF capacitor ceramic X7R 16 V	Generic manufacturer
C3	22 nF capacitor ceramic X7R 16 V	Generic manufacturer
C4	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C5	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C6	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 - Murata
C7	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 - Murata
C8	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C9	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 - Murata
D1	Schottky diode 30 V 2 A	MBR230LSFT1G - ON Semiconductor
L1	4.7 µH inductor 20% 2 A	SLF7045T-4R7M2R0-PF - TDK
R1	470 kΩ resistor 0.1 W	Generic manufacturer
R2	150 kΩ resistor 0.1 W	Generic manufacturer
U1	Step-down regulator 1 A 1 MHz	TS30041 - Semtech

Table 9: Components for the VCC supply circuit for SARA-R5 series modules, using a step-down regulator

☞ See the section 2.2.1.9, and in particular Figure 26 / Table 14, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using low drop-out linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission at the maximum Tx power, as specified in the SARA-R5 series data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the rated range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 21 and the components listed in Table 10 show an example of a power supply circuit for SARA-R5 series modules, where the module **VCC** is supplied by an LDO linear regulator capable of delivering maximum peak / pulse current specified for LTE use-case, with suitable power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits described in Figure 21 and Table 10). This reduces the power on the linear regulator and improves the thermal design of the circuit.

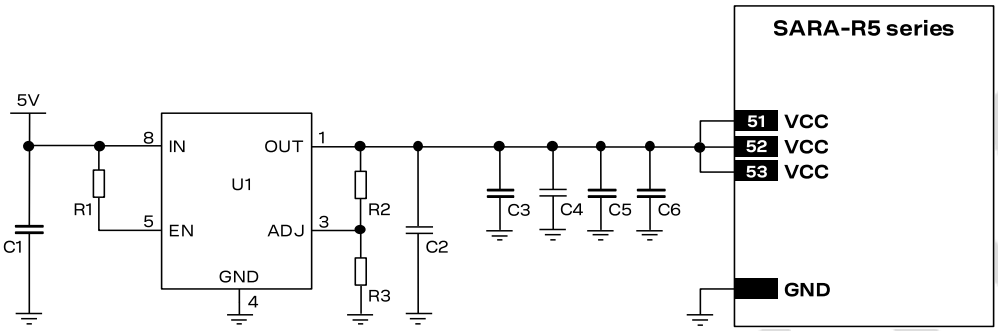

Figure 21: Example of VCC supply circuit for SARA-R5 series modules, using an LDO linear regulator

Reference	Description	Part number - Manufacturer
C1	1 µF capacitor ceramic X5R 6.3 V	Generic manufacturer
C2	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C3	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 - Murata
C4	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 - Murata
C5	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 - Murata
R1	47 kΩ resistor 0.1 W	Generic manufacturer
R2	41 kΩ resistor 0.1 W	Generic manufacturer
R3	10 kΩ resistor 0.1 W	Generic manufacturer
U1	LDO linear regulator 1.0 A	AP7361C – Diodes Incorporated

Table 10: Components for VCC supply circuit for SARA-R5 series modules, using an LDO linear regulator

☞ See the section 2.2.1.9, and in particular Figure 26 / Table 14, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during a transmission at maximum Tx power, as specified in SARA-R5 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during a transmission at maximum Tx power, as specified in SARA-R5 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.6 Guidelines for external battery charging circuit

SARA-R5 series modules do not have an on-board charging circuit. Figure 22 provides an example of a battery charger design, suitable for applications that are Li-Ion (or Li-Pol) battery powered.

In the application circuit, a rechargeable Li-Ion (or Li-Pol) battery cell, that features the correct pulse and DC discharge current capabilities and the appropriate DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the battery charger IC, which from a USB power source (5.0 V typ.), linearly charges the battery in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the battery charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value.

Using a battery pack with an internal NTC resistor, the battery charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The battery charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see section 2.2.1.7 for the specific design-in).

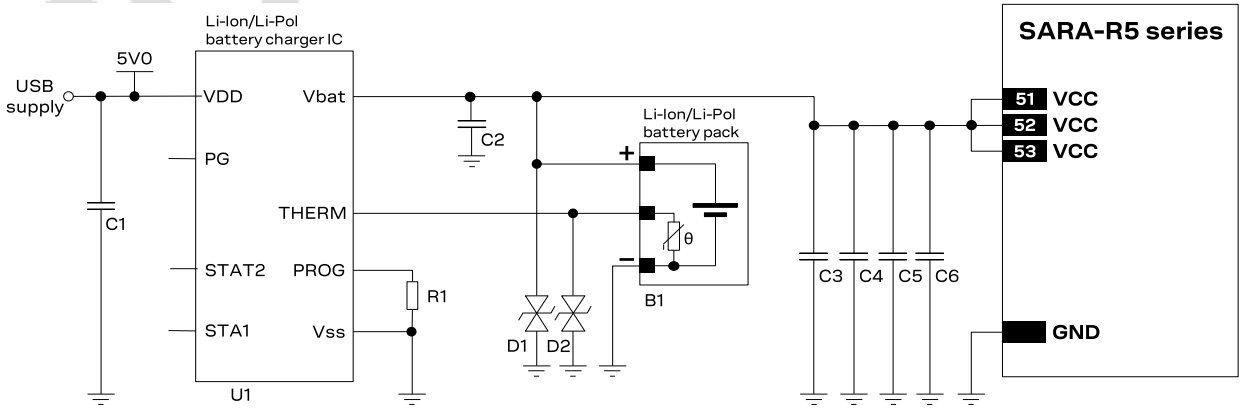

Figure 22: Li-Ion (or Li-Pol) battery charging application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with 470 Ω NTC	Generic manufacturer
C1, C2	1 µF capacitor ceramic X7R 16 V	Generic manufacturer
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JB01 - Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 - Murata
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 - Murata
C6	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
R1	10 kΩ resistor 0.1 W	Generic manufacturer
U1	Single cell Li-Ion (or Li-Pol) battery charger IC	MCP73833 - Microchip

Table 11: Suggested components for the Li-Ion (or Li-Pol) battery charging application circuit

See the section 2.2.1.9, and in particular Figure 26 / Table 14, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 23 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator, which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system. The power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- High efficiency internal step down converter, with characteristics as indicated in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

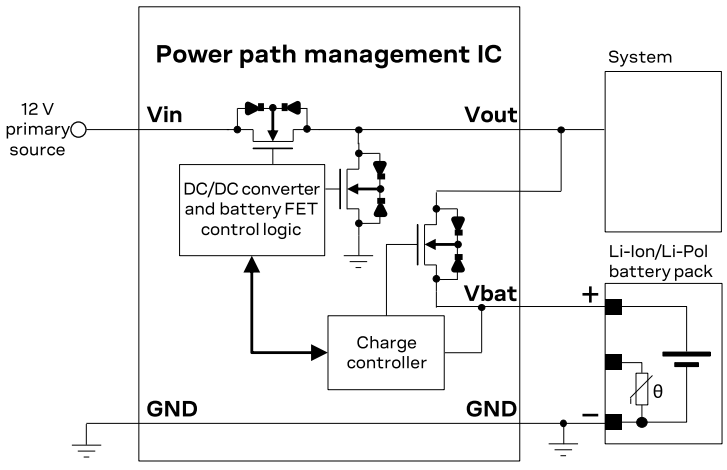

Figure 23: Charger / regulator with integrated power path management circuit block diagram

Figure 24 and the parts listed in Table 12 provide an application circuit example where the MPS MP2617H switching charger / regulator with integrated power path management function provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Pol) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

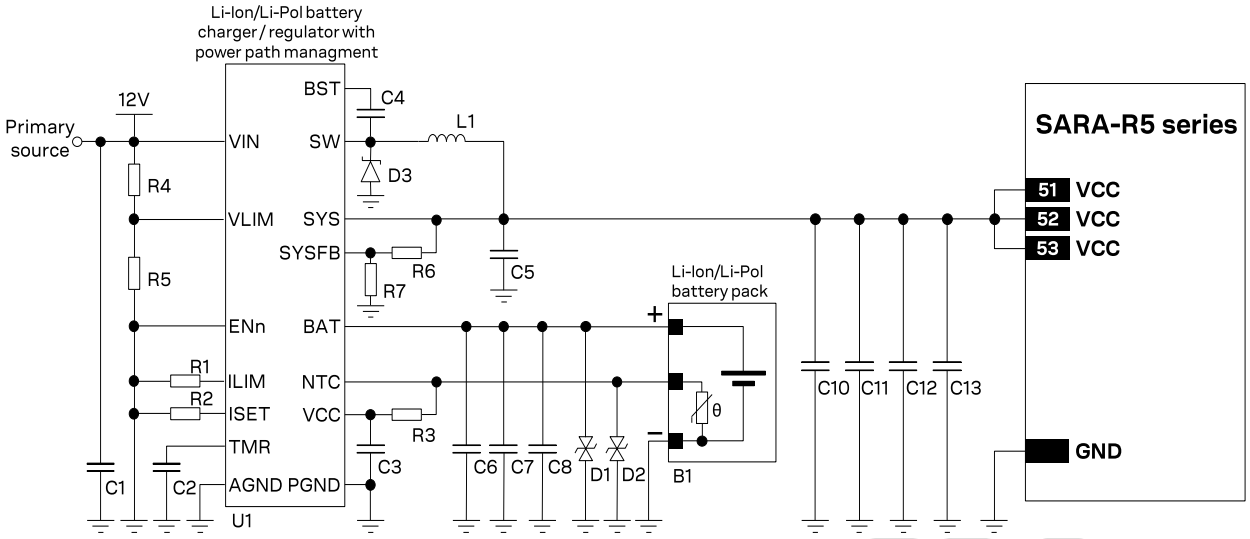

Figure 24: Li-Ion (or Li-Pol) battery charging and power path management application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF capacitor ceramic X5R 0603 10% 25 V	GRM188R60J226MEA0 - Murata
C2, C4, C10	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
C3	1 µF capacitor ceramic X7R 0603 10% 25 V	GCM188R71E105KA64 - Murata
C7, C12	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 - Murata
C8, C13	15 pF capacitor ceramic C0G 0402 5% 25 V	GJM1555C1H150JB01 - Murata
C11	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
D3	Schottky diode 40 V 3 A	MBRA340T3G - ON Semiconductor
R1, R3, R5, R7	10 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y - Bourns
U1	Li-Ion/Li-Pol battery DC-DC charger / regulator with integrated power path management function	MP2617H - Monolithic Power Systems (MPS)

Table 12: Suggested components for battery charging and power path management application circuit

☞ See the section 2.2.1.9, and in particular Figure 26 / Table 14, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Guidelines for removing VCC supply

Removing the **VCC** power can be useful to minimize the current consumption when the SARA-R5 series modules are switched off. The application processor can disconnect the **VCC** supply source from the module and zero out the module's current.

The **VCC** supply source can be removed using an appropriate low-leakage load switch or p-channel MOSFET controlled by the application processor as shown in Figure 25, given that the external switch has provided:

- Very low leakage current (for example, less than 1 μA), to minimize the current consumption
- Very low $R_{DS(ON)}$ series resistance (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum drain current (see the SARA-R5 series data sheet [1] for module current consumption figures)

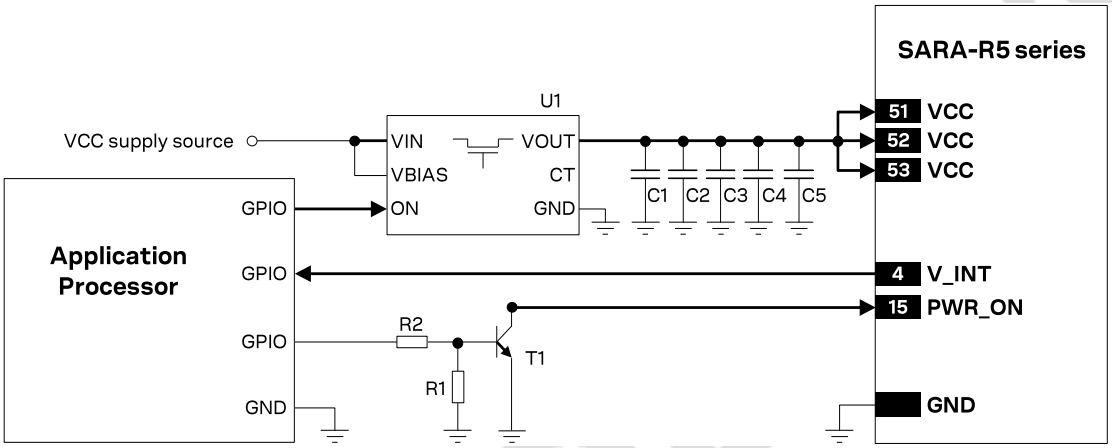

Figure 25: Example of application circuit for VCC supply removal

Reference	Description	Part number - Manufacturer
C1	10 μF capacitor ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 - Murata
C3	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 - Murata
C5	15 pF capacitor ceramic C0G 0402 5% 25 V	GJM1555C1H150JB01 - Murata
R1, R3	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
T1	NPN BJT transistor	BC847 - Infineon
U1	Ultra-low resistance load switch	TPS22967 - Texas Instruments

Table 13: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-R5 series normal operations: the **VCC** supply can be removed only after **V_INT** goes low, indicating that the module has entered deep-sleep power saving mode or power-off mode.

☞ See the section 2.2.1.9, and in particular Figure 26 / Table 14, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.9 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to the modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to **VCC** supply connection. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module minimizing series resistance.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with self-resonant frequency in the 700/800/900 MHz range (e.g. Murata GRM1555C1H680J), to filter EMI in the low cellular frequency bands
- 15 pF capacitor with self-resonant frequency in the 1700/1800/1900 MHz range (as Murata GRM1555C1H150J), to filter EMI in the high cellular frequency bands
- 10 nF capacitor (e.g. Murata GRM155R71C103K), to filter digital logic noise from clocks and data
- 100 nF capacitor (e.g. Murata GRM155R61C104K), to filter digital logic noise from clocks and data

An additional capacitor is recommended to avoid undershoot and overshoot at the start and at the end of RF transmission:

- 10 µF capacitor, or greater capacitor, with low ESR (e.g. Murata GRM188R60J106ME47)

An additional series ferrite bead is recommended for additional RF noise filtering, in particular if the application device integrates an internal antenna:

- Ferrite bead specifically designed for EMI suppression in GHz band (e.g. Murata BLM18EG221SN1), placed as close as possible to the **VCC** pins of the module, implementing the circuit described in Figure 26, to filter out EMI in all the cellular bands

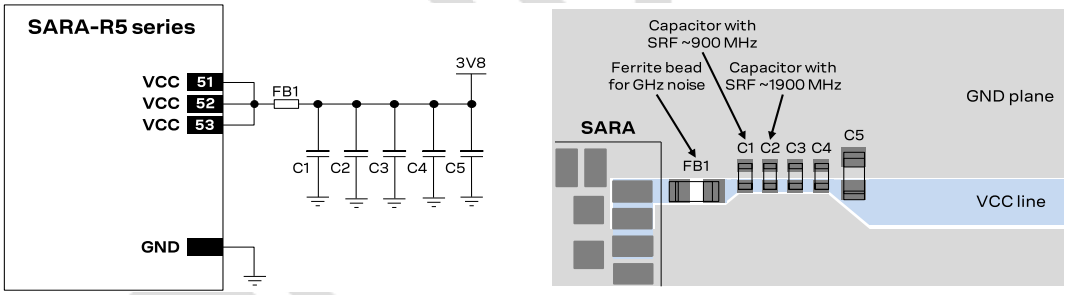

Figure 26: Suggested design to reduce ripple / noise on VCC, highly recommended when using an integrated antenna

Reference	Description	Part number - Manufacturer
C1	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 - Murata
C2	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JB01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 - Murata
C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
C5	10 µF capacitor ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
FB1	Chip Ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 14: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the parts described in Figure 26 / Table 14 if the application device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

2.2.1.10 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 27.
- Coupling between **VCC** and digital lines must be avoided.
- The tank bypass capacitor for current spikes smoothing described in section 2.2.1.9 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and module.
- The bypass capacitors in the pF range described in Figure 26 and Table 14 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the self-resonant frequency of the pF capacitors. This is highly recommended if the application device integrates an internal antenna.
- Since **VCC** input provides the supply to RF power amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-R5 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection function may be compromised).

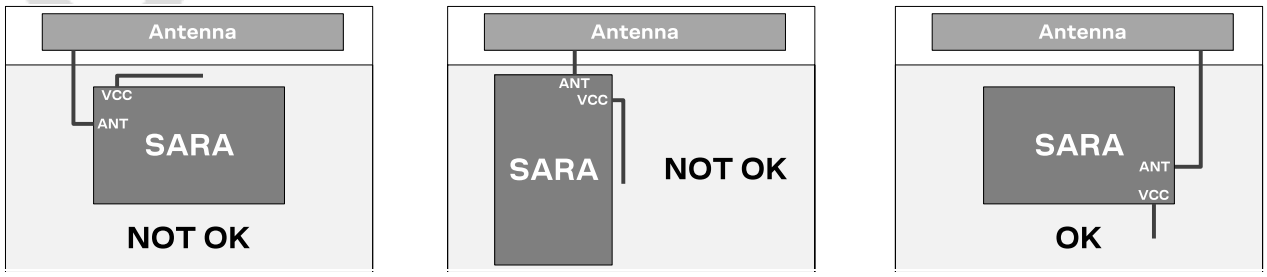

Figure 27: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.11 Guidelines for grounding layout design

Good connection of the module **GND** pins with application PCB solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application PCB as GND plane as wide as possible.
- If the application board is a multilayer PCB, then all the layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes.
- Provide a dense line of vias at the edges of each GND area, in particular along RF and high speed lines.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pads also ensures thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

SARA-R5 series modules provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on and it is not in the deep-sleep power saving mode
- Supply external devices, as voltage translators, instead of using an external discrete regulator (e.g. see 2.6.1)
- Pull-up SIM detection signal (see section 2.5 for more details)

☞ Do not apply loads which might exceed the maximum available current from **V_INT** supply (see SARA-R5 series data sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of SARA-R5 series modules: **VCC** supply can be removed only after **V_INT** goes low.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin.

2.2.2.2 Guidelines for V_INT layout design

V_INT digital interfaces supply output is generated by an integrated switching step-down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

SARA-R5 series **PWR_ON** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 28 and Table 15.

ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as described in Figure 28.

PWR_ON input pin should not be driven high by an external device, as it may cause start up issues.

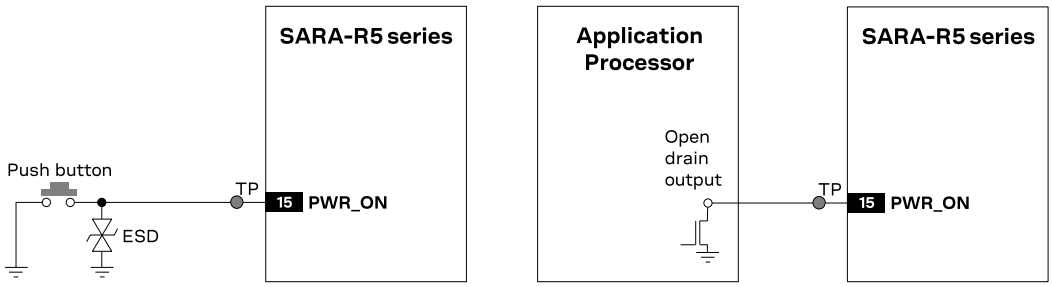

Figure 28: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number - Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 - TDK

Table 15: Example ESD protection component for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible test point directly connected to the **PWR_ON** pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout due to the pin function (see sections 1.6.1 and 1.6.2). It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

SARA-R5 series **RESET_N** is equipped with an internal active pull-up; an external pull-up resistor is not required and should not be provided.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 29 and Table 16.

☞ ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

An open drain output or open collector output is suitable to drive the **RESET_N** input from an application processor, as described in Figure 29.

☞ **RESET_N** input pin should not be driven high by an external device, as it may cause start up issues.

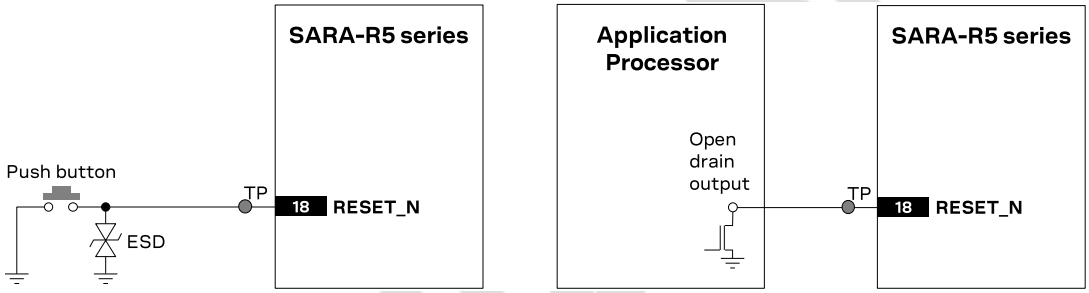

Figure 29: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number - Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 - TDK

Table 16: Example of ESD protection component for the RESET_N application circuits

☞ If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of an accessible test point directly connected to the **RESET_N** pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit require careful layout due to the pin function (see section 1.6.3). Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** pin as short as possible.

2.4 Antenna interfaces

SARA-R5 series modules provide a cellular RF interface for connecting the external cellular antenna: the **ANT** pin represents the cellular RF input/output for cellular signals transmission and reception.

SARA-R510M8S modules provide also a GNSS RF interface for connecting the external GNSS antenna: the **ANT_GNSS** pin represents the GNSS RF input for GNSS signals reception.

The **ANT** and **ANT_GNSS** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related physical antenna through a 50 Ω transmission line to allow clean transmission / reception of RF signals.

2.4.1 General guidelines for antenna interfaces

2.4.1.1 Guidelines for ANT and ANT_GNSS pins RF connection design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

A clean transition between the **ANT** and **ANT_GNSS** pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** and **ANT_GNSS** pads:

- On a multilayer board, the whole layer stack below the RF connections should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** and **ANT_GNSS** pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 30
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** and **ANT_GNSS** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 30

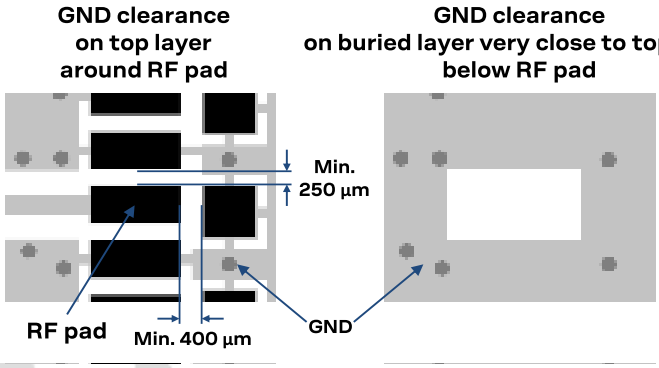

Figure 30: GND keep-out area on top layer around RF pad and on very close buried layer below RF pad (ANT / ANT_GNSS)

☞ Refer to section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.2 Guidelines for RF transmission lines design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

Any RF transmission line, such as the ones from the **ANT** and **ANT_GNSS** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 31 and Figure 32 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

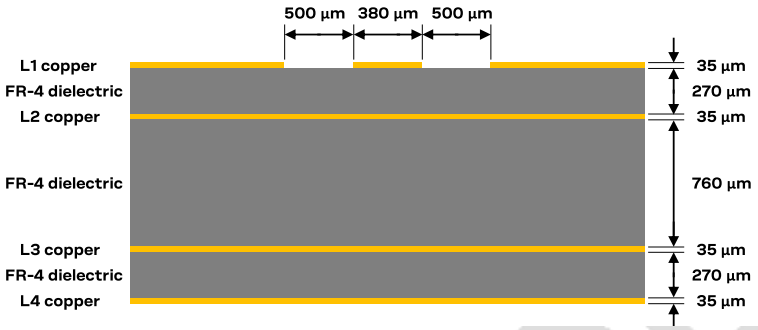

Figure 31: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

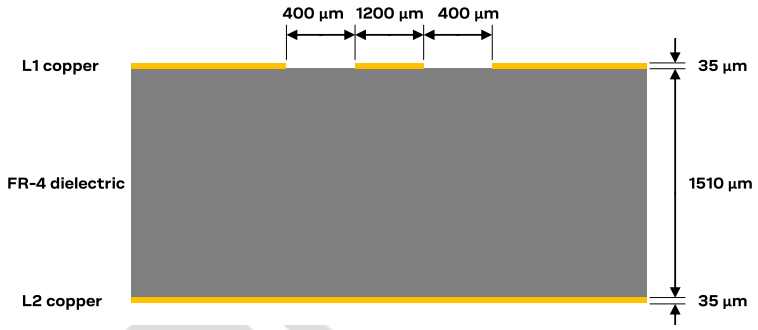

Figure 32: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, then the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad) taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the transmission line width must be chosen due to:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 31 and Figure 32)
- the thickness of the dielectric material between the top layer (where the line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 31, 1510 µm in Figure 32)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 31 and Figure 32)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 31, 400 µm in Figure 32)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the width of the line, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB,
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 μm, to reduce parasitic capacitance to ground,
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND,
- Add GND stitching vias around transmission lines, as described in Figure 33,
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 33,
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB),
- Avoid stubs on the transmission lines,
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer,
- Do not route microstrip lines below discrete component or other mechanics placed on top layer

Two examples of a suitable RF circuit design for **ANT** pin are illustrated in Figure 33, where the cellular antenna detection circuit is not implemented (if the cellular antenna detection function is required by the application, follow the guidelines for circuit and layout implementation detailed in section 2.4.4):

- In the first example shown on the left, the **ANT** pin is directly connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout.
- In the second example shown on the right, the **ANT** pin is connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout, with an additional high pass filter to improve the ESD immunity at the antenna port. (The filter consists of a suitable series capacitor and shunt inductor, for example the Murata GRM1555C1H150JB01 15 pF capacitor and the Murata LQG15HN39NJ02 39 nH inductor with SRF ~1 GHz.).

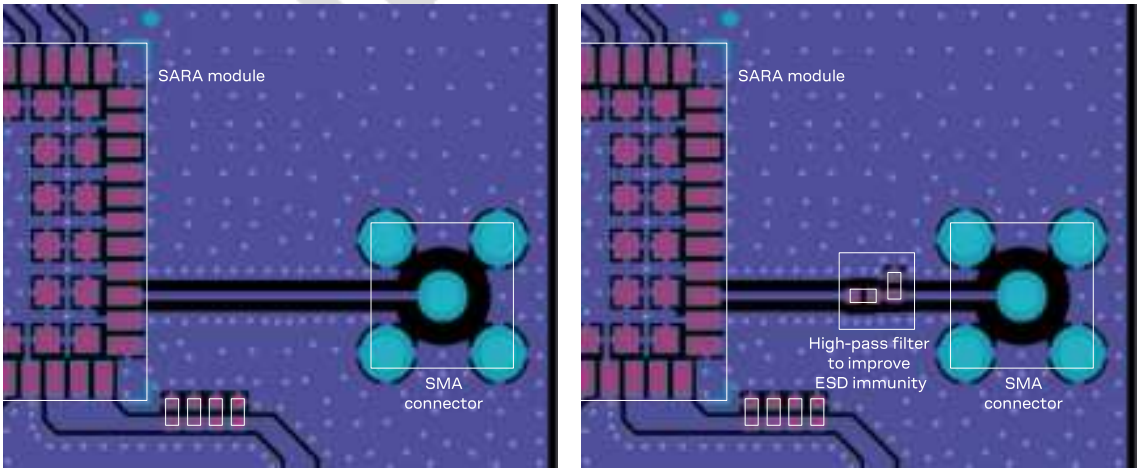

Figure 33: Example of circuit and layout for ANT RF circuits on the application board

☞ Refer to section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.3 Guidelines for RF termination design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of **ANT** and **ANT_GNSS** ports.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. So to reduce as much as possible any performance degradation due to antenna mismatching, the RF termination must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 6 and Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing a clean PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require a GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts, as illustrated in Figure 33 or in Figure 39.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as illustrated in 34.

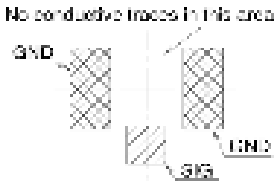

Figure 34: U.FL surface mounted connector mounting pattern layout

- Cut out the GND layer under the RF connector and close to any buried vias, to remove stray capacitance and thus keep the RF line at 50 Ω, e.g. the active pad of U.FL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If an integrated antenna is used, the integrated antenna represents the RF terminations. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer providing the best possible return loss.
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that needs to be radiated. As numerical example,
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for antenna matching design-in guidelines relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antennas within a closed metal case.
- Do not place the cellular antenna in close vicinity to the end user since the emitted radiation in human tissue is restricted by regulatory requirements.
- Place the antennas as far as possible from VCC supply line and related parts (see also Figure 27), from high speed digital lines (as USB) and from any possible noise source.

- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC or EMI issues.
- Be aware of interaction between co-located RF systems since the LTE transmitted power may interact or disturb the performance of companion systems (see also section 1.7.4).

☞ Refer to section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.2 Cellular antenna RF interface (ANT)

2.4.2.1 Guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the cellular compliance of the device integrating SARA-R5 series modules with all the applicable required certification schemes depends on antenna's radiating performance.

Cellular antennas are typically available as:

- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the SARA-R5 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides a clean PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antennas imply physical restriction to the design of the PCB: Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that needs to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered. As numerical example, the physical restriction to the PCB design can be considered as following:

    Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.

- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss / VSWR figure over all the operating frequencies.
- Select an antenna providing optimal efficiency figure over all the operating frequencies.
- Select an antenna providing appropriate gain figure (i.e. combined directivity and efficiency figure) so that the RF radiation intensity do not exceed the regulatory limits specified in some countries: refer to the FCC United States notice reported in section 4.2.2, the ISED Canada notice reported in section 4.3.1, the RED Europe notice reported in section 4.4).

2.4.2.2 Examples of cellular antennas

Table 17 lists some examples of possible internal on-board surface-mount cellular antennas.

Manufacturer	Part number	Product name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.26.A	Havok	LTE SMD dielectric antenna 617..960 MHz, 1710..2690 MHz 54.6 x 13.0 x 3.0 mm
Taoglas	PCS.66.A	Reach	Wideband LTE SMD antenna 600..6000 MHz 32.0 x 25.0 x 1.6 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm
Ethertronics	P822601		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
Ethertronics	P822602		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
Ethertronics	1002436		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2700 MHz 50.6 x 19.6 x 1.6 mm
Pulse	W3796	Domino	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1427..1661 MHz, 1695..2200 MHz, 2300..2700 MHz 42.0 x 10.0 x 3.0 mm
TE Connectivity	2118310-1		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 74.0 x 10.6 x 1.6 mm
Molex	1462000001		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1700..2700 MHz 40.0 x 5.0 x 5.0 mm
Cirocomm	DSAN0001		Ceramic LTE SMD antenna 698..960 MHz, 1710..2170 MHz 40.0 x 6.0 x 5.0 mm

Table 17: Examples of internal surface-mount cellular antennas

Table 18 lists some examples of possible internal off-board PCB-type cellular antennas with cable and connector.

Manufacturer	Part number	Product name	Description
PulseLarsen Antennas	W3929B0100		LTE FPC antenna with coax feed 617..960 MHz, 1710..2690 MHz, 3400..3900 MHz 115.8 x 30.4 mm
Taoglas	FXUB64.18.0150A	Cyclone	LTE wideband flex antenna 617..960 MHz, 1710..2690 MHz 130.0 x 30.0 mm
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Laird Tech.	EFF692SA3S	Revie Flex	Flexible LTE antenna 689..875 MHz, 1710..2500 MHz 90.0 x 20.0 mm
Antenova	SRFL026	Mitis	GSM / WCDMA / LTE antenna on flexible PCB with cable and U.FL 689..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 110.0 x 20.0 mm
Ethertronics	1002289		GSM / WCDMA / LTE antenna on flexible PCB with cable and U.FL 698..960 MHz, 1710..2700 MHz 140.0 x 75.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm

Table 18: Examples of internal cellular antennas with cable and connector

Table 19 lists some examples of possible external cellular antennas.

Manufacturer	Part number	Product name	Description
Taoglas	GSA.8842.A.105111		Wideband LTE I-Bar adhesive antenna with cable and SMA(M) 617..960 MHz, 1710..2700 MHz, 4900..5850 MHz 176.5 x 59.2 x 13.6 mm
Taoglas	TG.55.8113		LTE terminal mount monopole antenna with 90° hinged SMA(M) 617..960 MHz, 1427..2170 MHz, 2300..2690 MHz 172.0 x 23.88 x 13 mm
Taoglas	TG.35.8113W	Apex II	Wideband LTE dipole terminal antenna hinged SMA(M) 617..1200 MHz, 1710..2700 MHz, 4900..5900 MHz 224 x 58 x 13 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Pulse Electronics	SPDA24617/3900		Multiband swivel dipole antenna with SMA(M) 617..960 MHz, 1400..2700 MHz, 3200..3900 MHz 223.24 x 56.13 x 10.97 mm

Table 19: Examples of external cellular antennas

2.4.2.3 Antenna trace design used for SARA-R5 series modules' type approvals

The conformity assessment of u-blox SARA-R5 series LGA surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc. has been carried out with the SARA-R5 series modules mounted on a u-blox host printed circuit board with a 50 Ω grounded coplanar waveguide designed on it, herein referenced as "antenna trace design", implementing the connection of the **ANT** LGA pad of the module, consisting in the cellular RF input/output of the module, up to a dedicated 50 Ω SMA female connector, consisting in the cellular RF input/output of the host printed circuit board for external antenna and/or RF cable access.

☞ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC United States Grants and ISED Canada Certificates of SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of SARA-R5 series modules, described in this section.

☞ In case of antenna trace design change, an FCC Class II Permissive Change and/or ISED Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID and/or the ISES Multiple Listing (new application) procedure followed by an FCC C2PC and/or ISED C4PC application.

The antenna trace design is implemented on the u-blox host PCB as illustrated in Figure 35, using the parts listed in Table 20, with the support of the additional optional antenna detection capability. Guidelines to design a proper equivalent optional antenna detection circuit on a host printed circuit board are available in section 2.4.4.

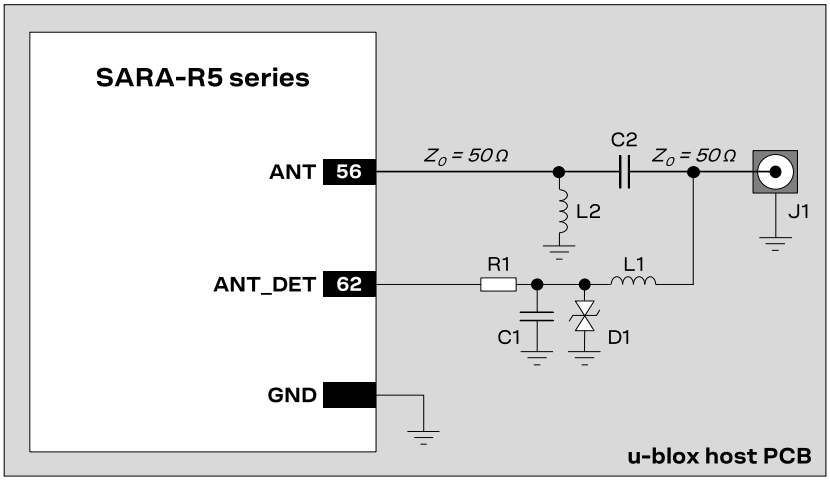

Figure 35: Antenna trace design implemented on the u-blox host PCB, with additional antenna detection circuit

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 - Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330JA16 - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 - Amphenol
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	Not Installed

Table 20: Parts in use on the u-blox host PCB for the antenna trace design, with additional antenna detection circuit

The u-blox host printed circuit board has a structure of 4 Copper layers with 35 µm thickness (1 oz/ft^2) each, using FR4 dielectric substrate material with 4.3 typical permittivity at 1 GHz, and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB designed to accommodate the **ANT** pad of SARA-R5 series module is described in Figure 36: the left side illustrates top layer copper mask and top layer solder resist mask, with top layer to bottom layer vias; the right side illustrates the PCB stack-up structure. Considering that the thickness of the dielectric material from the top layer to the buried layer is larger than 200 µm, no GND keep-out is implemented on the buried metal layer area below the **ANT** pad. Guidelines to design an equivalent proper connection for the **ANT** pad on a host printed circuit board are available in section 2.4.1.1.

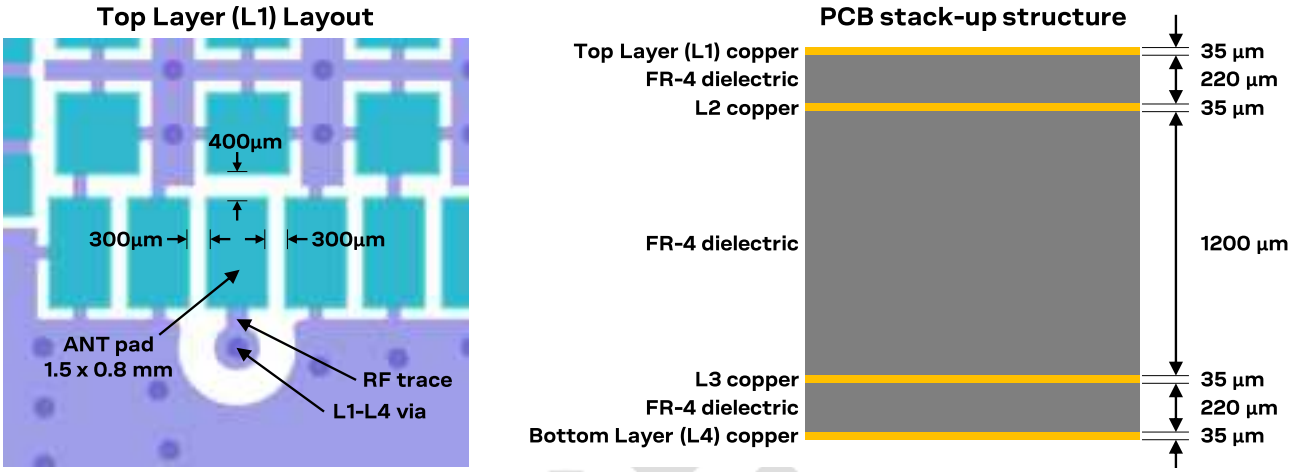

Figure 36: Top layer layout and stack-up structure of the u-blox host PCB for the ANT pad of the module

As illustrated on the left side of Figure 36, the antenna RF trace is routed from the RF pad on the top layer (L1) to the bottom layer (L4) through a dedicated via. After the via, the antenna RF trace, as 50 Ω transmission line, is connected to the antenna detection circuit described in Figure 35 and Table 20, with the layout illustrated on the left side of Figure 37. Guidelines to design a proper equivalent (optional) antenna detection circuit on a host printed circuit board are available in section 2.4.4.

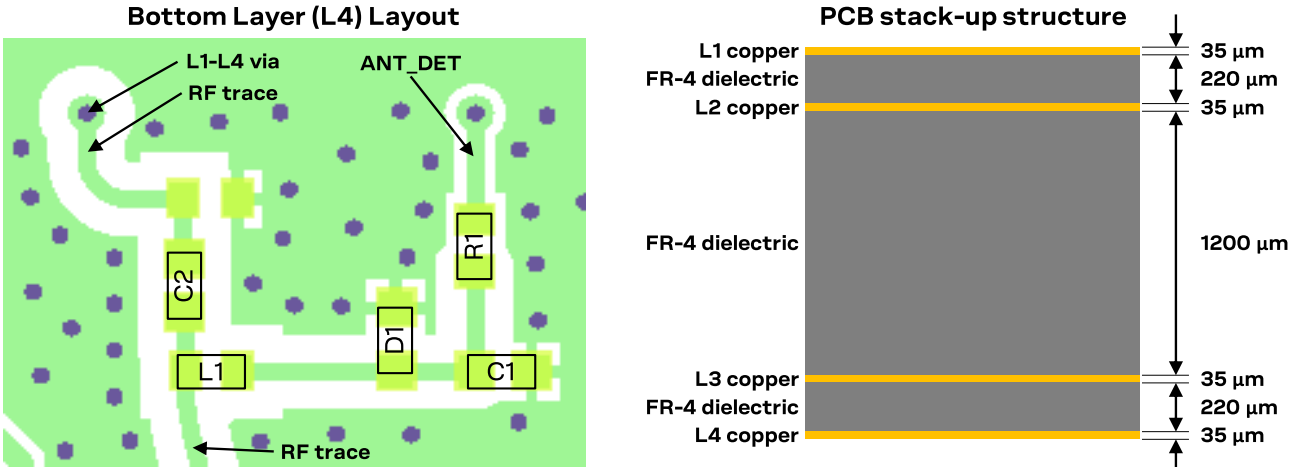

Figure 37: Bottom layer layout and stack-up structure of the u-blox host PCB for the antenna detection circuit

After the antenna detection circuit with the layout illustrated on the left side of Figure 37, the antenna RF trace is designed as a 50 Ω grounded coplanar waveguide on the bottom layer of the u-blox host printed circuit board, with total length ~29 mm, with layout and thickness, width, gap (signal to ground) characteristics illustrated in Figure 38. Guidelines to design a proper equivalent 50 Ω transmission line on a host printed circuit board are available in section 2.4.1.2.

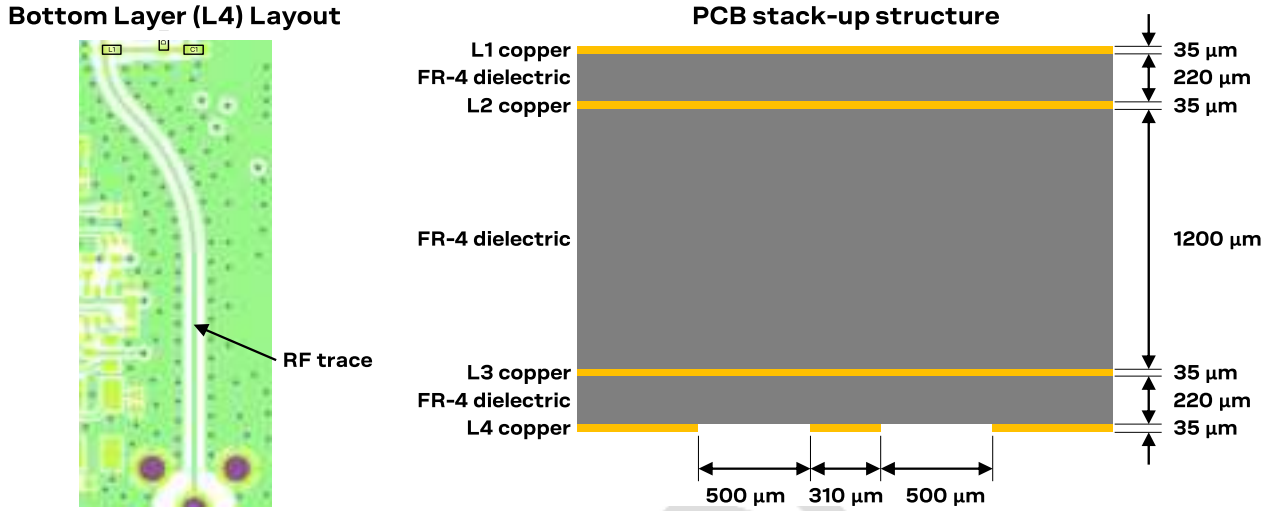

Figure 38: 50 Ω grounded coplanar waveguide transmission line designed on the u-blox host PCB bottom layer

The 50 Ω grounded coplanar waveguide routed on the bottom layer is terminated on a dedicated 50 Ω SMA female connector mounted on the top layer, consisting in the cellular RF input/output of the host PCB for external antenna and/or RF coaxial cable access, with board layout illustrated in Figure 39. Guidelines to design a proper equivalent 50 Ω termination on a host printed circuit board are available in section 2.4.1.3, with antenna selection and design guidelines available in section 2.4.2.1.

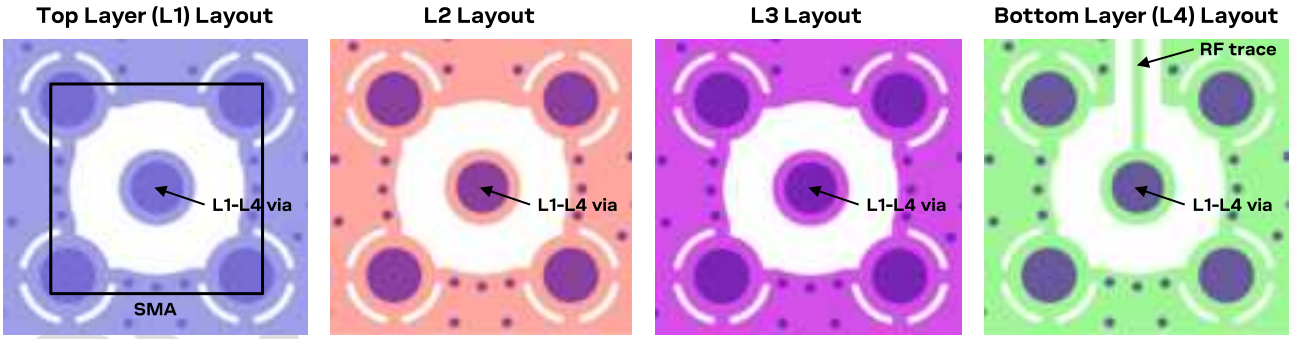

Figure 39: 50 Ω SMA female connector layout on the u-blox host PCB

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA female connector.

Compliance of the design with regulatory rules and specifications defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

2.4.3 GNSS antenna RF interface (ANT_GNSS)

The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

The antenna and its placement are critical system factors for accurate GNSS reception. Use of a ground plane will minimize the effects of ground reflections and enhance the antenna efficiency. A ground plane with a minimum diameter of 10 centimeter is recommended. Exercise care with rover vehicles that emit RF energy from motors etc. as interference may extend into the GNSS band and couple into the GNSS antenna suppressing the wanted signal.

Since SARA-R510M8S modules already include an internal SAW filter followed by an additional LNA before the u-blox M8 GNSS chipset (as illustrated in Figure 4), they are optimized to work with passive or active antennas without requiring additional external circuitry.

2.4.3.1 Guidelines for applications with a passive antenna

If a GNSS passive antenna with high gain and good sky view is used, together with a short 50 Ω line between antenna and receiver, and no jamming sources affect the GNSS passive antenna, the circuit illustrated in Figure 40 can be used. This provides the minimum BoM cost and minimum board space.

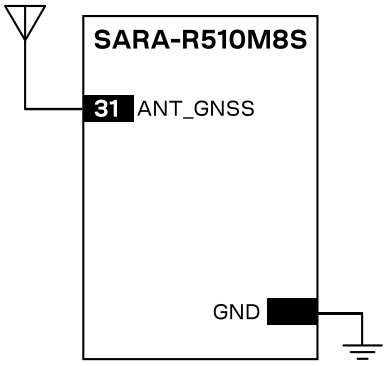

Figure 40: Minimum circuit with GNSS passive antenna

Where best performance needs to be achieved, and improved jamming immunity is needed due to strong out-band jammers close to the GNSS antenna (e.g. the cellular antenna), consider adding an external SAW filter (as for example Murata SAFFB1G56AC0F0A, or SAFFB1G56AC0F7F) close to the GNSS passive antenna, followed by an external LNA (as for example Maxim MAX2659ELT+, JRC New Japan Radio NJG1143UA2, NXP BGU8006, Infineon BGA524N6), as illustrated in Figure 41.

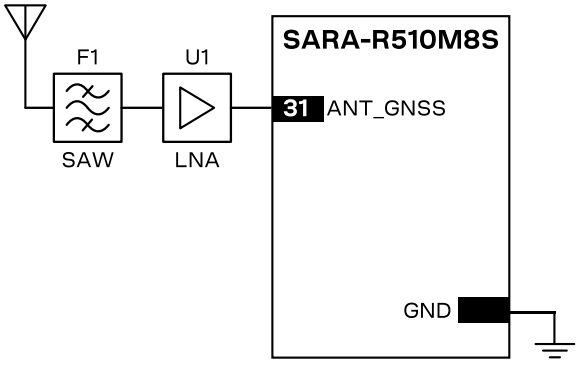

Figure 41: Typical circuit for best performance and improved jamming immunity with GNSS passive antenna

The external LNA can be selected to deliver the performance needed by the application in terms of:

- Noise figure (sensitivity)
- Selectivity and linearity (robustness against jamming)
- Robustness against RF power

Depending on the characteristics of the supply source (DC/DC regulator, linear LDO regulator or other) used to supply the external LNA, make sure some good filtering is in place for the external LNA supply because of the noise on the external LNA supply line can affect the performance of the LNA itself: consider adding a proper series ferrite bead (as for example the Murata BLM15HD182SN1, Murata BLM15HD102SN1, TDK MMZ1005F121E, or TDK MMZ1005A121E) and a proper decoupling capacitor to ground (as for example the Murata GCM1555C1H270JA16, 22 pF capacitor) at the input of the external LNA supply line.

It should be noted anyway that the insertion loss of the filter directly affects the system noise figure and hence the system performance. The selected SAW filter has to provide very low loss in the GNSS pass-band, beside providing very large attenuation in the out-band jammers cellular frequency bands (as for example the Murata SAFFB1G56AC0F0A, or the Murata SAFFB1G56AC0F7F).

Table 21 lists examples of passive antennas to be used with SARA-R510M8S modules.

Manufacturer	Part number	Product name	Description
Tallysman	TW3400P		Passive antenna GPS / SBAS / QZSS / GLONASS
Tallysman	TW3710P		Passive antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	CGGBP.35.3.A.02		Ceramic patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	CGGBP.18.4.A.02		Embedded patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Inpaq	PA1590MF6G		Patch antenna GPS / SBAS / QZSS / GLONASS
Yageo	ANT2525B00BT1516S		Ceramic patch antenna GPS / SBAS / QZSS / GLONASS
Antenova	SR4G008	Sinica	Ultra-low profile patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou

Table 21: Examples of GNSS passive antennas.

2.4.3.2 Guidelines for applications with an active antenna

Active antennas for GNSS applications are usually powered through a DC bias on the RF cable. A simple bias-T, as shown in Figure 42, can be used to add this DC current to the RF signal line. The inductance L is responsible for isolating the RF path from the DC path, while Rbias and C form a low pass filter to remove high frequency noise from the DC supply. L should be also selected to pass the DC fault current in case the antenna connection is shorted.

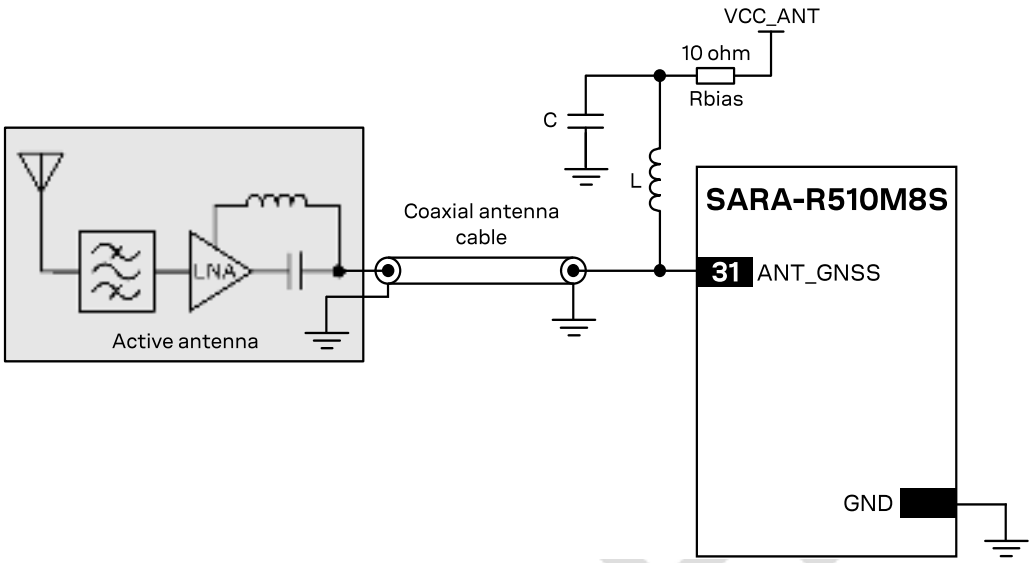

Figure 42: Typical circuit with active antenna connected to GNSS RF interface of SARA-R510M8S, using an external supply.

Refer to the antenna datasheet and/or manufacturer for proper values of the inductance L and capacitance C.

Table 22 lists examples of active antennas to be used with SARA-R510M8S modules.

Manufacturer	Part number	Product name	Description
Tallysman	TW3400		Active antenna, 2.5 - 16 V GPS / SBAS / QZSS / GLONASS
Tallysman	TW3710		Active antenna, 2.5 – 16 V GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	AA.162.301111	Ulysses	Ultra-Low profile miniature antenna, 1.8 – 5.5V GPS / SBAS / QZSS / GLONASS / Galileo
Taoglas	MA310.A.LB.001		Magnet mount antenna, 1.8 – 5.5 V GPS / SBAS / QZSS / GLONASS
Inpaq	B3G02G-S3-01-A		SMA plug active antenna, 3.3 V typical GPS / SBAS / GLONASS
Inpaq	GPSH237N-N3-37-A		Patch circular antenna, 3.0 V typical GPS / SBAS / QZSS
Abracon LLC	APAMP-110		Module RF antenna 5dBic SMA adhesive, 2.5 – 3.5 V GPS / SBAS / QZSS
TE Connectivity	2195768-1		Active antenna, 3.0 V typical GPS / SBAS / QZSS

Table 22: Examples of GNSS active antennas.

2.4.4 Cellular antenna detection interface (ANT_DET)

2.4.4.1 Guidelines for ANT_DET circuit design

Figure 43 and Table 23 describe the recommended schematic / components for the cellular antenna detection circuit to be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve antenna detection functionality.

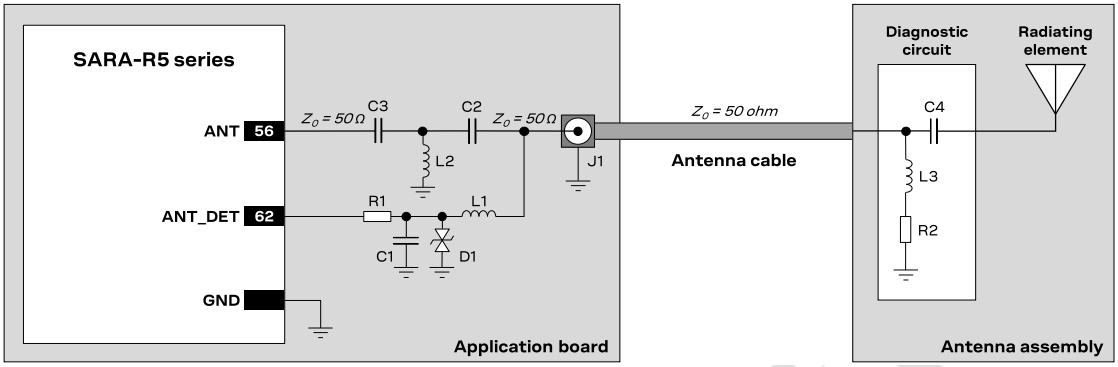

Figure 43: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 - Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330JA16 - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 - Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
C4	22 pF capacitor Ceramic C0G 0402 5% 25 V	GCM1555C1H270JA16 - Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ resistor for diagnostics	Generic manufacturer

Table 23: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection and diagnostic circuit suggested in Figure 43 and Table 23 are here explained:

- When antenna detection is forced by the +UANTR AT command (see the SARA-R5 series AT commands manual [1]), the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for accurate measurements through the +UANTR AT command. It also acts as an ESD protection.
- Additional components (C1 and D1 in Figure 43) are needed at the **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 43) is provided as ESD immunity improvement
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 43, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self-Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is correctly connected.
- Values close to the measurement range maximum limit or an open-circuit “over range” report (see the SARA-R5 series AT commands manual [2]) means that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, a damaged antenna or incorrect value of the antenna load resistor for diagnostics.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 33.

2.4.4.2 Guidelines for ANT_DET layout design

Figure 44 describes the recommended layout for the cellular antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 43 and Table 23:

- The **ANT** pin must be connected to the cellular antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.2 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pin (C2) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line must be placed as ESD protection.
- The additional high pass filter (C3 and L2) on the **ANT** line is placed as ESD immunity improvement

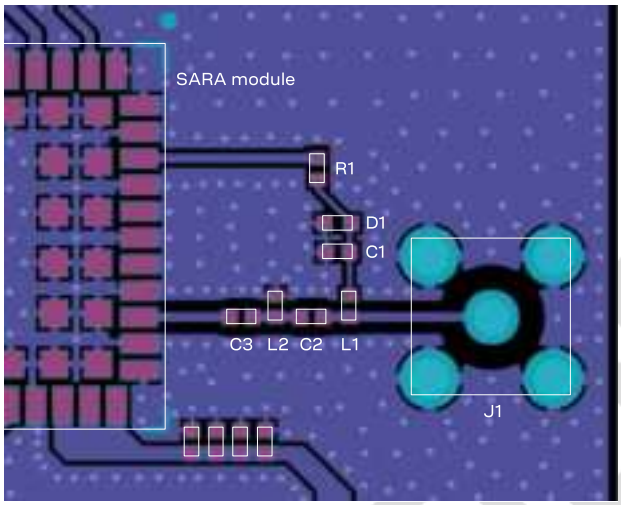

Figure 44: Suggested layout for antenna detection circuit on application board

2.4.5 Cellular antenna dynamic tuning control interface

SARA-R5 series modules support a wide range of frequencies, from 600 MHz to 2200 MHz. To provide more efficient antenna designs over a wide bandwidth, **I2S_TXD** and **I2S_WA** pins can be configured to change their output value according to the LTE band used by the module (see sections 1.11 and 2.8).

These pins, paired with an external antenna tuner IC or RF switch, can be used to:

- tune antenna impedance to reduce power losses due to mismatch
- tune antenna aperture to improve total antenna efficiency
- select the optimal antenna for each operating band

Table 24 reports the antenna dynamic tuning pins setting at the related module operating band.

I2S_TXD	I2S_WA	LTE frequency band in use
0	0	B71 (< 700 MHz)
0	1	B12, B13, B28, B85 (700..800 MHz)
1	0	B5, B8, B18, B19, B20, B26 (800..900 MHz)
1	1	B1, B2, B3, B4, B25, B66 (> 1000 MHz)

Table 24: SARA-R5 series modules antenna dynamic tuning truth table

Figure 45 shows the example application circuits implementing impedance tuning and aperture tuning. The module controls an RF switch which is responsible for selecting the appropriate matching element for the operating band. Table 25 reports suggested components implementing the SP4T RF switch functionality.

In Figure 45(a), tuning the antenna impedance optimizes the power delivered into the antenna by dynamically adjusting the RF impedance seen by **ANT** pin of SARA-R5 series module. By creating a tuned matching network for each operating band, the total radiated power (TRP) and the total isotropic sensitivity (TIS) metrics are improved.

In Figure 45(b), antenna aperture tuning enables higher antenna efficiency over a wide frequency range. The dynamically tunable components are added to the antenna structure itself, thereby modifying the effective electrical length of the radiating element. Thus the resonant frequency of the antenna is shifted into the module's operating frequency band. Aperture tuning optimizes radiation efficiency, insertion loss, isolation and rejection levels of the antenna.

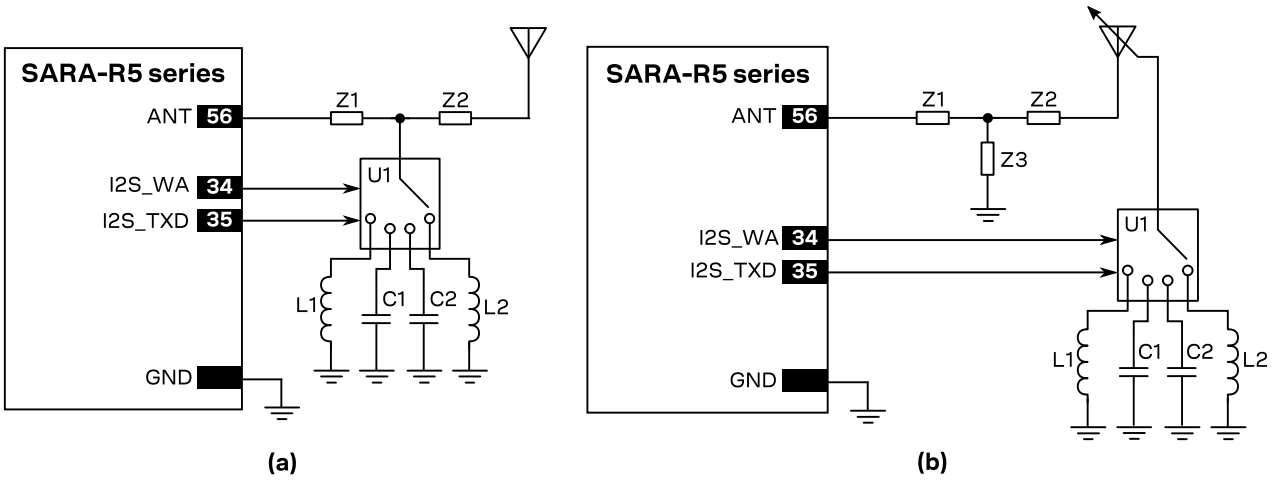

Figure 45: Examples of schematics for cellular antenna dynamic impedance tuning (a) and aperture tuning (b).

Refer to the antenna datasheet and/or manufacturer for proper values of matching components Z1, Z2, Z3, L1, L2, C1, C2. These components should have low losses to avoid degrading the radiating efficiency of the antenna, thereby hindering the positive effects of dynamic tuning.

Manufacturer	Part number	Description
Peregrine Semiconductor	PE42442	30..6000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE613050	5..3000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE42440	50..3000 MHz UltraCMOS SP4T RF switch
Skyworks Solutions	SKY13414-485LF	100..6000 MHz SP4T antenna switch
Skyworks Solutions	SKY13626-685LF	400..3800 MHz SP4T high-power RF switch
Skyworks Solutions	SKY13380-350LF	20..3000 MHz SP4T high-power RF switch
AVX / Ethertronics	EC646	100..3000 MHz ultra-small SP4T RF switch
AVX / Ethertronics	EC686	100..3000 MHz ultra-low R_{ON} SP4T RF switch
Qorvo	RF1654A	100..2700 MHz SP4T RF switch

Table 25: Examples of RF switches for cellular antenna dynamic tuning.

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

2.5.1.1 Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 5 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Surface-Mounted UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by the ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux. contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP (Progr. supply) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A Surface-Mounted SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Surface-Mounted SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

2.5.1.2 Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of SARA-R5 series modules as described in Figure 46, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

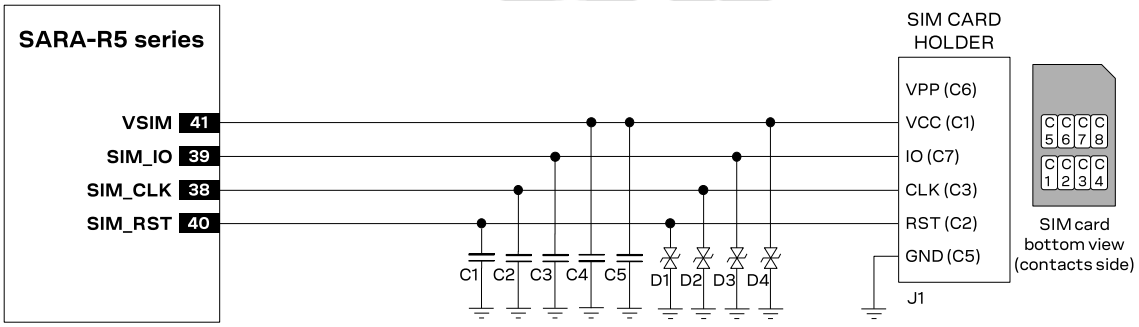

Figure 46: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
D1, D2, D3, D4	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
J1	SIM card holder, 6 positions, without card presence switch	Generic manufacturer, as C707 10M006 136 2 - Amphenol

Table 26: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

2.5.1.3 Guidelines for single SIM chip connection

A Surface-Mounted SIM chip (M2M UICC form factor) must be connected to the SIM card interface of the SARA-R5 series modules as described in Figure 47.

Follow these guidelines to connect the module to a Surface-Mounted SIM chip without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

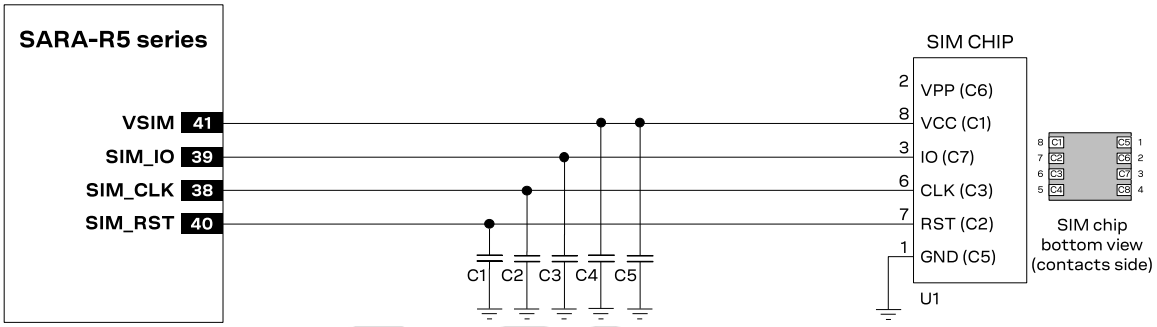

Figure 47: Application circuits for the connection to a single Surface-Mounted SIM chip, with SIM detection not implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1	SIM chip (M2M UICC form factor)	Generic manufacturer

Table 27: Example of components for the connection to a single SMD SIM chip, with SIM detection not implemented

2.5.1.4 Guidelines for single SIM card connection with detection

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 48, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.

- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 48) to the **GPIO5** input pin, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 48).
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 48) to **V_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 48)
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. The ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

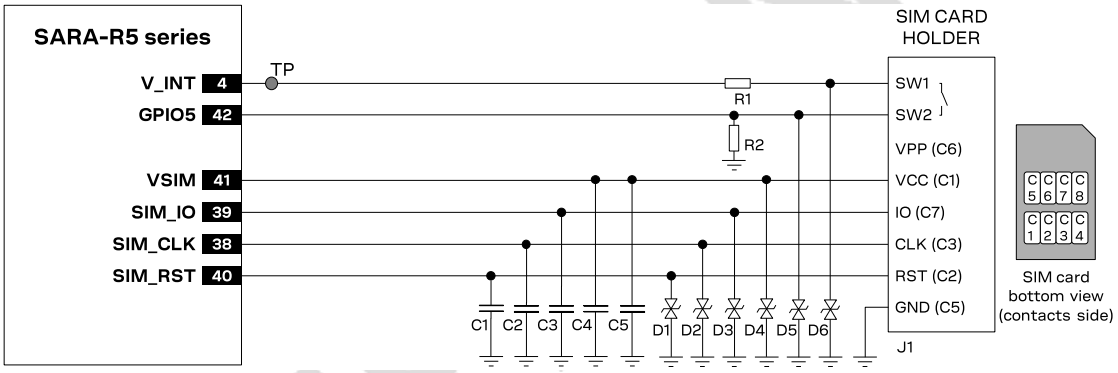

Figure 48: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	470 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
J1	SIM card holder, 6 + 2 positions, with card presence switch	Generic manufacturer, as CCM03-3013LFT R102 - C&K Components

Table 28: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-R5 series modules or in close proximity to the cellular antenna (and/or GNSS antenna, for SARA-R510M8S modules): these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF lines or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels (and/or GNSS channels, for SARA-R510M8S modules) whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 46, Figure 47, Figure 48 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.