4 Bluetooth Circuit Operation Theory

The bluetooth module is connected to Bulverde. Bluetooth system mainly consists of Balun + Bandpass filter, and TI BRF6150 chip. The TI BRF6150 bluetooth solution is a single chip and Bluetooth 1.2 specification conformance

.

4.1 TI Bluetooth chip BRF6150 connectivity with Bulverde

The TI BRF6150 standard universal asynchronous receiver transmitter (UART) interface is used for communicating with Intel Bulverde bluetooth UART. The Codec interface of BRF6150 been connected to G2 MCSI interface.

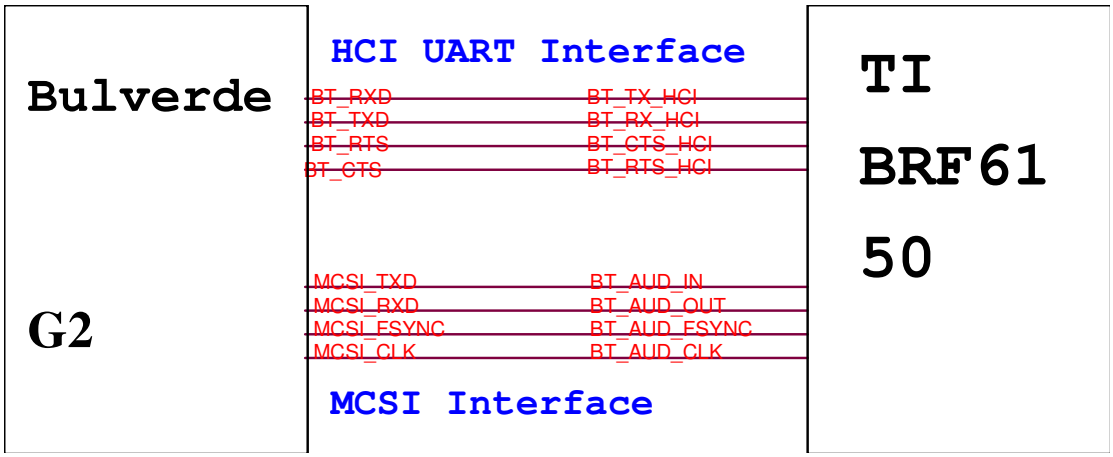

Fig 55

4.2 TI BRF6150 System Architecture

The BRF6150 offers an integrated solution for Bluetooth applications with 10 low cost passive external components. BRF6150 requires 11 components for operation with battery voltage (2.7-5.5V) and 10 components for operation with regulated voltage (1.78-3.6V). These components include a Balanced Filter and 9-10 capacitors.

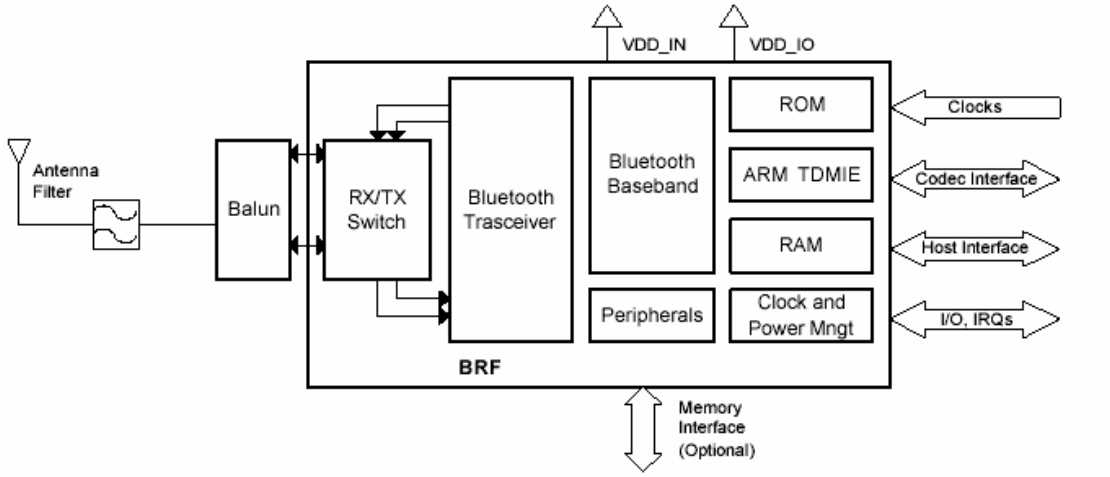

Fig 56

4.2.1. Digital radio processor (DRP).

The BRF6150 architecture comprises a digital radio processor and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMIE core. The device includes several on-chip peripherals to enable easy communication with a host system and the Bluetooth core

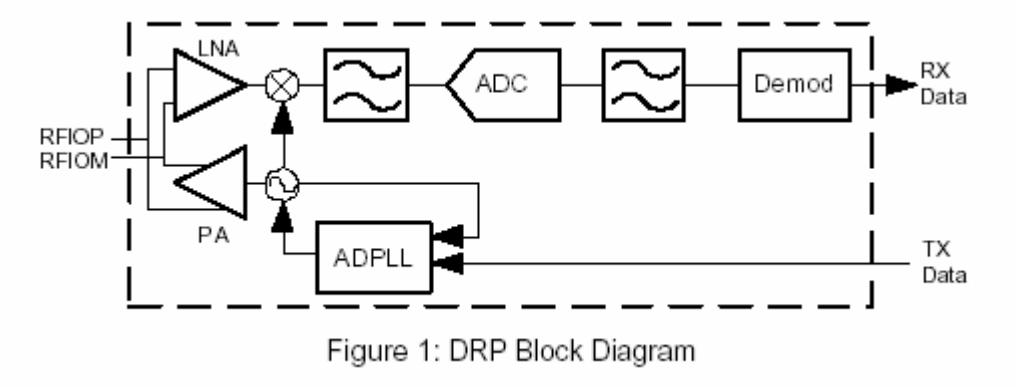

Figure 1: DRP Block Diagram

Fig 57

4.2.2 Transmitter

The transmitter is based on an all-digital sigma-delta PLL with a digitally controlled oscillator (DCO) at 2.4 GHz as the RF frequency clock. The modulation is achieved by directly modulating the digital PLL within a closed loop. The power amplifier is digitally controlled.

4.2.3 Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. The external Balun is followed by an internal RF switch and a differential LNTA (low-noise trans-conductance amplifier). The LNTA amplifies the input and converts it to a current-mode signal. The LNTA feeds the sampling capacitors in the MTDSM (MultiTap Direct Sampling Mixer). The MTDSM performs anti-aliasing filtering and down-conversion by sampling the RF signal. The local oscillator used by the MTDSM is created by the same frequency synthesizer used for the transmitter. The IF

sampled signal output of the MTDSM is then filtered to suppress in-band interference. After this filtering, the signal is quantized by a sigma-delta ADC and passed through decimation FIR (DFIR) to further reduce the level of interference. The demodulator then digitally down converts the signal to zero IF, performs digital filtering, suppresses the image, and recovers the data bit by an adaptive decision mechanism. The BRF6150 is the second generation of TI Bluetooth single chip using DRP architecture. To improve radio performances some features or modifications have been added:

§ LNA input bandwidth has been narrowed to increase blocking performance.

§ A passive pole has been added to the mixer's output to improve anti-aliasing filtering and blocking performance as well.

§ IFA pole location has been optimized for co-channel performance.

§ A new MLSE (Maximum Likelihood Sequence Estimation) decision block has been added to the detector increasing the sensitivity.

4.2.4 Frequency plan

§ Transmit chain use a two-point modulation scheme. The RF oscillator core is running at a doubled frequency. Hence, the frequency of the transmitted signal is identical to the frequency of the synthesizer's output, while the oscillator core is running at an instantaneously double frequency.

§ RX chain uses a near-zero IF scheme, with a 0.5MHz IF frequency. Hence the LO signal is set to a frequency which is 0.5MHz higher than the desired input signal. The DCO core is still running with a doubled frequency (~5GHz)

4.3. Power Supply

The BRF6150 includes several on-chip voltage regulators, which helps to increase the immunity to noise and interference.

4.3.1 Power Source

The BRF6150 device requires two kinds of power source:

§ The main power supply for the core.

§ The power source for the I/O ring.

4.3.2 Power supply for the Core

The BRF6150 includes an improved power management design that reduces the use of external components (LDO and stability capacitors) and supports applications that needs a direct battery connection. It supports two ranges of supply voltage:

§ Direct battery connection – 2.7v to 5.5v.

§ Via external LDO – 1.78v to 3.6v.

The BRF6150 power management system reduces the quiescent current by using a KA (keep alive) technique. It has a shut down input pin that can shut down the entire chip in order to reduce the current consumption to minimum (only leakage current through the battery connections).When working with external regulator as the power supply source, the following configuration is used:

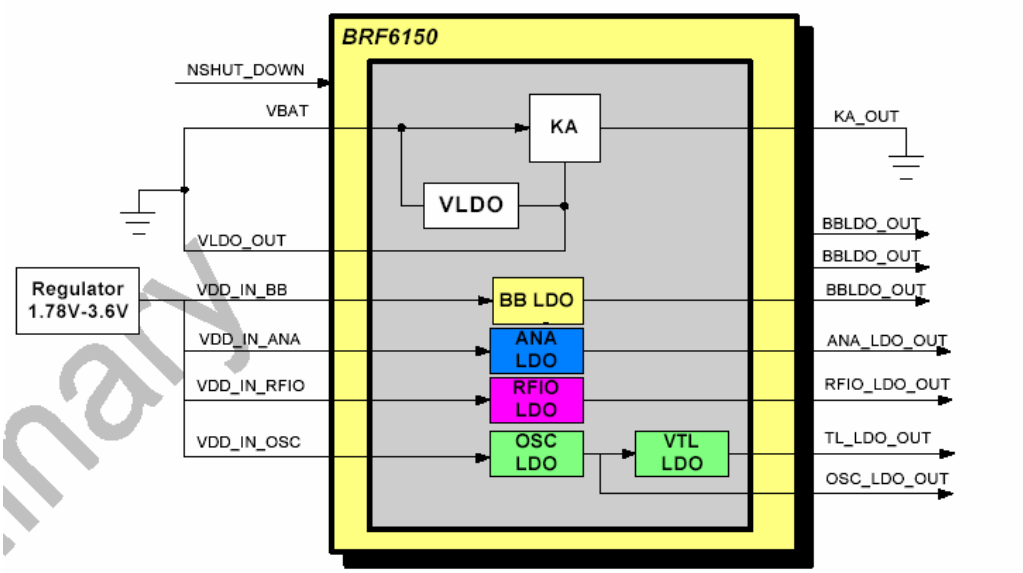

Fig 58

4.4 Clock Control

The BRF6150 operates on two different input clocks: fast and slow. Clock sources for the fast clock are either from a crystal or from an analog clock input, which is fed through an squarer cell. The source of the slow clock can be either from external or

internal source.

4.4.1 Slow clock

4.4.1.1 External Clock

The external slow clock input SLOW_CLK_IN can accept a digital signal in the following range:

VIL < 0.3V, 1.5V < VIH < 3.3V.

The slow clock must be 32.768 KHz signal with up to ±250 ppm tolerance (Bluetooth requirements).

The external slow clock needs to be stable at most 1.5 msec after NSHUT_DOWN is released.

4.4.1.2 Internal Clock

The BRF6150 also supports the option to operate from an internal slow clock source.

This internal slow clock cell has two modes:

§ Active Mode – The cell generates a digital 32.768 kHz slow clock

§ Shut Down – When an external digital slow clock is available, the cell is shut down to minimize the current consumption. After reset, the device detects if an external slow clock source is present and shut down the internal cell automatically.

4.4.2 Fast clock

The BRF6150 supports any clock input frequency in the range of 12–40 MHz. Among the supported frequencies are all the Cellular standard clock frequencies: 12 MHz, 13 MHz, 16 MHz, 16.2 MHz, 19.2 MHz, 19.44 MHz, 26 MHz, and 38.4 MHz. The BRF6150 supports one of two fast clock sources: crystal or external analog frequency source (oscillator or other source). When the slow clock is provided externally, an automatic clock recognition algorithm allows detecting the clock frequency (in 20KHz resolution for input clock of up to 20 MHz, and 40KHz resolution for clock greater than 20 MHz). The device is then initialized accordingly.

The following figure illustrates the configuration of an external source as the fast clock source.

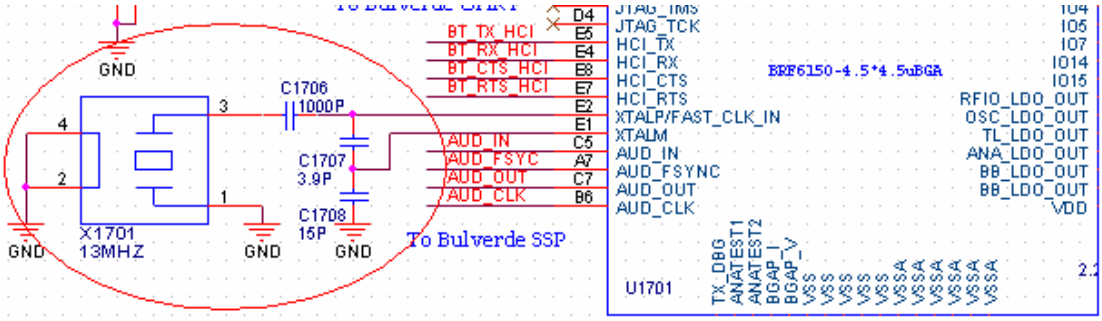

Fig 59

4.5 Reset and clocks wake timing

The BRF6150 supports an internal power on reset mechanism initiated by the external active low reset signal -NSHUT_DOWN. This pin can be also used to shut down the entire chip in order to reduce the current consumption to minimum (4 uA typical). In

case the host wants to put the BRF6150 in Reset state, it must ensure that the pulse on NSHUT_DOWN pin fulfills the following timing requirements:

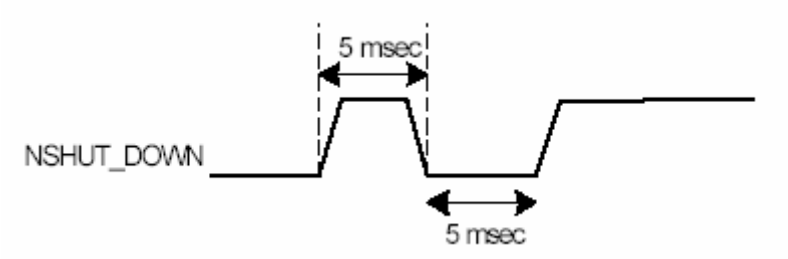

Fig 60

Note: this minimum pulse width is related to a change of operating state only (active to shut down or shut down to active) and not to a normal power up conditions. FW initialization time is approximately 150msec (when using a 13MHz fast clock), at the end of which the HCI UART RTS signal is asserted low, signaling to the host that the BRF6150 is ready to communicate via the HCI interface.

A timing diagram is given below.

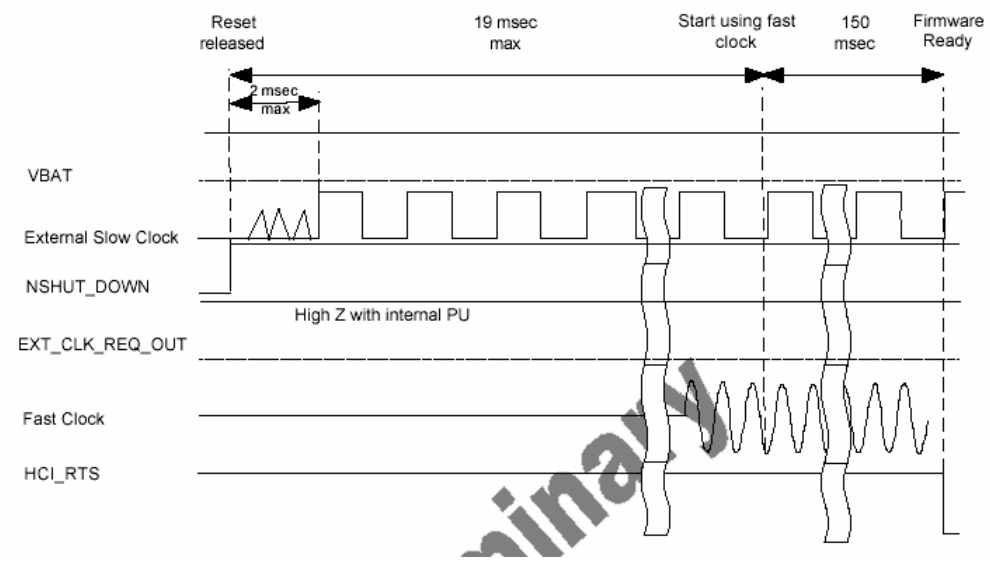

Fig 61

4.5.1 Reset behavior of the I/O Pins

All I/O-pins are set to input or high impedance state after power up of the BRF6150 device in order to prevent driver conflicts with connected signal lines. Internal pull resistors are enabled on each of the I/O pins as described in the terminal function description section. These pull resistors are disabled after start-up in order to minimize the power consumption. During the power up phase of the chip, the pull resistor and the I/O levels depend on the internal Power ON Reset (POR) and NSHUT_DOWN input. The following figure describes the behavior of the I/Os and the Pull resistors on power up. The software disables some of the pull resistors after the power up stage.

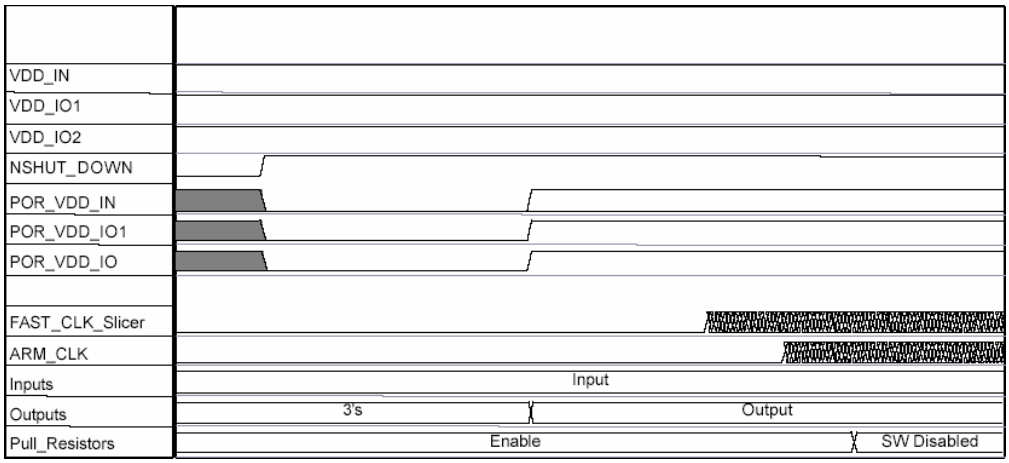

Fig 62

4.6. Audio CODEC interface

The CODEC interface is a fully dedicated programmable serial port that provides the

necessary logic to interface to several kinds of PCM or I2S CODECs. This interface supports two channels.

4.6.1 PCM interface

This interface consists of four signals: a clock AUD_CLK, a data input AUD_IN, a data output AUD_OUT, and a frame-synchronization signal AUD_FSYNC. This interface offers a wide flexibility by providing parameters configurable by a vendor-specific HCI command. These parameters are:

§ PCM highway master/slave role selection

§ PCM highway clock frequency

§ Frame-synchronization format (short frame, long frame, frame polarity)

§ Data position in the Frame

The Master/Slave mode selects the source of the clock and synchronization signals on the PCM highway.

The BRF6150 is receives both clock and frame of the audio codec when G2 is master.

4.6.2 Clock frequency and frame synchronization

When in slave mode, the BRF6150 AUD_CLK input can accept clock frequency between 64 kHz 10 MHz. In cases where the frame Sync line is an input (e.g. when the BRF6150 is the PCM slave) the interface supports any frame sync duty cycle and period (up to 2048 clock cycles width). The interface's hardware can detect and report

events where the configured Frame Sync period does not match the actual Frame Sync period so that the firmware can report the event to the host and/or correct the configuration.

4.6.3 Flexible data format

The data format is fully configurable:

§ The data length can be from 1 to 40 bits in 1 bit increments when working with two channels or up to 80 bits when using 1 channel. If the data length is not byte aligned it will be zero padded to the nearest 8bit multiple. Data length can be set independently for each channel.

§ The data position within a frame is also configurable in with 1 clock (bit) resolution and can be set independently for each channel. (The data position is relative to the edge of the Frame Sync signal.)

The Data Out line can be configured to switch to 'High-Z' output when it is not in use (i.e. between data words). This feature is required when the BRF6150 is a bus slave in a multi-slave PCM bus, so there will be no collisions on the Master's Data In line.

4.6.4 A 2 Channel PCM bus Example

In the following figure a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer)

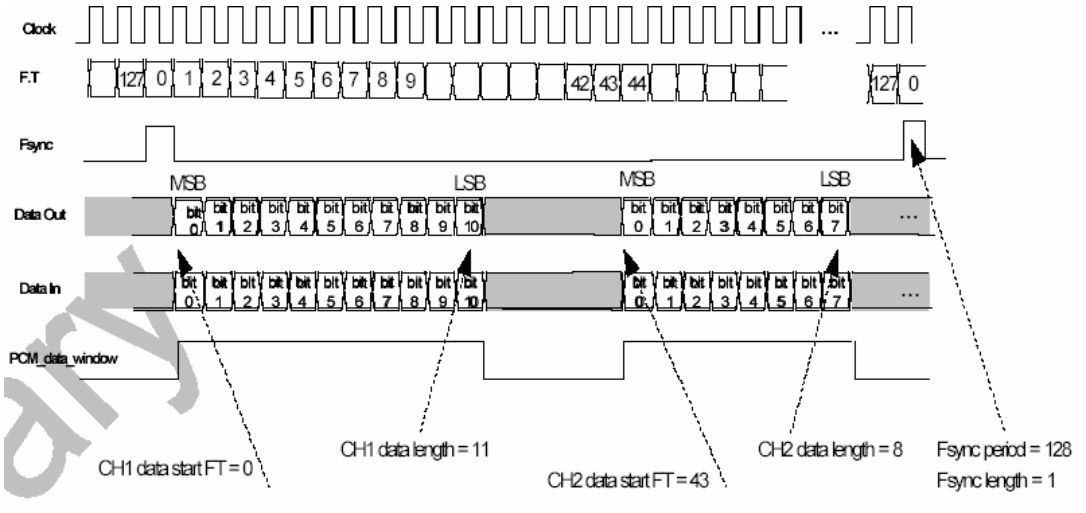

Fig 63

4.6.5 Audio Encoding

The BRF6150 CODEC interface can use one of four audio coding patterns:

§ A-law (8-bit)

§ m-Law (8-bit)

§ Linear (8 or 16-bit)

§ Transparent

4.7. Firmware structure and support

The BRF6150 implements the Bluetooth protocol stack up to HCI layer. This software stack incorporates the link controller (LC), link manager (LM), host controller interface (HCI) and the HCI transport layer as shown in the following diagram.

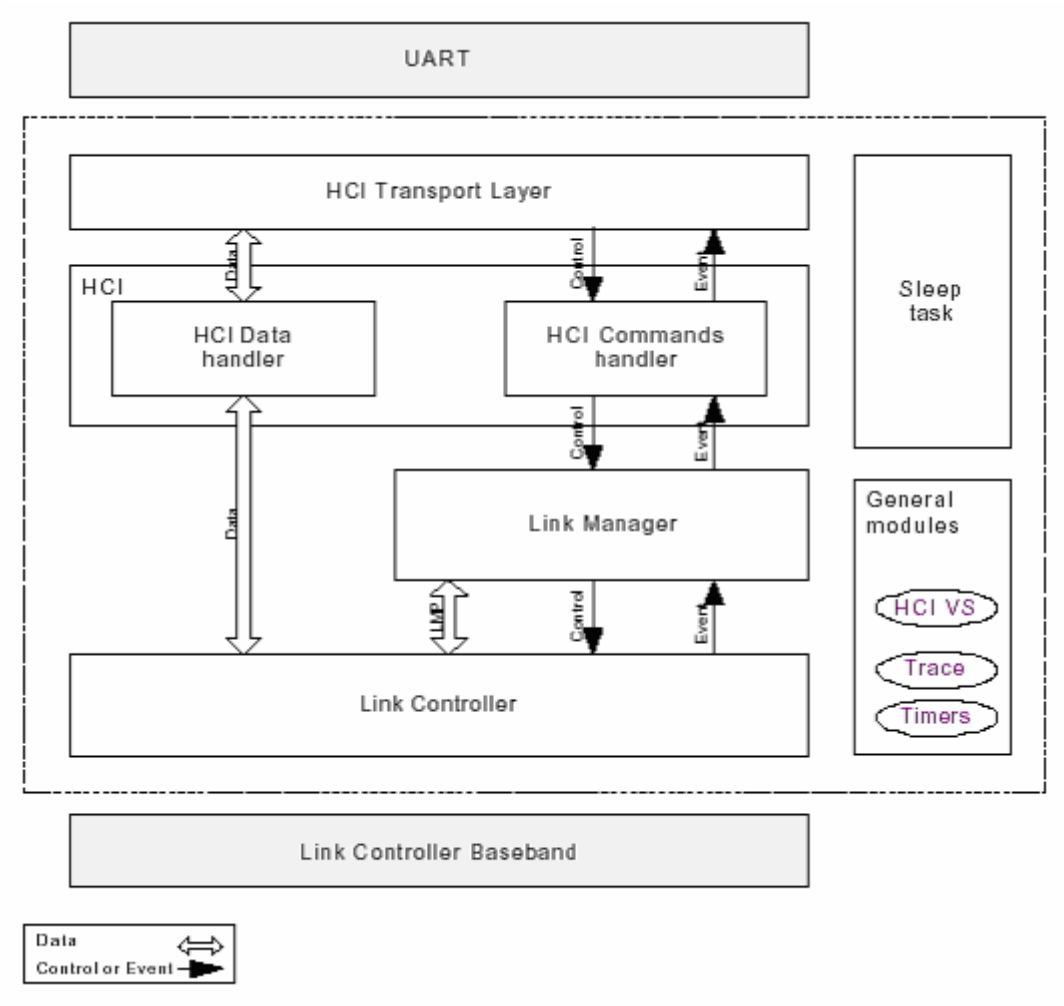

Fig 64

The BRF6150 firmware supports all the features described in Bluetooth Specification 1.2 with backward compatibility with Bluetooth Specification 1.1.