DATA SHEET

NEC

SILICON POWER MOS FET
NE5510279A

4.8 V OPERATION SILICON RF POWER LD-MOS FET FOR 1.8 GHz 2 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5510279A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 4.8 V GSM 1 800 handsets. Dies are manufactured using our NEWMOS technology (our 0.6 μm WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. The device can deliver 33.0 dBm output power with 47% power added efficiency at 1.8 GHz under the 4.8 V supply voltage.

FEATURES

- High output power : P_{out} = 35.5 dBm TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 900 MHz, P_{in} = 25 dBm)
  : P_{out} = 33.0 dBm TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 1.8 GHz, P_{in} = 25 dBm)
- High power added efficiency : η_{add} = 65% TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 900 MHz, P_{in} = 25 dBm)
  : η_{add} = 47% TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 1.8 GHz, P_{in} = 25 dBm)
- High linear gain : G_L = 16.0 dB TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 900 MHz, P_{in} = 10 dBm)
  : G_L = 10.0 dB TYP. (V_{DS} = 4.8 V, I_{Dset} = 300 mA, f = 1.8 GHz, P_{in} = 10 dBm)
- Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.
- Single supply : V_{DS} = 3.0 to 6.0 V

APPLICATIONS

- Digital cellular phones : 4.8 V GSM 1 800 class 1 handsets
- Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5510279A-T1	79A	W2	• 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.
Part number for sample order: NE5510279A

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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The mark ★ shows major revised points.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

	Parameter	Symbol	Ratings	Unit
★	Drain to Source Voltage	V_{DS}	20.0	V
	Gate to Source Voltage	V_{GS}	5.0	V
	Drain Current	I_{DS}	1.0	A
	Drain Current (Pulse Test)	I_{DS} Note	2.0	A
	Total Power Dissipation	P_{tot}	20	W
	Channel Temperature	T_{ch}	125	°C
	Storage Temperature	T_{stg}	–65 to +125	°C

Note Duty Cycle ≤ 50%, T_{on} ≤ 1 s

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V_{DS}		3.0	4.8	6.0	V
Gate to Source Voltage	V_{GS}		0	2.0	3.5	V
Drain Current (Pulse Test)	I_{DS}	Duty Cycle ≤ 50%, T_{on} ≤ 1 s	–	1.0	1.5	A
Input Power	P_{in}	f = 1.8 GHz, V_{DS} = 4.8 V	25	–	27	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

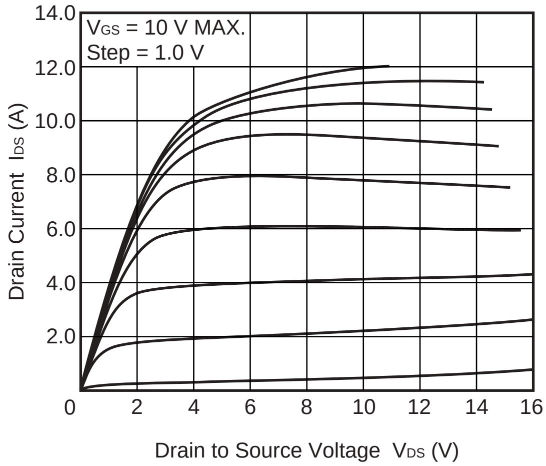
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I_{GSS}	V_{GSS} = 5.0 V	–	–	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	I_{DSS}	V_{DSS} = 8.5 V	–	–	100	nA
Gate Threshold Voltage	V_{th}	V_{DS} = 4.8 V, I_{DS} = 1 mA	1.0	1.35	2.0	V
Transconductance	g_m	V_{DS} = 4.8 V, I_{DS} = 600 mA	–	1.50	–	S
Drain to Source Breakdown Voltage	BV_{DSS}	I_{DSS} = 10 μA	20	24	–	V
Thermal Resistance	R_{th}	Channel to Case	–	5	–	°C/W
Linear Gain	G_L	f = 900 MHz, P_{in} = 10 dBm, V_{DS} = 4.8 V, I_{Dset} = 300 mA, **Note 1, 2**	–	16.0	–	dB
Output Power	P_{out}	f = 900 MHz, P_{in} = 25 dBm, V_{DS} = 4.8 V, I_{Dset} = 300 mA, **Note 1, 2**	–	35.5	–	dBm
Operating Current	I_{op}		–	1 000	–	mA
Power Added Efficiency	η_{add}		–	65	–	%
Linear Gain	G_L	f = 1.8 GHz, P_{in} = 10 dBm, V_{DS} = 4.8 V, I_{Dset} = 300 mA, **Note 1, 2**	–	10.0	–	dB
Output Power	P_{out}	f = 1.8 GHz, P_{in} = 25 dBm, V_{DS} = 4.8 V, I_{Dset} = 300 mA, **Note 1, 2**	32.0	33.0	–	dBm
Operating Current	I_{op}		–	750	–	mA
Power Added Efficiency	η_{add}		38	47	–	%

Notes 1. Peak measurement at Duty Cycle ≤ 50%, T_{on} ≤ 1 s.

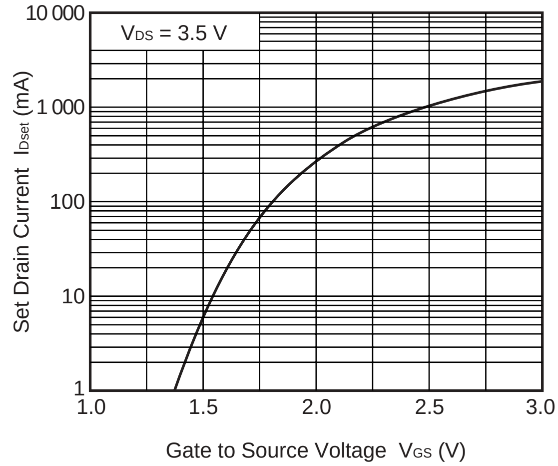
2. DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (T_A = +25°C)

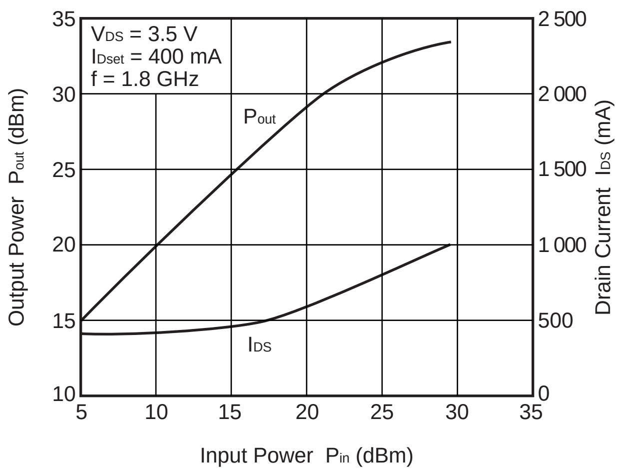
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



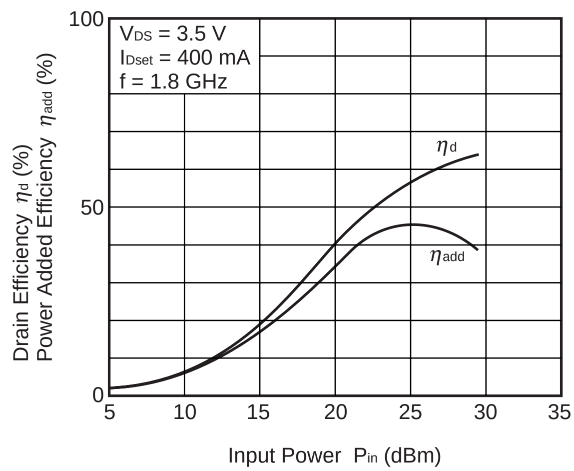
SET DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE



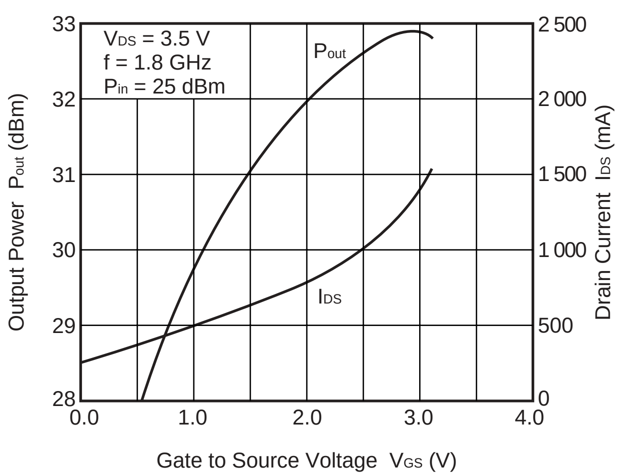
OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



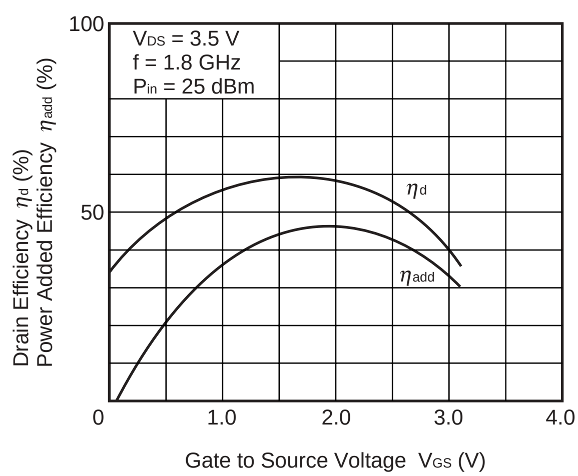
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. INPUT POWER



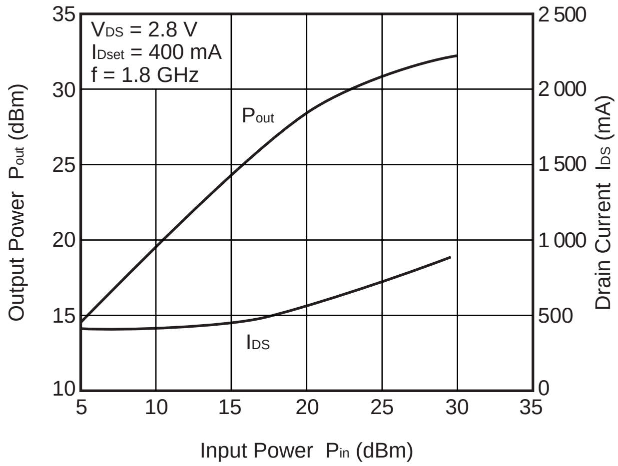
OUTPUT POWER, DRAIN CURRENT
vs. GATE TO SOURCE VOLTAGE



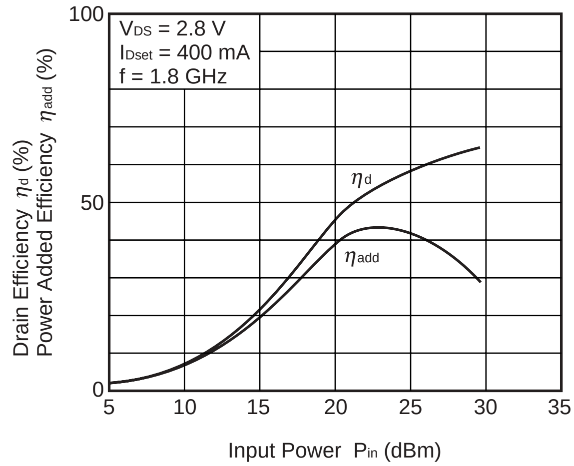
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. GATE TO SOURCE VOLTAGE



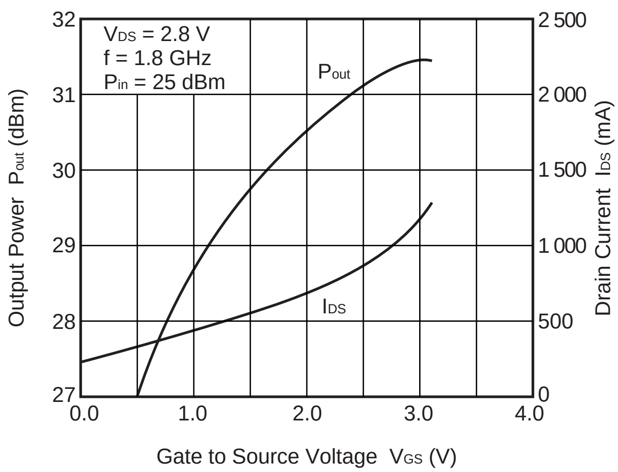
OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



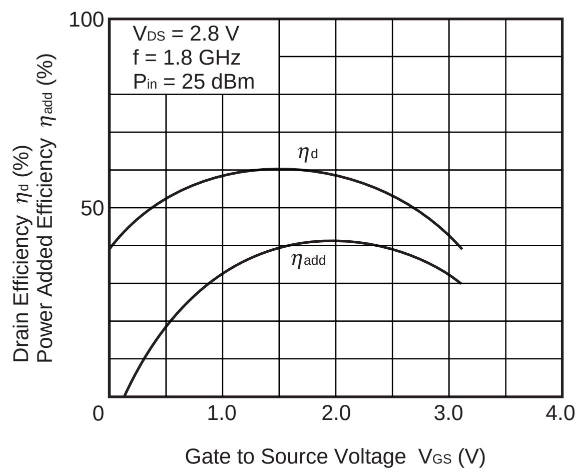
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. INPUT POWER



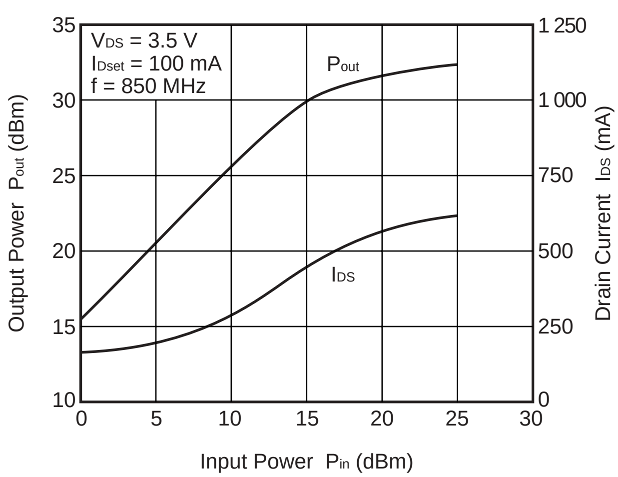
OUTPUT POWER, DRAIN CURRENT
vs. GATE TO SOURCE VOLTAGE



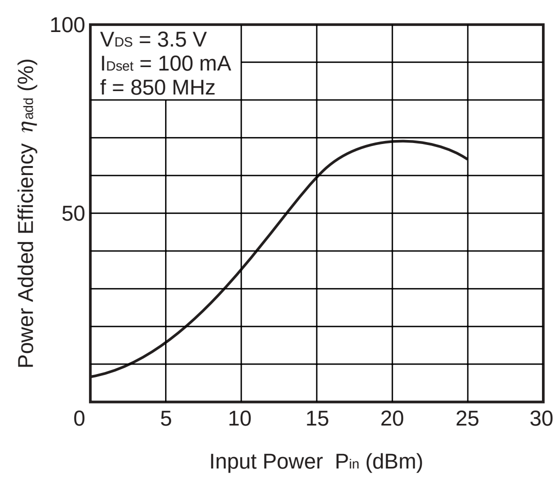
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. GATE TO SOURCE VOLTAGE



OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



POWER ADDED EFFICIENCY
vs. INPUT POWER



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

Test Conditions: V_{DS} = 3.5 V, I_{Dset} = 400 mA

Frequency	S_{11}		S_{21}			S_{12}			S_{22}		MAG Note	MSG Note	K
GHz	MAG.	ANG.	dB	MAG.	ANG.	dB	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.889	–149.7	18.8	8.66	99.8	–34.4	0.019	14.6	0.854	–173.8		26.6	
0.2	0.872	–165.4	12.9	4.41	87.5	–34.0	0.020	3.4	0.861	–177.7		23.4	
0.3	0.871	–170.9	9.3	2.91	82.0	–34.0	0.020	–1.8	0.875	–178.6		21.6	
0.4	0.871	–173.7	6.6	2.13	76.1	–34.4	0.019	–4.1	0.869	–179.6		20.5	
0.5	0.873	–175.6	4.6	1.69	71.5	–34.4	0.019	–9.5	0.886	179.7		19.5	0.04
0.6	0.880	–176.9	2.7	1.37	67.7	–34.9	0.018	–11.8	0.886	179.2		18.8	0.22
0.7	0.884	–177.9	1.4	1.17	63.9	–35.9	0.016	–10.6	0.893	178.9		18.6	0.40
0.8	0.897	–179.1	–0.1	0.99	60.5	–35.9	0.016	–10.2	0.898	178.0		17.9	0.40
0.9	0.905	–179.9	–1.2	0.87	56.3	–37.1	0.014	–15.0	0.914	177.6		17.9	0.41
1.0	0.919	178.1	–2.3	0.77	53.8	–37.1	0.014	–7.8	0.928	176.0		17.4	0.16
1.1	0.930	175.9	–3.2	0.69	48.8	–38.4	0.012	–13.7	0.938	174.8		17.6	0.11
1.2	0.923	174.2	–4.4	0.60	46.9	–38.4	0.012	–11.0	0.927	172.9		17.0	0.59
1.3	0.919	172.9	–5.4	0.54	42.6	–40.0	0.010	–10.5	0.923	171.8	14.1		1.29
1.4	0.918	171.8	–6.4	0.48	41.0	–40.0	0.010	–4.7	0.922	170.6	12.2		1.62
1.5	0.918	170.6	–7.1	0.44	37.6	–39.2	0.011	–8.0	0.924	170.1	11.7		1.53
1.6	0.920	168.9	–7.7	0.41	36.7	–41.9	0.008	–5.5	0.927	168.7	10.4		2.46
1.7	0.918	167.5	–8.9	0.36	33.6	–41.9	0.008	4.3	0.922	167.9	8.5		3.27
1.8	0.927	166.2	–9.1	0.35	30.9	–40.9	0.009	12.5	0.935	165.9	10.3		1.95
1.9	0.922	164.1	–10.2	0.31	28.2	–43.1	0.007	20.9	0.932	164.9	7.9		3.67
2.0	0.923	162.6	–10.5	0.30	27.8	–43.1	0.007	32.4	0.942	163.0	8.6		3.08
2.1	0.928	159.9	–11.7	0.26	25.2	–43.1	0.007	48.5	0.928	161.8	6.2		4.46
2.2	0.926	158.6	–12.0	0.25	23.2	–44.4	0.006	36.8	0.938	160.0	6.3		4.89
2.3	0.929	156.6	–13.2	0.22	20.0	–41.9	0.008	50.0	0.935	157.6	5.4		4.01
2.4	0.925	154.5	–13.2	0.22	18.0	–40.9	0.009	45.1	0.945	156.2	6.2		3.01
2.5	0.928	152.2	–14.0	0.20	18.1	–43.1	0.007	61.4	0.941	154.5	4.8		4.77
2.6	0.933	150.4	–14.0	0.20	17.2	–40.9	0.009	56.3	0.938	152.5	5.2		3.43
2.7	0.930	148.4	–15.9	0.16	15.0	–39.2	0.011	70.0	0.933	150.3	2.5		4.13
2.8	0.929	146.2	–15.4	0.17	11.1	–37.7	0.013	59.4	0.952	148.1	5.4		2.01
2.9	0.931	144.4	–15.9	0.16	11.6	–37.7	0.013	74.0	0.937	146.9	3.2		3.01
3.0	0.933	142.6	–16.5	0.15	10.0	–37.1	0.014	67.5	0.950	145.0	4.3		2.10

Note When K ≥ 1, the MAG (Maximum Available Gain) is used. $\text{MAG} = \left|\frac{S_{21}}{S_{12}}\right| (K - \sqrt{(K^2 - 1)})$

When K < 1, the MSG (Maximum Stable Gain) is used. $\text{MSG} = \left|\frac{S_{21}}{S_{12}}\right|$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12}| \cdot |S_{21}|}$,

$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$

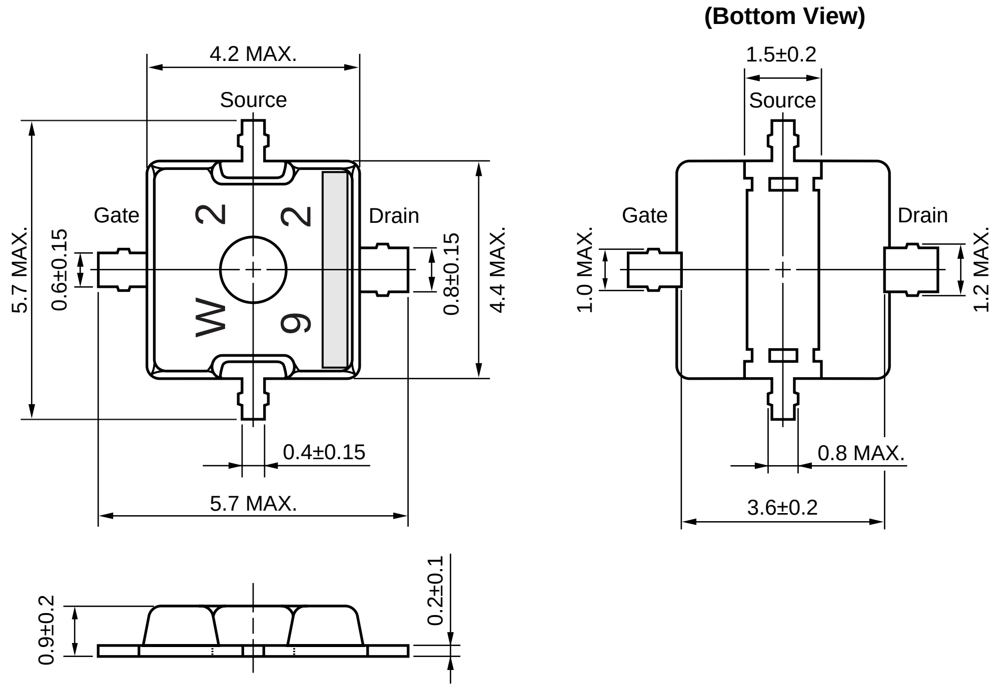
LARGE SIGNAL IMPEDANCE (V_{DS} = 3.5 V, I_{Dset} = 400 mA, P_{in} = 25 dBm)

f (GHz)	Z_{in} (Ω)	Z_{OL} (Ω) Note
1.8	TBD	TBD

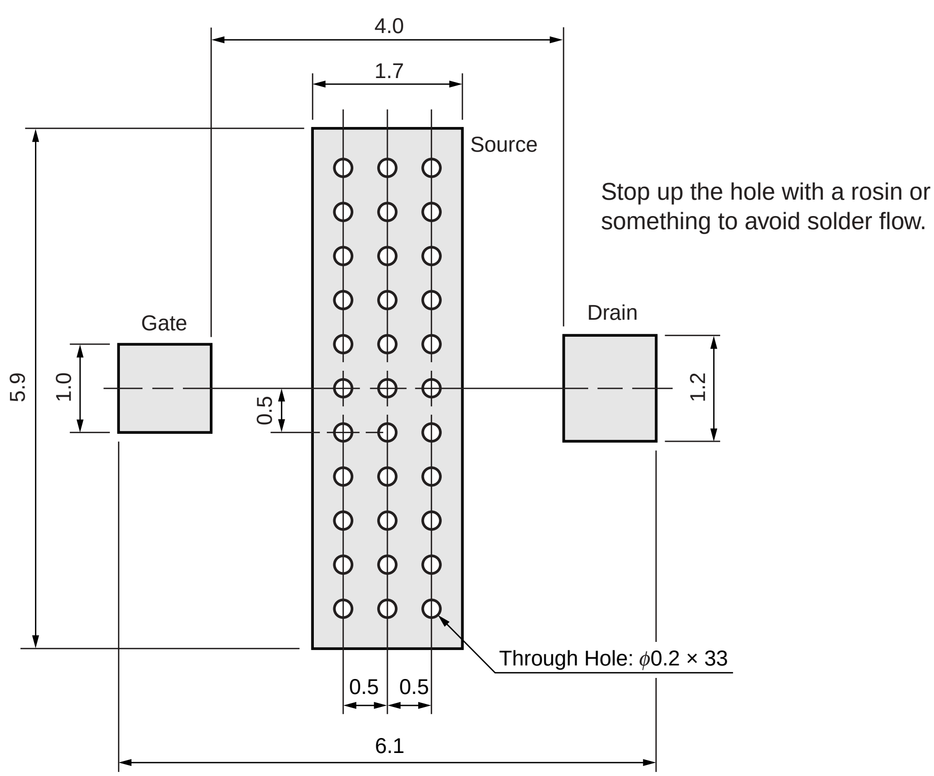
Note Z_{OL} is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per pin of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).

▶**Business issue**

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▶**Technical issue**

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