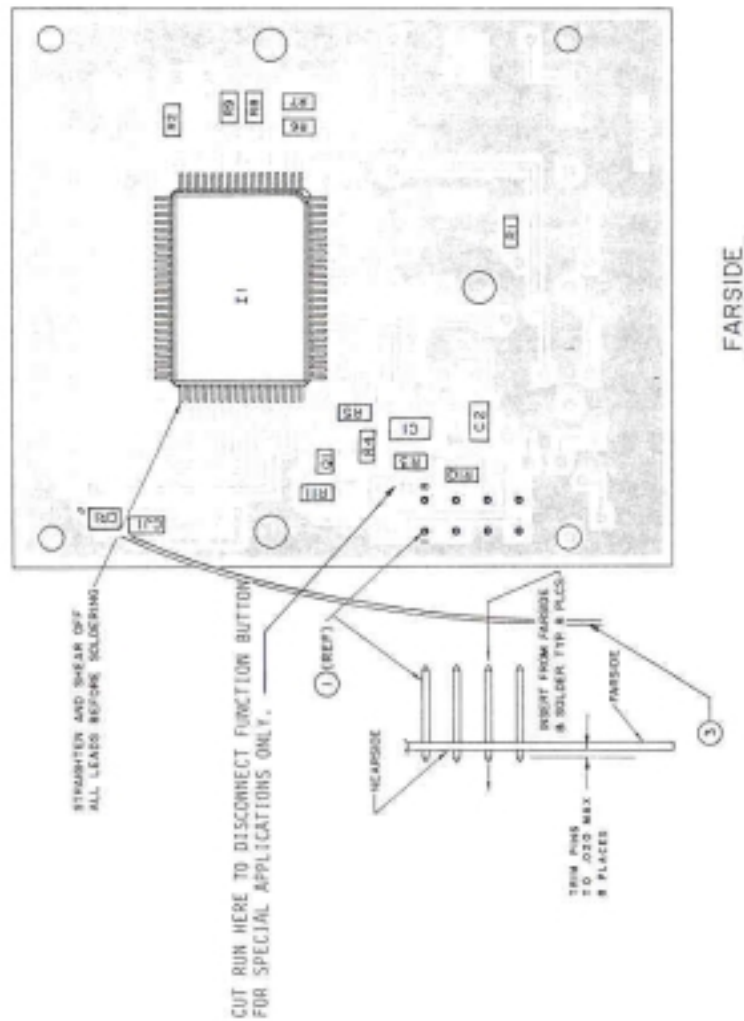
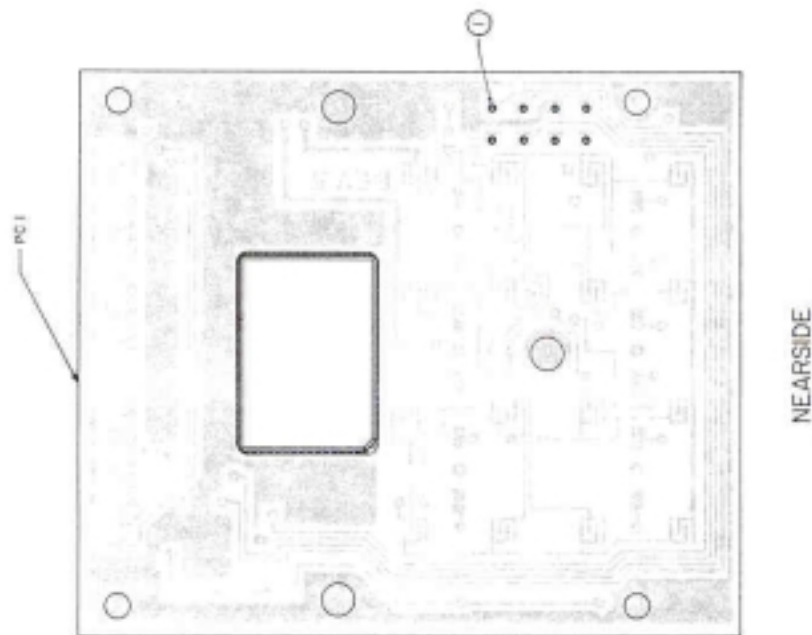


ILLUSTRATED PAIRTS LIST

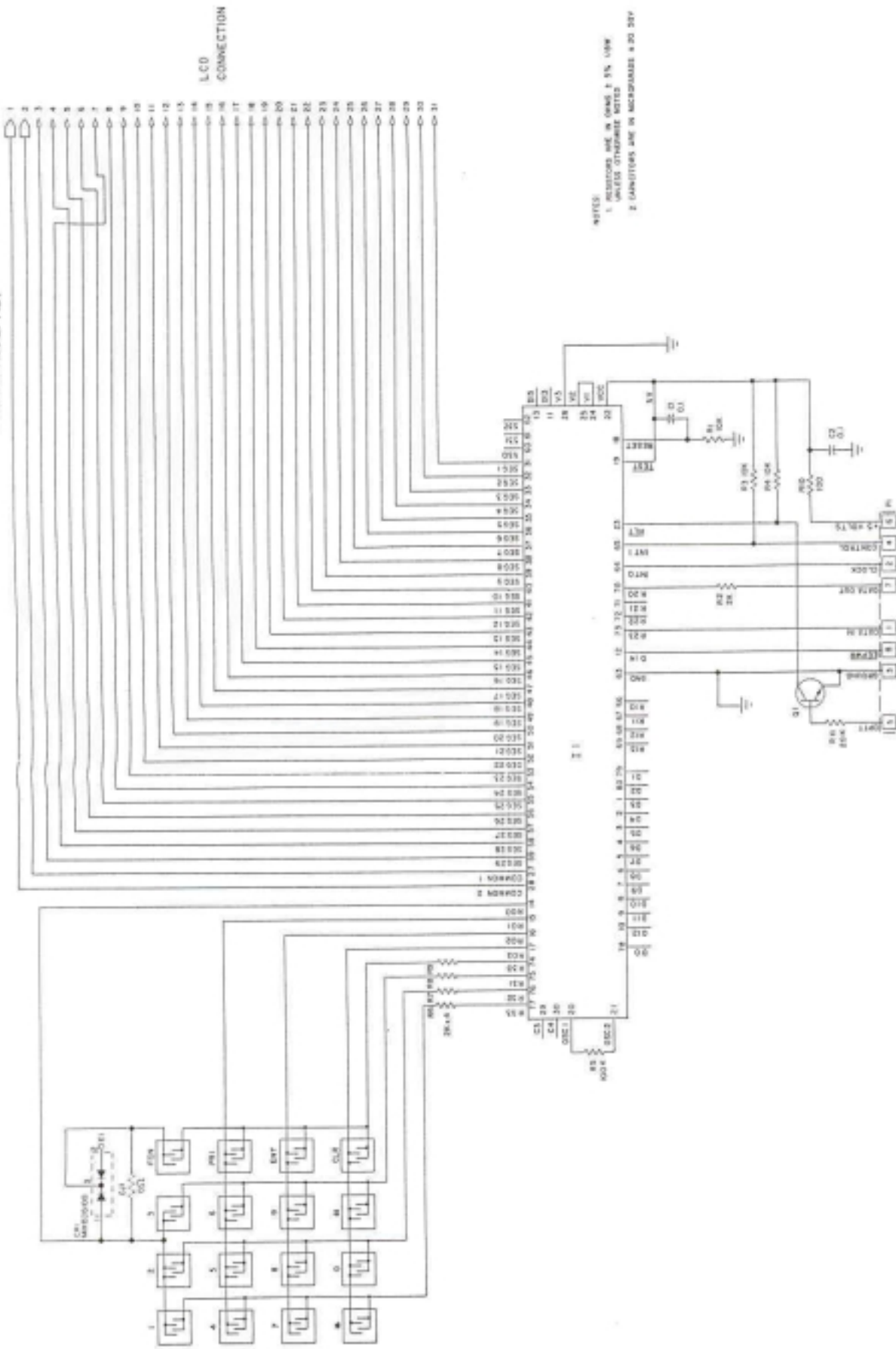
KEYBOARD DISPLAY BOARD

[illegible]

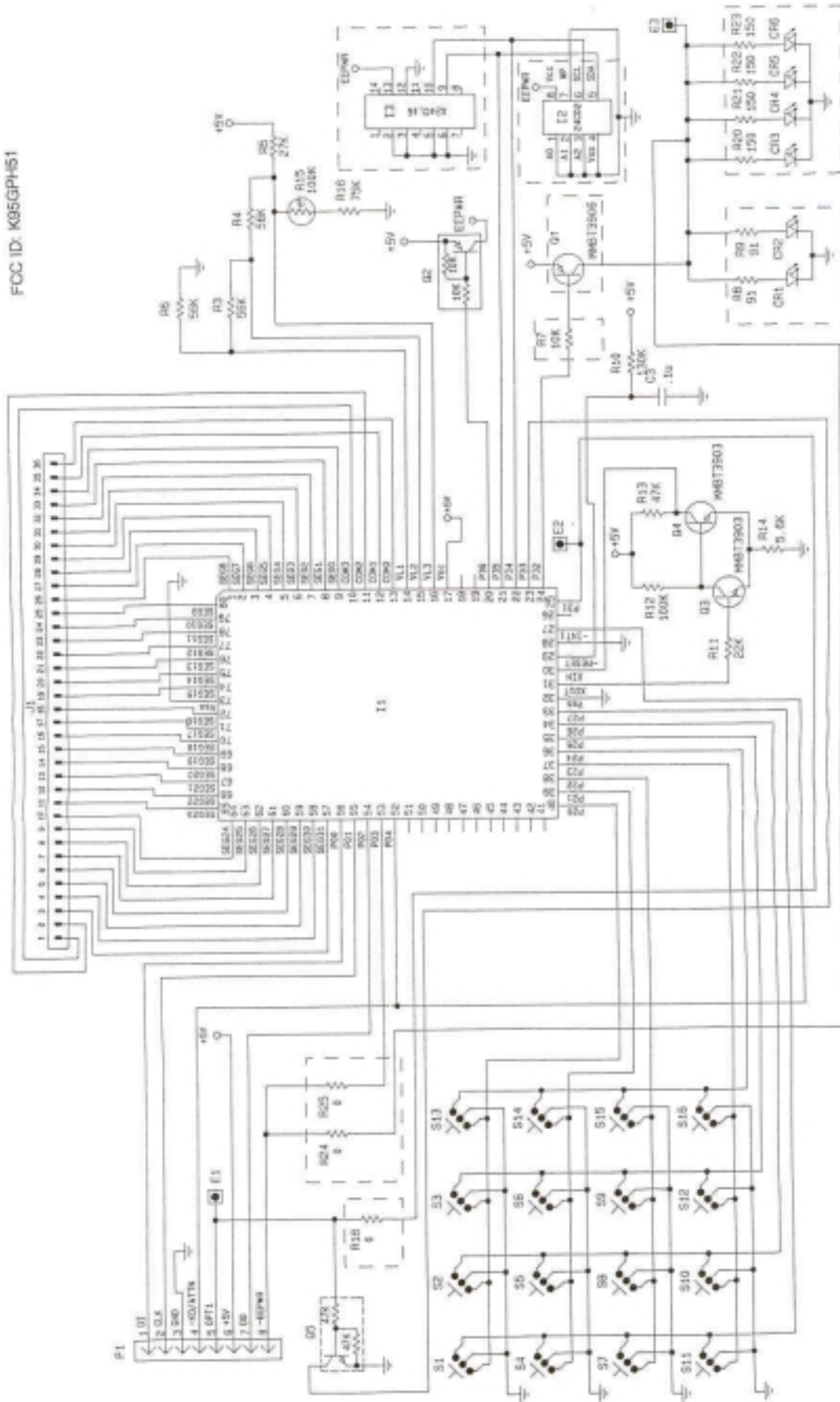
FCC ID: K95GPH51

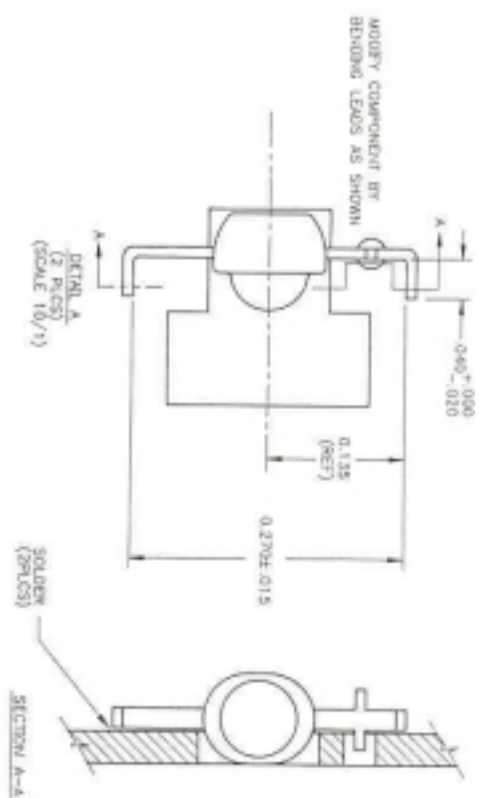


FCC ID: K95GPH51



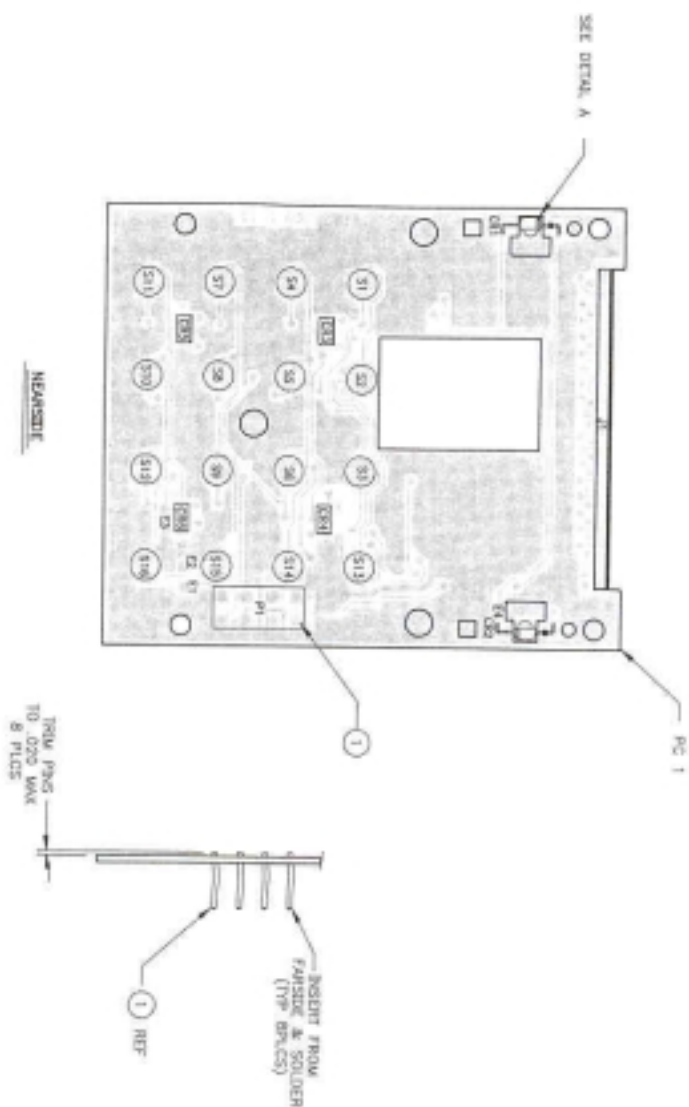
FCC ID: K95GPH451

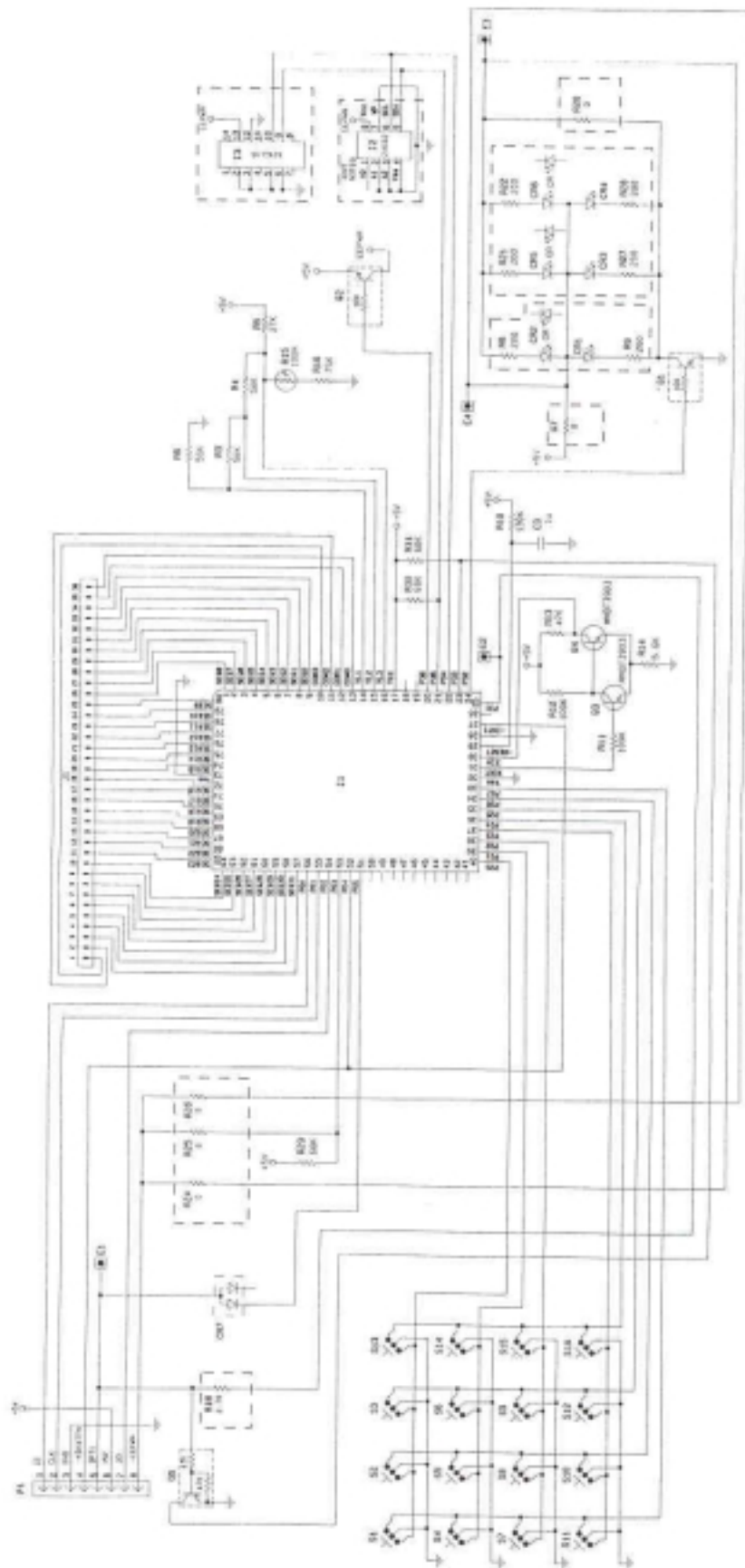




NOTES: UNLESS OTHERWISE SPECIFIED:

1. CR2 IS SHOWN IN ITS ALTERNATE POLARITY WHICH IS STANDARD FOR RADIOS USING +5V FOR THEIR LIGHTING SUPPLY. (SEE NOTE 5 OF 002-06924-0010)





APPENDIX A INTEGRATED CIRCUIT DATA

INTRODUCTION

This appendix contains descriptions of certain integrated circuits as an aid to understanding the operation of this equipment. Detailed information on IC's containing basic logic elements, op-amps, and other simple circuits are not included in this appendix as their theory of operation is summarized below and the operation of such circuits within this equipment may be readily understood from a review of this summary and the schematic diagrams included in Section VI of this manual.

BASIC LOGIC ELEMENTS

BUFFER



$$Z = A$$

A	Z
0	0
1	1

INVERTER



$$Z = \overline{A}$$

A	Z
0	1
1	0

OR GATE



$$Z = A + B + C$$

A	B	C	Z
0	0	0	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

NOR GATE



$$Z = \overline{A + B + C}$$

A	B	C	Z
0	0	0	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	0

AND GATE



$$Z = ABC$$

A	B	C	Z
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

NAND GATE



$$Z = \overline{ABC}$$

A	B	C	Z
0	0	0	1
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	0

EXCLUSIVE OR GATE

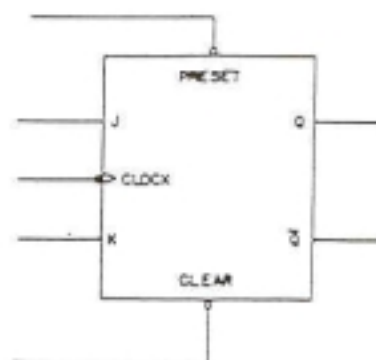


$$Z = A \oplus B$$

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

J K FLIP-FLOP

The flip-flop logic element is the basic data storage element of digital logic. It has two outputs that are always at opposite logic levels. That is, when one output is HI the other is LO. The flip-flop will remain in a particular state until that state is changed by an input signal.



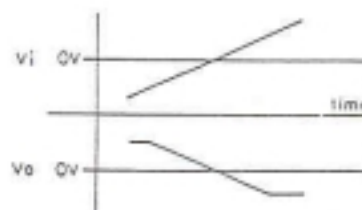
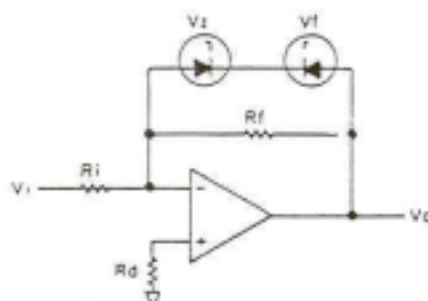
J	K	Q	$\bar{Q}$
L	L	Q_0	$\bar{Q}_0$
H	L	H	L
L	H	L	H
H	H	Toggle	Toggle

BASIC OP-AMP CIRCUITS

LIMITER

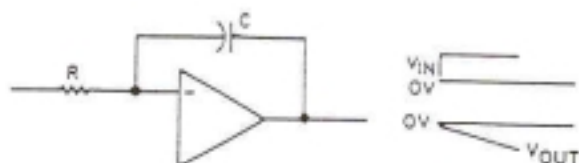
An output voltage may be limited to certain levels by selection appropriate zener diodes and placing them in parallel with the feedback resistor. Voltage limiting can be accomplished in both directions in this manner.

$$V_o [\max] = V_z + V_f$$

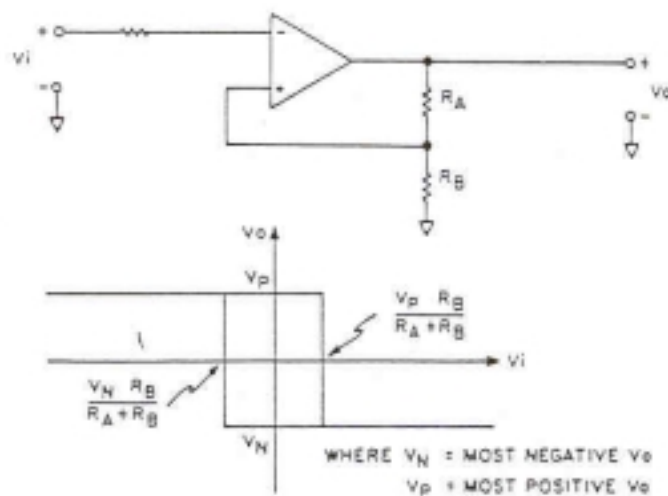


INTEGRATOR

An op-amp in which the only feedback element is a capacitor. The output of an integrator is a ramp, the slope of which is determined by the amplitude of the steady state input and the RC time constant.

ZERO CROSSING DETECTOR

The positive feed back path causes the output voltage to drive to the saturation potential of opposite polarity as the input voltage. Ideally, the output switches from one saturation level to the opposite saturation level as the input voltage passes through zero. Noise immunity demands the addition of R_B which requires that the input reach a certain magnitude after passing zero before the output will switch.



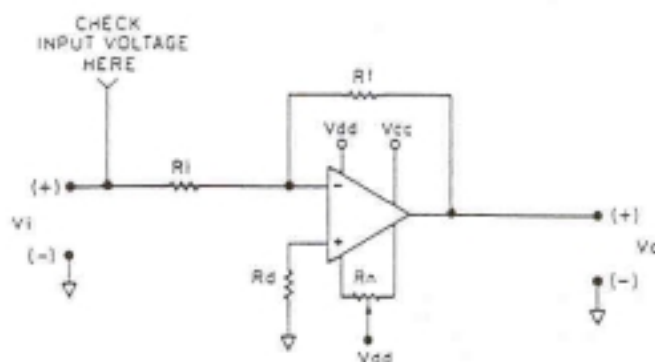
INVERTING OP-AMP AMPLIFIER

A voltage applied at the inverting (-) input will cause an output voltage [Vo] of opposite polarity as the applied voltage. The relationship of the input and output voltages is shown in the following equations:

$$V_o = (R_f/R_i) V_i$$

$$\text{GAIN} = -(R_f/R_i)$$

From the above equation, a zero input voltage should give a zero output if Rn has been adjusted to the null of the amplifier.

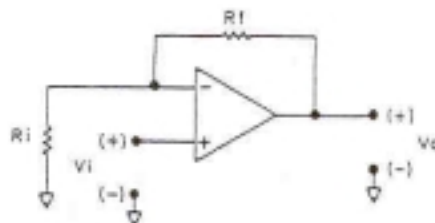


NON-INVERTING OP-AMP AMPLIFIER

A voltage applied at the non-inverting (+) input will cause an output voltage [Vo] of the same polarity as the applied voltage. The relationship of the input and output voltages is shown in the following equations:

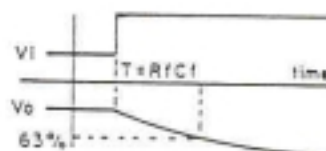
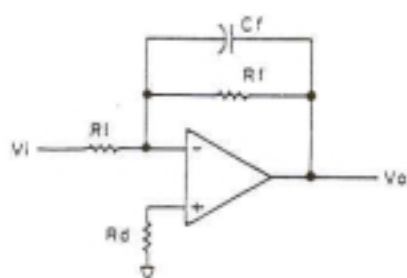
$$V_o = [1 + (R_f/R_i)] V_i$$

$$\text{GAIN} = 1 + (R_f/R_i)$$

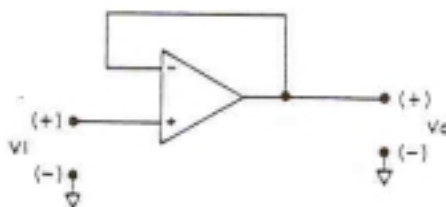


LOW PASS FILTER

The low pass filter is a variation of an inverting op-amp circuit. The addition of capacitor C_f to the feedback network around the amplifier provides low pass filtering to the input voltage. The expression $T = R_f C_f$ gives the time required for V_o to reach 63% of the final value.

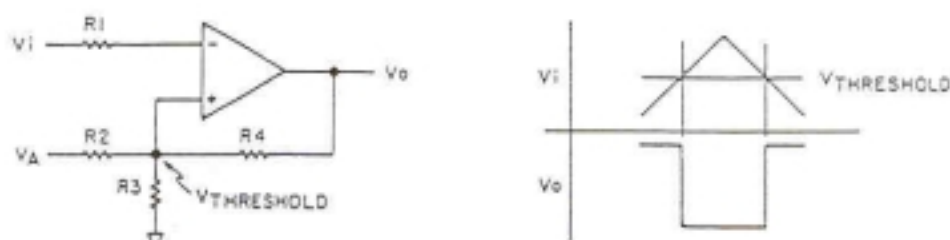
VOLTAGE FOLLOWER AMPLIFIER

This configuration is a special case of the non-inverting amplifier previously discussed, with R_f equal to zero. Therefore the relationship of the input and output voltage reduces to $V_o = V_i$, or unity gain. It is used to provide high input impedance and buffering action.



THRESHOLD DETECTOR

Threshold detectors use positive feedback to toggle the op-amp output when the input voltage (V_i) is above or below a voltage level (V threshold) set by R_2 and R_3 . R_4 provides the positive feedback required for a clean switch from one saturation level to another. The voltage polarity (V_A) determines the initial output state of the amplifier and the polarity of the threshold being detected.

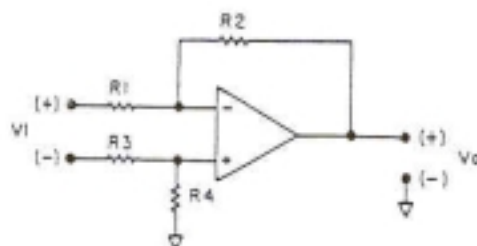


DIFFERENTIAL AMPLIFIER

The principal use of the differential amplifier is to translate signals, from sources referenced to some level other than signal ground, to signals referenced to signal ground. The relationship of the input and output voltages is shown in the following equations:

$$V_o = -(R_f/R_i) V_i \text{ if } R_1 = R_3 \text{ and } R_2 = R_4$$

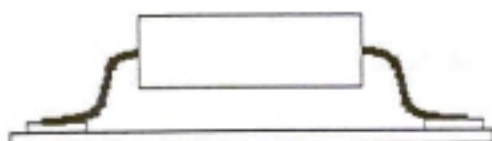
$$\text{GAIN} = -(R_f/R_i)$$



SURFACE MOUNT COMPONENTS

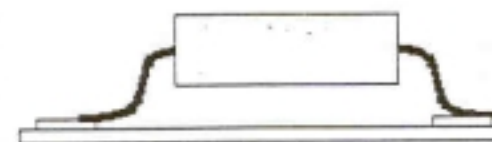
Round leaded and flat leaded components can be mounted on the surface of a board rather than through plated holes on a board.

The illustrations below demonstrate acceptable mounting practices for round leaded components on surface mount boards.



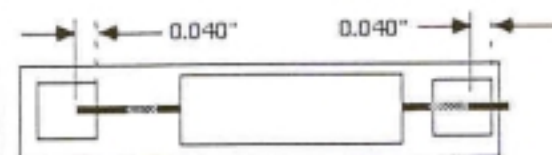
PREFERRED

Lead is centered on the pad. At least 0.040" (the thickness of a dime) is in contact with the pad. The lead does not overhang the pad.



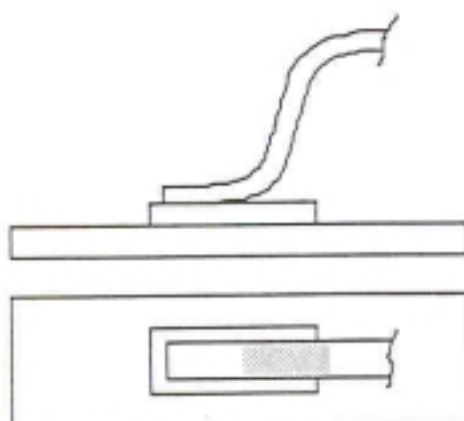
ACCEPTABLE MINIMUM

The lead has a minimum of contact area and has a slight overhang. The lead is not centered on the pad. The lead is at the edge of the pad. The contact area is not less than 0.040".



SURFACE MOUNT COMPONENTS (CON'T)

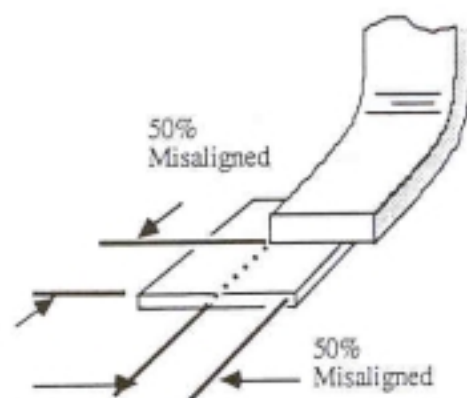
The illustrations below show acceptable ways of mounting flat leaded components.



PREFERRED

Lead is centered within the confines of the pad.

Heel rises before leaving pad area.

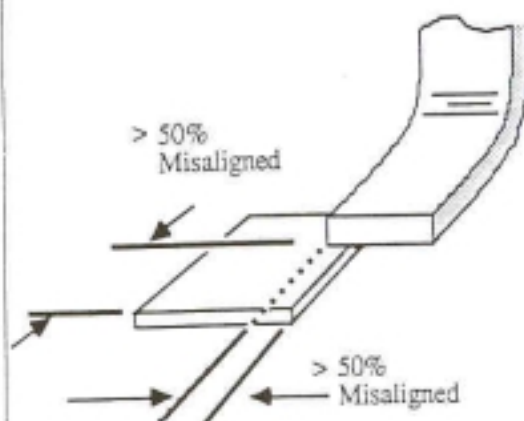


MINIMUM ACCEPTABLE

Lead misalignment is not more than 50%.

SURFACE MOUNT COMPONENTS (CON'T)

The illustration below shows an unacceptable way of mounting a flat leaded component.

**UNACCEPTABLE - REWORK**

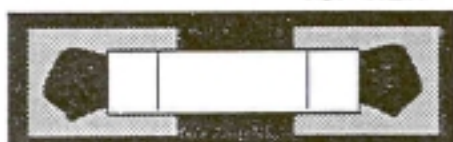
Lead is misaligned with the side of the pad or the length of the pad by more than 50%.

SURFACE MOUNT COMPONENTS (CON'T)

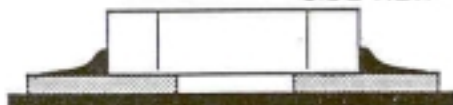
The following illustrations show acceptable solder height, amount of fillet, conductor spacing, and amount of allowable chip float.

The illustrations below show acceptable fillet heights.

TOP VIEW



SIDE VIEW

**PREFERRED**

Solder fillet height is 30% of the end height.

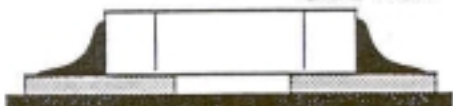
There is complete wetting of the pad and device end termination.

When the chips are wave soldered, it is permissible for the solder to come to the top or even over the cap of the end termination.

TOP VIEW



SIDE VIEW

**ACCEPTABLE**

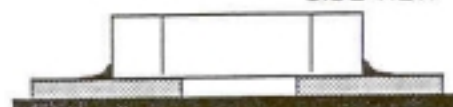
Solder fillet height is to the top of the end termination.

There is good wetting.

TOP VIEW



SIDE VIEW

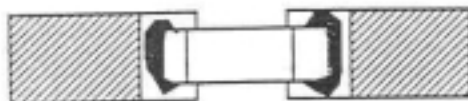
**MINIMUM
ACCEPTABLE**

The fillet height is 10% of the end termination.

There is incomplete wetting of the pad and termination.

SURFACE MOUNT COMPONENTS (CON'T)

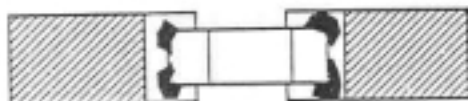
The illustrations below show acceptable amounts of solder applied to surface mount chips.

PREFERRED

The solder fillet is continuous around the perimeter of the chip termination.

There is good wetting of the land and termination.

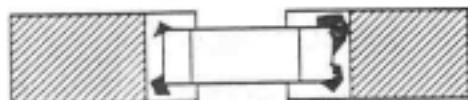
Fillet height is approximately 30% of the termination height.

MINIMUM ACCEPTABLE

There is 50% solder coverage of the perimeter of the chip.

The fillet height is at least 10% of the termination height.

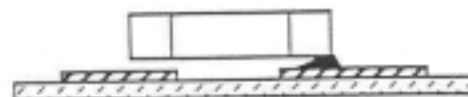
The illustration below shows a chip component that should be re-worked because of insufficient solder. There is less than 50% solder coverage around the perimeter and bottom of the chip.

**UNACCEPTABLE - REWORK**

There is less than 50% solder coverage on the perimeter of the chip.

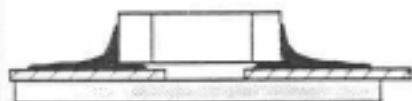
There is less than 50% solder coverage on the bottom of the chip.

The solder fillet is insufficient.



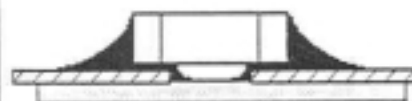
SURFACE MOUNT COMPONENTS (CON'T)

The two illustrations below show acceptable conductor spacing after solder flow. The spacing is not less than 50% of the original width or less than 0.005".



PREFERRED

The solder holds the chip to the pads and normal conductor spacings are maintained.



MINIMUM ACCEPTABLE

The spacing between the pads is reduced to 50% of the original spacing.

The illustration below shows an unacceptable chip component, where the spacing between pads is reduced by more than 50% because of excess solder. This component must be reworked.

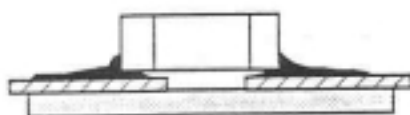


REWORK - UNACCEPTABLE

The spacing between the pads is reduced by more than 50% because of excess solder.

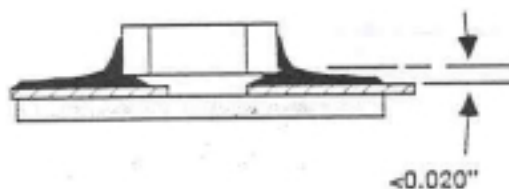
SURFACE MOUNT COMPONENTS (CON'T)

The illustrations below show acceptable components that have not floated higher than 0.020" above their pads.



PREFERRED

The solder height is minimal.
The fillet is concave.
There is good wetting.
The chip is raised less than 0.020".



ACCEPTABLE

The solder has floated the chip off its adhesive (if used) but the amount of float is not greater than 0.020".