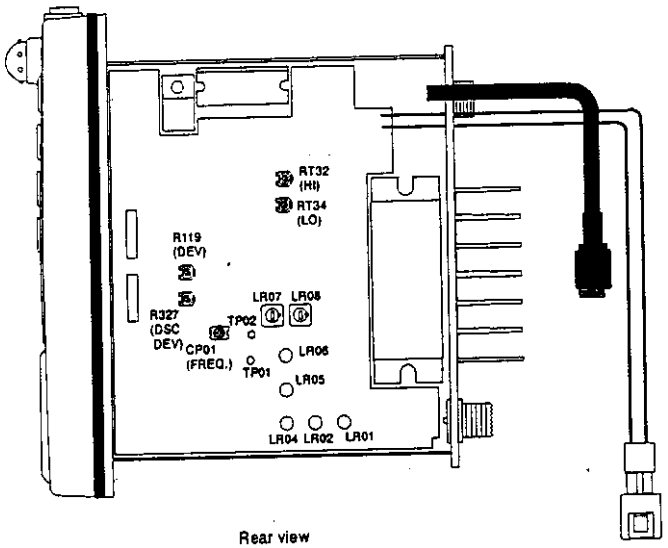
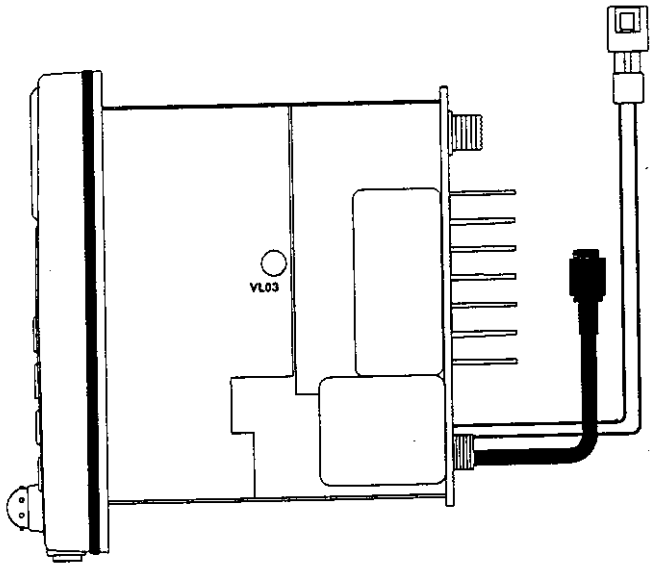
ALIGNMENT

Refer to Figure 1 for the location of alignment point.



Rear view



Front view

Figure 1Test Points

1 General

the test mode has been built in the microprocessor in order to adjust and confirm the performance of transceiver.

1. Loosen the four screws on the rear of the transceiver and remove the cover.
2. Set up the equipment as shown in Figure 1. Confirm that the power supply is set for 13.8 VDC

measured at the transceiver.

3. To turn on the radio on the test mode while the H/L and POS keys are hold down. Then press and hold down the volume knob until the LCD display will show a model name. And set the volume and squelch for mid-rang.

2. Voltage-Controlled Oscillator (VCO) Adjustment

1. Select channel 16 and adjust LV03 of VCO for a voltage reading 2.2VDC at test point marked "Lock TP".

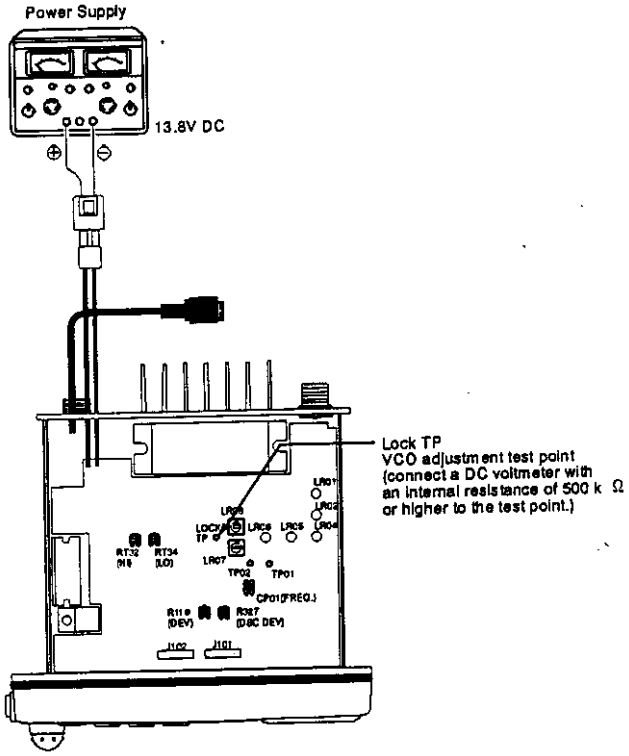


Figure 2

3. Transmitter

1. Key the transmitter. Adjust RT32 for 24W.
2. Unkey the radio.
3. Set the radio to low power. Key the radio and adjust RT34 for 0.8W. Unkey the radio.
4. Set the radio to high power. Key the radio and adjust CP01 for a service monitor reading of 156.800MHz +/-50Hz.
5. Unkey the radio.
6. Key the radio and set the output level of the audio generator as to produce +/- 3.0kHz deviation. Increase the audio generator output by 20dB and adjust R119 for +/- 4.5kHz deviation.
7. Unkey the radio.
8. Select channel 70 and key the radio. Adjust R327 for +/- 3.0kHz deviation.

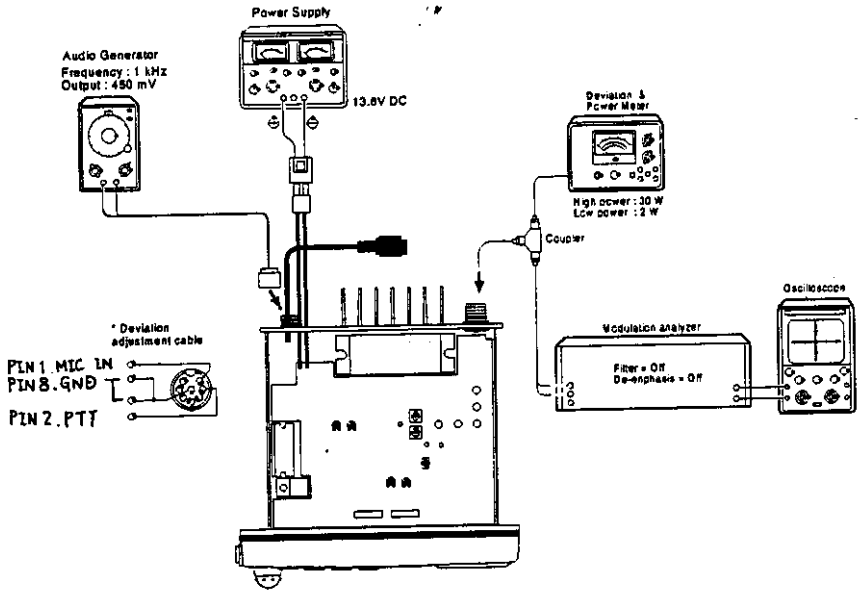


Figure 3

4. Receiver

1. With the channel selector on The front panel, set the transceiver to channel 06 (156.05MHz).
2. Adjust LR07 and LR08 until the spectrum analyzer is maximum.
3. Repeat steps 2 for weather channel WX01.

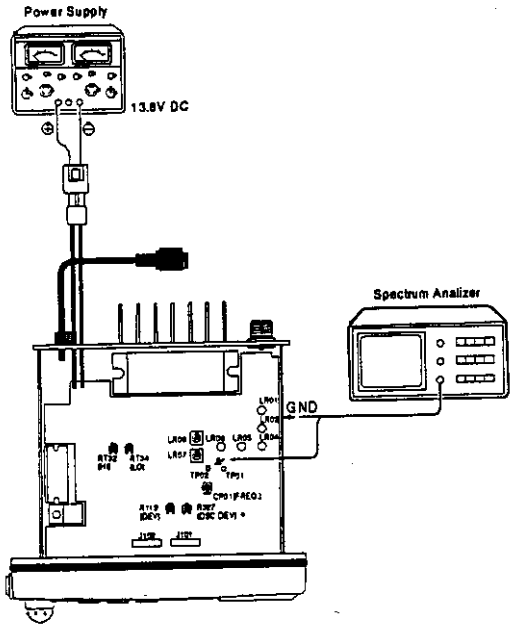


Figure 4

5. Front End

1. Adjust LR01, LR02, LR04, LR05 and LR06. So that the data on the spectrum analyzer as shown below.

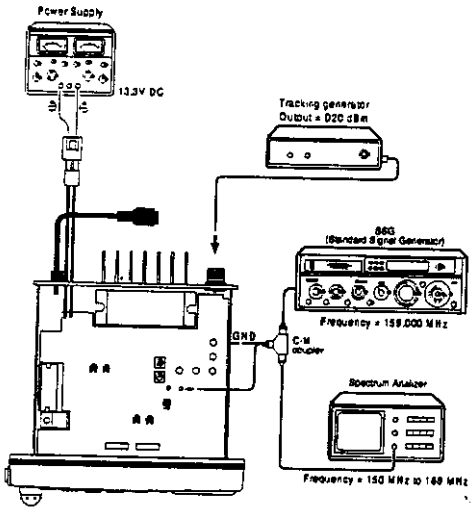


Figure 4

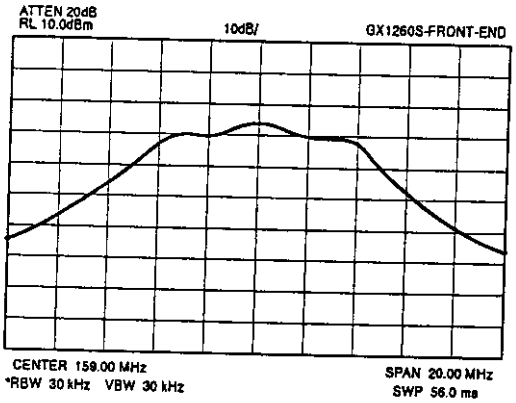


Figure 5

6. Sensitivity

1. With the channel selector on the front panel, set the transceiver to channel 06 (156.300MHz).
2. Confirm that the 12dB SINAD sensitivity is 0.45uV or less and that the 20dB QS sensitivity is 0.5uV.
3. Repeat steps 1 and 2 for channel 28(162.000MHz).

< How to confirm the DSC DOT PATTERN DATA >

1. Push the H/L key and POS key and turn on.
   (Condition : Test Mode)
2. Set TX Power to CH16 by pushing H/L key.
3. Set to CH70.
4. Every time you push the PTT switch, it turns to 1300Hz, 2100Hz, DOT PATTERN.
   The condition TX is valid only when pushing the PTT switch.

3.1 Phase-Locked Loop (PLL)

Refer to Figure 3-1.

The Phase-locked loop (PLL) consists of VCO ZZ01, reference oscillator XP01, PLL IC QP01, and PLL loop filter QP02, QP03, QP04 and QP05. The microprocessor QL01 supplies the clock, data, and strobe signals determined by the operating frequency set by the UP/DOWN keys. This data is output from pins 36, 37, and 39 of microprocessor QL01 and applied to pins 9, 10, and 11 of PLL IC QP01. The first local oscillator frequency is output from pin 3 of VCO ZZ01 (TX LO = TX Frequency RX LO = RX Frequency -21.4 MHz).

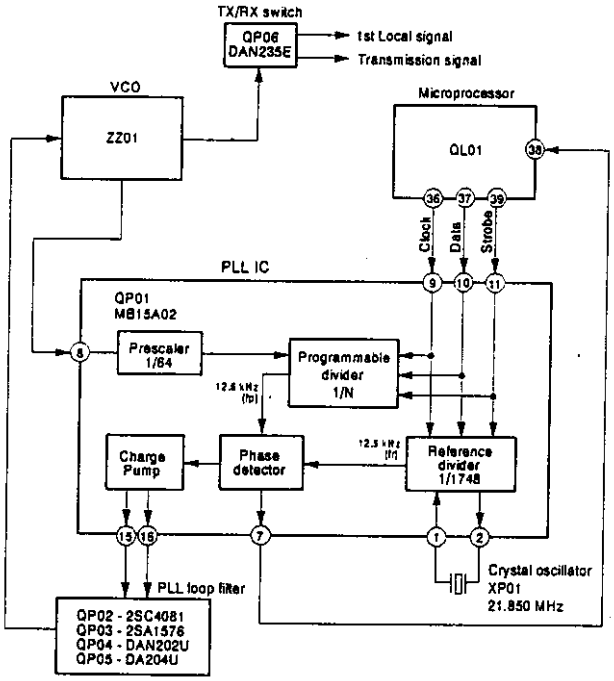


Figure 3-1 PLL Block diagram

3.1.1 Programmable Divider

The microprocessor QL01 determines a divide-by number (N) which is sent to PLL IC QP01, Inside QP01, the programmable divider divides the VCO frequency by N after being supplied to the divide-by-64 prescaler to produce a 12.5 kHz signal. Changing the operating frequency will cause the N number from the microprocessor QL01 and the frequency from the prescaler to the programmable divider to change so that the programmable divider is consistently providing a 12.5 kHz signal to the phase detector.

3.1.2 Phase Detector

The phase detector compare between frequency from the programmable divider (fp) and the reference frequency (fr).

3.1.3 Reference Divider

The 21.850 MHz frequency produced by the crystal oscillator XP01 passes through pin 1 of PLL IC QP01 and applied to the reference divider. The reference frequency (12.5 kHz) is produced by dividing the reference oscillator frequency by 1748. It is then applied to the phase detector in QP01.

3.1.4 PLL Loop Filter

The PLL loop filter is a low pass filter comprised of QP02, QP03, QP04, and QP05. It eliminates any frequency components that may be present in the voltage output from pins 15 and 16 of PLL IC QP01. The filtered voltage is then fed to pin 1 of VCO ZZ01.

3.1.5 Voltage-Controlled Oscillator (VCO)

During receive, pin 21 of microprocessor QL01 outputs a low voltage (0 V) which allows the 8 V regulator Q205 to supply RX+B to pin 2 of VCO ZZ01 through Q206. During receive, the first LO signal from pin 3 of VCO ZZ01 is applied to the first local amplifier QR05 for amplification.

During transmit, pin 21 of microprocessor QL01 outputs a high voltage (5 V) to the base of TX +B switch Q208 which turns off RX +B switch Q206 and allows the voltage to pass through Q208 and be applied to pin 4 of VCO ZZ01. Also during transmit, the audio supplied from the microphone is amplified by microphone amps Q311 and Q107 then applied to R119 for deviation adjustment, after through Q103. The signal is then applied to pin 5 VCO ZZ01 which modulates the transmit signal, The output from pin 3 of VCO ZZ01 is applied to TX amplifier pre-driver QT01, in the transmitter circuit, to be amplified.

3.1.6 Unlock Detector Circuit

The PLL circuit is locked or unlocked (operational/not operational) depending on the output of pin 7 of PLL IC QP01.

When there is no phase difference between the reference and programmable frequencies in the phase detector of PLL IC QP01, the PLL is locked and a 0 V level is output from pin 7 of QP01. This voltage is applied to pin 38 of microprocessor QL01. When 0 V is applied pin 38 of microprocessor QL01, to supply the N number to the PLL IC QP01. When there is a phase difference between the reference and programmable frequencies in QP01, the PLL is unlocked and 0 V is output from pin 7 of PLL IC QP01. This is applied to applied to pin 38 of microprocessor QL01 that will keep the N number from being supplied to the PLL IC QP01.

3.2 Receiver

Refer to Figure 3-2.

The receiver is a double-conversion super-heterodyne with a first intermediate frequency (IF) of 21.4 MHz and a second IF of 450 kHz.

The receiver circuit consists of RF amplifier QR03, first mixer QR04, first IF amplifier QF01, second IF AMP circuit QF02, audio control circuits Q102, Q103, Q104, Q108 and audio circuit Q109 to operate in the frequency range of 156.050 to 163.275 MHz.

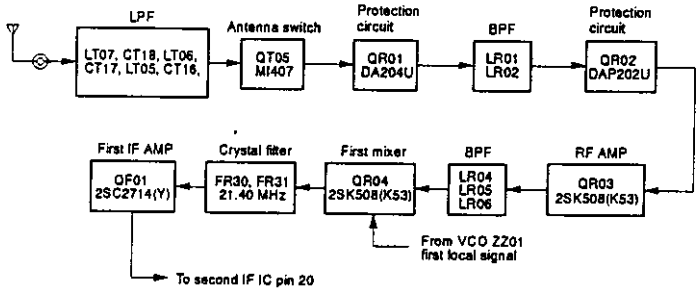


Figure 3-2 Receiver Block diagram

3.2.1 RF Amplifier Circuit

The incoming signal through the antenna socket (JT01) passes through the low pass filter comprised of LT07, CT18, LT06, CT17, LT05, and CT16. It then passes through antenna switch QT05 and the over input protection circuit QR01 and is applied to the band-pass filter. The receiving frequency is passed through the band-pass filter comprised of LR01 and LR02 and is applied to RF amplifier QR03. The incoming receive frequency is amplified by QR03 and applied to another narrow band-pass filter comprised of LR04, LR05, and LR06 to eliminate unwanted signals. The receiving frequency is then applied to the gate of first mixer QR04. The front-end test point (TP01) may be used to balance the band-pass filters, or used to check if the RF Amplifier and associated circuitry are operational.

3.2.2 First Mixer Circuit

The first local signal is applied to the source of first mixer QR04, The receive frequency and the first local signal are mixed in QR04 and produce four frequencies (the sum, the difference, receive, and LO). The first LO is comprised of the RX frequency minus 21.4 MHz. These signals are applied to the crystal filter comprised of FR30 and FR31. A 21.4 MHz signal is filtered from the adjacent signals. The first IF signal of 21.4 MHz is then applied to first IF amplifier QF01.

3.2.3 First IF Amplifier

The 21.4 MHz first IF signal is amplified by QF01 and then applied pin 20 of second IF IC QF02.

The local test point (TP02) may be used to balance the LO band-pass filters, or used to check if the VCO (first LO) and associated circuitry are operational.

3.2.4 Second IF Circuit

Refer to Figure 3-3.

The first IF signal through pin 20 of second IF IC QF02 is applied to the second mixer in QF02. In the second mixer, the first IF (21.4 MHz) and second local (21.850 MHz from XP01) signals are mixed to produce a 450 kHz second IF signal. The signal passes through pin 4 of QF02 and applied to ceramic filter FF01 to eliminate adjacent signals. It is then applied to pin 6 of QF02 where it is amplified by a second IF amplifier and fed to a quadrature detector where it is converted to an audio signal and output from pin 11.

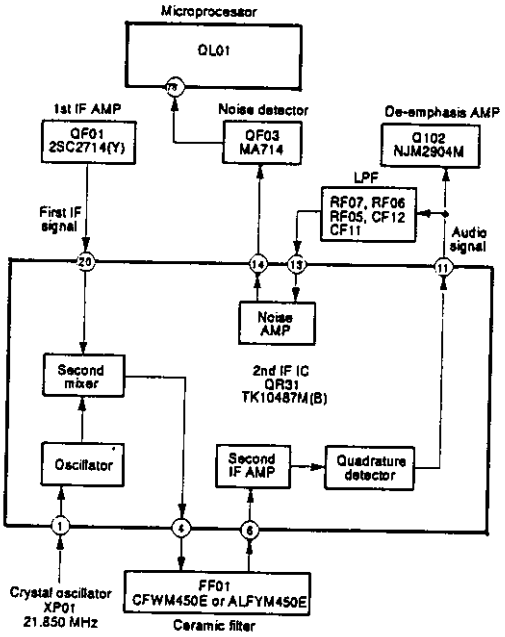


Figure 3-3 Second IF IC Block diagram

3.2.5 Audio Circuit

A portion of the audio signal output from second IF IC QF02 is applied to pin 2 and pin 6 of the dual de-emphasis amplifier Q102 where the frequency of the audio signal is compensated and then applied to pin 1 and pin 3 of the multiplexer Q103. This multiplexer control AF signal flow in normal mode and in intercom mode.

- Normal mode -

The AF signals that are applied to Q103 are output from pin 4 and pin 15 of Q103, which are applied to pin 4 and pin 15, respectively, of the electrical potentiometer Q108. After the output level has been adjusted by the electrical potentiometer Q108, the AF signals are output from pin 6 and pin 16 of Q108, applied to pin 5 and pin 2 of the dual AF power amplifier, and then output from pin 7 and pin 10.

The AF signal that is output from pin 7 of the dual AF power amplifier is output to pin 4 of the second microphone connector JJ05 via pin 11 of J103 and external speaker jack JA02 via pin 1 of J105. In addition, the AF signal that is output from pin 10 of the dual AF power amplifier is output to the front speaker EG01 and pin 3 of the first microphone connector via pin 1 and 2 of J102.

- Intercom mode -

The AF signals that are applied to pin 1 and pin 3 of Q103 are interrupted here. In intercom mode, this multiplexer Q103 controls the AF signals for the first and second MICs. The AF signals that is output from pin 7 of the low pass filter amplifier Q107 (2/2) is applied to pin 14 of the multiplexer Q103. This signal is applied to pin 1 of the first/second MIC switch Q104. If this signal is the signal from the first MIC, it is output from pin 7 of Q104 and is then applied to the dual AF power amplifier Q108 via pin 5 and pin 4 of Q103. If this signal is the signal from the second MIC, it is output from pin 6 of Q104 and is then applied to the dual AF power amplifier Q108 via pin 2 and pin 15 of Q103.

3.2.6 Noise Squelch Circuit

A portion of the audio signal from pin 11 of QF02 is applied to the low pass filter comprised of RF07, RF06, RF05, CF11, and CF12. The audio signal is then applied to pin 13 of QF03. The noise component of the signal is output from pin 14 of QF02. It is converted into DC voltage in noise detector QR32 to produce a squelch signal; the voltage of the squelch signal passes through pin 23 of J102 and applied to pin 78 of QL01. This voltage is compare with the squelch volume voltage (This voltage is applied from the squelch volume RL50 to pin 79 of QL01.).

When the squelch signal voltage is higher than the voltage from the squelch volume, the "Hi" level is output from pin 28 of QL01, and then is applied to the AF mute switch Q111, then squelch is in operation (no sound is emitted from the transceiver).

When the squelch signal voltage is lower than the voltage from the squelch volume, the "Low" level is output from pin 28 of QL01, and then is applied to the AF mute switch Q111, then squelch is off (noise is emitted from the transceiver). Similarly, when squelch is in operation, the "Hi" level is output from pin 30 of QL01, and then is applied to the 1st AMP mute switch Q110 (1/2). When squelch is in operation, the "Low" level is output from pin 31 of QL01, and then is applied to the 2nd AMP mute switch Q110 (2/2).

3.2.7 WX Alert

Refer to Figure 3-4.

The weather alert tone signal is applied to pin 2 of band pass filter amplifier Q301 (1/2) and unwanted signals are eliminated by this circuit. Then the weather alert tone signal is applied to pin 6 of comparator circuit Q301 (2/2). The weather alert tone signal is passed through the comparator circuit Q301 (2/2) to create a square wave, and is supplied to pin 97 of microprocessor QL01. The weather alert tone signal is analyzed by QL01 to determine the type of weather alert signal. When the proper frequency (1050 Hz) is detected by the microprocessor QL01, a high voltage is output from pin 28 (AFMUTE). This voltage is sent to the AF Mute circuits Q111 and Q101 which are turned on allowing the transceiver to be unsquelched interrupting the scan function. The WX Alert Beep Tone is output from pin 2 of microprocessor QL01 (BEEP) and sent to pin 4 and pin 15 of AF electrical volume IC Q108. Then this Beep is sent to pin 2 and pin 5 of dual AF amplifier which outputs the WX Alert Beep Tone to external speaker jack JA02, to 2nd microphone jack JJ05 and to the internal speaker EG01.

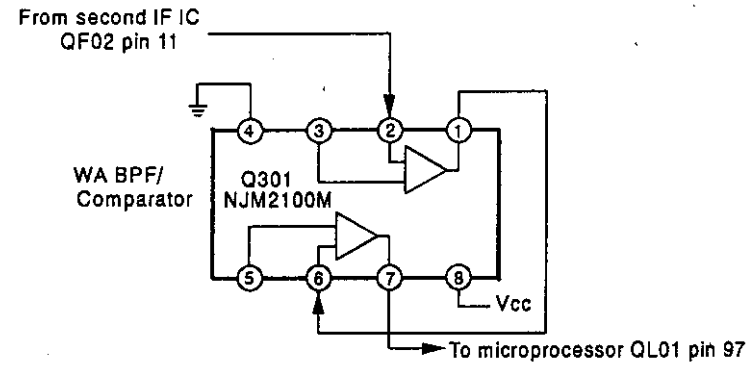


Figure 3-4 Weather alert BPF / comparator Block diagram

3.3 Transmitter

3.3.1 Microphone Amplifier

Refer to Figure 3-5.

When the push-to-talk (PTT) switch of the microphone is pressed, pin 4 of JL01 (microphone connector) is pulled Hi (5 V). This is applied to pin 53 of microprocessor QL01. When this happens, pin 21 of microprocessor QL01 (T/R B cont.) outputs a Hi to the TX+B switch Q210 which turns it on and supplies to TX+B switch Q208 and supplies to the transmit circuits. Microphone audio is input from pin 1 of JL01 (microphone connector) and applied to the pre-emphasis amplifier Q311. This signal passes through Q305 then applied to pin 2 of limiting amplifier Q107 (1/2) for amplitude limiting. The limited signal is applied to pin 6 of low pass filter Amplifier Q107 (2/2).

Q107 (2/2) contains a low pass filter circuit that attenuates audio signals higher than 3 kHz by 18 dB/Oct. The signal level is passed pins 14 and 13 of multiplexer Q103 and is adjusted by Deviation Adjustment R119. And this is applied to pin 5 of VCO ZZ01 to modulate the VCO.

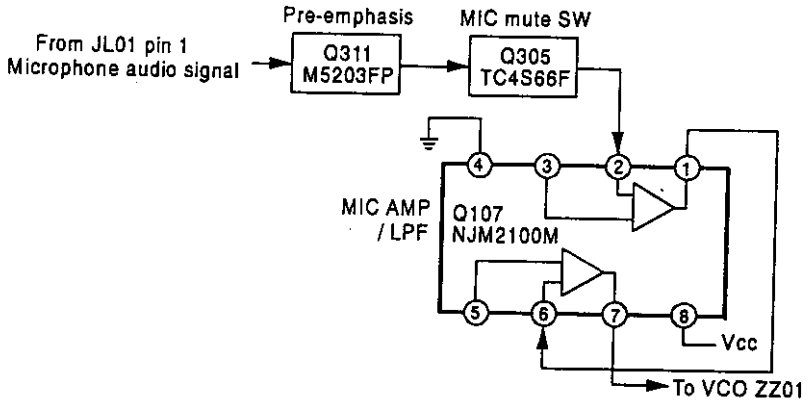


Figure 3-5 MIC amp / LPF Block diagram

3.3.2 TX Amplifiers

Refer to Figure 3-6.

The TX amplifier circuit consists of QT01 (pre-driver) and QT02 (driver). This circuit is used to amplify a transmitting RF signal of 1 mW from the VCO to 200 mW. The amplified signal is applied to pin 1 of final power amplifier QT04.

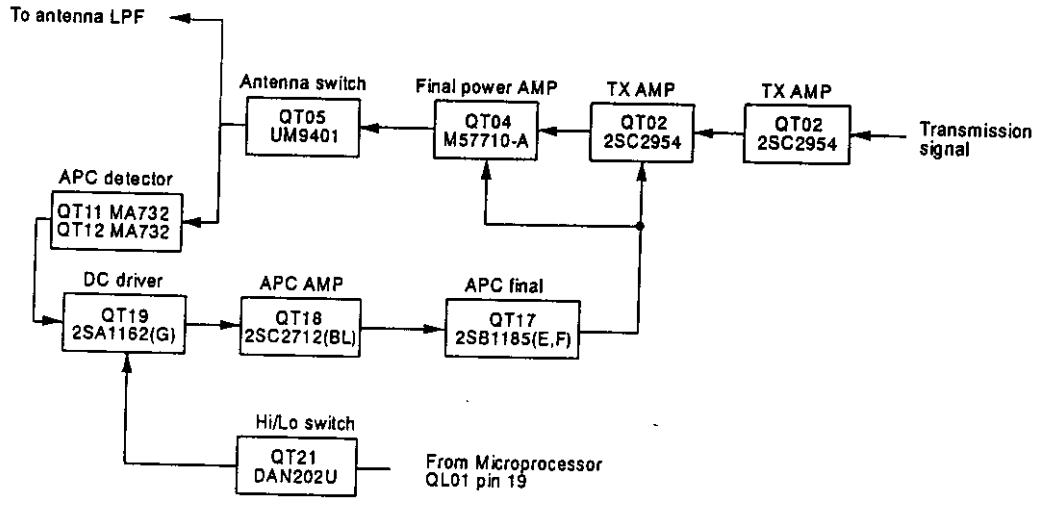


Figure 3-6 Transmission circuit Block diagram

3.3.3 Final Power Amplifier

When the 200 mW signal from the TX amplifier circuit is applied to pin 1 of Final Power Amplifier QT04, it is amplified and output from pin 4. The transmitting signal output passes through a low pass filter comprised of LT05, LT06 and LT07 to eliminate harmonics and spurious signals. The signal then passes through antenna socket JT01 and output through the antenna.

3.3.4 High/Low Power

The RF power can be set to either 1 watt or 25 watts by the H/L key on the front panel of the transceiver. If 1 watt is selected, pin 19 of microprocessor QL01 pulls the emitter of QT19 low and 0.6 V is applied to the automatic power control (APC) circuit. If 25 watts is selected, pin 19 of QL01 outputs 5 V, which is applied to the APC circuit.

3.3.5 Automatic Power Control (APC) circuit

A portion of the transmit signal output from pin 4 of final amplifier QT04, is applied to APC detectors QT11 and QT12 which converts it to a DC voltage.

The detected DC voltage passes through QT13 and RT32 (high power adjust), and is applied to the APC circuit comprised of QT17, QT18, and QT19. When voltage is supplied to DC driver QT19, the APC AMP QT18 and APC final QT17 (series-pass transistor) are turned on and supply a level of voltage to QT02, and to pin 2 of final amplifier QT04. The levels of voltage supplied to QT19 are determined by the H/L key and pin 19 of microprocessor QL01 and can be adjusted by RT32 (high power adjust) and RT34 (low power adjust).

3.4 Control

3.4.1 Microprocessor QL01

The functions of the In/Out ports of microprocessor QL01 are listed below.

No.	Port name	S.I/O	S.PD	Signal name	I/O	Active	Initial	P.UD	Function
1	Vcc	sys	—	Vcc	–	—	—	—	+5 V
2	CS7/TMO0/TP8/PB0	TMO0	—	BEEP	O	—	—	—	Beep signal output
3	CS6/TMIO1/TP9/PB1	TMIO1	—	FOG BEEP	O	—	—	—	FOG Beep signal output
4	CS5/TMO2/TP10/PB2	PB2	CMOS	NC	I	—	—	—	Not used (open)
5	CS4/TMIO3/TP11/PB3	PB3	CMOS	NC	I	—	—	—	Not used (open)
6	TP12/PB4	PB4	CMOS	LCD SOD	O	—	—	—	LCD driver control data output terminal
7	TP11/PB5	PB5	CMOS	LCD SID	I	—	—	—	LCD driver control data input terminal
8	TP10/PB6	PB6	CMOS	LCD SCLK	O	—	—	—	LCD driver control clock output terminal
9	TP9/PB7	PB7	CMOS	LCD CS	O	Low	High	E-UP	LCD driver chip select output terminal
10	RESO/FEW	R/F	—	RESO/FEW	O/I	High	Low	E-DN	Mask: RESO, Flash: FEW
11	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
12	TXD0/P90	TXD0	—	NMEA OUT	O	—	—	—	NMEA data output terminal
13	TXD1/P91	TXD1	—	TXD	O	—	—	E-UP	UART data output terminal
14	RXD0/P91	RXD0	—	NMEA IN	I	—	—	—	NMEA data input terminal
15	RXD1/P93	RXD1	—	RXD	I	—	—	E-UP	UART data input terminal
16	IRQ4/SCK0/P94	P94	CMOS	NC	I	—	—	—	Not used (open)
17	IRQ5/SCK1/P95	P95	CMOS	NC	I	—	—	—	Not used (open)
18	D0/P40	P40	CMOS	NC	I	—	—	—	Not used (open)
19	D1/P41	P41	CMOS	HL CONT	O	High	High	—	Transmit power switch output terminal
20	D2/P42	P42	CMOS	PWR CONT	O	High	High	E-UP	System power on/off switch output terminal
21	D3/P43	P43	CMOS	TR CONT	O	High	Low	E-DN	TX/RX switch output terminal
22	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
23	D4/P44	P44	CMOS	TX PWR B CNT	O	High	Low	E-DN	TX+B control terminal
24	D5/P45	P45	CMOS	RF DET	I	Low	High	—	RF level detect terminal
25	D6/P46	P46	CMOS	NC	I	—	—	—	Not used (open)
26	D7/P47	P47	CMOS	NC	I	—	—	—	Not used (open)
27	D8/P30	P30	CMOS	1st/2nd MIC SW	O	Low	Low	—	Attached mic/CMP23 switch output terminal
28	D9/P31	P31	CMOS	AF MUTE	O	Low	High	—	AF mute switch output terminal
29	D10/P32	P32	CMOS	IC/NORM SW	O	Low	High	—	Intercom/normal microphone operation switch
30	D11/P33	P33	CMOS	1st AMP MUTE	O	High	High	—	Attached mic. AF amp mute output terminal
31	D12/P34	P34	CMOS	2nd AMP MUTE	O	High	High	—	CMP23 microphone amp mute output terminal
32	D13/P35	P35	CMOS	MIC MUTE	O	High	Low	—	Microphone mute switch output terminal
33	D14/P36	P36	CMOS	NC	I	—	—	—	Not used (open)
34	D15/P37	P37	CMOS	NC	I	—	—	—	Not used (open)
35	Vcc	sys	—	Vcc	–	—	—	—	+5 V
36	P10/A0	P10	CMOS	CLK	O	—	—	—	PLL IC, E-Vol. control clock output terminal
37	P11/A1	P11	CMOS	DATA	O	—	—	—	PLL IC, E-Vol. control data output terminal
38	P12/A2	P12	CMOS	UNLOCK	I	Low	High	—	PLL unlock detect terminal
39	P13/A3	P13	CMOS	PLL STB	O	—	—	—	PLL strobe output terminal
40	P14/A4	P14	CMOS	EVOL STB	O	—	—	—	Electronic volume strobe terminal
41	P15/A5	P15	CMOS	VS STB	O	—	—	—	Voice scrambler strobe terminal
42	P16/A6	P16	CMOS	VS THRU	I/O	L/H	H/L	E-DN	Voice scrambler on/off switch terminal
43	P17/A7	P17	CMOS	TEST SW	I	Low	High	E-UP	Test mode start
44	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
45	P20/A8	P20	CMOS	SCL	O	—	—	—	EEPROM clock output terminal
46	P21/A9	P21	CMOS	SDA	I/O	—	—	—	EEPROM data input/output terminal
47	P22/A10	P22	CMOS	DIM1	O	High	High	E-DN	Dimmer switch terminal 1
48	P23/A11	P23	CMOS	DIM2	O	High	High	E-DN	Dimmer switch terminal 2
49	P24/A12	P24	CMOS	EXP SW	I	Low	High	E-UP	Expansion setting mode start

No.	Port name	S.I/O	S.PD	Signal name	I/O	Active	Initial	P.UD	Function
50	P25/A13	P25	CMOS	MMSID SW	I	Low	High	E-UP	MMSID setting mode start
51	P26/A14	P26	CMOS	INTL SW	I	Low	High	E-UP	Initial International channelization start
52	P27/A15	P27	CMOS	16/9	I	Low	High	E-UP	16/9 Key input terminal
53	P50/A16	P50	CMOS	1st PTT	I	Low	High	E-UP	Attached microphone PTT input terminal
54	P51/A17	P51	CMOS	2nd PTT	I	Low	High	E-UP	CMP23 PTT input terminal
55	P52/A18	P52	CMOS	UP	I	Low	High	E-UP	Attached microphone UP KEY input terminal
56	P53/A19	P53	CMOS	DOWN	I	Low	High	E-UP	Attached microphone DOWN KEY input terminal
57	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
58	P60/WAIT	P60	CMOS	PA CONT	O	High	Low	E-DN	PA output control terminal
59	P61/BREQ	P61	CMOS	LB CONT	O	High	Low	E-DN	Listen back output control terminal
60	P62/BACK	P62	CMOS	FOG CONT	O	Low	High	—	Fog output control terminal
61	P67/ϕ	P67	CMOS	NC	I	—	—	—	Not used (open)
62	STBY	STBY	—	STBY	I	—	—	—	+5 V
63	RES	sys	—	RESET	I	Low	High	E-UP	System reset input
64	NMI	NMI	—	NMI	I	—	—	—	+5 V
65	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
66	EXTAL	EXTAL	—	EXTAL	I	—	—	—	Connected to main system clock crystal
67	XTAL	XTAL	—	XTAL	I	—	—	—	Connected to main system clock crystal
68	Vcc	sys	—	Vcc	–	—	—	—	+5 V
69	P63/AS	P63	CMOS	BUS-CLK	O	—	—	E-UP	Communication clock input/output
70	P64/RD	P64	CMOS	BUS-DATA	I/O	—	—	E-UP	Communication data input/output
71	P65/HWR	P65	CMOS	NC	I	—	—	—	Not used (open)
72	P66/LWR	P66	CMOS	NC	I	—	—	—	Not used (open)
73	MD0	MD0	—	MD0	I	—	High	E-UP	Mode 7, Used to single chip advantest mode
74	MD1	MD1	—	MD1	I	—	High	E-UP	Mode 7, Used to single chip advantest mode
75	MD2	MD2	—	MD2	I	—	High	E-UP	Mode 7, Used to single chip advantest mode
76	AVcc	sys	—	AVcc	–	—	—	—	+5 V
77	VREF	sys	—	VREF	–	—	—	—	+5 V
78	AN0/P70	AN0	—	SQL	I	—	—	—	Squelch level input terminal
79	AN1/P71	AN1	—	SQL VOL	I	—	—	—	Squelch volume level input terminal
80	AN2/P72	AN2	—	AF VOL	I	—	—	—	Volume level input terminal
81	AN3/P73	AN3	—	BATT CHK	I	—	—	E-UP	Battery voltage detect terminal
82	AN4/P74	AN4	—	KEY1	I	—	—	E-UP	Front key data potential input terminal
83	AN5/P75	AN5	—	KEY2	I	—	—	E-UP	Front key data potential input terminal
84	DA0/AN6/P76	AN6	—	KEY3	I	—	—	E-UP	Front key data potential input terminal
85	DA1/AN7/P77	AN7	—	LCD CONTRAST	O	—	—	—	LCD contrast adjustment output terminal
86	AVss	sys	—	AVss	–	—	—	—	Ground voltage for A/D converter
87	IRQ0/P80	IRQ0	—	BUS-DATA	I	—	—	E-UP	Key command interruption input
88	CS3/IRQ1/P81	IRQ1	—	PWR SW	I	Low	High	E-UP	WAKE UP interruption input
89	CS2/IRQ2/P82	IRQ2	—	ROTARY UP	I	Low	High	E-UP	Rotary switch interruption input (UP)
90	ADTRG/CS1/IRQ3/P83	IRQ3	—	ROTARY DN	I	Low	High	E-UP	Rotary switch interruption input (DOWN)
91	CS0/P84	P84	CMOS	NC	I	—	—	—	Not used (open)
92	Vss	sys	—	Vss	–	—	—	GND	Ground voltage
93	TCLKA/TP0/PA0	PA0	CMOS	DSC-ENC	O	—	—	—	DSC data output terminal
94	TCLKB/TP1/PA1	PA1	CMOS	NC	I	—	—	—	Not used (open)
95	TCLKC/TIOCA0/TP2/PA2	TIOCA0	—	DSC-DEC	I	—	—	—	DSC data input terminal
96	TCLKD/TIOCB0/TP3/PA3	PA3	CMOS	NC	I	—	—	—	Not used (open)
97	A23/TIOCA1/TP4/PA4	TIOCA1	—	WA DET	I	—	—	—	WA tone detection signal input
98	A22/TIOCB1/TP5/PA5	PA5	CMOS	NC	I	—	—	—	Not used (open)
99	A21/TIOCA2/TP6/PA6	PA6	CMOS	NC	I	—	—	—	Not used (open)
100	A20/TIOCB2/TP7/PA7	PA7	CMOS	NC	I	—	—	—	Not used (open)

3.4.2 LCD

LCD driver QL03 is controlled by microprocessor QL01. Data controlling the LCD consist of four signals: output data (SOD), input data (SID), clock (SCLK), and chip select (CS). This signal is output from pins 6, 7, and 8 of microprocessor QL01 and applied to pins 50, 48, and 49 of LCD driver QL03.

The LCD contrast feature includes microprocessor QL01. Microprocessor QL01 pin 85 is a pulse-width-modulated signal sent to pin 58 of LCD driver QL03.

3.4.3 DSC (Digital Selective Calling) Logic

- DSC Encoder -

DSC data signal is produced by microprocessor QL01. The type of signal output is determined by serial data output from pin 93 of microprocessor QL01. The DSC data signal is applied to pin 1 of low pass filter Q303, and is passes through low pass filter Q303 to eliminate higher harmonics signals. The DSC data signal is adjusted by DSC deviation Adjustment R327, and is applied to pin 2 of limiting amplifier Q107 (1/2) for amplitude limiting.

- DSC Decoder -

The reception signal is supplied to pin 3 of DSC band pass filter Q302 and unwanted signals are eliminated by this circuit. The reception signal is then applied to pin 2 of FSK decoder Q304. The FSK decoder Q304 consists of tracking phase-locked loop, quadrature detector, and FSK comparator. The FSK decoder Q304 converts the RX data into a logic level, which is then transferred to pin 95 of microprocessor QL01.