Fibocom
PERFECT WIRELESS EXPERIENCE

FG160-NA

Hardware Guide

V1.1

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Contents

Applicable Model

No.	Applicable Model	Description
1	FG160-NA-00	North America version of the 5G communication module which for varieties of eMBB scenarios

Change History

V1.1 (2022-08-11)	Chapter 2.2.2, delete support PCIe 4.0 information. Chapter 2.2, add LTE B7, NR N7/N78 and description, updated NSA DL peak rate. Chapter 2.4, add B7/N7/N78 antenna configuration Chapter 4.4, add B7/N7/N78 transmitting power and receiver sensitivity, update 3GPP requirement and note. Chapter 3.2, updated the pin definition of “mmW” part in Table 7 Chapter 5.1.1 updated the Power supply voltage drop diagram in Figure 4 Chapter 5.2.2, add control sequence about FG160 is configured as PCIe EP mode Chapter 5.8, add “PCIe boot control interface” chapter Chapter 8.2, updated dimension of structure in Figure 21
V1.0 (2022-02-14)	Initial version

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of FG160-NA-00 (hereinafter referred to as FG160). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of FG160 modules and develop products.

1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 38.300 V16.7.0: 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone
- 3GPP TS 38.521-3 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V11.13.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface

- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express Base Specification Revision 3.0
- Universal Serial Bus 3.1 Specification

1.3 Related Document

FIBOCOM Design Guide_RF Antenna

2 Overview

2.1 Introduction

The FG160 series module is a 5G module which supports NSA and SA network architectures. The FG160 integrates core devices such as Baseband, Memory, PMU, Transceiver, and PA. It supports 5G NR Sub6, FDD-LTE and TDD-LTE long-distance communication modes. Supports uplink 2×2 MIMO and downlink 4×4 MIMO multi-antenna configuration in SA mode. It also supports GNSS wireless positioning technology. The FG160 is designed in an LGA package and is suitable for a variety of eMBB scenarios, such as CPE, VR/AR, gateway, TV box, and intelligent monitoring.

2.2 Specification

2.2.1 RF Characteristic

Table 1. Operating bands

Model	FG160-NA
FDD-LTE	Band 2/4/5/7/12/13/29/30/66/71
TDD-LTE	Band 41/48/46（LAA）
SA	n2/5/7/12/14/25/30/41/48/66/70/71/77/78
NSA	n2/5/7/12/25/30/41/66/71/77/78
GNSS	GPS/GLONASS/Galileo/BDS/QZSS

Table 2. Data throughput

Model	FG160-NA
LTE	DL peak rate 1.6Gbps (CAT19) UL peak rate 211Mbps (CAT18)

	DL 4×4 MIMO (Support Band B2/4/5/7/12/13/30/41/48/66/71)
NSA	DL peak rate 3.66Gbps UL peak rate 555Mbps DL 4×4 MIMO LTE (Support Band B2/4/5/7/12/13/30/41/48/66) DL 4×4 MIMO NR (Support Band n2/5/7/25/30/41/66/71/77/78)
SA	DL peak rate 2.47Gbps UL peak rate 900Mbps DL 4×4 MIMO (Support Band n2/5/7/12/14/25/30/41/48/66/70/71/77/78) UL 2×2 MIMO (n41/77/78)

Table 3. Modulation characteristic

Model	FG160-NA
LTE	Support max DL 5CA Support max UL 2CA Support 3GPP R16 Support DL 256-QAM, UL 256-QAM Support RF bandwidth 1.4MHz–20MHz
NSA	Support max DL LTE 4CA + NR 1CA Support max DL LTE 4CA + NR 2CA (reserved) Support max UL LTE 1CA + NR 1CA LTE Modulation: DL-256QAM, UL-256QAM NR Modulation: DL-256QAM, UL-256QAM
SA	Support max DL 2CA

	Support max UL 2CA Support DL 256QAM, UL 256QAM Support RF bandwidth 5MHz–100MHz Support carrier spacing 15KHz (FDD) and 30KHz (TDD)
SRS antenna switching	SA: 2T4R NSA: 1T4R 1T2R

2.2.2 Key Features

Table 4. Key features

Performance	Description
Power Supply	DC: 3.3-4.4V, typical voltage: 3.8V
Temperature	Normal operating temperature: –30 to 75℃[1] Extended operating temperature: –40 to 85℃[2] Storage temperature: –40 to 85℃
Physical Characteristics	Dimension: 41 × 44 × 2.75 mm Package: 392 pin LGA Weight: about 12g
CPU	Qualcomm SDX62, 7nm process, ARM Cortex-A7, up to 1.5 GHz
Memory	8Gb LPDDR4x + 8Gb NAND Flash
Interface	
USB Interface	USB2.0 high speed (HS) interface, data transmission rate up to 480Mbps USB3.1 Gen2 Super-speed (SS) interface, data transmission rate up to

	10Gbps
PCIe Interface	PCIe Gen3, x2 lanes
SIM Interface	Dual SIM: 1.8V/3V SIM1: USIM SIM2: USIM/eSIM
I2Cs	I2C interface x2
ADCs	Two A/D conversion channel
Software	
Firmware update	USB
Operating System	Linux

1. When temperature keeps in the range of –30 to 75°C, module can work normally. Module performance meets the 3GPP specifications.
2. When temperature keeps in the range of –40 to 85°C, module performance may be slightly out of 3GPP specifications.

2.3 Application Framework

The application framework below shows the main hardware functions of the FG160 module:

- Baseband
- RF transceiver
- PMU

- Memory
- Peripheral interface

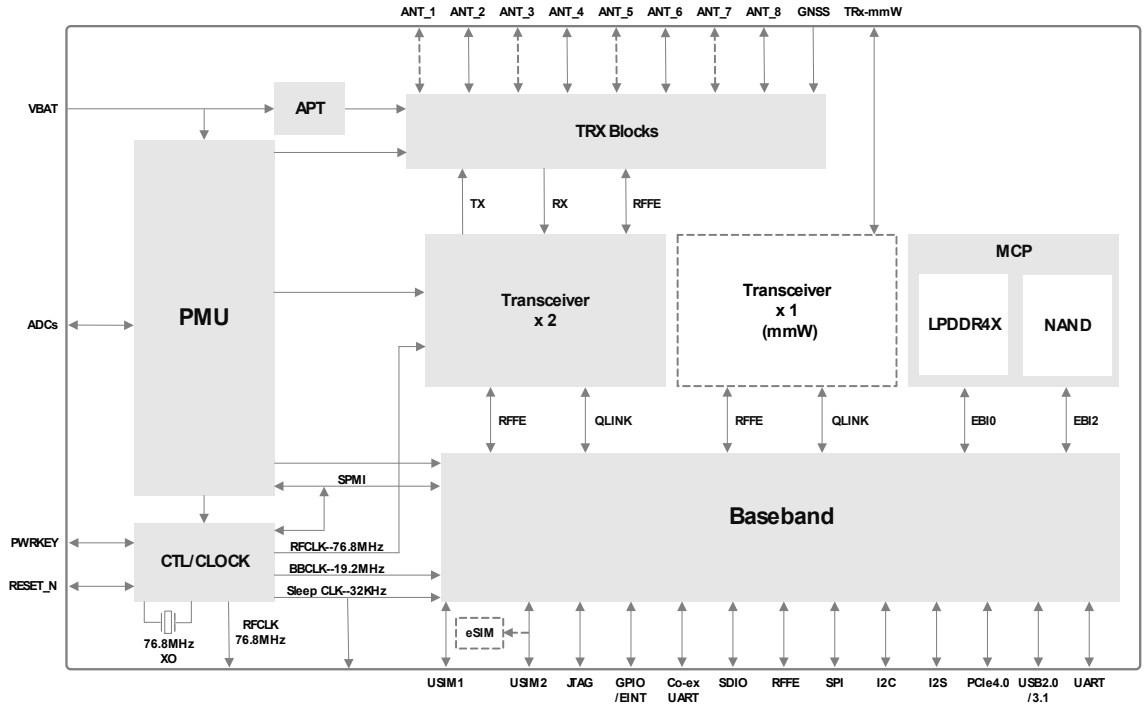

Figure 1. Hardware block diagram

2.4 Antenna Configuration

The FG160 supports eight NR/LTE antennas and one GNSS antenna. The antenna interface is defined as shown in the following table.

Table 5. Antenna configuration

Pin Name	Function Description	Band Configuration (TX)	Band Configuration (RX)	Frequency Range (MHz)
ANT_1	Reserved	--	--	--
ANT_2	Secondary TX / MIMO PRX	B5 n5	B5/12/13/71 n5/12/14/71	617-960
	Main TX / PRX	B2/4/7/30/66/41/48	B2/4/7/30/66/41/48	1427-2690

Pin Name	Function Description	Band Configuration (TX)	Band Configuration (RX)	Frequency Range (MHz)
		n2/7/25/30/41/48/66/70/77/78	n2/7/25/30/41/48/66/70/77/78	3300-4200 5150-5925
ANT_3	Reserved	--	--	--
ANT_4	MIMO DRX	--	B5/12/13/71 n5/12/14/71	617-960
	DRX	--	B2/4/7/30/66/41 n2/7/25/30/41/66/70	1427-2690
	MIMO PRX	--	B48 n48/77/78	3300-4200
	PRX	--	B46	5150-5925
ANT_5	Reserved	--	--	--
ANT_6	DRX	--	B5/12/13/29/46/71 n5/12/14/71	617-960 5150-5925
	MIMO DRX	--	B2/4/7/30/66/41/48 n2/7/25/30/41/48/66/70/77/78	1427-2690 3300-4200
ANT_7	Reserved	--	--	--
ANT_8	Main TX / PRX	B5/12/13/71 n5/12/14/71	B5/12/13/29/71 n5/12/14/71	617-960
	Secondary TX / MIMO PRX	B2/4/41/66 n2/25/41/66	B2/4/7/30/41/66 n2/7/25/30/41/66/70	1427-2690
	Secondary TX	n48/77/78	B48	3300-4200

Pin Name	Function Description	Band Configuration (TX)	Band Configuration (RX)	Frequency Range (MHz)
	/ DRX		n48/77/78	
ANT_10	GNSS	--	GNSS receive	1559-1607

2.5 Waring

2.5.1 Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the

instructions, require that the host product manufacturer must notify to Fibocom Wireless

Inc. that they wish to change
the antenna trace design. In this case, a Class II permissive change application is required to be filed
by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new
application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOFG160NA”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4)The max allowed antenna gain is 3.76dBi for external monopole antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer

considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.5.2 FCC Statement

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the

OEM integrator is still responsible for testing their end-product for any additional compliance

requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

3 Pin Definition

The FG160 module applies LGA interface with 392 pins.

3.1 Pin Assignment

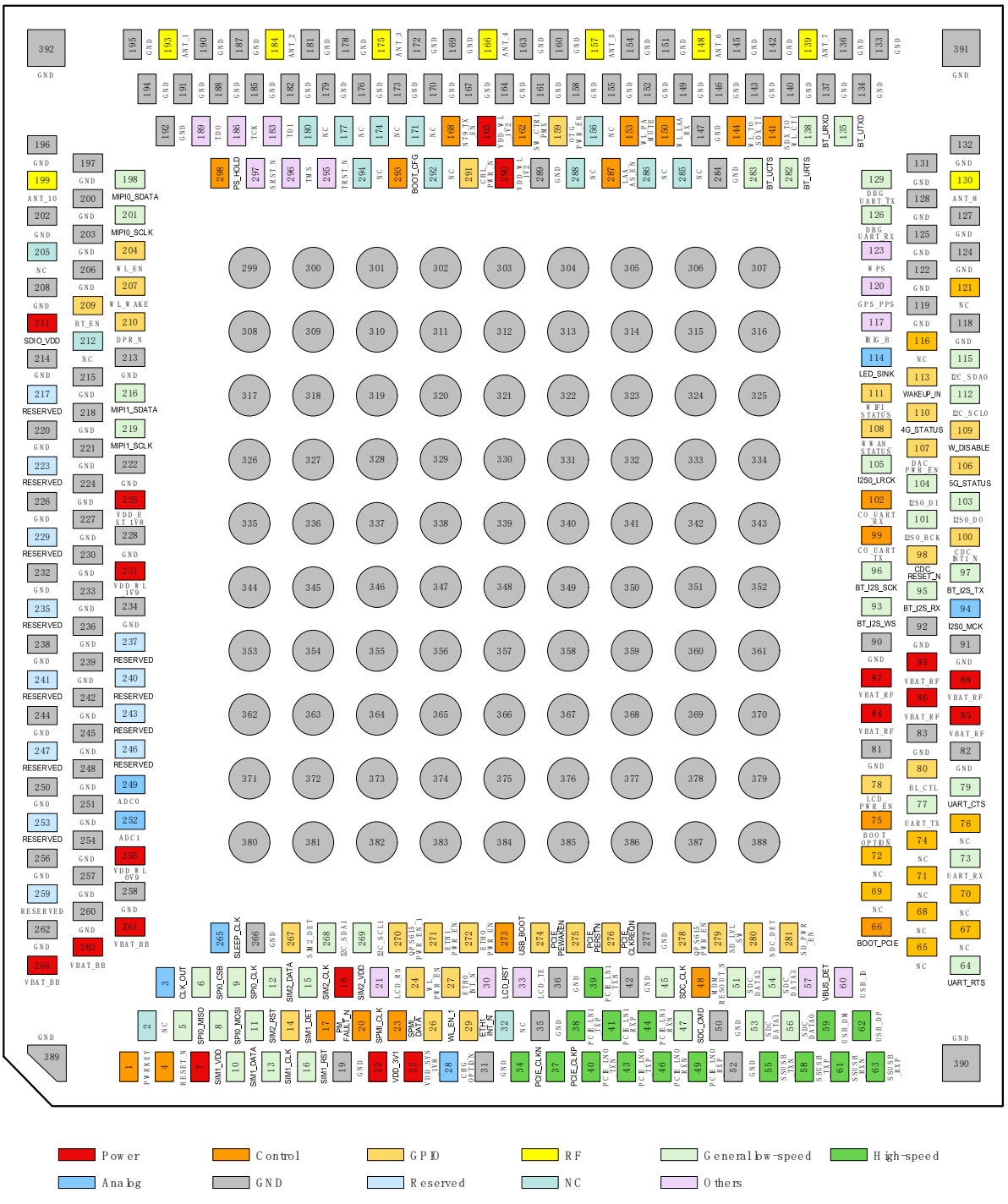

Figure 2. Pin assignment

The pin "RESERVED" means that the position pin is reserved and does not need to be connected.

3.2 Pin Definition

Table 6. IO Parameter definition

Type	Description
PI	Power Input
PO	Power Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
OD	Open Drain
PU	Internal pull up
PD	Internal pull down
Hi-Z	High impedance

Table 7. LGA pin description

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
Power					
VBAT_BB	261, 263, 264	PI	--	--	Baseband power input
VBAT_RF	84, 85, 86, 87, 88, 89	PI	--	--	RF power input
VDD_EXT_1V8	225	PO	--	--	1.8V power output
VDD_3V1	22	PO	--	--	Power for PM7250B USB PHY
VDD_SYS_1V8	25	PO	--	--	Power for PM7250B IO
VDD_WL_1V2	165, 290	PO	--	--	Power for WCN6856 RFA and PCIe PHY
VDD_WL_1V9	231	PO	--	--	Power for WCN6856 RFA and PCIe PHY
VDD_WL_0V9	255	PO	--	--	Power for WCN6856 CX,MX,RFA,AON,RFCMN,BT
USB					
SSUSB_TXN	55	AO	--	--	USB super speed transmit data minus
SSUSB_TXP	58	AO	--	--	USB super speed transmit data plus

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
SSUSB_RXN	61	AI	--	--	USB super speed receive data minus
SSUSB_RXP	63	AI	--	--	USB super speed receive data plus
USB_DM	59	AIO	--	--	USB high speed data minus
USB_DP	62	AIO	--	--	USB high speed data plus
VBUS_DET	57	DI	--	--	USB VBUS detection
OTG_PWR_EN	159	DO	1.8V	PD	USB OTG power enable, reserved
USB_ID	60	DI	1.8V	PD	USB ID, reserved
USIM					
SIM1_VDD	7	PO	--	--	SIM1 power supply, 3V/1.8V
SIM1_DATA	10	DIO	1.8/3.0V	PD	SIM1 data input/output
SIM1_CLK	13	DO	1.8/3.0V	PD	SIM1 clock signal
SIM1_RST	16	DO	1.8/3.0V	PD	SIM1 reset signal
SIM1_DET	14	DI	1.8V	PD	SIM1 detect signal
SIM2_VDD	18	PO	--	--	SIM2 power supply, 3V/1.8V
SIM2_DATA	12	DIO	1.8/3.0V	PD	SIM2 data input/output
SIM2_CLK	15	DO	1.8/3.0V	PD	SIM2 clock signal
SIM2_RST	11	DO	1.8/3.0V	PD	SIM2 reset signal
SIM2_DET	267	DI	1.8V	PD	SIM2 detect signal
GPIO					

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
W_DISABLE	109	DI	1.8V	PD	Module flight mode control signal, reserved
WAKEUP_IN	113	DI	1.8V	PD	Module wake up input from host, reserved
5G_STATUS	106	DO	1.8V	PD	5G status indicator, reserved
4G_STATUS	110	DO	1.8V	PD	4G status indicator, reserved
WIFI_STATUS	111	DO	1.8V	PD	WIFI status indicator, reserved
WWAN_STATUS	108	DO	1.8V	PD	Module status indicator, reserved
IRIG_B	117	DO	1.8V	PD	B code output, reserved
GPS_PPS	120	DO	1.8V	PD	PPS signal output, reserved
LED_SINK	114	AI	--	Hi-Z	LED negative drive signal, reserved
DPR_N	210	DI	1.8V	PD	DPR mode control signal, reserved
ANT					
ANT_1	193	AIO	--	--	RF antenna interface, ANT_1, reserved
ANT_2	184	AIO	--	--	RF antenna interface, ANT_2
ANT_3	175	AIO	--	--	RF antenna interface, ANT_3, reserved
ANT_4	166	AIO	--	--	RF antenna interface, ANT_4

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
ANT_5	157	AIO	--	--	RF antenna interface, ANT_5, reserved
ANT_6	148	AIO	--	--	RF antenna interface, ANT_6
ANT_7	139	AIO	--	--	RF antenna interface, ANT_7, reserved
ANT_8	130	AIO	--	--	RF antenna interface, ANT_8
NC	121	--	--	--	NC
ANT_10	199	AI	--	--	GNSS antenna
NC	205	--	--	--	NC
ANT Tuner Control					
MIPI0_SDATA	198	DIO	1.8V	PD	External Tuner MIPI Control Data Pin
MIPI0_SCLK	201	DO	1.8V	PD	External Tuner MIPI Control Clock Pin
MIPI1_SDATA	216	DIO	1.8V	PD	External Tuner MIPI Control Data Pin
MIPI1_SCLK	219	DO	1.8V	PD	External Tuner MIPI Control Clock Pin
Module Control					
PWRKEY	1	DI	1.8V	PU	Module power-key control signal
RESET_N	4	DI	1.8V	PU	Module reset control signal
CBL_PWR_N	291	DI	1.8V	PU	Module power on signal

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
WPS	123	DI	1.8V	PD	Interrupt input signal, used for WPS key input signal, reserved
USB_BOOT	273	DI	1.8V	PD	Force into USB download boot mode
RESOUT_N	48	DO	1.8V	PD	Reserved, keep floating
BOOT_CFG	293	DI	1.8V	PD	PCIE boot configure signal
BOOT_PCIE	66	DIO	1.8V	PD	PCIE boot control signal
BOOT_OPTION	75	DIO	1.8V	PD	Reserved, keep floating
PM_FAULT_N	17	DIO	1.8V	PD	PMIC fault signal used for PM7250B
CHG_OPTION	28	AI	--	--	Charger configure option input
SD					
SDC_CMD	47	DIO	1.8/3.0V	PD	SDC interface command signal
SDC_CLK	45	DO	1.8/3.0V	PD	SDC interface clock signal
SDC_DATA0	56	DIO	1.8/3.0V	PD	SDC interface DATA0 signal
SDC_DATA1	53	DIO	1.8/3.0V	PD	SDC interface DATA1 signal
SDC_DATA2	51	DIO	1.8/3.0V	PD	SDC interface DATA2 signal
SDC_DATA3	54	DIO	1.8/3.0V	PD	SDC interface DATA3 signal
SDC_DET	280	DI	1.8V	PD	SD card insert detection

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
SD_PWR_EN	281	DO	1.8V	PD	SD card power supply enable
SDIO_VDD	211	PI	--	--	SDC interface I/O power domain
SD_LVL_SW	279	DO	1.8V	PD	GPIO, used for control SD I/O Power enable signal
PCIE					
PCIE_CLKN	34	AIO	--	--	PCIe reference clock minus
PCIE_CLKP	37	AIO	--	--	PCIe reference clock plus
PCIE_LN0_TXN	40	AO	--	--	PCIe Tx0 minus
PCIE_LN0_TXP	43	AO	--	--	PCIe Tx0 plus
PCIE_LN1_TXN	39	AO	--	--	PCIe Tx1 minus
PCIE_LN1_TXP	38	AO	--	--	PCIe Tx1 plus
PCIE_LN0_RXN	46	AI	--	--	PCIe Rx0 minus
PCIE_LN0_RXP	49	AI	--	--	PCIe Rx0 plus
PCIE_LN1_RXN	44	AI	--	--	PCIe Rx1 minus
PCIE_LN1_RXP	41	AI	--	--	PCIe Rx1 plus
PCIE_PEWAKEN	274	DIO	1.8V	PU	PCIe wake-up signal
PCIE_PERSTN	275	DIO	1.8V	PD	PCIe reset signal
PCIE_CLKREQN	276	DIO	1.8V	PU	PCIe clock request signal
JTAG					
TDI	183	DI	1.8V	PD	JTAG TDI，reserved

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
TCK	186	DI	1.8V	PD	JTAG TCK，reserved
TDO	189	DO	1.8V	PD	JTAG TDO，reserved
TRST_N	295	DI	1.8V	PD	JTAG TRST，reserved
TMS	296	DI	1.8V	PD	JTAG TMS，reserved
SYSRSTB	297	DI	1.8V	PD	System reset，reserved
PS_HOLD	298	DO	1.8V	PD	Power Supply hold on signal
I2C					
I2C_SDA0	115	DIO	1.8V	PU	I2C data
I2C_SCL0	112	DO	1.8V	PU	I2C clock
I2C_SDA1	268	DIO	1.8V	PU	I2C data used for PCIe switch
I2C_SCL1	269	DO	1.8V	PU	I2C clock used for PCIe switch
I2S					
I2S0_DO	103	DO	1.8V	PD	I2S data output signal
I2S0_MCK	94	DO	1.8V	PD	I2S clock output signal
I2S0_DI	104	DI	1.8V	PD	I2S data input signal
I2S0_BCK	101	DO	1.8V	PD	I2S data bit clock signal
I2S0_LRCK	105	DO	1.8V	PD	I2S frame clock signal
ADC					
ADC0	249	AI	--	--	A/D conversion channel 0
ADC1	252	AI	--	--	A/D conversion channel 1

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
Debug UART					
DBG_UART_TX	129	DO	1.8V	PU	Debug UART transmit signal
DBG_UART_RX	126	DI	1.8V	PU	Debug UART receive signal
UART					
UART_CTS	79	DI	1.8V	PD	UART receive ready signal
UART_RTS	64	DO	1.8V	PD	UART transmit request signal
UART_TX	77	DO	1.8V	PD	UART transmit signal
UART_RX	73	DI	1.8V	PD	UART receive signal
SPI					
SPI0_MISO	5	DI	1.8V	PD	SPI interface input signal
SPI0_MOSI	8	DO	1.8V	PD	SPI interface output signal
SPI0_CSB	6	DO	1.8V	PD	SPI interface chip select signal
SPI0_CLK	9	DO	1.8V	PD	SPI interface clock signal
LCD					
LCD_RS	21	DO	1.8V	PD	LCD Command / data select
LCD_PWR_EN	78	DO	1.8V	PD	LCD power enable signal
LCD_TE	33	DI	1.8V	PD	LCD frame synchronization signal
LCD_RST	30	DO	1.8V	PD	LCD reset signal
BL_CTL	80	DO	1.8V	PD	LCD Backlight control signal

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
AUDIO CODEC					
CDC_RESET_N	98	DO	1.8V	PD	External CODEC reset signal, reserved
CDC_INT1_N	100	DI	1.8V	PD	External CODEC interrupt signal, reserved
DAC_PWR_EN	107	DO	1.8V	PD	External CODEC power enable, reserved
CLOCK OUT					
SLEEP_CLK	265	AO	--	--	32KHz clock output
CLK_OUT	3	AO	--	--	76.8MHz clock output
WLAN/BT/LAN					
BT_UTXD	135	DO	1.8V	PD	UART TX signal, reserved for BT
BT_URXD	138	DI	1.8V	PD	UART RX signal, reserved for BT
BT_URTS	282	DO	1.8V	PD	UART RTS signal, reserved for BT
BT_UCTS	283	DI	1.8V	PD	UART CTS signal, reserved for BT
BT_I2S_TX	97	DO	1.8V	PD	I2S data output, reserved for BT
BT_I2S_RX	95	DI	1.8V	PD	I2S data input, reserved for BT

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
BT_I2S_SCK	96	DO	1.8V	PD	I2S clock output, reserved for BT
BT_I2S_WS	93	DO	1.8V	PD	I2S synchronization signal, reserved for BT
BT_EN	209	DO	1.8V	PD	GPIO, used for BT control signals
ETH0_INT_N	27	DI	1.8V	PD	GPIO, reserved
ETH1_INT_N	29	DI	1.8V	PD	GPIO, reserved
WL_EN	204	DO	1.8V	PD	GPIO, reserved
WL_EN_1	26	DO	1.8V	PD	GPIO, reserved
WL_PWR_EN	24	DO	1.8V	PD	GPIO, reserved
QPS615_PWR_EN	278	DO	1.8V	PD	GPIO, reserved
QPS615_PWR_EN_1	270	DO	1.8V	PD	GPIO, reserved
ETH0_PWR_EN	272	DO	1.8V	PD	GPIO, reserved
ETH1_PWR_EN	271	DO	1.8V	PD	GPIO, reserved
SDX_TO_WL_CTI	141	DO	1.8V	PD	Used for WWAN control WLAN, reserved
WL_TO_SDX_TI	144	DI	1.8V	PD	Used for WLAN control WWAN, reserved
WL_LAA_RX	150	DO	1.8V	PD	Used for enable WCN6856 FE High Gain High Isolation for WAN PRX/DRX, reserved

Pin Name	Pin No	I/O	Level	Reset Value	Pin Description
SW_CTRL_PMX	162	DIO	1.8V	PD	WIFI/BT and RF coexistence control signals, reserved
WL_PA_MUTE	153	DO	1.8V	PD	Used for disable WLAN TX prior to switching to WWAN, reserved
LAA_AS_EN	287	DO	1.8V	PD	Used for enable WCN6856 Front End Control, reserved
N79_TX_EN	168	DO	1.8V	PD	N79 transmitter indication signal, reserved
CO_UART_TX	99	DO	1.8V	PD	WIFI/BT and RF coexistence control signals, reserved
CO_UART_RX	102	DI	1.8V	PD	WIFI/BT and RF coexistence control signals, reserved
SPMI					
SPMI_CLK	20	DO	1.8V	PD	SPMI clock signal
SPMI_DATA	23	DIO	1.8V	PD	SPMI data signal PD

mmW					
QTM0	237	--	--	--	Reserved
IFH3	223	--	--	--	Reserved
IFV4	217	--	--	--	Reserved
QTM1	240	--	--	--	Reserved
IFH1	235	--	--	--	Reserved
IFV2	229	--	--	--	Reserved
QTM2	243	--	--	--	Reserved
IFH2	247	--	--	--	Reserved
IFV1	241	--	--	--	Reserved
QTM3	246	--	--	--	Reserved
IFH4	259	--	--	--	Reserved
IFV3	253	--	--	--	Reserved

Pin Name	Pin No
NC	
NC	2, 32, 65, 67, 68, 69, 70, 71, 72, 74, 76, 116, 156, 171, 174, 177, 180, 207, 212, 285, 286, 288, 292, 294
GND	
GND	19, 31, 35, 36, 42, 50, 52, 81, 82, 83, 90, 91, 92, 118, 119, 122, 124, 125, 127, 128, 131, 132, 133, 134, 136, 137, 140, 142, 143, 145, 146, 147, 149, 151, 152, 154, 155, 158, 160, 161, 163, 164, 167, 169, 170, 172, 173, 176, 178, 179, 181, 182, 185, 187, 188, 190, 191, 192, 194, 195, 196, 197, 200, 202, 203, 206, 208, 213, 214, 215, 218, 220, 221, 222, 224, 226, 227, 228, 230, 232, 233, 234, 236, 238, 239, 242, 244, 245, 248, 250, 251, 254, 256, 257, 258, 260, 262, 266, 277, 284, 289, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392

The PWRKEY, CBL_PWR_N and RESET_N pins have internal pull-up. The pull-up power supply is in exclusive mode, external pull-up is not required.

4 Electrical Characteristics

4.1 Recommended Operating Conditions

Table 8. Recommended operating voltage

Pin Name	Type	Min (V)	Typ (V)	Max (V)	Current Limit Max (mA)
VBAT_BB, VBAT_RF	PI	3.3[1]	3.8	4.4[1]	4000
VDD_EXT_1V8	PO	1.7	1.8	1.9	50
VDD_3V1	PO	--	3.088	--	25
VDD_SYS_1V8	PO	1.7	1.8	1.9	25
VDD_WL_1V2	PO	1.23	1.28	1.3	TBD
VDD_WL_1V9	PO	1.83	1.88	2	TBD
VDD_WL_0V9	PO	0.62	0.85	0.98	TBD
SIM1_VDD/ SIM2_VDD	PO	1.7	1.8	1.9	200
		2.75	2.95	3.0	200
SDIO_VDD	PI	1.7	1.8	1.9	200
		2.75	2.85	3.0	200
PWRKEY	DI	0	--	1.85	--
RESET_N	DI	0	--	1.85	--
CBL_PWR_N	DI	0	--	1.85	--
VBUS_DET[2]	DI	0	--	5.5	--
ADC0	AI	0	--	1.875	--
ADC1	AI	0	--	VBAT_BB	--

1. Directly measured at Module. Voltage must stay within the min/max values, including voltage drop, ripple and spikes.
2. When VBUS_DET input voltage ⩾1.3V, USB detection trigger.

4.2 I/O Logic Characteristics

Table 9. I/O port logic characteristics

Parameters	Min	Typical	Max	Unit
1.8V logic level				
V_{IH}	1.3	1.8	1.89	V
V_{IL}	-0.3	0	0.6	V
V_{OH}@2mA	1.35	--	1.8	V
V_{OL}	0	--	0.45	V
3.0V logic level				
V_{IH}	2.3	3	3.1	V
V_{IL}	-0.3	0	0.7	V
V_{OH}	2.6	--	3.0	V
V_{OL}	0	--	0.45	V

4.3 Power Consumption

Table 10. Power consumption

State	Mode	Condition	Typical Current/mA
I_{OFF}	Power off	Power supply, module power-off	0.18

State	Mode	Condition	Typical Current/mA
I_{IDLE} (USB Disconnection.)	TDD LTE	DPC (Default Paging Cycle) =#128	TBD
	FDD LTE	DPC (Default Paging Cycle) =#128	TBD
	SA	Long DRX (ms10)	TBD
	Radio Off	AT+CFUN=4 Flight Mode	TBD
I_{SLEEP} (USB Disconnection.)	LTE FDD	DPC (Default Paging Cycle) =#128	TBD
	LTE TDD	DPC (Default Paging Cycle)=#128	TBD
	SA	Long DRX (ms10)	TBD
	Radio Off	AT+CFUN=4, Flight mode.	TBD
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data call Band 2 @+23dBm	TBD
		LTE FDD Data call Band 4 @+23dBm	TBD
		LTE FDD Data call Band 5 @+23dBm	TBD
		LTE FDD Data call Band 12 @+23dBm	TBD
		LTE FDD Data call Band 13 @+23dBm	TBD
		LTE FDD Data call Band 30 @+22dBm	TBD
		LTE FDD Data call Band 66 @+23dBm	TBD
		LTE FDD Data call Band 71 @+23dBm	TBD
	LTE TDD	LTE TDD Data call Band 41 @+23dBm	TBD
		LTE TDD Data call Band 48 @+21dBm	TBD
	LTE HPUE	LTE TDD Data call Band 41 @+26dBm	TBD
$I_{NSA-RMS}$	EN-DC	EN-DC Data call B2+n5 @20dBm+20dBm	TBD

State	Mode	Condition	Typical Current/mA
		EN-DC Data call B2+n71 @20dBm+20dBm	TBD
		EN-DC Data call B66+n66 @20dBm+20dBm	TBD
		EN-DC Data call B5+n66 @20dBm+20dBm	TBD
		EN-DC Data call B2+n66 @20dBm+20dBm	TBD
		EN-DC Data call B2+n12 @20dBm+20dBm	TBD
		EN-DC Data call B66+n25 @20dBm+20dBm	TBD
		EN-DC Data call B48+n5 @20dBm+20dBm	TBD
		EN-DC Data call B66+n30 @20dBm+20dBm	TBD
		EN-DC Data call B48+n66 @20dBm+20dBm	TBD
	EN-DC HPUE	EN-DC Data call B2+n41 @23dBm+23dBm	TBD
		EN-DC Data call B66+n41 @23dBm+23dBm	TBD
		EN-DC Data call B41+n41 @23dBm+23dBm	TBD
		EN-DC Data call B12+n77 @23dBm+23dBm	TBD
		EN-DC Data call B2+n77 @23dBm+23dBm	TBD
		EN-DC Data call B48+n77 @23dBm+23dBm	TBD
I_{SA-RMS}	SA FDD SA TDD	n2@max power (10MHz, Inner full RB)	TBD
		n5@max power (10MHz, Inner full RB)	TBD
		n12@max power (10MHz, Inner full RB)	TBD
		n14@max power (10MHz, Inner full RB)	TBD
		n25@max power (10MHz, Inner full RB)	TBD

State	Mode	Condition	Typical Current/mA
		n30@max power (10MHz, Inner full RB)	TBD
		n66@max power (10MHz, Inner full RB)	TBD
		n70@max power (10MHz, Inner full RB)	TBD
		n71@max power (10MHz, Inner full RB)	TBD
		n41@max power (100MHz, Inner full RB)	TBD
		n48@max power (40MHz, Inner full RB)	TBD
		n77@max power (100MHz, Inner full RB)	TBD
	SA TDD HPUE	n41@max power (100MHz, Inner full RB)	TBD
		n77@max power (100MHz, Inner full RB)	TBD
	SA UL MIMO	n41@max power (100MHz, Inner full RB)	TBD
		n77@max power (100MHz, Inner full RB)	TBD

Test condition: temperature 25℃, VBAT_BB&VBAT_RF: 3.8V.

4.4 Radio Frequency

4.4.1 Transmitting Power

The transmit power for each band of the FG160 module is shown in the following table:

Table 11. RF transmit power

Mode	Band	3GPP Requirement (dBm)	Tx Power (dBm)	Note
LTE FDD	Band 2	23±2.7	23±1.5	10MHz BW, 12RB
	Band 4	23±2.7	23±1.5	10MHz BW, 12RB
	Band 5	23±2.7	23±1.5	10MHz BW, 12RB
	Band 7	23±2.7	23±1.5	10MHz BW, 12RB
	Band 12	23±2.7	23±1.5	10MHz BW, 12RB
	Band 13	23±2.7	23±1.5	10MHz BW, 12RB
	Band 30	23±2.7	22±1	10MHz BW, 12RB
	Band 66	23±2.7	23±1.5	10MHz BW, 12RB
	Band 71	23+2.7/-3.2	23±1.5	10MHz BW, 12RB
LTE TDD	Band 41	23±2.7	23±1.5	10MHz BW, 12RB
	Band 41 HPUE	26±2.7	26±1.5	10MHz BW, 12RB
	Band 48	23+3.0/-4.0	21±1	10MHz BW, 12RB
5G NR	n2	23±2.7	23±1.5	10MHz BW, inner Full
	n5	23±2.7	23±1.5	10MHz BW, inner Full
	n7	23±2.7	23±1.5	10MHz BW, inner Full
	n12	23±2.7	23±1.5	10MHz BW, inner Full
	n14	23±2.7	23±1.5	10MHz BW, inner Full
	n25	23±2.7	23±1.5	10MHz BW, inner Full
	n30	23±2.7	22±1	10MHz BW, inner Full
	n48	23+3/-4	21±1	10MHz BW, inner Full

Mode	Band	3GPP Requirement (dBm)	Tx Power (dBm)	Note
	n66	23±2.7	23±1.5	10MHz BW, inner Full
	n70	23±2.7	23±1.5	10MHz BW, inner Full
	n71	23+2.7/-3.2	23±1.5	10MHz BW, inner Full
	n41	23±3	23±1.5	100MHz BW, inner Full
	n41 HPUE	26+3/-4	26±1.5	100MHz BW, inner Full
	n41 UL MIMO	24.5+3/-4	24.5±1.5	100MHz BW, inner Full
	n77	23+3/-4	23±1.5	100MHz BW, inner Full
	n77 HPUE	26+3/-4	26±1.5	100MHz BW, inner Full
	n77 UL MIMO	24.5+3/-4	24.5±1.5	100MHz BW, inner Full
	n78	23+3/-4	23±1.5	100MHz BW, inner Full
	n78 HPUE	26+3/-4	26±1.5	100MHz BW, inner Full
	n78 UL MIMO	24.5+3/-4	24.5±1.5	100MHz BW, inner Full

4.4.2 Dual Antenna Receiver Sensitivity

The receiver sensitivity with dual antenna for each band of FG160 module is shown in below table:

Table 12. RF receiver sensitivity

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
LTE FDD (10MHz)	Band 2	-94.3	TBD	10MHz BW
	Band 4	-96.3	TBD	10MHz BW

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
	Band 5	-94.3	TBD	10MHz BW
	Band 7	-94.3	TBD	10MHz BW
	Band 12	-93.3	TBD	10MHz BW
	Band 13	-93.3	TBD	10MHz BW
	Band 29	TBD	TBD	10MHz BW
	Band 30	-95.3	TBD	10MHz BW
	Band 66	-95.8	TBD	10MHz BW
	Band 71	-93.5	TBD	10MHz BW
LTE TDD (10MHz)	Band 41	-94.3	TBD	10MHz BW
	Band 46	TBD	TBD	10MHz BW
	Band 48	-95	TBD	10MHz BW
NR	n2	-94.8	TBD	SCS 15KHz 10MHz BW
	n5	-94.8	TBD	SCS 15KHz 10MHz BW
	n7	-94.8	TBD	SCS 15KHz 10MHz BW
	n12	-93.8	TBD	SCS 15KHz 10MHz BW
	n14	-93.8	TBD	SCS 15KHz 10MHz BW
	n25	-93.3	TBD	SCS 15KHz 10MHz BW
	n30	-95.8	TBD	SCS 15KHz 10MHz BW
	n41	-84.7	TBD	SCS 30KHz 100MHz BW
	n48	-96.1	TBD	SCS 30KHz 10MHz BW
	n66	-96.3	TBD	SCS 15KHz 10MHz BW

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
	n70	-96.8	TBD	SCS 15KHz 10MHz BW
	n71	-94	TBD	SCS 15KHz 10MHz BW
	n77	-85.1	TBD	SCS 30KHz 100MHz BW
	n78	-85.6	TBD	SCS 30KHz 100MHz BW

4.4.3 Four Antenna Receiver Sensitivity

The L/M/H bands can support DL 4 MIMO, the receiver sensitivity of L/M/H bands is shown in the following table:

Table 13. RF receiver sensitivity

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
LTE FDD (10M)	Band 2	-97	TBD	10MHz BW
	Band 4	-99	TBD	10MHz BW
	Band 5	TBD	TBD	10MHz BW
	Band 7	-97	TBD	10MHz BW
	Band 12	TBD	TBD	10MHz BW
	Band 13	TBD	TBD	10MHz BW
	Band 30	-98	TBD	10MHz BW
	Band 66	-98.5	TBD	10MHz BW
	Band 71	TBD	TBD	10MHz BW
LTE TDD (10M)	Band 41	-97	TBD	10MHz BW
	Band 48	TBD	TBD	10MHz BW

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
5G NR	n2	-97.5	TBD	SCS 15KHz 10MHz BW
	n5	TBD	TBD	SCS 15KHz 10MHz BW
	n7	-97.5	TBD	SCS 15KHz 10MHz BW
	n12	TBD	TBD	SCS 15KHz 10MHz BW
	n14	TBD	TBD	SCS 15KHz 10MHz BW
	n25	TBD	TBD	SCS 15KHz 10MHz BW
	n30	-98.5	TBD	SCS 15KHz 10MHz BW
	n66	-99	TBD	SCS 15KHz 10MHz BW
	n70	-99.5	TBD	SCS 15KHz 10MHz BW
	n71	TBD	TBD	SCS 15KHz 10MHz BW
	n41	–87.4	TBD	SCS 30KHz100MHz BW
	n48	-98.3	TBD	SCS 30KHz 10MHz BW
	n77	–87.3	TBD	SCS 30KHz 100MHz BW
	n78	–87.8	TBD	SCS 30KHz 100MHz BW

4.4.4 GNSS

FG160 module supports GNSS with ANT_10 antenna, the GNSS includes GPS/GLONASS/ Galileo/BDS/QZSS. GNSS performance is shown in below table:

Table 14. GNSS performance

Description	Condition	Test Result (Typ)
Current	Fixing	TBD
	Tracking	TBD

Description	Condition	Test Result (Typ)
	Sleep	TBD
TTFF	Cold start	TBD
	Warm start	TBD
	Hot Start	TBD
Sensitivity	Tracking	TBD
	Acquisition	TBD

4.4.5 Operating Band

Table 15. Operating band

Band	Mode	Tx (MHz)	Rx (MHz)
Band 2	LTE FDD	1850–1910	1930–1990
Band 4	LTE FDD	1710–1755	2110–2155
Band 5	LTE FDD	824–849	869–894
Band 7	LTE FDD	2500-2570	2620-2690
Band 12	LTE FDD	699–716	729–746
Band 13	LTE FDD	777–787	746–756
Band 29	LTE FDD	--	717–728
Band 30	LTE FDD	2305–2315	2350–2360
Band 41	LTE TDD	2496–2690	
Band 46	LTE TDD	--	5150–5925
Band 48	LTE TDD	3550–3700	
Band 66	LTE FDD	1710–1780	2110–2200

Band	Mode	Tx (MHz)	Rx (MHz)
Band 71	LTE FDD	663–698	617–652
n2	NR FDD	1920–1980	2110–2170
n5	NR FDD	703–748	758–803
n7	NR FDD	2500-2570	2620-2690
n12	NR FDD	699–716	729–746
n14	NR FDD	788–798	758–768
n25	NR FDD	1850–1915	1930–1995
n30	NR FDD	2305–2315	2350–2360
n41	NR TDD	2496–2690	
n48	NR TDD	3550–3700	
n66	NR FDD	1710–1780	2110–2200
n70	NR FDD	1695–1710	1995–2020
n71	NR FDD	663–698	617–652
n77	NR TDD	3300–4200	3300–4200
n78	NR TDD	3300–3800	3300–3800
GPS L1	--	--	1575.42±1.023
GPS L5	--	--	1176.45±10.23
GLONASS G1	--	--	1602.5625±4
Galileo E1	--	--	1575.42±2.046
BDS B1	--	--	1561.098±2.046
QZSS	--	--	1575.42±1.023

4.4.6 Antenna Requirements

Table 16. Module antenna requirements

FG160 module antenna requirements	
LTE/NR	VSWR: ≤ 2:1 Input power (W): > 28dBm average power LTE & NR Input impedance (Ω): 50 Antenna isolation (dB): > 25
GNSS	Frequency range: 1559MHz–1607MHz VSWR: < 2: 1

5 Interface Introduction

5.1 Power

The DC power input range of FG160 module is 3.3V to 4.4V, and the recommended value is 3.8V. DC power continuous output ability requires more than 3A. The performance of the power supply, such as load capacity and ripple size, will directly affect the performance and stability of the module.

5.1.1 Power Supply

FG160 module provides power supply via VBAT_BB and VBAT_RF.

The power supply design is shown in following figure:

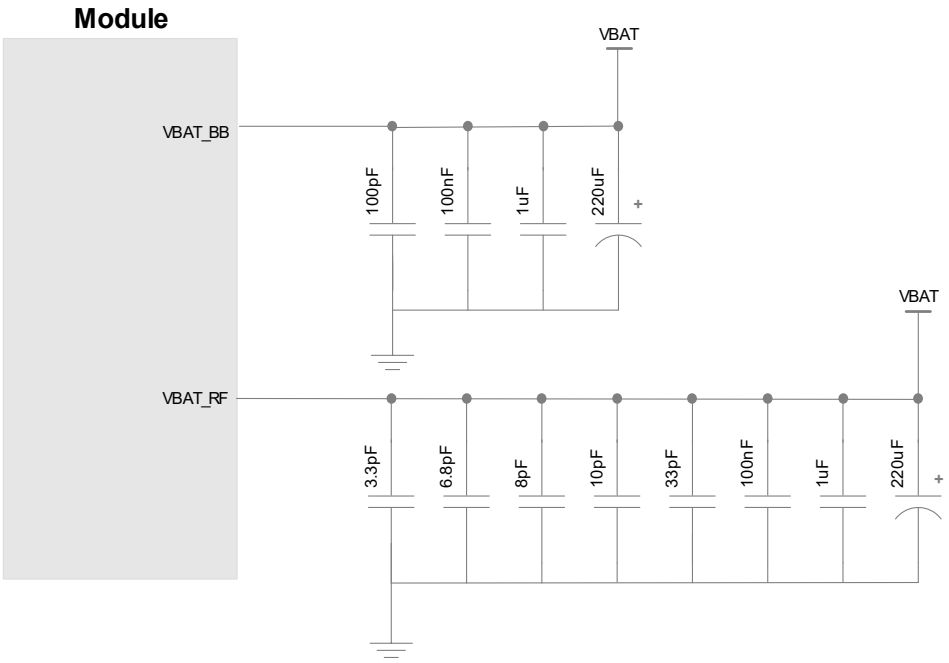

Figure 3. Power supply design

The filter capacitor design for power supply as shown in the following table:

Table 17. Power supply filter capacitor design

Recommended Capacitance	Description
220uF × 2	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. LDO or DC/DC power supply requires the capacitor no less than 440uF. The capacitor for battery power supply can be reduced to 100-200uF.
1uF × 2,100nF × 2	Filter out the interference generated from the clock and digital signals
33pF	Filter out 600/700/850/900MHz frequency band RF interference(low band)
3.3pF,6.8pF,8pF, 10pF	Filter out 1700/1800/1900/2100/2300/2500/2600/3500/3700MHz,5GHz frequency band RF interference(high band)

The stable power supply can ensure the normal operation of FG160 module, and the ripple of the power supply should be less than 300mV in design. Because module support 5G NR Sub-6 download, when module operates with the maximum data transfer throughput, the peak current can reach to upper 4000 mA. It requests the power source voltage should not be lower than 3.3V, otherwise module may shut down or restart. The power supply requirement is shown in following figure:

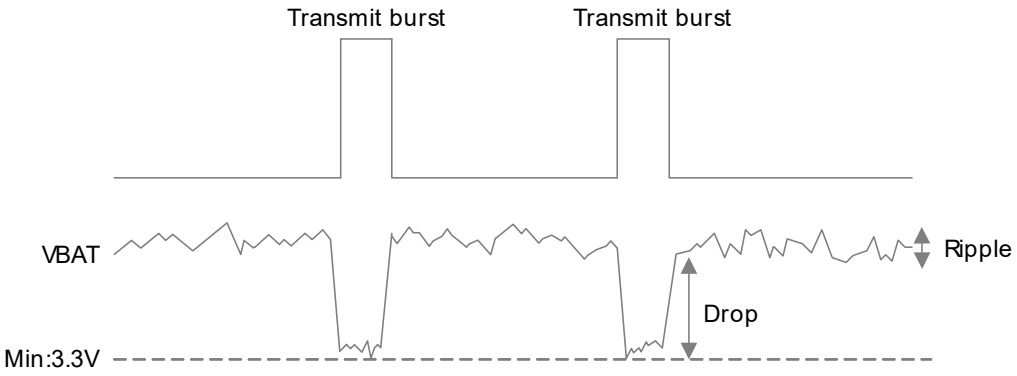

Figure 4. Power supply voltage drop diagram

The filter capacitor is located near the pin of the power supply and arranged in order of capacity size. It is recommended that the PCB traces of the power supply be as short as possible. It is wide enough power supply traces to ensure that no large voltage drops occur in maximum transmit power status.

5.2 Control Interface

The FG160 module provides three control signals for power-on/off and reset operations, the pins are defined in the following table:

Table 18. Control signal

Pin name	Pin No	I/O	Description
CBL_PWR_N	291	DI	Module power on input, internal pull up Pull down CBL_PWR_N for more than some time, Module will power on from power off status.
PWRKEY	1	DI	Module power on/off input, internal pull up Pull down PWRKEY with pulse, module will power on from power off status. Pull down PWRKEY with pulse, module will power off from power on status.
RESET_N	4	DI	Pull down RESET_N with pulse, module will reset
PCIE_PERSTN	275	DIO	PCIe link reset signal

CBL_PWR_N signal can only be used for module startup, not shutdown. It is mainly used for automatic startup applications

5.2.1 Normal Mode

5.2.1.1 Module Start-up

When the module is in shutdown mode, pull down PWRKEY with pulse to enable the module to start. The way to control the PWRKEY pin is directly through a push button switch. A TVS (EGA10402V05AH-A recommended) should be placed near the button for ESD protection. The reference circuit is shown below:

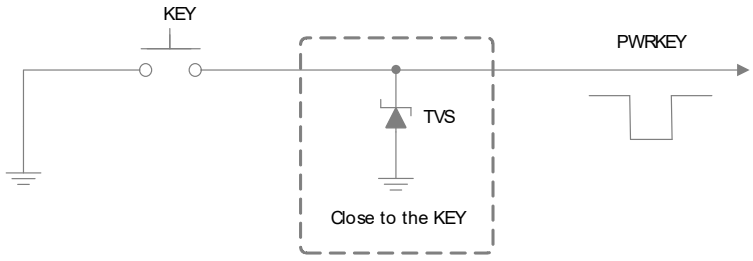

Figure 5. Normal mode start-up circuit

The start-up timing sequence is shown in following figure:

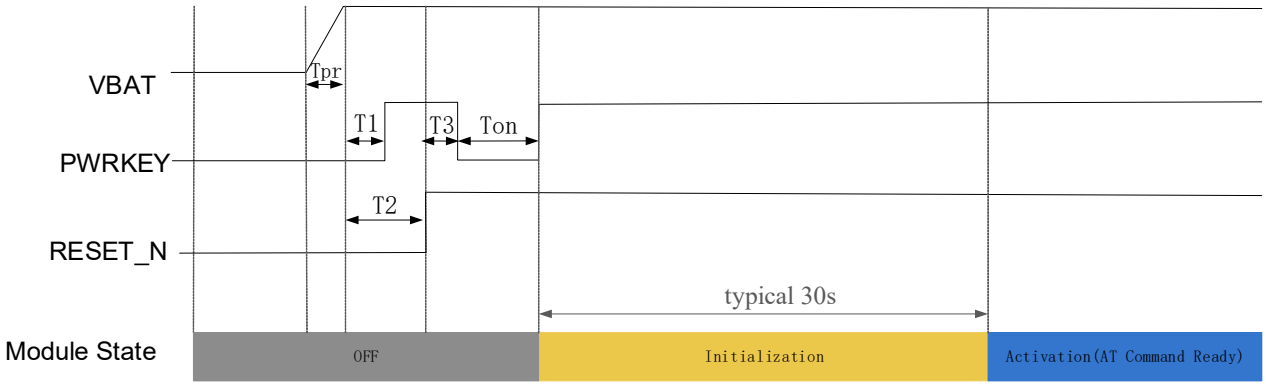

Figure 6. Normal mode timing control for start-up

Index	Min.	Recommended	Max.	Comments
Tpr	0ms	--	--	The delay time of power supply rising from 0V up to 3.3V. If power supply always ready, it can be ignored
T1		0.5ms		PWRKEY pin ready time after power on. This pin is high when ready due to internal pull-up
T2		75ms		RESET_N pin ready time after power on. This pin is high when ready due to internal pull-up
T3	0ms			Delay time from RESET_N pin ready to pulse trigger signal start point.
Ton	50ms	--	1000ms	Power-on pulse signal width

Before pulling down the PWRKEY pin, ensure that the VBAT voltage is more than 3.3V.

5.2.1.2 Module Shutdown

The module support the following shutdown mode:

Table 19. Shutdown mode

Shutdown Type	Shutdown Method	Remark
Hardware shutdown	Pull down PWRKEY with pulse then release	--

The shutdown timing sequence is shown in following figure:

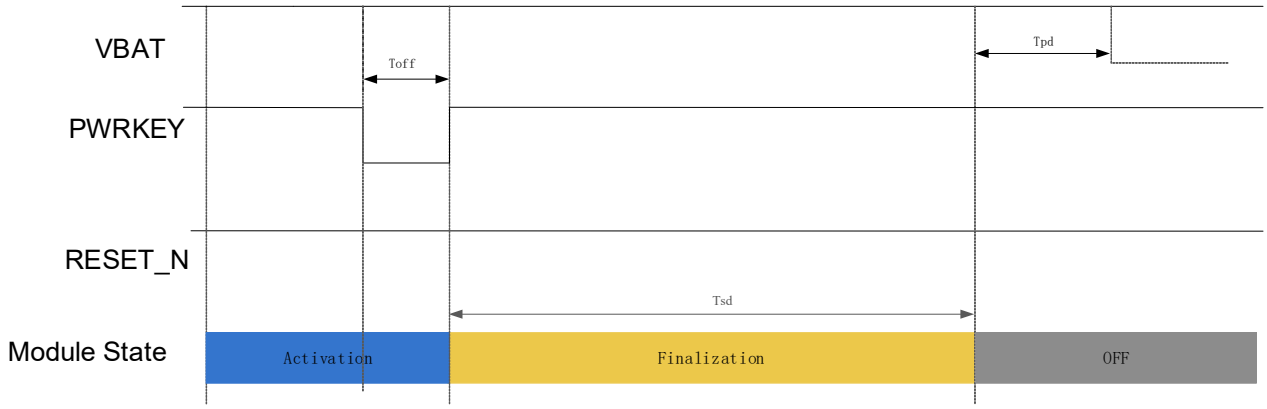

Figure 7. Normal mode shutdown timing

Index	Min.	Recommended	Max.	Comments
T_{off}	2500ms	--	5000s	Power-off pulse signal width
T_{pd}	10ms	100ms	--	VBAT power supply goes down time. If power supply is always on, it can be ignored

After the PWRKEY signal is released, the next power-on trigger can be performed at least 2s later. This interval is reserved for the module shutdown process and the power release of the peripheral circuit connecting with module interface.

5.2.1.3 Module Reset

There is a type of module reset: hardware reset.

Table 20. Reset method

Reset type	Reset method
Hardware reset	Pull down the RESET_N pin with pulse, then release

The way to control the RESET_N pin is directly through a push button switch. A TVS (EGA10402V05AH-A recommended) should be placed near the button for ESD protection. The reference circuits are shown in the following figure:

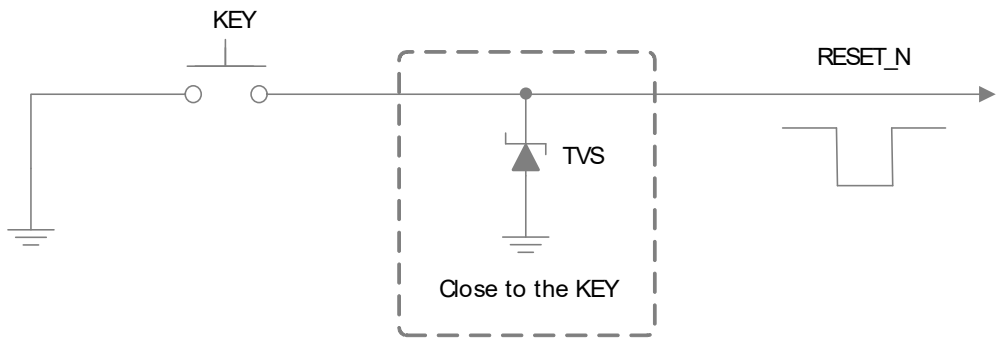

Figure 8. Normal mode reset circuit

Reset timing sequence is shown in the following figure:

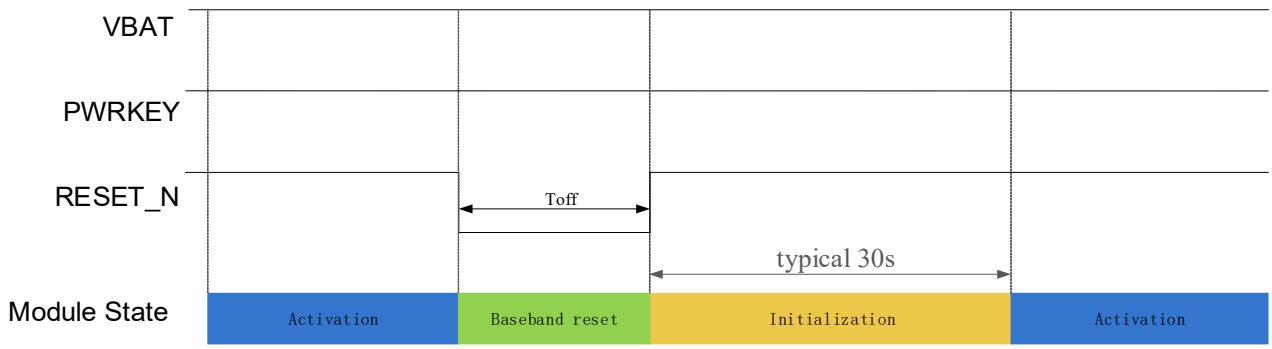

Figure 9. Normal mode reset timing

Index	Min.	Recommended	Max.	Comments
t_{off}	600ms	--	750ms	Pull down the RESET_N pin with pulse, then release

50 seconds minimum before next reset operation. The RESET_N pin of module has internal pull-up, no need external pull-up.

5.2.2 PCIe EP Mode

When FG160 is configured as PCIe EP mode (slave mode), there will be some differences in control timing, and there are some related design should be applied refer to chapter 5.8

5.2.2.1 Module Start-up

It is recommended to use the following OC driver circuit to control the PWRKEY pin. The reference circuit is shown in the following figure:

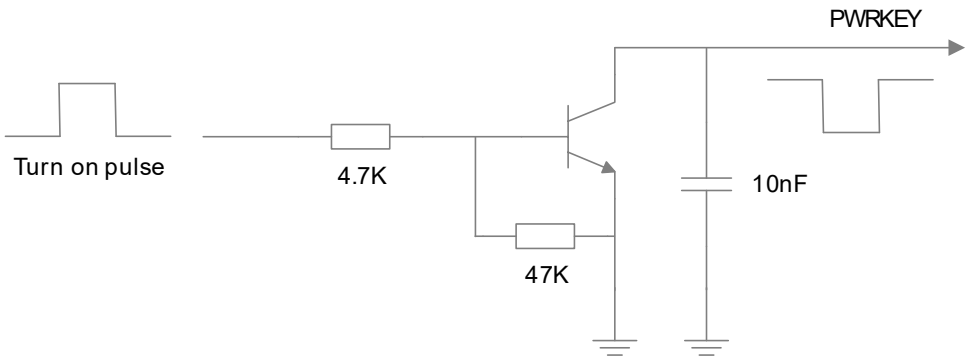

Figure 10. PCIe EP mode start-up circuit

The start-up timing sequence is shown in following figure:

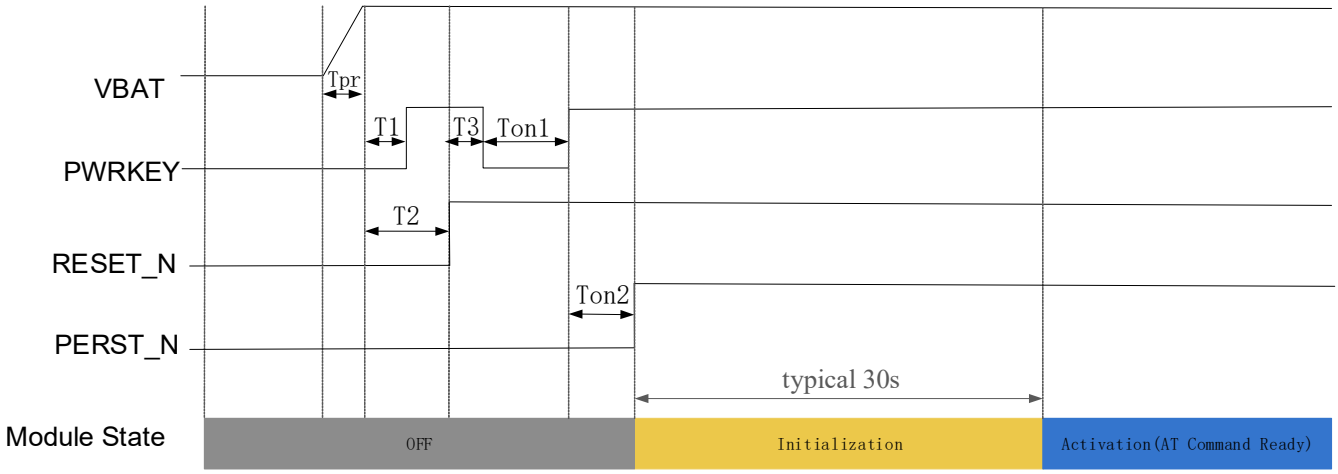

Figure 11. PCIe EP mode timing control for start-up

Index	Min.	Recommended	Max.	Comments
Tpr	0ms	--	--	The delay time of power supply rising from 0V up to 3.3V. If power supply always ready, it can be ignored
T1		0.5ms		PWRKEY pin ready time after power supply ready. This pin is high when ready due to internal pull-up
T2		75ms		RESET_N pin ready time after power supply ready. This pin is high when ready due to internal pull-up
T3	0ms			Delay time from RESET_N pin ready to pulse trigger signal start point.
Ton1	50ms	--	1000ms	Power-on pulse signal width
Ton2	50ms	100ms	--	Delay time from PWRKEY achieved to PERST_N de-asserted

Before pulling down the PWRKEY pin, ensure that the VBAT voltage is more than 3.3V.

5.2.2.2 Module Shutdown

The shutdown timing sequence is shown in following figure:

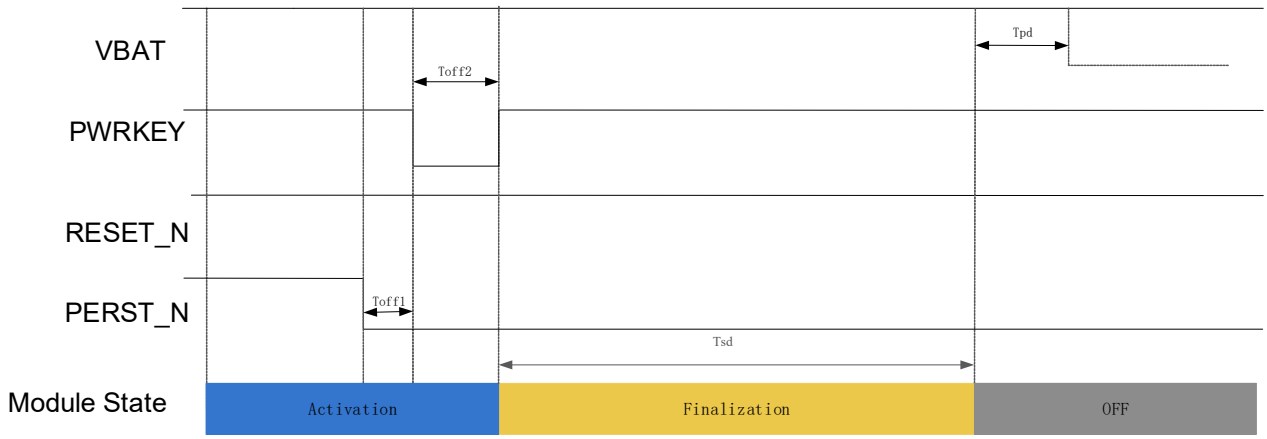

Figure 12. PCIe EP mode shutdown timing

Index	Min.	Recommended	Max.	Comments
T_{off1}	16ms	20ms	--	Delay time from PERST_N assert to pulse trigger signal start point
T_{off2}	2500ms	--	5000ms	Power-off pulse signal width
T_{pd}	10ms	100ms	--	VBAT power supply goes down time. If power supply is always on, it can be ignored

5.2.2.3 Module Reset

It is recommended to use the following OC driver circuit to control the RESET_N pin. The reference circuit is shown in the following figure:

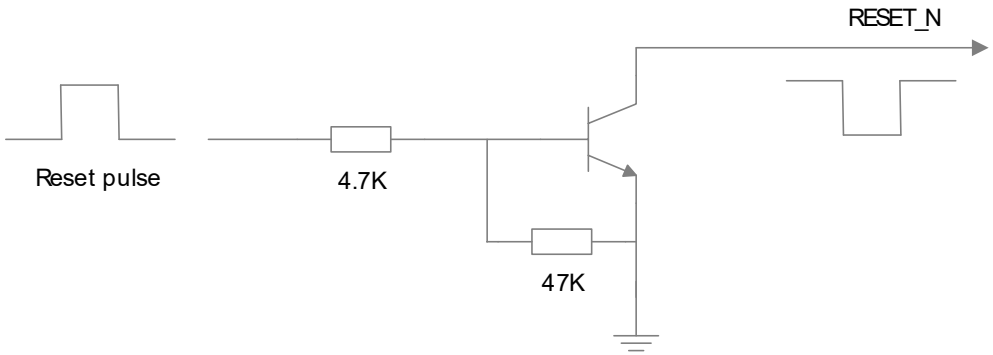

Figure 13. PCIe EP mode reset circuit

Reset timing sequence is shown in the following figure:

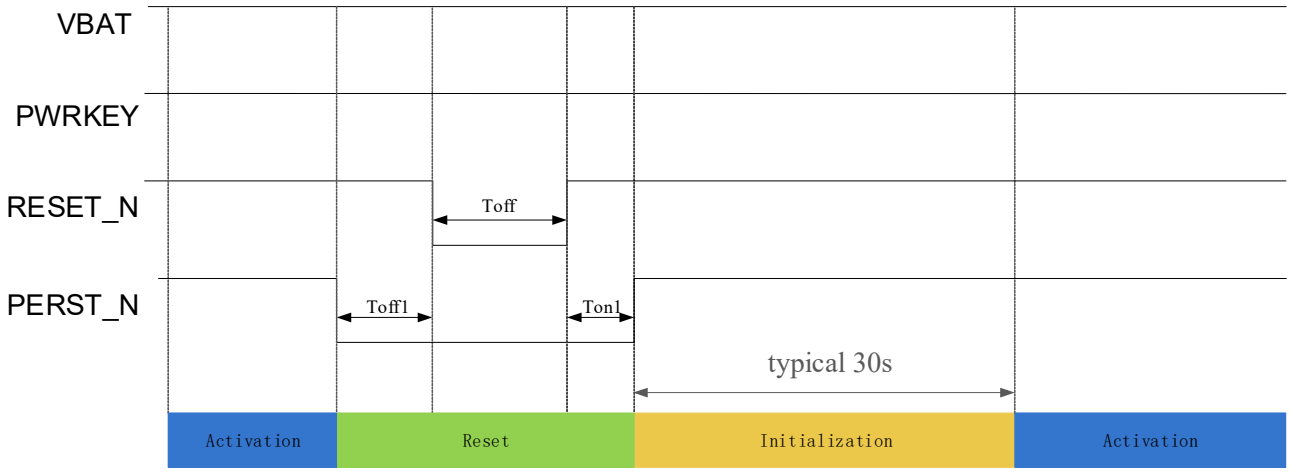

Figure 14. PCIe EP mode reset timing

Index	Min.	Recommended	Max.	Comments
T_{off1}	16ms	20ms	--	RESET_N should be asserted after PERST_N
T_{off}	600ms	--	750ms	Pull down the RESET_N pin with pulse, then release
T_{off2}	50ms	100ms	--	The time delay of PERST_N de-asserted after RESET_N de-asserted

50 seconds minimum before next reset operation. The RESET_N pin of module has internal pull-up, no need external pull-up.

5.3 Network Status Indicator Interface

The module provides four status indicator signal interfaces. The pin definition is shown in Table 21.

Table 21. Status indicator pin

Pin Name	Pin No	I/O	Description
5G_STATUS	106	DO	5G status indicator, Reserved
4G_STATUS	110	DO	4G status indicator, Reserved
WWAN_STATUS	108	DO	Module status indicator, Reserved Module power on: high level Module power off: low level
WIFI_STATUS	111	DO	WIFI status indicator, Reserved

5.3.1 Interface Status Description (Reserved)

The network status indicator interface is used to drive the status indicator, which is used to indicate the network status of the module as Table 22.

Table 22. Status indicator output mode

Mode	Module Network Status	Indicator Pin status	LED Status

1	Data T-put transfer	75ms high level / 75ms low level	Flash, 75ms on / 75ms off
2	Network ready	High level	ON
3	Network not ready	Low level	OFF

The network status indicator reference circuit is as follows:

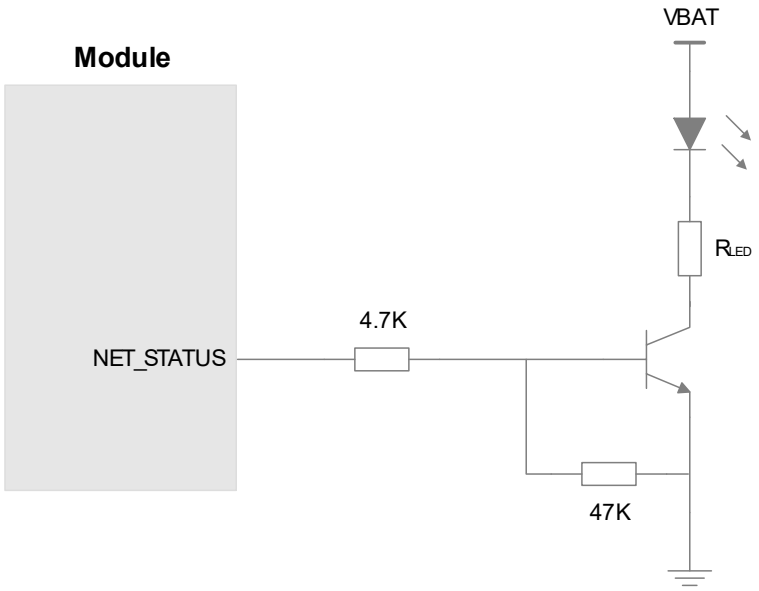

Figure 15. Indicator drive circuit diagram

The LED brightness depends on resistance of R_{LED}.

5.4 SIM Card Interface

The FG160 module support dual SIM. There are two SIM card interface and can supports 1.8V and 3.0V SIM cards.

5.4.1 SIM Card Interface Definition

SIM pin definition is shown in the following table:

Table 23. SIM pin definition

Pin name	Pin No	I/O	Description
SIM1_VDD	7	PO	SIM1 power output, 3V/1.8V
SIM1_DATA	10	DIO	SIM1 data signal
SIM1_CLK	13	DO	SIM1 clock signal
SIM1_RST	16	DO	SIM1 reset signal
SIM1_DET	14	DI	SIM1 insert detection signal, internal 390K pull-up. Active high, high level indicates SIM card inserted and low level indicates SIM card plugged out.
SIM2_VDD	18	PO	SIM2 power output, 3V/1.8V
SIM2_DATA	12	DIO	SIM2 data signal
SIM2_CLK	15	DO	SIM2 clock signal
SIM2_RST	11	DO	SIM2 reset signal
SIM2_DET	267	DI	SIM2 insert detection signal, internal 390K pull-up. Active high, high level indicates SIM card inserted and low level indicates SIM card plugged out.

The SIM2 interface is NC (not connected) when module has embedded eSIM.

5.4.2 SIM Card Interface Circuit

SIM card interface reference circuit is shown in following figure.

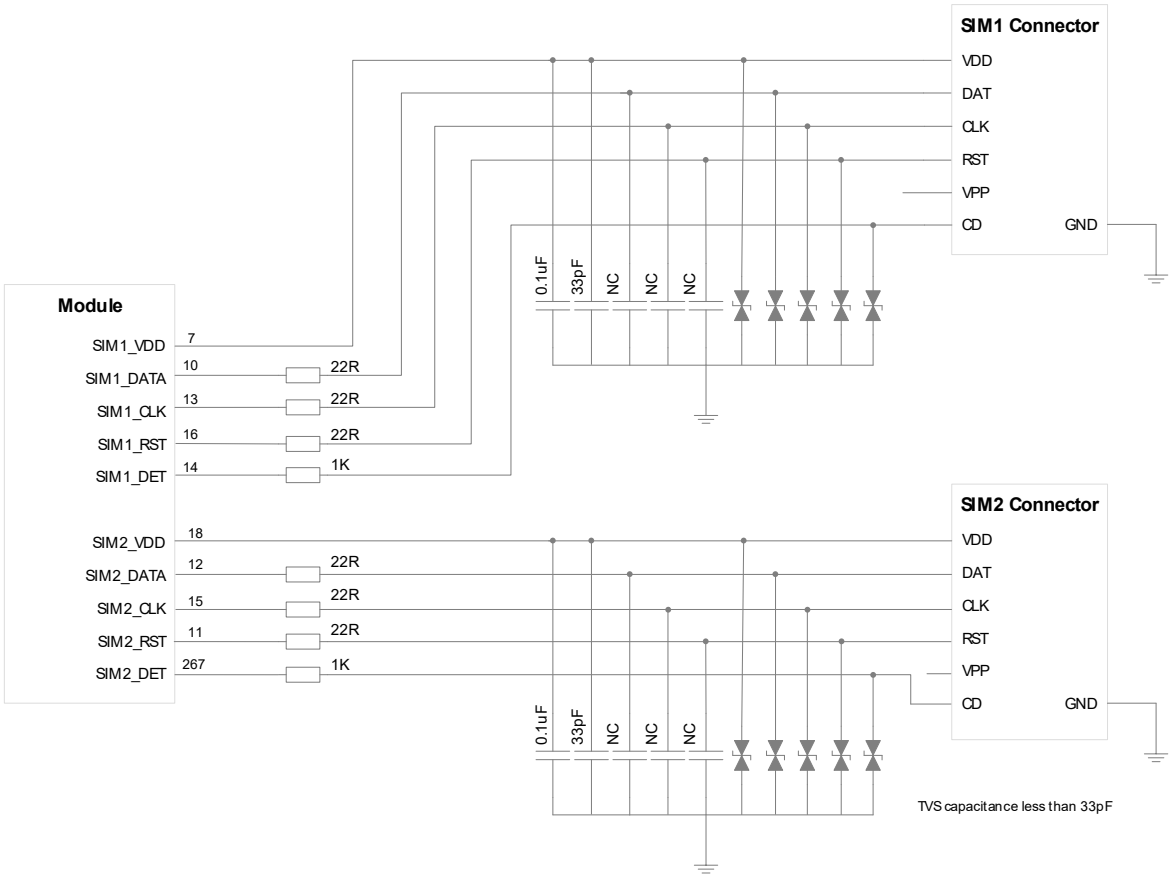

Figure 16. SIM interface reference circuit

5.5 USB Interface

FG160 module supports USB3.1 Gen2, USB2.0, compatible with USB1.1.

5.5.1 USB Interface Definition

Table 24. USB interface pin definition

Pin Name	Pin No	I/O	Description
SSUSB_TXN	55	AO	USB super speed transmit data minus
SSUSB_TXP	58	AO	USB super speed transmit data plus
SSUSB_RXN	61	AI	USB super speed receive data minus
SSUSB_RXP	63	AI	USB super speed receive data plus
USB_DM	59	AIO	USB high speed data minus

USB_DP	62	AIO	USB high speed data plus
VBUS_DET	57	DI	USB VBUS detection

5.5.2 USB Interface Circuit

USB interface reference circuit is shown in the following figure:

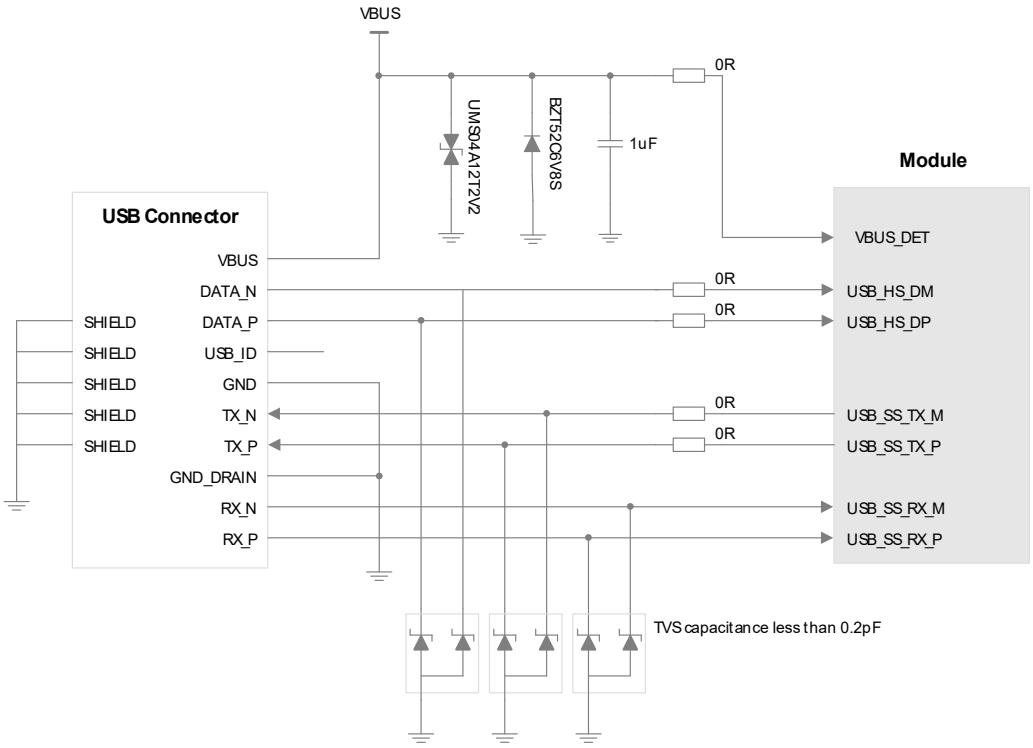

Figure 17. USB interface reference design

5.5.3 USB Routing Rules

5.5.3.1 USB2.0 Routing Rules

- The USB_DM / USB_DP trace length mismatch is controlled within ≤ 50mil, and the differential impedance is controlled as 90Ω ± 10%.
- USB_D- and USB_D+ signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

5.5.3.2 USB3.1 Routing Rules

- SSUSB _RXP/N and SSUSB_TXP/N are two sets of differential signals, with differential impedance controlled as 90Ω ± 10%; the length match of the intra differential pair ≤ 5mil.
- The two pairs of differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

5.6 ADC Interface

The FG160 module provides two analog-to-digital conversion interfaces.

5.6.1 ADC Interface Definition

Table 25. ADC interface definition

Pin Name	Pin No	I/O	Description
ADC0	249	AI	A/D conversion channel 0
ADC1	252	AI	A/D conversion channel 1

5.6.2 ADC Electrical Characteristics

Table 26. ADC electrical characteristics

Pin Name	Input Voltage Range (V)	Resolution (uV)
ADC0	0-1.875	64.879
ADC1	0-VBAT_BB	194.637

Please keep ADC signals connect to ground if not used.

5.7 Forced-download Interface

The FG160 module has a forced-download signal shown in Table 27.

Table 27. Forced-download interface

Pin Name	Pin No	I/O	Description
USB_BOOT	273	DI	Forced into USB download boot mode Default low, high active.

5.7.1 Configuration Signal Interface Circuit

Reference circuit is shown in following figure:

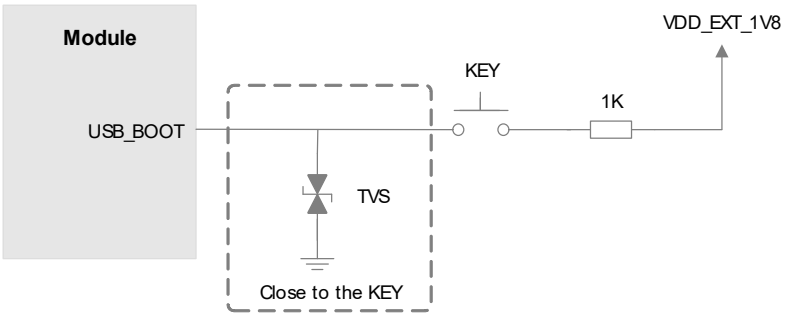

Figure 18. Configuration signal circuit

5.8 PCIE Boot Control Interface

Table 28. PCIe boot control pin

Pin Name	Pin No.	I/O	Description
BOOT_PCIE	66	DIO	PCIE boot control signal
BOOT_CFG	293	DO	PCIE boot configure signal

When need to configure as PCIe EP mode, the circuit below should be applied.

If not, just keep BOOT_CFG and BOOT_PCIE floating.

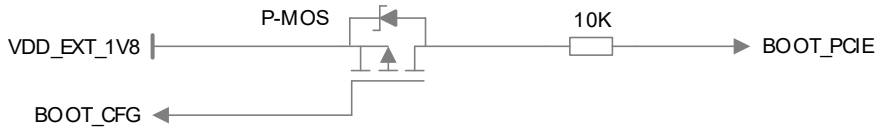

Figure 19. PCIe boot mode configure circuit

5.9 Flight Mode Control Interface (Reserved)

Pull down the W_DISABLE pin to enter flight mode

Table 29. Flight mode control pin

Pin Name	Pin No.	I/O	Description
W_DISABLE	109	DI	Module flight mode control signal, reserved

5.10 GPIO Interface

Table 30. GPIO table

Pin Name	Pin No	Power Domain	Default Pull Type	EINT	GPIO No
WIFI_STATUS	111	1.8V	PD	N	GPIO97
4G_STATUS	110	1.8V	PD	N	GPIO01(PMU)
W_DISABLE	109	1.8V	PD	Y	GPIO86
5G_STATUS	106	1.8V	PD	N	GPIO14(PMU)
WPS	123	1.8V	PD	N	GPIO09(PMU)
WWAN_STATUS	108	1.8V	PD	N	GPIO04(PMU)
DAC_PWR_EN	107	1.8V	PD	N	GPIO06(PMU)
BT_EN	209	1.8V	PD	N	GPIO15(PMU)
WL_EN	204	1.8V	PD	N	GPIO91

WL_EN_1	26	1.8V	PD	N	GPIO87
WL_PWR_EN	24	1.8V	PD	N	GPIO102
QPS615_PWR_EN	278	1.8V	PD	N	GPIO101
QPS615_PWR_EN_1	270	1.8V	PD	N	GPIO107
ETH1_PWR_EN	271	1.8V	PD	N	GPIO106
ETH0_PWR_EN	272	1.8V	PD	N	GPIO105

All GPIO in the table above can be configured according to the requirements.

5.11 PCIE Interface

FG160 module support 1 group PCIe Gen3, x2 lanes. Both RC mode and EP mode support.

5.11.1 PCIe Interface Definition

Table 31. PCIe signal list

Pin Name	Pin No	I/O	Pin Description
PCIE_CLKN	34	AIO	PCIe reference clock minus
PCIE_CLKP	37	AIO	PCIe reference clock plus
PCIE_LN0_TXN	40	AO	PCIe Tx0 minus
PCIE_LN0_TXP	43	AO	PCIe Tx0 plus
PCIE_LN1_TXN	39	AO	PCIe Tx1 minus
PCIE_LN1_TXP	38	AO	PCIe Tx1 plus
PCIE_LN0_RXN	46	AI	PCIe Rx0 minus
PCIE_LN0_RXP	49	AI	PCIe Rx0 plus
PCIE_LN1_RXN	44	AI	PCIe Rx1 minus

Pin Name	Pin No	I/O	Pin Description
PCIE_LN1_RXP	41	AI	PCIe Rx1 plus
PCIE_PEWAKEN	274	DIO	PCIe wake-up signal
PCIE_PERSTN	275	DIO	PCIe reset signal
PCIE_CLKREQN	276	DIO	PCIe clock request signal

5.11.2 PCIE Routing Rules

The PCIe bus can up to 8 GT/s speed. The following rules should be followed strictly in PCB layout:

- The impedance of differential pair lines are recommended to be 85Ω ± 10%. The length match of the intra differential pair ⩽ 5mil;
- The differential signal pair lines shall be short if possible and be controlled within 180 mm.

5.11.3 PCIE Application Circuit

Please refer to *FIBOCOM FG160_Reference Design HDK* for PCIE application circuit.

5.12 SD Interface

FG160 module supports SD interface, the standard is as follows:

Physical Layer Specification version 3.0, SDIO Card Specification version 3.0

5.12.1 SD Interface Definition

Table 32. SD signal list

Pin Name	Pin No	I/O	Pin Description
SDC_CMD	47	DIO	SDC interface command signal

Pin Name	Pin No	I/O	Pin Description
SDC_CLK	45	DO	SDC interface clock signal
SDC_DATA0	56	DIO	SDC interface DATA0 signal
SDC_DATA1	53	DIO	SDC interface DATA1 signal
SDC_DATA2	51	DIO	SDC interface DATA2 signal
SDC_DATA3	54	DIO	SDC interface DATA3 signal
SDC_DET	280	DI	SD card insert detection
SD_PWR_EN	281	DO	SD card power supply enable
SDIO_VDD	211	PI	SDC interface I/O power domain
SD_LVL_SW	279	DO	GPIO, used for control SD I/O Power enable signal

5.12.2 SD Interface Routing Rules

The length of the signal line is controlled to ⩽100mm, and the difference between the length of the clock signal and the data signal is controlled to 6mm.

5.12.3 SD Interface Application Design

Refer to *FIBOCOM FG160_Reference Design HDK* for detail information including Block Diagram and Schematic.

5.13 I2C Interface

The FG160 module supports one I2C interface, applying the standard *I2C Specification, version 3.0*

Table 33. I2C Interface Definition

Pin Name	Pin No	I/O	Pin Description
I2C_SDA0	115	DIO	I2C data
I2C_SCL0	112	DO	I2C clock
I2C_SDA1	268	DIO	I2C data used for PCIe switch
I2C_SCL1	269	DO	I2C clock used for PCIe switch

5.14 I2S Interface

The FG160 module supports one I2S interface and default mode is PCM. The default sampling rate is 8KHz.

Table 34. I2S interface definition

Pin Name	Pin No	I/O	Pin Description
I2S0_DO	103	DO	I2S data output signal, can be defined as PCM_OUT
I2S0_DI	104	DI	I2S data input signal, can be defined as PCM_IN
I2S0_BCK	101	DO	I2S data bit clock signal, can be defined as PCM_CLK
I2S0_LRCK	105	DO	I2S frame clock signal, can be defined as PCM_SYNC
I2S0_MCK	94	DO	I2S main clock output, used for external audio codec

5.15 UART Interface

The FG160 module supports three UART interfaces which defined in the following tables.

Table 35. UART interface 1

Pin Name	Pin No	I/O	Pin Description
DBG_UART_TX	129	DO	UART transmit signal
DBG_UART_RX	126	DI	UART receive signal

Table 36. UART interface 2

Pin Name	Pin No	I/O	Pin Description
UART_CTS	79	DI	UART receive ready signal
UART_RTS	64	DO	UART transmit request signal
UART_TX	77	DO	UART transmit signal
UART_RX	73	DI	UART receive signal

Table 37. UART interface 3

Pin Name	Pin No	I/O	Pin Description
BT_UTXD	135	DO	UART transmit signal, Reserved for BT
BT_URXD	138	DI	UART receive signal, Reserved for BT
BT_URTS	282	DO	UART transmit request signal, Reserved for BT
BT_UCTS	283	DI	UART receive ready signal, Reserved for BT

UART interface 1 is debug UART port, used to access the main chip kernel and print log information, and default baud rate is 115200.

UART interface 2 is general UART port used to send AT command and transmission of information

UART interface 3 is BT UART port, used to transmission of BT information

5.16 SPI Interface

The FG160 module supports 1 SPI interface, works in master mode, and the clock supports up to 50MHz.

Table 38. SPI interface definition

Pin Name	Pin No	I/O	Pin Description
SPI0_MISO	5	DI	SPI interface input signal
SPI0_MOSI	8	DO	SPI interface output signal
SPI0_CSB	6	DO	SPI interface chip select signal
SPI0_CLK	9	DO	SPI interface clock signal

5.17 Other Interfaces

For the application of other interfaces, please refer to the recommended design. If the application scenario and the recommended design are not consistent, please contact our technicians for confirmation.

6 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

ESD performance parameters are as follows (temperature: 25 ° C, humidity: 45%)

Table 39. ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
GND	TBD	TBD	KV
RF Antenna Interface	TBD	--	KV
GNSS Antenna Interface	TBD	--	KV

The data is based on the test of FIBOCOM ADP-FG160-NA-00-00 development board.

ESD performance is related to PCB design. Pay special attention to the protection of important control signals such as reset signals and the preservation of the complete ground plane.

7 Thermal Design

FG160 is designed to work on an extreme temperature range, to make sure the module can work properly for a long time and achieve a better performance on conditions such as maximum power or high data transmission.

8 Structural Specification

8.1 Product Appearance

The appearance of the FG160 module product is as shown:

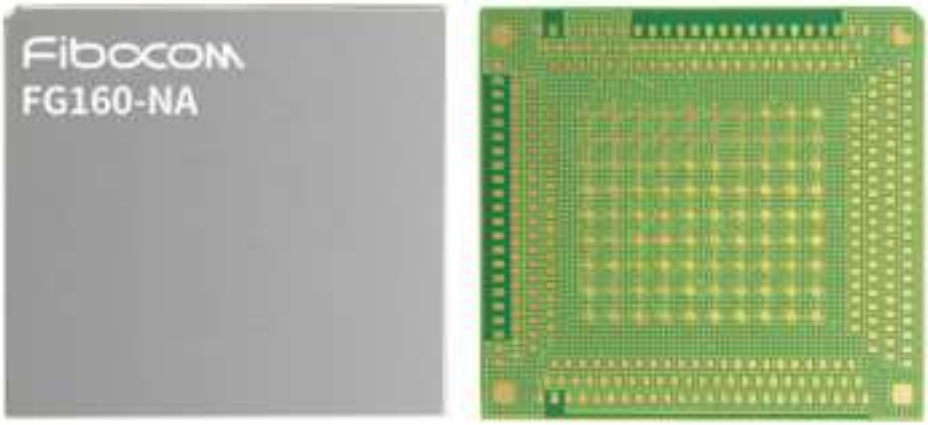

Figure 20. Module product appearance

8.2 Dimension of Structure

The structural dimensions of the FG160 module are shown in the following figure:

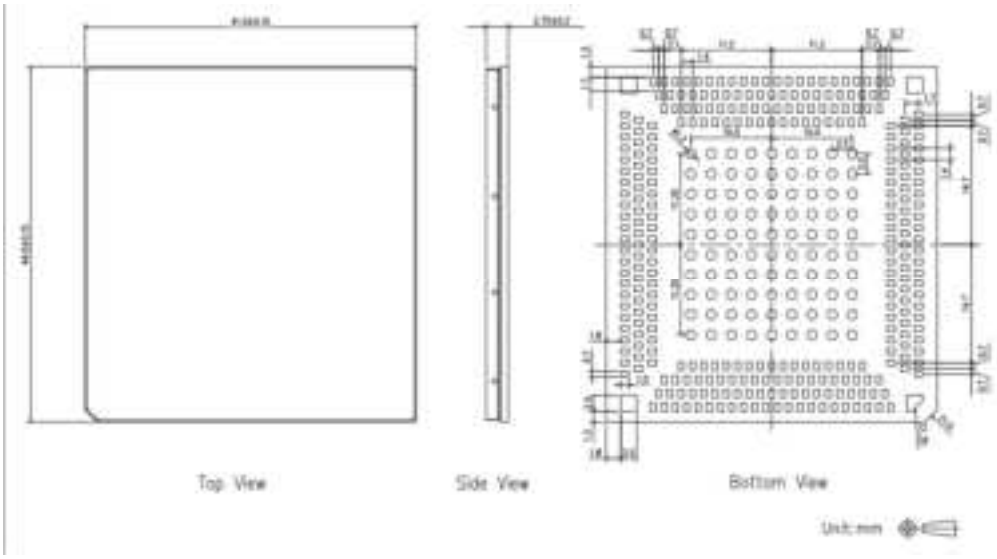

Figure 21. Structure size chart

Unmarked dimensional tolerances are 0.1 mm.

8.3 Storage

Refer to *FIBOCOM FG160-NA Series SMT Design Guide.*

8.4 Packing

Refer to *FIBOCOM FG160-NA Series SMT Design Guide.*