BRIEF CIRCUIT DESCRIPTION

INTRODUCTION

The VHF and UHF radio comprise two PCBs (RF and digital PCB). These boards are connected by 18-pin female and male connector. The digital board which controls radio and data receiving and sending is interfaced with external data equipment through the 15-pin d-sub female (DB-15) connector.

DIGITAL CIRCUITS

The Digital circuit contains the CPU, the channel select switch, and associated digital circuits.

TX-SIGNAL CIRCUIT

Generally, there are two signal paths in the TX-signal circuit. One is FSK data signal path and the other is audio signal path. In case of FSK data signal from Pin 1 of DB-15 connector (CON401) goes through IC406-C. That is amplified by IC404-C and then its amplitude is limited by IC404-D. After that, this signal is filtered by 8th order low pass filter (IC405) in order to reduce the required transmission bandwidth. First one stages of 8th order LPF consist of Gaussian filter for the improvement of ramp function response and last three stages use Butterworth filter to have enough attenuation. The output of LPF is then fed to the RF board for TX modulation.

Audio signal from Pin 7 of DB-15 connector is fed into the 300Hz High pass filter (IC408) through the IC406-B and IC409. HPF removes sub-audible voice products for application of Sub-audio (Tone) squelch system (CTCSS, DCS) and then the output from IC408 is fed into IC404-A&B with associated parts forming a mic amplifier and pre-emphasis circuit. After that, the pre-emphasized TX-audio signal is inputted to the RF board for TX modulation through FSK data signal path.

RX-SIGNAL CIRCUIT

The RX signal circuit also has two signal paths. One is data signal path and the other is audio signal path. The RX signal comes from the pin 10 of CON405 of Digital board connected with pin 10 of CON1 in RF board. In case of data signal, switched in IC406-D by Busy signal which is activated when radio receives valid RF signal, it is filtered by IC416-A and then its amplitude level is adjusted (amplified) by IC416-B. The amplitude-adjusted signal goes to pin 2 of DB-15 connector (CON401).

In the meantime, audio signal is inputted to the 300Hz High pass filter (IC408) to eliminate sub-audible voice products via IC409. The output of HPF is switched by IC406-A and de-emphasized by resister R471 and C452. After that, its level is adjusted by RV401 and then amplified by IC412 (LM386: Audio

amplifier). The amplified signal flows into pin 9 of CON401 (DB-15).

ANALOG SWITCH

IC409 (MC14053B) is a digitally controlled analog switch which internally consists of three single poles and double throw switches. Besides, there are three control lines, A, B, and C set a high at 5V or low at 0V respectively. The A controls the X ports, the B controls the Y ports, and the C controls the Z ports. Example: A high on control A would connect X to X1.Alow on control A would connect X to X0.

HIGH PASS FILTER

The 300Hz high pass filter is an 8-pole 1dB Chebeyshev active filter that comprises IC410 and peripheral components. Received audio passes to IC408 from Pin 4 of IC409 where sub-audible tones below 300Hz are removed. TX (Mic)audio is also fed into IC408 via IC409 (Pin 4) where sub-audible voice products below 300Hz are also removed.

CTCSS/DCS DECODE CIRCUITS

Discriminated audio from Pin 9 of IC6 is fed into IC411-B and associated parts which are the first 2 poles part of a 6th order 250 Hz Chebeyshev low pass filter. The output from pin 1 (IC411-B) is fed into IC409 (Pin 2) and out at pin 15 (IC409). The output signal is then fed to Pin 8 on IC410 which is a 6th order low pass Butterworth switched capacitor filter. The output from the Butterworth filter (Pin 3 of IC410) is then fed to the remaining second 4 poles part of the 6th order Chebeyshev filter, which consist of IC411-D and one of the two internal operational amplifiers of IC410 (MSNBLPS) along with associated components. Both the Chebeyshev and the Butterworth filter are combined to make a 4dB ripple low pass filter when programmed for 250Hz. The output of IC411-D (Pin 14) is fed into the remaining internal operational amplifier of IC410 (MSNBLPS) which forms the squaring circuit for the signal decode. The signal is out from Pin 2 of IC411 (MSNBLPS) and fed into IC401 (MCU) where it is compared whether that is matched with a preprogrammed data or not. If matched, a valid data is decoded and shown by a green L.E.D. on the top panel of the SD-160 data radio, and audio is released through pin 9 of DB-15 Connector. If unmatched, the busy Yellow L.E.D. would be shown.

CTCSS/DCS ENCODE CIRCUITS

During TX encode, the tone squelch digital signal is produced as a 3-bit parallel word at Pins 33, 34, and 35 of the micro controller (IC401). The 3-bit digital signal is converted to an analog signal by resistors

R481, 482 and 483. The analog signal is fed into Pin 1of IC409 and out on Pin 15 (IC409) and again flowed into Pin 8 of IC410 (6th order Butterworth clock tuned low pass filter). The filtered encode output from Pin 3 (IC410) is fed to IC411-A and RV402 (sub-audible gain control), the output at IC411-A is then fed to the audio mixer circuit of RF board.

TWO TONE DECODE CIRCUITS

Two tone uses same frequency with audio. Discriminated audio from the RF board is inputted to the comparator (two tone decoder: IC403-B) which forms the squaring circuit for the decode signal. The signal is out from Pin 7 of IC403-B and fed into IC401 (MCU) where it is compared whether that is matched with a preprogrammed data or not. If matched, a valid data is decoded, which is shown by a green L.E.D. on the top panel of the SD-160 data radio and audio is released through pin 9 of DB-15 Connector. If unmatched, the busy Yellow L.E.D. would be shown.

RSSI DETECTOR

From the RF board, the RSSI (Received Signal Strength Indicator) signal flows to Pin 31 of IC401(MCU) through R513. Micro controller unit (IC401) detects received signal level using the inner 8-bit ADC(Analog to Digital Converter). The output of ADC is compared with Programmed RSSI level. If the MCU detects existence of received signal through this comparison, yellow L.E.D. is shown on the top panel of the SD-160 data radio.

EEPROM

RX / TX channel and RSSI detection level as well as other data from the programmer are stored in the EEPROM. The stored data is retained without power supply. This is a non-volatile memory and re-programmable. IC402 is an EEPROM with 4096 (8 x 512) capacity and data is able to be written and read serially.

CHANNEL SELECTOR

One of 16 channels may be selected using the Dip Switch (SW401) and serial commands. In case of hardware selector, SW401 encodes 4-bit binary code according to selected each switch's position. At this point, the binary code plus one is the channel number. The binary code is decoded by the CPU, which enables the appropriate RX or TX frequency and associated data to be selected from the EEPROM. In external serial commands, that comes from Pin 8 of DB-15 Connector (CON401) and then fed into the

Pin 41 of IC401 (MCU). Micro controller Unit uses UART (Universal asynchronous receiver transceiver) for serial communication and decodes serial commands in order to control radio.

DC TO DC CONVERTER

The main DC power is supplied to the switched mode DC to DC converter. The DC to DC converter regulates the various input power supply voltage and generates a constant voltage of 6.5volts (SD-161, SD-164) or 7.5 volts (SD-160). It is a source for all of the RF and digital circuits. The DC to DC converter is formed by IC801, Q801, Q802, L801, R804, and voltage divider (R805, R806, R802). IC801 is a kind of PWM Controller that controls pulse width of switching pulse output. Various input voltage leads to various output voltage of voltage divider. IC801 detects the voltage difference between inner reference voltage and voltage divider output and then controls the width of switching pulse in proportion to its difference. Wanted output voltage is decided by product of input voltage and duty ratio of switching pulse. As the switching pulses, Q801and Q802 switch the input DC of various supply voltages and generate the constant DC of supply voltage. Moreover, IC801 controls maximum current of DC to DC converter by current detection through voltage drop of R804.

RF CIRCUITS

PLL SYNTHESIZER

12.8 MHz TCXO

The TCXO contains the 3-stage thermistor compensation network and crystal oscillator, and modulation ports. Its compensation is ±5 PPM or less at -30℃ to +60℃.

PLL IC DUAL MODULES PRESCALER

Inputted frequency of 12.8MHz to pin 1 of IC2 MB15A02 (or MB15E03SL) is divided to 6.25kHz or 5kHz by the reference counter and then supplied to the comparator. RF signal input from VCO is divided to 1/64 at the 64/65 modulus prescaler in IC2, divided by A and N counter in IC2 to determine frequency steps, and then supplied to the comparator. PLL comparison frequency is 6.25/5kHz, so its minimum programmable frequency step is 6.25/5kHz. The A and N counter is programmed to obtain the desired frequency by serial data in the CPU. In the comparator, the phase difference between reference and VCO

signal is compared. When the phase of the reference frequency is leading, ΦP is the output, but when VCO frequency is leading, ΦR is the output. When ΦP= ΦR, output of phase detector is a very small pulse.

EXTERNAL CHARGE PUMP

This is used to increase dynamic range of VCO which is decided by supply voltage of charge pump supplied by DC to DC converter. In case of SD-160 series data radio, 0~12v is necessary to control the VCO. In addition, SD-160 series use current mode charge pump to take direct control such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation. ΦP, ΦR logic signals are converted into current pulses to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

REFERENCE FREQUENCY LPF

The Loop Filter circuit contains R9, C1, and C2. Settling time of LPF is 12mS with 1 kHz frequency, which reduces the residual side-band noise for the best signal-to-noise ratio.

DC TO DC CONVERTER

The DC to DC converter converts the 5v to 14~16v for using enough dynamic range of the VCO.

VCO

SD-160 series adopt two VCO systems for RX and TX in order to maximize each performance. TX and RX VCO generate RF carrier and local frequency and each VCO is switched by TX/RX power source. It is configured as a colpitts oscillator and connected to the buffer as a cascade, but bias circuit is cascode configuration to save power. The varicap diodes D201 and D301 are low-resistance elements and have different capacitance for a reverse bias voltage. So, using the change of reverse bias voltage (2 ~ 11V), wanted frequency for each channel can be obtained. L203 and L303 are resonant coils and C208 and C308 are used to change the control voltage by the tuning core. Modulation diode, D202, modulates the audio signal. C204 compensates the non-linearity of the VCO due to modulation diode and maintains a constant modulation regardless of frequency.

TRANSMITTER

The transmitter consists of:

1. Buffer
2. P.A. Module
3. Low Pass Filter
4. Antenna Switch
5. A.C.C. Circuits

BUFFER

Output level of VCO is about -4dBm and amplified to +10dBm or so. The buffer consists of Q9 and Q10 for reverse isolation and gain.

P.A. BLOCK

The P.A. Block uses three-stage amplifier configuration with Q501, Q502, and Q503. In case of SD-160, different amplifiers are applied compared with SD-161(4) because different output power specification is needed. Q501 amplifies the TX signal from +10dBm to 100mW and Q502 amplifies to 0.5W and Q503 amplifies to 2W(SD-161, SD-164) or 6W(SD-160) and then matched to 50 Ohms using the L.C. matching network or strip line, at the same time, its unwanted harmonics are reduced below -30dBc.

LOW PASS FILTER

L7, L8, L9, C36, C37, C38, and C39 are the 7th order Chebyshev low pass filter. Unwanted harmonics are reduced by -70dBc.

ANTENNA SWITCH

During transmitting, the diodes D3 and D5 are forward biased to make RF signal path to the antenna, in other words, D5 is shorted to ground to block the RF signal to front-end. In receive, however, the diodes, D3 and D5, are reverse biased to pass a received signal from the antenna through L10 and C61 to the front-end without signal loss.

AUTOMATIC CURRENT CONTROL (ACC) CIRCUITS

The ACC circuit consists of R63, variable resistor RV4, IC5(B), and transistors Q11 and Q12. The supplied current to P.A. block is monitored by the voltage difference on R63 (0.1 Ohm). Namely, If the

current varies by RF power output or other reasons, it produces voltage difference on R63, and then IC5A provides some bias voltage with Q15 in proportion to that difference. The adjusted output value of Q15 by RV4 is compared with reference voltage in IC5B, and then its differential voltage at the output of IC5B is applied to Q12 and Q11. By this working process, bias voltage of P.A. module maintains proper value to keep a desired and constant power output. Consequently, RV4 is used to adjust the RF power level.

RECEIVER

FRONT-END

The front-end block consists of two band pass filters and low noise amplifier (LNA). Band pass filter is used for elimination of image frequency, at the same time, impedance matching network and LNA amplifies weak RF signal without any increase of noise. The received signal from antenna inputs into a band pass filter of front-end block, composing C601 through C610, and L601 through L604 at UHF and C622 through C608, L607 through L604 at VHF, and is coupled to the base of Q601 served as an RF amplifier. Also, Diode D601 protects Q601 from static RF overload from nearby transmitters. The output of Q601 is then coupled to a second band pass filter consisting of C611 through C623 and L606 through L609 at UHF and C607 through C601, L603 through L601 at VHF. The output of front-end block is then coupled to the double balanced diode mixer, D6. Actually, Front-end block is pre-tuned at factory and no more adjustment is required

FIRST MIXER

Double balanced diode mixer which consists of D9, T1, and T2 generates the 45.1MHz intermediate frequency from RF and local frequency. The filtered frequency from the front-end module is coupled to T1 and local frequency from RX VCO is coupled to T2. The 45.1MHz IF output is matched with the input of the 2-pole monolithic filter by L12 and C66. These crystal filters provide a bandwidth of ±7.5kHz with the operating frequency for diminishing high degrees of spurious and inter-modulation distortion. Moreover, IF filter additionally attenuates image frequency level of second mixer. The output impedance of the filter is matched with the base of the post amplifier Q16 by C67 and C70.

SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post amplifier, Q16, is coupled via C71 to the input of IC6 (TA31136FN). IC6 is a

monolithic single conversion FM transceiver, containing a mixer, the second local oscillator, limiter, and quadrature detector. Crystal X1, 44.645MHz, is used to make the second IF, 455kHz signal, at second mixer in IC6. The mixer output is then routed to CF1 (455F) or CF2 (455HT) and these two ceramic filters provide the adjacent channel selectivity of 25kHz or 12.5kHz bandwidth with the filtered signal. After that, that signal is fed to limiter and then desired audio signal is obtained from limited signal at the quadrature detector.

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is output from pin 12 on IC6. This is analog DC voltage and its level varies as much as received signal strength. Low pass filter (IC4-B) filters unwanted noise of the RSSI signal and filtered signal is used for squelch system. Also, a thermistor (TH3) compensates this signal level at temperature.