F1 DSC VHF Transceiver RF Module: Circuit Description

(Corresponding circuit diagram: 84-500C)

Function
The RF module contains all the RF transmitting and receiving circuits for the radio, in addition to audio handling and amplification functions. The RF module is linked to (and is controlled by) the Audio and Control module.

Audio modulation
Audio signals, converted by the electret microphone, are pre-emphasised and level controlled by the emphasis / ALC circuit centered around U18, Q30, Q40, Q28, Q29, Q33 and Q34. Signals from front or rear microphone paths are muted (via Q31 and Q39) depending on which PTT key input (rear or front) is detected. Maximum deviation is limited to ±5kHz. The processed audio signal is then routed, via deviation adjustment potentiometer R16, to modulate the LO.

Transmitter
When the PTT key is pressed (and the transmitter frequency synthesizer is in lock), the Transmit/Receive pin-diode switch - D7/D9 is biased to block RF energy from entering the receiver stages. The carrier is generated by synthesizer (LO) U16 (this is a dual synthesizer and also serves the receiver stages). The LO output is fed via a buffer stage, providing gain, reverse isolation and filtering, and then to the PA, (comprising power module U14 and associated components). Power output is current controlled via differential amplifier U13 and Q22 which monitor potential across a low resistance in series with the PA d.c. supply. Temperature stabilization is also performed by modifying the current to the PA in response to temperature changes at R159. High (25W) and low (1W) power settings are achieved with current control via Q19, Q28, Q36, Q22 and U13. L-C harmonic filters are employed due to the class C amplification stage.

DSC modulation
DSC FSK modulation from the DAC output of the microprocessor is applied at the input of the pre-emphasis limiting circuit, adjacent to the audio path from the microphone.

Receiver
Incoming RF energy from the antenna (when the Transmit/Receive pin-diode switch - D7/D9 - is suitably biased for receiving) is passed through the antenna filter to suppress out-of-band signals. The antenna filter is designed to have a low insertion loss and comprises the L-C matching network and the SAW filters FI9, FI10 and FI11 and associated components, which form a low noise amplifier stage, and also perform signal splitting and image filtering.

The signal is split to feed the main and auxiliary (channel 70) receiver stages.

Main receiver
The main receiver comprises the mixer U12 to the first IF at 21.4MHz, and IF filters FI7/FI8, the frequency being set by main LO U16. The first IF is fed to the FM/IF stage U10 and 455kHz filter FI6 and then the demodulated audio to the de-emphasis circuit (using operational amplifiers U8). Squelch is adjusted by potentiometer R50 which sets the threshold to open squelch on the input to the comparator U8. When squelch is open, the MAIN_MUTE signal from the microprocessor U4 is made inactive.The audio signal is then routed to the audio amplifiers U19 feeding the speaker and rear audio output, via the volume control R45. The rear speaker output employs a common mode choke. Muting of either audio path is under control of the microprocessor U4 which operates the EXT_SP_EN and INT_SP_EN control signals for front and rear audio outputs. Earphone signals are routed to audio amplifier U2.

Auxiliary receiver
The signal to the auxiliary receiver (fixed receiver on channel 70) is mixed at U7 to the first IF of 10.7MHz, limited by filters FI3/FI4, and then to another FM/IF stage U6 and 455kHz filter FI2. Demodulated audio (DSC tones) is de-emphasised in the circuit comprising operational amplifiers U5 and associated components. The DSC signal is compared at U5 to produce a signal AUX_BUSY when the DSC channel is busy. The DSC signal is fed to U4 where it is sampled by the internal ADC. A demodulation / decoding algorithm is then applied to recover the DSC information, which is accumulated to extract messages.

Power supply
DC (10.8V to 15.6V) is routed from the rear connector via a common mode choke, fuse and reverse protection zener diode to the FET power switch (Q3). This transistor is set to a ‘on’ or ‘off’ state when the latch formed by Q4, Q35, C3 and related components is pulsed (by pushing the front panel power key). The operational, power and audio amplifiers are supplied with decoupled +12V, and the RF ICs are supplied with either 8V or 3.3V. Logic ICs are supplied with 5V. Regulators U4 and U23 provide the 8 and 5V supplies respectively, while Q24 sources 3.3V to the dual synthesizer U16.

External data signal conditioning
NMEA data (GPS), in balanced / differential form, is routed, via limiting circuitry, to an opto-coupler U1. The ground referenced NMEA signal is then detected by the microprocessor.

RS485
RS485 level translation,and bi-directional interface capability is achieved by means of U22.

Data control
Serial data from the processor for programming the synthesizer is routed directly to the synthesizer serial data inputs. Other RF module-state serial control signals are latched at shift registers U2 and U3 and output in parallel format.