MCMURDO G4 406 GPS EPIRB

FCC ID: KLS-82-501

CIRCUIT DESCRIPTION

The G4 EPIRB is powered by three 3V3 Lithium Manganese Dioxide batteries connected in series, which gives a nominal operating voltage of 9.4V. The battery pack is protected by a 4A PTC. The battery pack is designed to last for at least 48hours at –20 deg C and be capable of supplying 1.8A pulses every 50 seconds.

Refer to drawing 82-560C

ACTIVATION

The EPIRB is activated by energising Q13, this can be done by either pressing the ON membrane switch, the HOLD TO TEST membrane switch, or via the seawater switch contacts.

The seawater switch operates when the resistance across the contacts is less then 47K ohms. This allows IC9d output to switch high. IC9c will switch low after a delay of 3 to 7 seconds due to the time constant formed by R65 and C55. This enables D14 to conduct and Q13 to turn on. In this state, the unit may only be turned off by removal from water. C55 will discharge through R78 causing Q10 to switch off after a delay of 3 to 7 seconds.

The combination of IC9a and IC9b form a set-reset bistable. When the ON membrane switch is pressed, the output of IC9b switches low and is latched by IC9c switching low. D5 conducts, turning Q13 on. In this state the latch may only be reset by pressing the HOLD TO TEST switch.

When the HOLD TO TEST membrane switch is pressed and held, D6 conducts allowing Q13 to turn on. The TST line to the microcontroller will also be pulled low via D3, causing the self-test routine to be initiated.

Self Test

1) The ON LED illuminates.
2) The LCK line is checked to ensure that the PLL is locked.
3) After 7 seconds a 406MHz test message is made. The output of the RF detector is checked to ensure the correct power level.
4) The 121.5MHz homer performs three sweeps. The output of the RF detector is checked to ensure the correct power level.

5) The GPS module is powered up and the output data is checked to be the correct NMEA protocol.
6) If the levels and protocol are correct, the strobe flashes three times to indicate correct performance.

MICRO-CONTROLLER

The G4 EPIRB is controlled by IC1, an 8-bit microcontroller, with internal EEPROM. The microcontroller is responsible for all board operations. The microcontroller is powered by a 3V4 regulator, IC3, and run by 4MHz crystal X2. The micro-controller may be programmed during self-test with the data to be encoded in the 406 message. Data is input to the RX line from an infrared photodiode Q11, and stored in EEPROM. In operational mode the micro-controller provides the following control signals:

1) Every 2.6 seconds pulses the strobe trigger line high to flash the strobe
2) Flashes a red LED every 2.6 seconds to indicate normal operation.
3) Sets the PLL line high to enable the 121.5 MHz oscillator.
4) Generates frequency swept square waves on the MOD line to modulate the 121.5MHz transmission.
5) Every 50 seconds makes a 406MHz transmission.
6) Sets the PLL line low to enable the PLL and VCO circuits.
7) Loads division ratio data to the PLL via the LAT, DAT and CLK lines.
8) Sets the PA line high to enable the 406MHz PA.
9) Holds the DAT and CLK lines static for 160ms to generate unmodulated carrier.
10) Pulses the DAT and CLK lines for 360ms to phase modulate the carrier with encoded data.
11) Turns the GPS regulator, IC11, on for 5 minutes when initially activated and thereafter for 2 minutes every 20 minutes.
12) Accepts serial NMEA format data from the GPS module and encodes valid position data into the 406MHz message.
13) Flashes a green LED every 2.6 seconds when valid GPS data has been received.

STROBE CIRCUIT

Q15, T1 and C54 form an astable oscillator, running at 8KHz to 15KHz. The output waveform of the secondary of T1 is rectified by D8 to 300V and clamped at 270V by D11. Capacitors C69 and C70 are thus charged to 270V (and so is C68 via R79). The strobe trigger line is pulsed high for 2us every 2.6 seconds, forceing SCR1 to conduct. This causes C68 to discharge through the primary of T2, which generates a 3KV voltage across the Xenon tube, which causes the strobe to flash. Once C69 and C70 are discharged, the charging cycle repeats until clamped by D11.

121.5MHz TRANSMITTER

The transistor Q4 forms part of a modified crystal controlled Colpitts oscillator, IC6 is a programmable regulator which supplies the oscillator with a regulated 5V supply. The oscillator is switched on and off by the microcontroller via D1 and R7.
FET Q5 is a modulator/buffer. Amplitude modulation of the 121.5MHz signal is generated by the microcontroller. Modulation is in the form of a square wave, swept down from 1300Hz to 600Hz, with a duty cycle of 41%. The FET modulator/buffer produces an output power of 8dBm that drives the power amplifier Q8.
The power amplifier is operated in Class C mode and produces an output of 20dBm. The output of the power amplifier is fed to a diplexer. The diplexer acts to combine the 121.5MHz signal with the 406MHz signal which is then output to the antenna via the antenna tuning unit (A.T.U).
The 121.5MHz output power level is detected and converted to a DC level by the network C67, L15 and D9. This level is monitored during the self-test sequence to confirm the correct operation of the 121.5MHz circuit.

406MHz TRANSMITTER

During normal operation of the G4 EPIRB, all 406MHz circuitry, except for the 5V supply to the ovened oscillator OSC1, is shut down. The 406MHz transmission sequence starts when pin 8 of IC1 switches LOW. This enables regulator IC4, powering the 406MHz synthesiser and VCO circuits.
A short time later, the 406MHz PA is enabled by pin 1 of the microcontroller switching high. At the end of the 520ms transmission, the PA, synthesiser and VCO circuits are shut down.

406MHz synthesiser

The 406MHz phase locked loop comprises of a high performance programmable synthesiser, IC2, and a discrete VCO, (Q6 and associated components). Internal frequency division ratios are programmed into the synthesiser via the LAT, DAT and CLK lines which are output from the microcontroller.
OSC1 is used as the reference oscillator for the phase locked loop. This is an ovened oscillator with high phase stability characteristics. It is powered continually to maintain the internal reference crystal at a near constant temperature. This runs at 12.688375MHz and is divided down by 6 within the synthesiser to set the internal reference comparison frequency to 2.1147292MHz. A portion of the VCO output is applied to the input of the PLL prescaler at pin 8 of IC2. After appropriate division, the frequency is compared to the internal reference frequency. Deviation from the reference will result in a change in voltage at the charge-pump output at pin 5. This voltage is applied to

a varactor diode in the VCO and will drive the VCO to the correct frequency. Phase lock is indicated by Q1 being turned on and applying a logic high signal to the LCK input on the microcontroller.

The VCO is based on a modified Clapp oscillator configuration. The oscillation frequency determining network is formed by D2, C19, C20, C22 and TL1, a strip-line inductor. Variable capacitor C20 is adjusted to centre the varactor drive voltage at mid-rail. Frequency control is then achieved by the synthesiser applying a correction voltage to varactor diode D2. The nominal tuning range of the VCO is 380MHz to 420 MHz for a control voltage swing of 3.5V.

Q2 and associated components act as a phase modulator. By drawing additional current from the synthesiser charge pump output, the relative phase of the 406MHz signal is shifted. The LAT and DAT lines from the microcontroller output the encoded message data to Q2 via the scaling network R8, 9, 49, 80 and VR1. The resultant base drive voltage will result in current being drawn from the charge-pump output thus phase modulating the 406MHz signal. The magnitude of the peak modulation is adjustable by VR1.This is adjusted for a nominal modulation of $\pm$ 1.1 radians. Diodes D13 and D14 act to provide temperature compensation for the modulator over the range -20 C to +55 C.

406MHz Power Amplifier

The VCO output is buffered by pad R32, 33 and 37, and provides a drive of 0dBm to Q7. Q7 generates 12dBm drive at the power amplifier module input. The PA is turned on by the PA line switching high. This turns Q9 and 10 on, which switch on Q14, applying 9.4V to the PA DC supply input.
The PA output power is set by adjustment of VR2 which varies the output of regulator IC7, which provides the bias voltage to the PA module. The output level of the PA is set to 37dBm $\pm$ 0.2dB.
The 406MHz signal is then fed to a diplexer, then to the antenna via the antenna tuning unit (A.T.U). The 406MHz output power level is detected and converted to a D.C. level by network C67, L15 and D9. This level is monitored during the self-test sequence to confirm the correct operation of the 406MHz circuit.
Q9, 10 and 14 also act as a shut down circuit that monitors the power amplifier to limit the duration of a 406MHz transmission. The switched supply rail to the power amplifier is fed to the base of Q9 via the time constant formed by R56 and C78. If the power amplifier is on for typically 5 seconds, sufficient voltage will be developed across C78 to turn on. This will result in Q10 and Q14 switching off thus removing the DC supply to the power amplifier.

Antenna Tuning Unit

The network comprising L17, 18 and 15 with C73, 75, 83 and 84 match the 50 ohm output from the diplexer to the antenna impedance at both 121.5 and 406MHz.

GPS FUNCTIONS

GPS antenna and LNA

Signals from the GPS satellites are received by a 18mm square dielectric patch antenna which is mounted directly on the strobe board. The patch is resonant at the L1 band centre of 1.57542GHz and provides about 3dBi of gain. The output of the patch antenna is fed to the input of LNA IC12, which is mounted on the opposite side of the strobe board under the patch. This stage provides a further 13dB of gain. The output is fed to the input of the GPS module via a miniature coaxial cable, which also acts to feed the supply voltage for the LNA from the GPS module.

GPS module

The GPS module is mounted on a daughter board secured to the rear of the synthesiser board by stand off pillars.
Power to the GPS module is provided by regulator IC11 which provides a nominal 3V3 at 150mA. The regulator is switched on and off by the microcontroller as position updates are only required every 20 minutes.
NMEA format $GGA data is output from the module to the microcontroller UART input. This message contains the position data, the number of satellites used to calculate the position,HDOP and acquisition quality bit.
If the quality bit is set to ‘1’ and the HDOP figure is less then ‘4’, the position data is encoded into the relevant field of the 406MHz message, and transmitted in the next message transmission. (The GPS regulator is then turned off for 20 minutes). If these criteria are not met, default position data is transmitted.