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Thundercomm TurboX C40x SOM

Datasheet

Trande name:TurboX, Model: TurboX C405-D

Rev. V2.3.2
Jun 01, 2022

DN: tc-i-13123.2

Revision History

Version	Date	Description
V0.1	2019-11-01	Initial release.
V0.2	2020-02-01	• Add TurboX C405 information and updated SOM pin definitions. • Add descriptions of HDMI, MIPI DSI, DECAP, Sleep Clock and SPMI interfaces.
V0.3	2020-02-06	• SOM marking 5-3 • Content for Figures and Tables
V0.5	2020-02-20	Update 3.16.2 BT Performance
V0.6	2020-02-26	Update 3.16.2 BT Performance
V0.7	2020-03-16	Update in 5.2 Package dimensions
V0.8	2020-03-27	Update SDC2 performance description
V0.9	2020-09-16	Correct the description error of the Bluetooth version.
V1.0	2020-10-15	• Add C403 information. • Update the pin definition of SOM.
V1.1	2020-11-23	Fix the inconsistency of LDO output current description, such as LDO6 and LDO7.
V1.2	2020-12-29	Delete the description about FM.
V1.3	2021-01-14	Delete the description about BT2.
V1.4	2021-03-02	Update current consumption data.
V1.5	2021-03-10	• Add certification information. • Delete the RF Performance.
V1.6	2021-03-24	Add the 3.16. RF Performance.
V1.7	2021-04-13	Add FCC test information.
V1.8	2021-04-22	Update Table 1-3 by adding a configuration selection.
V1.9	2021-06-09	Add comment for SPDIF_RX_COAX_EP, the configuration of the SOM as QCS403 is not supported.
V2.0	2021-08-11	• Update Figure 1-1 and Table 2-26. • Add 1.7.Stencil design and aperture.
V2.1	2021-08-20	Update Figure 1-1.
V2.2	2021-11-08	• Change the total amount of pins from 287 to 281 in Chapter 1. Overview. • Update Table 1-1. Key features and performance of TurboX C40x SOM. • Remove ***Section 1.3. Major component location***. • Update Table 2-3. Power supply definition. • Update Table 2-20. Sensor interrupt definition. • Add a note below Table 2-26. Antenna interface definition. • Remove ***Appendix 1 Compliance and Certificate Information***.

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Version	Date	Description
V2.3	2022-01-27	• Update 1.5. SOM ID. • Modify description of USB0_HS_DM and USB0_HS_DP in Table 2-10. USB interface definition.
V2.3.1	2022-04-20	• Remove weight information from Chapter 1. Overview. • Add a note in 1.6. Module laser marking. • Add new section 1.7. SMT assembly guide. • Update function description for C27, D5 and D6 in Table 2-2. Pin List. • Update GND pin location in Table 2-3. Power supply definition. • Update description in 2.3.10 SDIO interface. • Remove TX, RX, CTS_N and RFR_N from description of BLSP Number 4 in Table 2-16. BLSP interface-1 definition. • Update Table 2-19. • Remove the note in 3.2. Operating conditions. • Fix format problems.
V2.3.2	2022-06-01	• Update 1.6. Module laser marking. • Add a note in 3.2. Operating conditions. • Add Table 3-3. • Fix format problems.

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Table List

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- Illustrations in this documentation might look different from your product and are thus for reference only
- Depending on the model, some optional accessories, features, and software programs might not be available on your device.
- Depending on the version of operating systems and programs, some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice. Thundercomm makes constant improvements on the documentation of the products, including this guidebook.

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Chapter 1. Overview

TurboX C40x is a high-level performance intelligent module, integrating Linux system, based on Qualcomm QCS40x processor. It includes a 64-bit Arm Cortex-A53 qual-core (dual-core for C403) 1.4 GHz application processor, two Qualcomm® Hexagon™ QDSP6 v66 with Low Power Island and Voice accelerators.

➲ **NOTE:** "TurboX" referred to herein is the English text of our registered trademark TURBOX.

TurboX C40x integrated 2 × 2 WCN3999 (or 1 × 1 WCN3980) WLAN 802.11 a/b/g/n/ac, Bluetooth v5.x specification.

TurboX C40x provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, SOM common standard protocol interfaces such as USB3.0, USB2.0, SPI, RGMII, I2S and SLIMBUS.

TurboX C40x provide convenient and stable system software solution for use in the Smart Speaker and Sound bar markets.

The size of TurboX C40x module is 33.8mm*33.8mm*2.6mm, with 281 pins.

1.1. Key features

Table 1-1. Key features and performance of TurboX C40x SOM

Processors	
Applications Processor	Arm Cortex-A53 microprocessor cores, 64-bit processor, Quad-core (Dual-core for C403) 1.4 GHz.
Digital signal processing	Two Qualcomm® Hexagon™ QDSP6 v66 with Low Power Island and Voice accelerators.
Operating System	LE (Linux Enablement): QCS40X_2020.SPF.1.2.
Memory	• eMCP,8GB eMMC5.1 + 8Gb LPDDR3. • eMCP,4GB eMMC + LPDDR3 512MB (for C403 only).
Multimedia	
Display	• **TurboX C404 and TurboX C403:** General display interfaces: not supported. • **TurboX C405:** General display interfaces: One 4-lane MIPI DSI ports, DSI support up to 720P, HDMI support up to 1080p 30FPS. Graphics: Adreno 306 at 600 MHz
Audio	
Audio	MP3, AAC, ALAC, FLAC, He-AAC v1/v2, WMA 9/Pro, Dolby Digital, Dolby Digital Plus, Dolby TruHD, DTS:X ➲ **NOTE:** Dolby is supported on C405-D only.

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Wireless connectivity	
WLAN	• 2.4G/5G, support 802.11 a/b/g/n/ac • Support SoAP mode
Bluetooth	• Support Bluetooth 5.x + HS • BLE • Backwards compatible with Bluetooth 1.2, 2.X + enhanced data rate.
Connectivity	
USB	One USB 2.0 high-speed and one USB 3.0 super-speed.
PCIe	1x PCIe, PCIe v2 PHY and 2.1 controller.
Ethernet RGMI	1x Ethernet RGMII.
SDIO	• 4-bit, SD 3.0. • SDC2 is Dual-V. • SD/MMC card, eMMC NAND, eSD/eMMC boot.
BLSP	Can be configured as 2x SPI or 3x I2C or 5x UART.
UART	Up to 4 MHz
I2C	Sensors etc.
SPI	Sensors etc.
SLIMbus	One, highly multiplexed, high-speed, baseline WCD9335.
MI2S	• Full duplex stereo or up to quad channel TX/Rx MI2S (x1). • Up to 2 channels for multi-channel audio applications (x1).
PCM	Short and long sync PCM support.
Sleep Clock	32.768 KHz sleep clock output.
SPMI	Dedicated power management interface for external charging system.
GPIOs	10+ general GPIO, LPI GPIO and PM GPIO ports.
Others	
ADC Interface	• Support ADC interface. • Used for input voltage sense, battery temperature detection and general-purpose ADC.
Touchscreen support	Capacitive panels via exit IC (I2C, SPI, and interrupts).
Physical size	• Size: 33.8mm x 33.8mm x 2.6mm. • Weight: approx. 6.8g.
Operating temperature	-20°C ~ +70°C
RoHS	All hardware components are fully compliant with EU RoHS directive.

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1.2. Hardware block diagram

N/A.

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1.3. Mechanical size

Size: 33.8mm x 33.8mm x 2.6mm

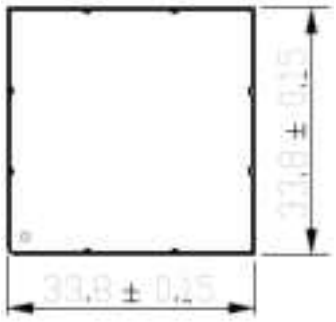

Figure 1-2. Top View

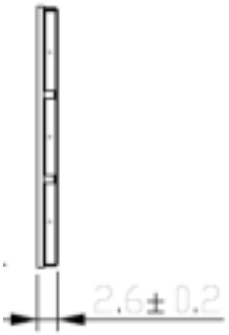

Figure 1-3. Side View

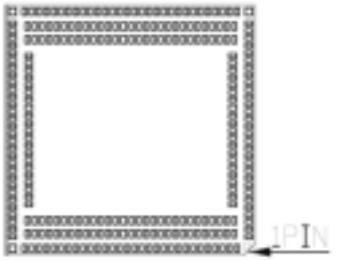

Figure 1-4. Bottom View

1.4. Package dimensions

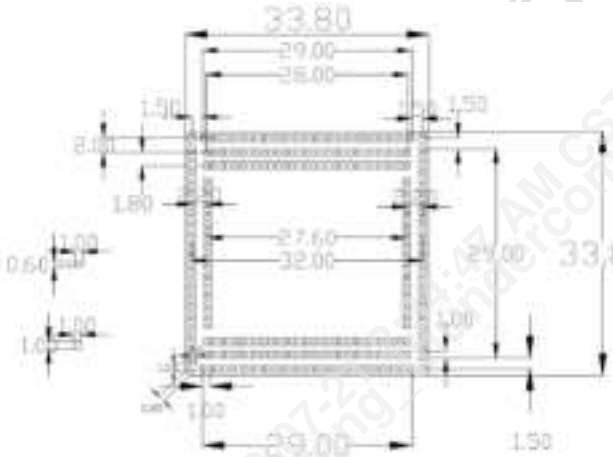

Figure 1-5. Package Dimensions (Top View)

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1.5. Stencil design and aperture

To supply sufficient soldering paste and keep reliable soldering joints, add the thickness of stencil partly on the top surface. The stencil aperture for single sheet cannot be greater than 3.0mm×4.0mm and the exceeded part should be divided into smaller apertures with applicable shelves. A clearance of over 2.0mm should be kept between the outward end of the aperture and the component if there are components around the module.

➲ **NOTE**:

- For the convenience of heating and repairing, it is recommended that no components should be placed in the area at the backside of the module on PCB.
- In order to avoid reverse polarity of the module, it is recommended to use asymmetric pads at the bottom of the module to identify the module polarity during module placement.
- It is not recommended to add any silkscreen in the area where the module is mounted to avoid the height that may influence the solder paste printing and soldering quality.
- When there is a need to step-up the stencil, all 01005/0201, 0.4mm-pitch and 0.5mm-pitch components should be kept over 5.0mm away from the stepped-up area to avoid solder bridging that is caused by thicker solder paste.

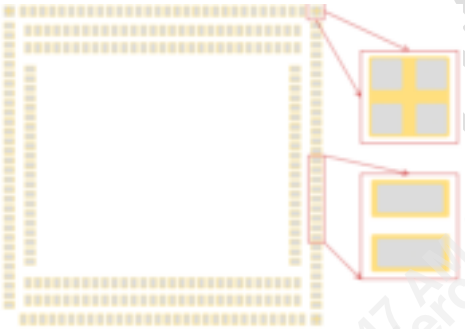

Figure 1-6. Stencil Aperture

- **Stencil thickness**

  Area of the module should be partly stepped-up to 0.15mm-0.18mm.
- **Pads on four sides**

  The aperture for each single pad should be centered with area reduced to 75%-85%. And the shape should be rectangle with round chamfers (see Figure 1-6).
- **Pads at four corners**

  The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-6).

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1.6. Module laser marking

Figure 1-7. C40x SOM Module Laser Marking

Table 1-2. Module laser marking description

1. Company name/logo	5. Product number
2. SOM brand: TurboX	6. Serial number
3. PCBA version	7. Eco-mark
4. Certificate information	8. QR code

➲ **NOTE**:

- Figure 1-7 is for reference only and may vary with the specific module.
- Descriptoin of PCBA version "Qxx –xx-SKUx":
  - Qxx: Project number
  - Xx: PCB version
  - SKUx: specific configuration. For more information on configuration, refer to the table below.

Table 1-3. TurboX C40x configuration

SOC	SKU	Meomry	WCN	Q'ty of Antennas	TPN (Thundercomm Product No.)	Model
QCS405	Q29-SKU1	1GB+8GB	WCN3999	3	C405-E18-369PW03	C405
QCS404	Q29-SKU3	1GB+8GB	WCN3999	2	C404-E18-369PW02	C404
QCS405-2	Q29-SKU4	1GB+8GB	WCN3999	3	C405-D-E18-369PW03	C405-D
QCS405-2	Q29-SKU7	1GB+8GB	WCN3999	2	C405-D-E18-369PWX2	C405-D
QCS404	Q29-SKU9	1GB+8GB	WCN3999	3	C404-E18-369PW03	C404

1.7. SMT assembly guide

Refer to *TurboX Common SMT Assembly Guidelines.*

For more information, please contact us at service@thundercomm.com.

Chapter 2. Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on TurboX C40x SOM module.

2.1. Interfaces parameter definitions

Table 2-1. Interfaces parameter definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DSI	Supply voltage for MIPI_DSI I/Os; tied to VDD_MIPI (1.2 V only)
DO	Digital output (CMOS)
H	High-voltage tolerant
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3，it is 1.8V.
P2	SDC Power group 2，it is 1.8V or 2.95V.
P12	SSC Power group 12，it is 1.8V.
V_Internal	Internally generated supply voltage for some power-on circuits
V_Config	Software configurable (3.6V or 1.8V)

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2.2. Pin description

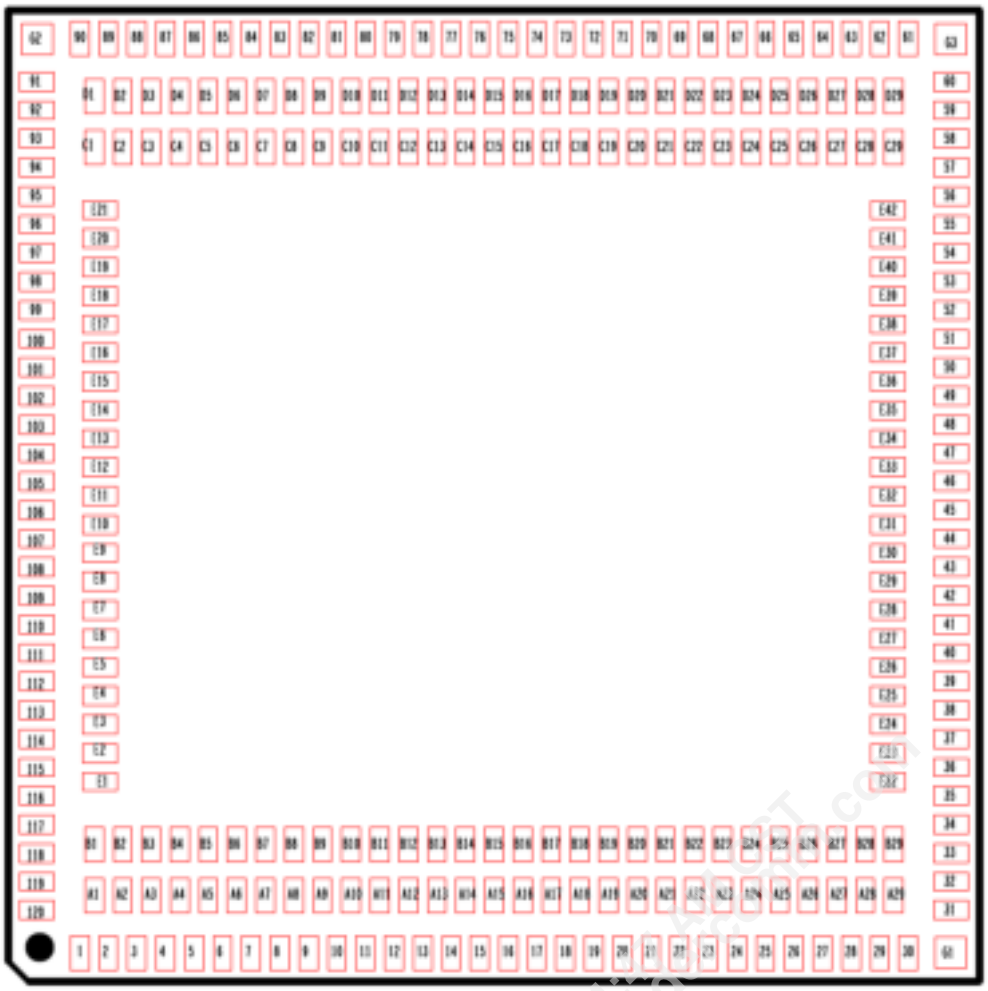

Figure 2-1 TurboX C40x PIN Map (Top View)

Table 2-2. Pin List

Pad#	Function	Voltage	Type	Function description
1	MIPI_DSI0_CLK_M	-	-	MIPI display serial interface 0 clock negative. For TurboX C404 and C403: do not connect.
2	MIPI_DSI0_CLK_P	-	-	MIPI display serial interface 0 clock positive. For TurboX C404 and C403: do not connect.
3	GND	-	-	-
4	MIPI_DSI0_L2_M	-	-	MIPI display serial interface 0 lane 2 negative For TurboX C404 and C403: do not connect.
5	MIPI_DSI0_L2_P	-	-	MIPI display serial interface 0 lane 2 positive. For TurboX C404 and C403: do not connect.
6	GND	-	-	-
7	MIPI_DSI0_L3_M	-	-	MIPI display serial interface 0 lane 3 negative For TurboX C404 and C403: do not connect.
8	MIPI_DSI0_L3_P	-	-	MIPI display serial interface 0 lane 3 positive. For TurboX C404 and C403: do not connect.
9	GND	-	-	-
10	PCIE0_TX_P	-	DO	PCIE transmitter plus
11	PCIE0_TX_M	-	DO	PCIE transmitter minus
12	GND	-	-	-
13	USB0_HS_DM	-	IO	USB0 HS data minus
14	USB0_HS_DP	-	IO	USB0 HS data plus
15	GND	-	-	-
16	GPIO_35	1.8V	IO	Can be configured as GPIO

Pad#	Function	Voltage	Type	Function description
17	GPIO_34	1.8V	IO	Can be configured as GPIO
18	GND	-	-	-
19	SPDIF_RX_COAX_RCA	-	DI	SPDIF receive port for electrical input
20	SPDIF_RX_COAX_EP	-	DI	SPDIF receive port for optical input
21	GND	-	-	-
22	GPIO_26	1.8V	IO	Can be configured as GPIO
23	GPIO_27	1.8V	IO	Can be configured as GPIO
24	GPIO_28	1.8V	IO	Can be configured as GPIO
25	GPIO_29	1.8V	IO	Can be configured as GPIO
26	GND	-	-	-
27	GPIO_39	1.8V	IO	Can be configured as GPIO
28	GPIO_40	1.8V	IO	Can be configured as GPIO
29	GPIO_41	1.8V	IO	Can be configured as GPIO
30	GPIO_42	1.8V	IO	Can be configured as GPIO
31	GND	-	-	-
32	LPI_GPIO_1	1.8V	IO	Can be configured as GPIO
33	LPI_GPIO_2	1.8V	IO	Can be configured as GPIO
34	LPI_GPIO_3	1.8V	IO	Can be configured as GPIO
35	LPI_GPIO_4	1.8V	IO	Can be configured as GPIO
36	GND	-	-	-
37	LPI_GPIO_15	1.8V	IO	Can be configured as GPIO
38	LPI_GPIO_14	1.8V	IO	Can be configured as GPIO
39	LPI_GPIO_13	1.8V	IO	Can be configured as GPIO
40	LPI_GPIO_12	1.8V	IO	Can be configured as GPIO
41	LPI_GPIO_11	1.8V	IO	Can be configured as GPIO
42	GND	-	-	-
43	GPIO_97	1.8V	IO	Can be configured as GPIO
44	GPIO_98	1.8V	IO	Can be configured as GPIO
45	GPIO_99	1.8V	IO	Can be configured as GPIO
46	GPIO_100	1.8V	IO	Can be configured as GPIO
47	GPIO_101	1.8V	IO	Can be configured as GPIO
48	GPIO_102	1.8V	IO	Can be configured as GPIO
49	GND	-	-	-
50	ANT_WL_Chain 1	-	RF IO	Antenna port for WCN3999 TX/Rx chain 1
51	GND	-	-	-
52	GND	-	-	-
53	NC	-	-	Do not connect
54	GND	-	-	-
55	GND	-	-	-
56	ANT_BT	-	RF IO	Antenna port for BT standalone
57	GND	-	-	-
58	GND	-	-	-
59	ANT_WL_Chain 0	-	RF IO	Antenna port for WCN3999 and WCN3980 Tx/Rx chain 0 (Wi-Fi only when BT standalone)
60	GND	-	-	-
61	GND	-	-	-
62	GND	-	-	-
63	GND	-	-	-

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Pad#	Function	Voltage	Type	Function description
64	GPIO_30	1.8V	IO	Can be configured as GPIO
65	GPIO_31	1.8V	IO	Can be configured as GPIO
66	GPIO_32	1.8V	IO	Can be configured as GPIO
67	GPIO_33	1.8V	IO	Can be configured as GPIO
68	GND	-	-	-
69	GPIO_37	1.8V	IO	Can be configured as GPIO
70	GPIO_38	1.8V	IO	Can be configured as GPIO
71	GND	-	-	-
72	GND	-	-	-
73	GND	-	-	-
74	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
75	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
76	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
77	GND	-	-	-
78	GND	-	-	-
79	GND	-	-	-
80	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
81	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
82	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
83	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
84	GND	-	-	-
85	GND	-	-	-
86	GND	-	-	-
87	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
88	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
89	VPH_PWR	3.8V	PI	Power supply input for SOM all operations.
90	VREG_L6_1P8	1.8V	PO	Low voltage switch supply output 1.8V for IO and pull up voltage;
91	GPIO_116	1.8V	IO	Can be configured as GPIO
92	GPIO_115	1.8V	IO	Can be configured as GPIO
93	GPIO_114	1.8V	IO	Can be configured as GPIO
94	GPIO_113	1.8V	IO	Can be configured as GPIO
95	GPIO_112	1.8V	IO	Can be configured as GPIO
96	GPIO_111	1.8V	IO	Can be configured as GPIO
97	GPIO_110	1.8V	IO	Can be configured as GPIO
98	LPI_GPIO_18	1.8V	IO	Can be configured as GPIO
99	LPI_GPIO_19	1.8V	IO	Can be configured as GPIO
100	GND	-	-	-
101	GPIO_96	1.8V	IO	Can be configured as GPIO
102	GPIO_95	1.8V	IO	Can be configured as GPIO
103	GPIO_94	1.8V	IO	Can be configured as GPIO
104	GPIO_93	1.8V	IO	Can be configured as GPIO
105	GPIO_92	1.8V	IO	Can be configured as GPIO
106	GPIO_91	1.8V	IO	Can be configured as GPIO
107	GPIO_90	1.8V	IO	Can be configured as GPIO
108	GPIO_89	1.8V	IO	Can be configured as GPIO
109	GPIO_88	1.8V	IO	Can be configured as GPIO
110	GPIO_87	1.8V	IO	Can be configured as GPIO
111	GND	-	-	-

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Pad#	Function	Voltage	Type	Function description
112	GPIO_43	1.8V	IO	Can be configured as GPIO
113	GPIO_44	1.8V	IO	Can be configured as GPIO
114	GPIO_45	1.8V	IO	Can be configured as GPIO
115	GPIO_46	1.8V	IO	Can be configured as GPIO
116	GND	-	-	-
117	GPIO_50	1.8V	IO	Can be configured as GPIO
118	GPIO_49	1.8V	IO	Can be configured as GPIO
119	GPIO_48	1.8V	IO	Can be configured as GPIO
120	GPIO_47	1.8V	IO	Can be configured as GPIO
A1	MIPI_DSI0_L0_P	-	-	MIPI display serial interface 0 lane 0 positive. For TurboX C404 and C403: do not connect.
A2	MIPI_DSI0_L1_P	-	-	MIPI display serial interface 0 lane 1 positive. For TurboX C404 and C403: do not connect.
A3	GND	-	-	-
A4	PCIE0_REFCLK_M	-	-	PCIE reference clock output (-)
A5	HDMI_TX2_P	-	-	HDMI TMDS data 2 positive. For TurboX C404 and C403: do not connect.
A6	HDMI_TX1_P	-	-	HDMI TMDS data 1 positive. For TurboX C404 and C403 do not connect.
A7	HDMI_TCLK_P	-	-	HDMI clock positive. For TurboX C404 and C403 do not connect.
A8	HDMI_TX0_P	-	-	HDMI TMDS data 0 positive. For TurboX C404 and C403 do not connect.
A9	PCIE0_RX_M	-	DI	PCIE receiver minus
A10	USB_SS_TX_M	-	DO	USB 3.0 transmitter differential pair minus
A11	USB_SS_RX_P	-	DI	USB 3.0 receiver differential pair plus
A12	USB1_HS_DP	-	IO	USB1 HS data plus
A13	GND	-	-	-
A14	SDC2_CLK	SDC2	IO	Secure digital controller 2 clock
A15	SDC2_DATA_1	SDC2	IO	Secure digital controller 2 data bit 1
A16	SDC2_DATA_3	SDC2	IO	Secure digital controller 2 data bit 3
A17	GND	-	-	-
A18	GPIO_14	1.8V	IO	Can be configured as GPIO
A19	GPIO_16	1.8V	IO	Can be configured as GPIO
A20	USB1_HS_ID	1.8V	DI	USB1 ID Pin
A21	GPIO_21	1.8V	IO	Can be configured as GPIO
A22	GND	-	-	-
A23	GND	-	-	-
A24	GND	-	-	-
A25	GPIO_52	1.8V	IO	Can be configured as GPIO
A26	GPIO_54	1.8V	IO	Can be configured as GPIO
A27	GPIO_56	1.8V	IO	Can be configured as GPIO
A28	GPIO_58	1.8V	IO	Can be configured as GPIO
A29	GND	-	-	-
B1	MIPI_DSI0_L0_M	-	-	MIPI display serial interface 0 lane 0 negative For TurboX C404 and C403: do not connect.
B2	MIPI_DSI0_L1_M	-	-	MIPI display serial interface 0 lane 1 negative For TurboX C404 and C403: do not connect.
B3	GND	-	-	-
B4	PCIE0_REFCLK_P	-	-	PCIE reference clock output (+)
B5	HDMI_TX2_M	-	-	HDMI TMDS data 2 negative. For TurboX C404 and C430: do not connect.
B6	HDMI_TX1_M	-	-	HDMI TMDS data 1 negative. For TurboX C404 and C430: do not connect.

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Pad#	Function	Voltage	Type	Function description
B7	HDMI_TCLK_M	-	-	HDMI clock negative. For TurboX C404 and C430 do not connect.
B8	HDMI_TX0_M	-	-	HDMI TMDS data 0 negative. For TurboX C404 and C430: do not connect.
B9	PCIE0_RX_P	-	DI	PCIE receiver plus
B10	USB_SS_TX_P	-	DO	USB 3.0 transmitter differential pair plus
B11	USB_SS_RX_M	-	DI	USB 3.0 receiver differential pair minus
B12	USB1_HS_DM	-	IO	USB1 HS data minus
B13	GND	-	-	-
B14	SDC2_DATA_2	SDC2	IO	Secure digital controller 2 data bit 2
B15	SDC2_DATA_0	SDC2	IO	Secure digital controller 2 data bit 0
B16	SDC2_CMD	SDC2	IO	Secure digital controller 2 command
B17	GND	-	-	-
B18	GPIO_15	1.8V	IO	Can be configured as GPIO
B19	GND	-	-	-
B20	USB0_HS_ID	1.8V	DI	USB0 ID Pin
B21	GND	-	-	-
B22	QCS_RESOUT_N	1.8V	DO	QCS reset output (active low)
B23	GND	-	-	-
B24	GPIO_51	1.8V	IO	Can be configured as GPIO
B25	GPIO_53	1.8V	IO	Can be configured as GPIO
B26	GPIO_55	1.8V	IO	Can be configured as GPIO
B27	GPIO_57	1.8V	IO	Can be configured as GPIO
B28	GPIO_59	1.8V	IO	Can be configured as GPIO
B29	GPIO_119	1.8V	IO	Can be configured as GPIO
C1	PON_1	V_Internal	DI	Level-high triggered power-on input (keep high)
C2	QCS_RESIN_N	1.8V	DI	System reset input for JTAG debugging
C3	WCD_MCLK	1.8V	DO	Audio reference clock output for Qualcomm audio codec
C4	PM_GPIO_06	1.8V	IO	PMS405 GPIO, and can be configured as GPIO
C5	PM_RESIN_N	1.8V	DI	Power management reset in (active low)
C6	KPDPWR_N	V_Internal	DI	Power-on trigger, level trigger (active low)
C7	PM_GPIO_04	1.8V	IO	PMS405 GPIO, and can be configured as GPIO
C8	NC	-	-	Do not connect
C9	GND	-	-	-
C10	VREG_L11_SDC2	SDC2	PO	Power output for SD card pull up voltage;
C11	VREG_L13_3P3	3.3V	PO	3.3V LDO power output,100mA
C12	GND	-	-	-
C13	GPIO_61	1.8V	IO	Can be configured as GPIO
C14	GPIO_63	1.8V	IO	Can be configured as GPIO
C15	GPIO_65	1.8V	IO	Can be configured as GPIO
C16	GPIO_67	1.8V	IO	Can be configured as GPIO
C17	GND	-	-	-
C18	GPIO_70	1.8V	IO	Can be configured as GPIO
C19	GPIO_72	1.8V	IO	Can be configured as GPIO
C20	GPIO_74	1.8V	IO	Can be configured as GPIO
C21	GPIO_76	1.8V	IO	Can be configured as GPIO
C22	GND	-	-	-
C23	GPIO_22	1.8V	IO	Can be configured as GPIO
C24	GPIO_24	1.8V	IO	Can be configured as GPIO

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Pad#	Function	Voltage	Type	Function description
C25	GND	-	-	-
C26	GPIO_17	1.8V	DO	MSM_UART_TX
C27	GPIO_19	1.8V	IO	Can be configured as GPIO
C28	GND	-	-	-
C29	GPIO_118	1.8V	IO	Can be configured as GPIO
D1	PA_THERM1	-	AI	ADC for external temperature sensor
D2	SLEEP_CLK	1.8V	DO	32.7 KHZ sleep clock output
D3	PM_GPIO_12	V_Config	IO	PMS405 GPIO, and can be configured as GPIO
D4	PM_GPIO_03	V_Config	IO	PMS405 GPIO, and can be configured as GPIO
D5	JTAG_MODE_0	1.8V	DI	For debug only (do not connect)
D6	JTAG_MODE_1	1.8V	DI	For debug only (do not connect)
D7	GND	-	-	-
D8	QCS_PS_HOLD	1.8V	DI	Power supply hold control input (for debugging)
D9	GND	-	-	-
D10	VREG_L7_1P8	1.8V	PO	1.8V LDO power output,100mA
D11	GND	-	-	-
D12	GPIO_60	1.8V	IO	Can be configured as GPIO
D13	GPIO_62	1.8V	IO	Can be configured as GPIO
D14	GPIO_64	1.8V	IO	Can be configured as GPIO
D15	GPIO_66	1.8V	IO	Can be configured as GPIO
D16	GPIO_68	1.8V	IO	Can be configured as GPIO
D17	GPIO_69	1.8V	IO	Can be configured as GPIO
D18	GPIO_71	1.8V	IO	Can be configured as GPIO
D19	GPIO_73	1.8V	IO	Can be configured as GPIO
D20	GPIO_75	1.8V	IO	Can be configured as GPIO
D21	GPIO_77	1.8V	IO	Can be configured as GPIO
D22	GND	-	-	-
D23	GPIO_23	1.8V	IO	Can be configured as GPIO
D24	GPIO_25	1.8V	IO	Can be configured as GPIO
D25	GND	-	-	-
D26	GPIO_18	1.8V	DI	MSM_UART_RX
D27	GPIO_20	1.8V	IO	Can be configured as GPIO
D28	GPIO_117	1.8V	IO	Can be configured as GPIO
D29	GND	-	-	-
E1	GND	-	-	-
E2	GPIO_78	1.8V	IO	Can be configured as GPIO
E3	GPIO_79	1.8V	IO	Can be configured as GPIO
E4	GPIO_80	1.8V	IO	Can be configured as GPIO
E5	GPIO_81	1.8V	IO	Can be configured as GPIO
E6	SPMI_CLK_CON	1.8V	DO	System power management interface clock.
E7	SPMI_DATA_CON	1.8V	IO	System power management interface data
E8	LPI_GPIO_5	1.8V	IO	Can be configured as GPIO
E9	LPI_GPIO_20	1.8V	IO	Can be configured as GPIO
E10	GND	-	-	-
E11	GPIO_86	1.8V	IO	Can be configured as GPIO
E12	GND	-	-	-
E13	GPIO_103	1.8V	IO	Can be configured as GPIO
E14	GND	-	-	-

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Pad#	Function	Voltage	Type	Function description
E15	GPIO_104	1.8V	IO	Can be configured as GPIO
E16	GPIO_105	1.8V	IO	Can be configured as GPIO
E17	GPIO_106	1.8V	IO	Can be configured as GPIO
E18	GPIO_107	1.8V	IO	Can be configured as GPIO
E19	GPIO_108	1.8V	IO	Can be configured as GPIO
E20	GPIO_109	1.8V	IO	Can be configured as GPIO
E21	GND	-	-	-
E22	GND	-	-	-
E23	LPI_GPIO_6	1.8V	IO	Can be configured as GPIO
E24	LPI_GPIO_7	1.8V	IO	Can be configured as GPIO
E25	GND	-	-	-
E26	LPI_GPIO_8	1.8V	IO	Can be configured as GPIO
E27	LPI_GPIO_9	1.8V	IO	Can be configured as GPIO
E28	LPI_GPIO_10	1.8V	IO	Can be configured as GPIO
E29	GND	-	-	-
E30	GND	-	-	-
E31	GND	-	-	-
E32	GND	-	-	-
E33	JTAG_SRST_N	/	DI	JTAG reset for debug
E34	JTAG_TCK	/	DI	JTAG clock input
E35	JTAG_TDI	/	DI	JTAG data input
E36	JTAG_TDO	/	DI	JTAG data output
E37	JTAG_TMS	/	B	JTAG mode-select input
E38	JTAG_TRST_N	/	DI	JTAG reset
E39	GND	-	-	-
E40	GPIO_36	1.8V	IO	Can be configured as GPIO
E41	GND	-	-	-
E42	GND	-	-	-
G1	GND	-	-	-
G2	GND	-	-	-
G3	GND	-	-	-

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2.3. Interfaces detail description

2.3.1. Power supply interface

Below table describes all interfaces of SOM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Table 2-3. Power supply definition

Pin Name	PIN Location	Type	Description
VPH_PWR	74,75,76,80,81,82,83,87,88,89	PI	Power supply input for SOM all operations.
VREG_L6_1P8	90	PO	Low voltage switch supply output 1.8V for IO and pull up voltage
VREG_L11_SDC2	C10	PO	Power output for SD card pull up;
VREG_L7_1P8	D10	PO	1.8V LDO power output, Max 100mA
VREG_L13_3P3	C11	PO	3.3V LDO power output, Max 100mA
GND	3, 6, 9,12, 15, 18, 21, 26, 31, 36, 42, 49, 51, 52, 54, 55, 57, 58, 60, 61, 62, 63, 68, 71, 72, 73, 77, 78, 79, 84, 85, 86, 100, 111, 116, A3, B3, A13, B13, A17, B17, B19, B21, A22, A23, B23, A24, A29, D7, C9, D9, D11, C12, C17, C22, D22, C25, D25, C28, D29, E1, E10, E12, E14, E21, E22, E25, E29, E30, E31, E32, E39, E41, E42, G1, G2, G3	GND	

2.3.2. RGMII interfaces

The SOM supports RGMII interfaces can connect Ethernet transceiver.

Table 2-4. RGMII interface definition

Pin Name	PIN Location	Voltage	Type	Description
GPIO_61	C13	1.8V	DI	Ethernet transceiver interrupt input
GPIO_63	C14	1.8V	DO	RGMII transmit clock output
GPIO_64	D14	1.8V	DO	RGMII transmit data 3 output
GPIO_65	C15	1.8V	DO	RGMII transmit data 2 output
GPIO_66	D15	1.8V	DO	RGMII transmit data 1 output
GPIO_67	C16	1.8V	DO	RGMII transmit data 0 output
GPIO_68	D16	1.8V	DO	RGMII transmit enable output
GPIO_69	D17	1.8V	DI	RGMII receive clock input
GPIO_70	C18	1.8V	DI	RGMII receive data 3 input
GPIO_71	D18	1.8V	DI	RGMII receive data 2 input
GPIO_72	C19	1.8V	DI	RGMII receive data 1 input
GPIO_73	D19	1.8V	DI	RGMII receive data 0 input
GPIO_74	C20	1.8V	DI	RGMII receive data valid, RGMII input
GPIO_75	D20	1.8V	IO	Management data
GPIO_76	C21	1.8V	DO	Management data clock reference

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2.3.3. SPDIF interface

The SOM has a digital audio dedicated interface SPDIF. It's an input port only, and receiving audio signals in SPDIF format.

Table 2-5. SPDIF interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
SPDIF_RX_COAX_RCA	19	-	DI	SPDIF receive port for electrical input	
SPDIF_RX_COAX_EP	20	-	DI	SPDIF receive port for optical input	QCS403 not support

2.3.4. Audio interface

The SOM provides the audio system digital processing functions.

The SOM provide SLIMBUS, I2S, SWR and DMIC interfaces for audio system. The multiplexing of these interfaces is as follows.

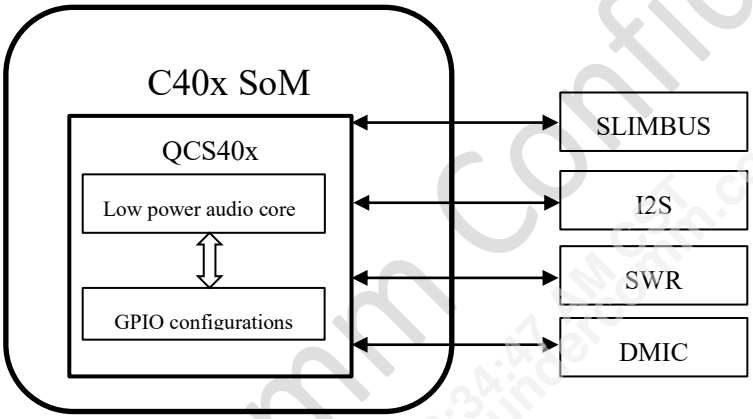

Figure 2-2. Audio Interface

One port Serial low-power inter chip media bus (SLIMBUS) interface is dedicate for external codec IC, which can build system's audio functions.

Table 2-6. SLIMBUS interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
LPI_GPIO_2	33	1.8V	DO	Audio SLIMBUS clock	
LPI_GPIO_3	34	1.8V	IO	Audio SLIMBUS data0	
LPI_GPIO_4	35	1.8V	IO	Audio SLIMBUS data1	

Six ports inter-IC sound (I2S) interfaces can connect audio devices.

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Table 2-7. I2S interface definition

Pin Name	PIN Location	Voltage	Type	Description
GPIO_87	110	1.8V	DO	I2S 1 SCK
GPIO_88	109	1.8V	DO	I2S 1 WS
GPIO_89	108	1.8V	IO	I2S 1 Data0
GPIO_90	107	1.8V	IO	I2S 1 Data1
GPIO_91	106	1.8V	IO	I2S 1 Data2
GPIO_92	105	1.8V	IO	I2S 1 Data3
GPIO_93	104	1.8V	IO	I2S 1 Data4
GPIO_94	103	1.8V	IO	I2S 1 Data5
GPIO_95	102	1.8V	IO	I2S 1 Data6
GPIO_96	101	1.8V	IO	I2S 1 Data7
GPIO_97	43	1.8V	DO	I2S 2 SCK
GPIO_98	44	1.8V	DO	I2S 2 WS
GPIO_99	45	1.8V	IO	I2S 2 Data0
GPIO_100	46	1.8V	IO	I2S 2 Data1
GPIO_101	47	1.8V	IO	I2S 2 Data2
GPIO_102	48	1.8V	IO	I2S 2 Data3
GPIO_104	E15	1.8V	DO	I2S 3A SCK
GPIO_105	E16	1.8V	DO	I2S 3A WS
GPIO_106	E17	1.8V	IO	I2S 3A Data0
GPIO_107	E18	1.8V	IO	I2S 3A Data1
GPIO_108	E19	1.8V	IO	I2S 3A Data2
GPIO_109	E20	1.8V	IO	I2S 3A Data3
GPIO_52	A25	1.8V	DO	I2S 3B SCK
GPIO_53	B25	1.8V	DO	I2S 3B WS
GPIO_54	A26	1.8V	IO	I2S 3B Data0
GPIO_55	B26	1.8V	IO	I2S 3B Data1
GPIO_56	A27	1.8V	IO	I2S 3B Data2
GPIO_57	B27	1.8V	IO	I2S 3B Data3
GPIO_110	97	1.8V	DO	I2S 4 SCK
GPIO_111	96	1.8V	DO	I2S 4 WS
GPIO_112	95	1.8V	IO	I2S 4 Data0
GPIO_113	94	1.8V	IO	I2S 4 Data1
GPIO_114	93	1.8V	IO	I2S 4 Data2
GPIO_115	92	1.8V	IO	I2S 4 Data3
LPI_GPIO_8	E26	1.8V	DO	I2S 5 SCK
LPI_GPIO_9	E27	1.8V	DO	I2S 5 WS
LPI_GPIO_10	E28	1.8V	IO	I2S 5 Data0
LPI_GPIO_11	41	1.8V	IO	I2S 5 Data1
LPI_GPIO_12	40	1.8V	IO	I2S 5 Data2
LPI_GPIO_13	39	1.8V	IO	I2S 5 Data3

One port Sound wire (SWR) interface is dedicated for external audio amplify of Qualcomm.

Table 2-8. SWR interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
LPI_GPIO_5	E8	1.8V	DO	Sound wire interface clock	
LPI_GPIO_20	E9	1.8V	IO	Sound wire interface data	

Four ports digital microphone (DMIC) interfaces can connect 8x digital microphones.

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Table 2-9. DMIC interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
LPI_GPIO_8	E26	1.8V	DO	Digital MIC0/1 clock	
LPI_GPIO_9	E27	1.8V	IO	Digital MIC0/1 data	
LPI_GPIO_10	E28	1.8V	DO	Digital MIC2/3 clock	
LPI_GPIO_11	41	1.8V	IO	Digital MIC2/3 data	
LPI_GPIO_12	40	1.8V	DO	Digital MIC4/5 clock	
LPI_GPIO_13	39	1.8V	IO	Digital MIC4/5 data	
LPI_GPIO_14	38	1.8V	DO	Digital MIC6/7 clock	
LPI_GPIO_15	37	1.8V	IO	Digital MIC6/7 data	

2.3.5. USB interface

The SOM support USB host and slave. Dual USB port support, one is USB 2.0 high-speed, the other is USB 3.0 super-speed/USB 2.0 high-speed compliant. The USB1 support host mode only.

Table 2-10. USB interface definition

SS/HS USB1 (3.0/2.0) Interface					
Pin Name	**PIN Location**	**Voltage**	**Type**	**Description**	**Notes**
USB_SS_TX_M	A10	-	DO	USB 3.0 transmitter differential pair minus	
USB_SS_TX_P	B10	-	DO	USB 3.0 transmitter differential pair plus	
USB_SS_RX_P	A11	-	DI	USB 3.0 receiver differential pair plus	
USB_SS_RX_M	B11	-	DI	USB 3.0 receiver differential pair minus	
USB1_HS_DP	A12	-	IO	USB1 HS data plus	Require differential impedance of 90Ω.
USB1_HS_DM	B12	-	IO	USB1 HS data minus	
PM_GPIO_12	D3	1.8V	DI	VBUS1 insertion detection	
USB1_HS_ID	A20	1.8V	DI	USB1 ID pin	
HS USB0 (2.0) Interface					
Pin Name	**PIN Location**	**Voltage**	**Type**	**Description**	**Notes**
USB0_HS_ID	B20	1.8V	AI	USB0 ID Pin	
USB0_HS_DM	13	-	IO	USB0 HS data minus	
USB0_HS_DP	14	-	IO	USB0 HS data plus	
PM_GPIO_06	C4	1.8V	DI	VBUS0 insertion detection	

2.3.6. PCIe interface

The SOM support one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

Table 2-11. PCIe interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
PCIE0_REFCLK_M	A4	-	-	PCIE reference clock output (-)	
PCIE0_REFCLK_P	B4	-	-	PCIE reference clock output (+)	
PCIE0_RX_M	A9	-	DI	PCIE receiver minus	
PCIE0_RX_P	B9	-	DI	PCIE receiver plus	
PCIE0_TX_M	11	-	DO	PCIE transmitter minus	
PCIE0_TX_P	10	-	DO	PCIE transmitter plus	

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2.3.7. MIPI DSI interface

The SOM supports MIPI of display, and can be up to FHD 30 FPS. This is one 4-lane MIPI DSI port, and supported only for TurboX C405.

Table 2-12. MIPI DSI interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
MIPI_DSI0_CLK_P	2	-	DO	MIPI display serial interface 0 clock positive	
MIPI_DSI0_CLK_M	1	-	DO	MIPI display serial interface 0 clock negative	
MIPI_DSI0_L0_P	A1	-	DO	MIPI display serial interface 0 lane 0 positive	
MIPI_DSI0_L0_M	B1	-	DO	MIPI display serial interface 0 lane 0 negative	
MIPI_DSI0_L1_P	A2	-	DO	MIPI display serial interface 0 lane 1 positive	
MIPI_DSI0_L1_M	B2	-	DO	MIPI display serial interface 0 lane 1 negative	
MIPI_DSI0_L2_P	5	-	DO	MIPI display serial interface 0 lane 2 positive	
MIPI_DSI0_L2_M	4	-	DO	MIPI display serial interface 0 lane 2 negative	
MIPI_DSI0_L3_P	8	-	DO	MIPI display serial interface 0 lane 3 positive	
MIPI_DSI0_L3_M	7	-	DO	MIPI display serial interface 0 lane 3 negative	

2.3.8. HDMI interface

HDMI support up to 1080p 30 FPS, and supported only for TurboX C405.

Table 2-13. HDMI interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
HDMI_TCLK_P	A7	-	DO	HDMI TMDS clock positive	
HDMI_TCLK_M	B7	-	DO	HDMI TMDS clock negative	
HDMI_TX0_P	A8	-	DO	HDMI TMDS data 0 positive	
HDMI_TX0_M	B8	-	DO	HDMI TMDS data 0 negative	
HDMI_TX1_P	A6	-	DO	HDMI TMDS data 1 positive	
HDMI_TX1_M	B6	-	DO	HDMI TMDS data 1 negative	
HDMI_TX2_P	A5	-	DO	HDMI TMDS data 2 positive	
HDMI_TX2_M	B5	-	DO	HDMI TMDS data 2 negative	
GPIO_14	A18	-	DO	HDMI_TX_CEC	
GPIO_15	B18	-	DO	HDMI_DDC_CLK	
GPIO_16	A19		IO	HDMI_DDC_DATA	
GPIO_77	D21		DI	HDMI_Hot_plug	

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2.3.9. JTAG interface

The SOM has a JTAG interface for debug.

Table 2-14. JTAG interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
JTAG_SRST_N	E33	-	DI,PU	JTAG reset for debug	
JTAG_TCK	E34	-	DI,PU	JTAG clock input	
JTAG_TDI	E35	-	DI,PU	JTAG data input	
JTAG_TDO	E36	-	-	JTAG data output	
JTAG_TMS	E37	-	B,PU	JTAG mode-select input	
JTAG_TRST_N	E38	-	DI,PD	JTAG reset	
QCS_RESIN_N	C2	1.8V	DI	System reset input	
QCS_PS_HOLD	D8	1.8V	DI	Power supply hold control input	

2.3.10. SDIO interface

The SOM supports 4-lane SDIO, SDC2 connected to the SD card.

The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 50 Mhz.
- The signals routing should be 36-50ohm impedance control.
- CLK to DATA/CMD length matching less than 2mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

Table 2-15. SDIO (SDC2) interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
SDC2 _CLK	A14	P2	DO	Secure digital controller 2 clock	
SDC2 _CMD	B16	P2	IO	Secure digital controller 2 command	
SDC2_DATA_3	A16	P2	IO	Secure digital controller 2 data bit 3	
SDC2_DATA_2	B14	P2	IO	Secure digital controller 2 data bit 2	
SDC2_DATA_1	A15	P2	IO	Secure digital controller 2 data bit 1	
SDC2_DATA_0	B15	P2	IO	Secure digital controller 2 data bit 0	
GPIO_59	B28	P3	DI	SD_CARD_DET_N need pull up to P3	

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2.3.11. BLSP interface

These GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, SPI, or I2C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus is supplemented by a 2.2kΩ pull-up resistor.

2-wire UART TX/Rx and I2C SDA/SCL ports can be used simultaneously.

Table 2-16. BLSP interface-1 definition

BLSP Number	GPIO	PIN Location	Voltage	Type	Description			Notes
					SPI	UART	I2C	
0	30	64	P3	IO	MOSI	TX	-	
	31	65	P3	IO	MISO	RX	-	
	32	66	P3	IO	CS_N	CTS_N	SDA	
	33	67	P3	IO	CLK	RFR_N	SCL	
1	22	C23	P3	IO	MOSI_A	TX	-	
	23	D23	P3	IO	MISO_A	RX	-	
	24	C24	P3	IO	CS_N_A	CTS_N	SDA	
	25	D24	P3	IO	CLK_A	RFR_N	SCL	
2	17	C26	P3	IO	MOSI	TX	-	
	18	D26	P3	IO	MISO	RX	-	
	19	C27	P3	IO	CS_N	CTS_N	SDA	
	20	D27	P3	IO	CLK	RFR_N	SCL	
4	37	69	P3	IO	MOSI	-	-	
	38	70	P3	IO	MISO	-	-	
	117	D28	P3	IO	CS_N	-	SDA	
	118	C29	P3	IO	CLK	-	SCL	

Table 2-17. BLSP interface-2 definition

BLSP Number	GPIO	PIN Location	Voltage	Type	Description			Notes
					SPI	UART	I2C	
5	26	22	P3	IO	MOSI	TX	-	
	27	23	P3	IO	MISO	RX	-	
	28	24	P3	IO	CS_N	CTS_N	SDA	
	29	25	P3	IO	CLK	RFR_N	SCL	
	44	113	P3	IO	CS1_N	-	-	
	45	114	P3	IO	CS2_N	-	-	
	46	115	P3	IO	CS3_N	-	-	

2.3.12. Power on interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source.

There are two events that will be triggered.

When a battery or other power supply is inserted and pulled down KPDPWR_N to ground up to 1s and released, SOM will be power on automatically.

Another power-on event, when pulled up PON_1 pin SOM will be power on automatically with the battery or power supply inserted, and high-level triggered with a valid trigger range between 1.17 V to VPH_PWR.

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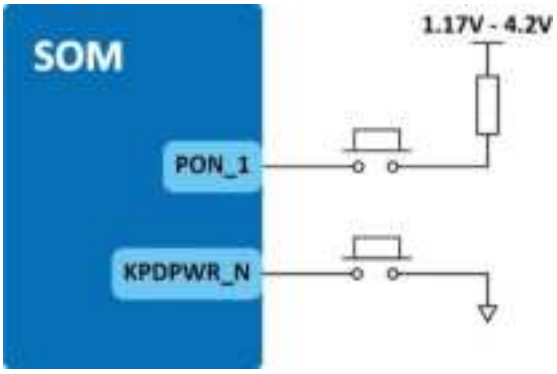

Figure 2-3. Power on Signal

Table 2-18. Power on interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
KPDPWR_N	C6	V_INT	DI	Power-on trigger, level trigger (active low)	
PON_1	C1	1.17V - 4.2V	DI	Level-high triggered power-on input (keep high)	

2.3.13. Reset interface

Three stages are available for resetting.

- Stage 1 reset – software-configurable bark

  PMIC generates interrupt, giving the QCS device the opportunity to fix the problem or gracefully reset the system. Example events can cause a bark: over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 – software-configurable bite

  If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 – hardware mandatory bite

  The user can generate a mandatory reset by a long key press of KYPD_PWR.

Table 2-19. Reset interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
PM_RESIN_N	C5	1.8V	DI	Power management reset in (active low)	
KPDPWR_N	C6	V_INT	DI	Long press to reset PMIC (active low)	

These reset triggers each have individual debounce and delay timers. Their default values are 10.256 seconds for stage 1 and 2 seconds for stage 2, respectively, and they share the stage 3 reset timer. Stage 1 and stage 2 timers run in series, and stage 3 timer runs independently (parallel) of stage 1 and stage 2 timers. If the stage 3 timer is set to a lower value than that of stage 1 and stage 2 combined, then the stage 3 reset happens first. The stage 3 default value is 128 seconds.

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2.3.14. Boot configuration interface

Configure fuses or BOOT_CONFIG pins.

- BOOT_CONFIG pins provide flexibility during product development.
- Fuses should be blown for production devices.
- BOOT_CONFIG [3:1] is MSB-aligned with Fast_Boot [2:0].

Table 2-20. Boot Configurations

BOOT_CONFIG[3:1]	Boot Options	Notes
0b000	Try SDC1 --> SDC2 --> USB2.0	Default
0b001	Try SDC2 --> SDC1	
0b010	Try SDC1	
0b011	Try USB2.0	

Default boot configuration (0b000) is eMMC on SDC1.

Special boot-related GPIO features:

- They are sensed for boot-purposes during IC reset (during fuse sense).
- After boot up, use them for normal GPIO functions.
- Do not have pull-ups on GPIO_55, GPIO_56, GPIO_57, and GPIO_49 prior to blowing FAST_BOOT fuses.

The boot configuration function of the preceding GPIOs is sampled at the rising edge of RESOUT_N reassertion.

Table 2-21. Boot Configuration GPIO definition

Boot Configuration Interface					
Pin Name	**PIN Location**	**Voltage**	**Type**	**Description**	**Notes**
GPIO_45	114	P3	IO	Forced USB boot; Configurable I/O	
GPIO_55	B26	P3	IO	Fast boot select bit 0 (configure external boot device); WDOG_DISABLE. Configurable I/O	
GPIO_56	A27	P3	IO	Boot select bit 1 (configure external boot device); Configurable I/O	
GPIO_57	B27	P3	IO	Boot select bit 2 (configure external boot device); Configurable I/O	
GPIO_49	118	P3	IO	Boot select bit 3 (configure external boot device); Configurable I/O	

Forced USB boot

During development or factory production, boot from USB_HS port are forced by using GPIO_45.

- FORCED_USB_BOOT (GPIO_45) always takes precedence, regardless of the state of the BOOT_CONFIG
- FORCED_USB_BOOT is checked first during the boot device detection prior to BOOT_CONFIG GPIOs.
- GPIO_45 = 1 forces the SDM device to boot from USB_HS port.

Blow the FORCE_USB_BOOT_DISABLE fuse to disable the feature that forces USB boot using GPIO_45.

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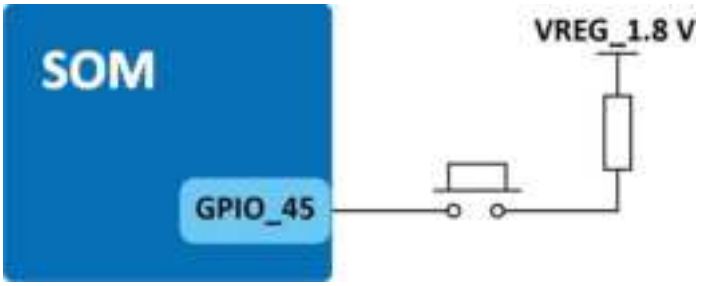

Figure 2-4. Power on Signal

Other boot configuration bits are listed in the table below, and do not have pull up on these IOs also.

Table 2-22. Other Boot Configuration interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_54	A26	P3	IO	Fast boot select bit 4 (configure external boot device); Configurable I/O	
GPIO_52	A25	P3	IO	Fast boot select bit 5 (configure external boot device); Configurable I/O	
GPIO_51	B24	P3	IO	Fast boot select bit 6 (configure external boot device); Configurable I/O	
GPIO_48	119	P3	IO	Fast boot select bit 7 (configure external boot device); Configurable I/O	
GPIO_59	B28	P3	IO	Fast boot select bit 8 (configure external boot device); Configurable I/O	
GPIO_46	115	P3	IO	Fast boot select bit 9 (configure external boot device); Configurable I/O	
GPIO_79	E3	P3	IO	Fast boot select bit 10 (configure external boot device); Configurable I/O	
GPIO_78	E2	P3	IO	Fast boot select bit 11 (configure external boot device); Configurable I/O	
GPIO_47	120	P3	IO	Fast boot select bit 12 (configure external boot device); Configurable I/O	
GPIO_50	117	P3	IO	Fast boot select bit 13 (configure external boot device); Configurable I/O	
GPIO_80	E4	P3	IO	Fast boot select bit 14 (configure external boot device); Configurable I/O	

2.3.15. Debug UART interface

This is interface dedicate for debug.

Table 2-23. Debug UART interface definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_17	C26	P3	DO	MSM_UART_TX	-
GPIO_18	D26	P3	DI	MSM_UART_RX	-

2.3.16. PWM

The GPIO_03 can be configured to send the output of the PWM waveform through special functions that can control the external current drivers for LED.

Table 2-24. PWM definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
PM_GPIO_03	D4	Software configurable: VIN0 = 3.6V (Nominal) VIN1 = 1.8V	DO	Configurable GPIO	-

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2.3.17. Sleep clock

The sleep-clock output from PMS405, and it is generated following ways:

- Calibrated low-frequency RC oscillator, periodically uses the 38.4 MHz XO signal for calibration, achieving accuracy suitable for the real-time clock.
- Using the 38.4 MHz XO circuit and dividing its output by 1172 to create a 32.7645 KHz signal. This signal is used as the start-up sleep clock.

Table 2-25. SLEEP_CLK definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
SLEEP_CLK	D2	1.8V	DO	32.7 KHZ sleep clock output.	-

2.3.18. SPMI

The SPMI is a bidirectional, two-line digital interface for communication between Qualcomm chipsets, which meets the relevant information for voltage and current level requirements.

Table 2-26. SPMI definition

Pin Name	PIN Location	Voltage	Type	Description	Notes
SPMI_CLK_CON	E6	1.8v	DO	System power management interface clock	
SPMI_DATA_CON	E7	1.8v	IO	System power management interface data	

2.3.19. Antenna interface

The SOM provides the fully-integrated WLAN, Bluetooth function.

- WLAN supports 2 × 2 (WCN3999) and 1 × 1 (WCN3980) multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards.
- Supports Bluetooth +LE5.x + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.
- Concurrent operation for WLAN and BT.

Table 2-27. Antenna interface definition

Pin Name	PIN Location	Voltage	Type	Description
ANT_WL_Chain 1	50	-	RF IO	Antenna port for WIFI TX/Rx chain 1 of WCN3999 only
ANT_WL_Chain 0	59	-	RF IO	Antenna port for WIFI/BT TX/Rx chain 0 of WCN3980 Antenna port for WIFI TX/Rx chain 0 of WCN3999 (BT standalone) Antenna port for WIFI/BT TX/Rx chain 0 of WCN3999
BT_ANT	56	-	RF IO	Antenna port for standalone BT antenna (BT standalone), NC in others

➲ **NOTE**:

- On Wi-Fi/BT shared chain 0 SOM, BT_ANT should be NC and BT signal is output from “ANT_WL_Chain 0”.
- On BT standalone SOM, BT signal is output from “BT_ANT”.
- BT_ANT and ANT_WL_Chain 0 are supported by different variants of the SOM.

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Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The SOM needs to be designed in the operating conditions which is shown as below table beyond its absolute maximum ratings may damage the device.

Table 3-1. Absolute rating condition

Parameter	Min	Max	Units
Input power voltage			
Voltage on any input or output pin	-0.5	VPH_PWR+0.5	V
VPH_PWR	-0.5	6.0	V

3.2. Operating conditions

The SOM needs to be designed in the operating conditions which is shown as in the table below.

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input power voltage				
VPH_PWR	+3.50	3.8	+5.0	V
Supply voltage, digital I/O	+1.75	-	+1.85	V
VPH_PWR	0.8			A
Thermal conditions				
Operating temperature	-20	25	70	°C
Storage temperature	-20	-	70	°C

➲ **NOTE:** The min and max operating temperatures specified in the above table shall not exceed those of relevant IC (see Table 3-3).

Table 3-3. IC temperature

Chipset	Thermal Condition (min, °C)	Thermal Condition (max, °C)
QCS40X	Ta=-25	Tj=105
PMS405	Tj=-40	Tj=150
WCN3999	Tc=-30	Tc=85
eMCP/DDR/eMMC	Ta=-25	Ta=85

➲ **NOTE:**

- Ta: a=ambient, temperature of the working environment.
- Tc: c=case, *surface temperature*, which can be simply understood as ambient temperature + CPU temperature rise. Generally speaking, Tc is slightly higher than the ambient temperature.
- Tj: j=junction, *junction temperature*, which can be simply understood as the chip internal temperature.

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3.3. Output power

The SOM provides power supply for external device.

Table 3-4. Output power

Function	Default voltage(V)	Programmable range(V)	Rated current(mA)	Default ON	Expected use
VREG_L6_1P8	+1.8	-	100	Y	1.8V IO pull up voltage;
VREG_L11_SDC2	+2.95	+1.8--+3.3	100	Y	Power output for SD card data pull up
VREG_L7_1P8	+1.8	+1.7--+1.89	100	N	1.8V LDO power output,100mA
VREG_L13_3P3	+3.3	+1.8--+3.3	100	N	3.3V LDO power output,100mA

3.4. Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage.

The SOM IO voltage level is the same with P3 except the SD card and analog input/output.

The I2C, USB, MIPI and UART comply with the standards, and additional specifications are not required.

All other digital I/Os require performance specifications and are organized within this section.

3.4.1. Digital GPIO characteristics

The GPIO ports are digital I/Os that can be programmed for a variety of configurations. General performance specifications for are the different configurations.

The following table shows the digital GPIO characteristics:

Table 3-5. Digital IO voltage performance

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.65* P3	-	V
VIL	Low-level input voltage, CMOS/Schmitt,	-	0.35* P3	V
VSHYS	Schmitt hysteresis voltage	100	-	mV
VOH	High-level output voltage, CMOS	P3-0.45	-	V
VOL	Low-level output voltage, CMOS	-	0.45	V
RPULL-UP	Pull-up and Pull-down resistance	55	390	KΩ
Rk	Keeper resistance	30	150	KΩ

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3.4.2. SD card digital I/O characteristics

The SD card is powered by P2; the power is 1.8V and 2.95V.the following table shows the SD card digital I/O characteristics:

Table 3-6. SD digital IO voltage performance (1.8V/2.95V)

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27V/1.84V	-	2.0V/2.98V	V
VIL	Low-level input voltage	-0.3	-	0.58/0.74	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/2.21	-	-	V
VOL	Low-level output voltage	0/0	-	0.45/0.36	V

Table 3-7. SD standards and exceptions

Applicable standard	Feature exceptions	Device variations
Multi Media Card Host Specification, version 5.1 (JESD84-B51 - JEDEC)	None	Timing specifications as shown in the following figures.
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 2.0	None	

Single data rate – SDR mode:

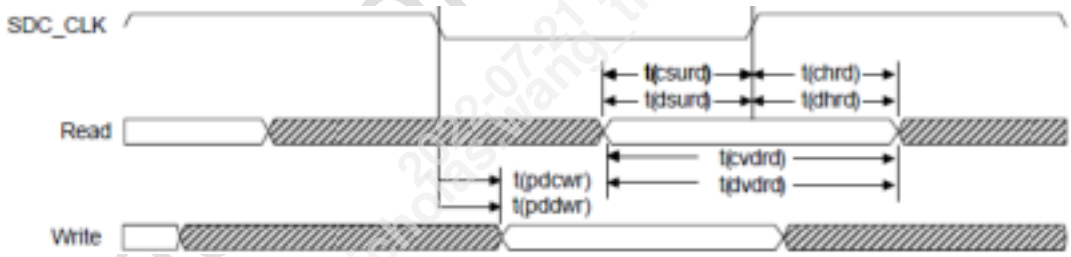

Figure 3-1. Secure Digital Interface Timing Diagram -SDR Mode

Double data rate – DDR mode:

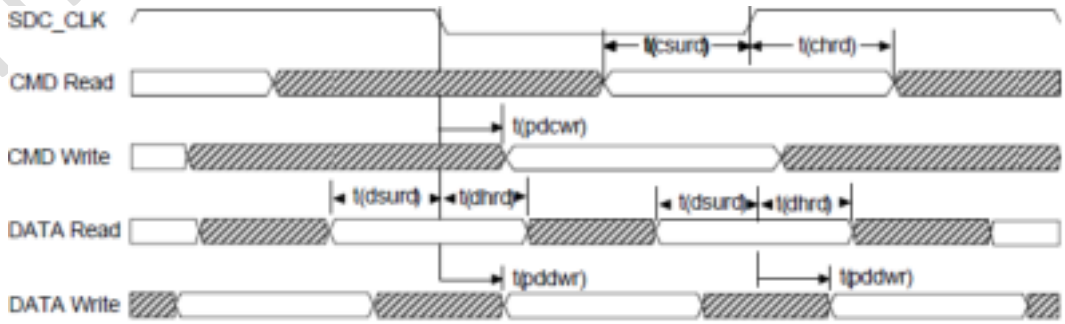

Figure 3-2. Secure Digital Interface Timing Diagram – DDR Mode

Table 3-8. SD digital IO timing characteristics

Parameter	Description	Min	Typical	Max	Units
DDR mode – SDC2, up to 50 MHz					
tchrd	Command hold	1.50	-	-	ns
tcsurd	Command setup	6.30	-	-	ns
tdhrd	Data hold	1.50	-	-	ns
tdsurd	Data setup	2.00	-	-	ns
tpddwr	Propagation delay on data write	0.80	-	6.00	ns
tpdcwr	Propagation delay on command write	-8.20	-	3.00	ns

3.5. USB

The SOM supports USB standards and exceptions.

Table 3-9. USB standards and exceptions

Applicable standard	Feature exceptions	APQ variation
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 or later)	Supports the host mode aspect of OTG only	None

3.6. SLIMbus

Table 3-10. SLIMbus standards and exceptions

Applicable standard	Feature exceptions	APQ variation
MIPI Alliance Specification for Serial Low-power Inter chip Media Bus, Version 1.01.011	• No support of the CHANGE_CONTENT message by any of the devices in the component. Only the manager is given the ability to manage data channels in the system. • No support for the elemental access mode for information and value elements. • No support for the following transport protocols. ▪ Asynchronous half-duplex ▪ Extended asynchronous half-duplex • No support for the locked transport protocol. • No support of a partial mask in CHANGE_VALUE message.	The maximum clock output slew rate might be greater than 20% * VDD [V/ns] for the 15 pF load condition.

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Table 3-11. SLIMbus frequencies

SLIMbus	SVS	Normal	Turbo	Units
Slimbus1 (IFM)	24.57	24.57	24.57	MHz
Slimbus2 (QCA) (IFM)	24.57	24.57	24.57	MHz
Slimbus1 (XFM)	23.1	23.1	23.1	MHz
Slimbus2 (XFM)	22.4	22.4	22.4	MHz

3.7. I2S

Legacy I2S interfaces for primary and secondary microphones and speakers.

The multiple I2S (MI2S) interface for microphone and speaker functions, including audio for HDMI.

Table 3-12. I2S standards and exceptions

Applicable standard	Feature exceptions	Device variations
Philips I2S Bus Specifications revised June 5, 1996	None	Timing – When an external SCK clock is used, a duty cycle between 45% to 55% is required.

High-level I2S timing

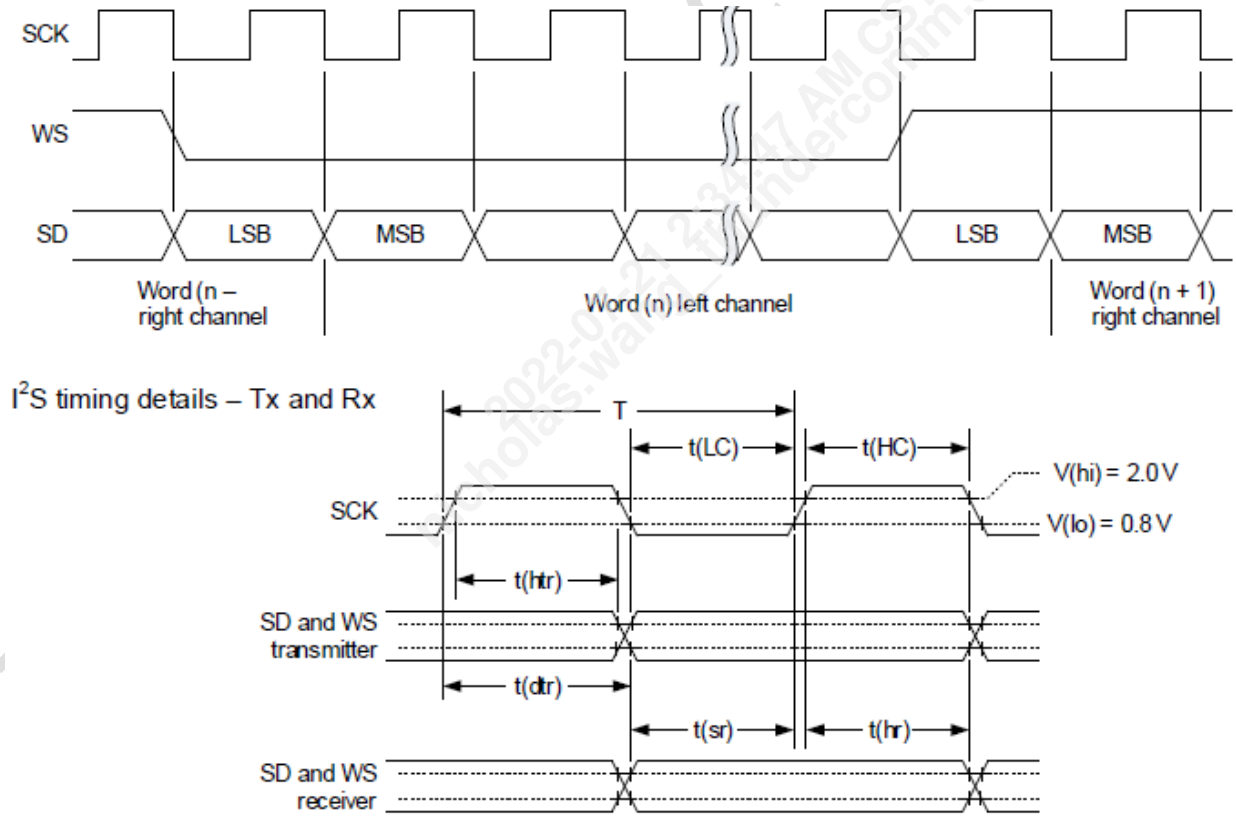

Figure 3-3. I2S Interface Timing

Table 3-13. I2S interface timing characteristics

Parameter	Description	Min	Typical	Max	Units
Using internal SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHz
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10 and 40pF.	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and 40pF.	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
Using external SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHz
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10 and 40pF.	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and 40pF.	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns

Table 3-14. I2S interface frequencies

Interface	Frequency achieved
I2S1	24.57 MHz
I2S2	12.288 MHz
I2S3A	12.288 MHz
I2S3B	12.288 MHz
I2S5	24.57 MHz
I2S6	12.288 MHz

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3.8. PDM

THE SOM PDM interfaces for primary and secondary digital microphones. DMIC interfaces running at 9.6 MHz clock.

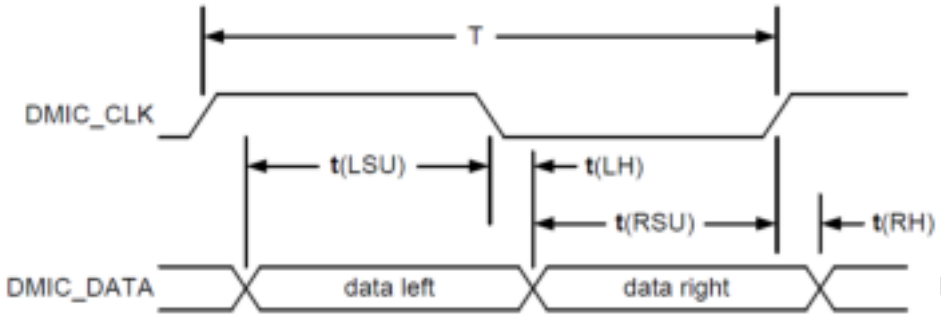

Figure 3-4. PDM Interface Timing Diagram

Table 3-15. PDM interface timing characteristics

Parameter	Description	Min	Typical	Max	Units
Using internal SCK					
T	DMIC clock period	163	-	1666	ns
t(LSU)	Data left setup time to the clock falling edge	5	-	-	ns
t(LH)	Data left hold time to the clock falling edge	0	-	-	ns
t(RSU)	Data right setup time to the clock rising edge	5	-	-	ns
t(RH)	Data right hold time to the clock falling edge	0	-	-	ns

3.9. I2C

Table 3-16. I2C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 5.0, October 2012	None

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3.10. SPI

The following are the SPI features and comparisons:

- Supports 4-bit (MISO, MOSI, CS, CLK) synchronous serial data link.
- Support for master-only mode, up to 50 MHz on all SPI interfaces.
- Master device initiates data transfers; Multiple slave devices are supported by using chip-selects.
- No explicit communication framing, error-checking, or defined data word lengths; The transfers are strictly at the raw bit level.
- As an SPI master, the core supports several SPI system configurations (as defined by the SPI protocol).

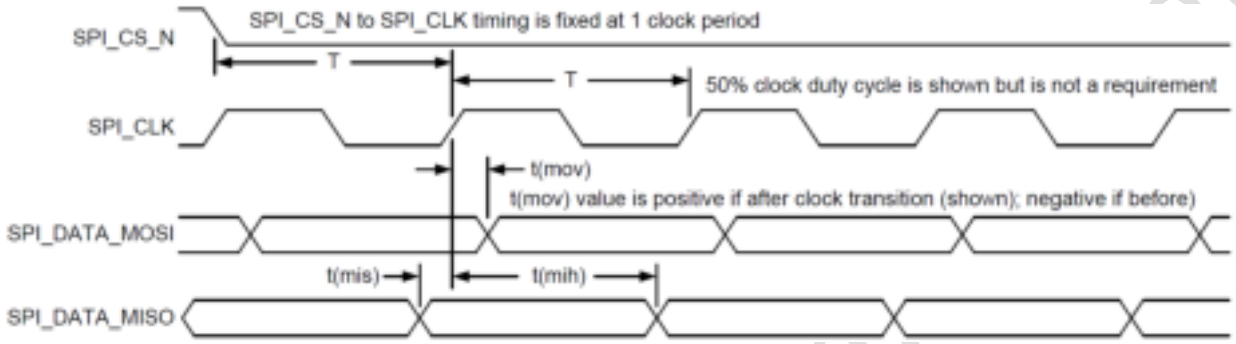

Figure 3-5. SPI Master Timing Diagram

Table 3-17. SPI master timing characteristics

Parameter	Description	Min	Typical	Max	Units
T	SPI clock period: 50 MHz maximum	20	-	-	ns
t(ch)	Clock high	9.0	-	-	ns
t(cl)	Clock low	9.0	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns
T	SPI clock period: 26 MHz maximum	38	-	-	ns
t(ch)	Clock high	17	-	-	ns
t(cl)	Clock low	17	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns

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3.11. Current sink

PM_GPIO_03 is capable of sinking current (up to 12 mA). In addition, since the PWM module can be routed to the current sink, different blinking and dimming patterns can be achieved.

Table 3-18. Current sink specification

Parameter	Description	Min	Typical	Max	Units
Rated current sink	-	9	-	12	mA

3.12. Sleep clock

The sleep clock output characteristics: (voltage levels, drive strength, and so on see Digital GPIO characteristics).

Table 3-19. Sleep clock specification

Parameter	Description	Min	Typical	Max	Units
Period jitter (rms)	38.4 MHz XO/1172	-	-	10	ns (RMS)
Frequency drift	Shift in frequency in any 2.5 sec window at constant temperature	-	-	2	ppm
RTC accuracy	CalRC provides a jittery clock that provides a long term averaged accurate RTC clock; time accuracy defined over long period	-	-	200	ppm

3.13. SPMI

Table 3-20. SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

3.14. MIPI DSI

Table 3-21. MIPI DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification v1.01 for Display Serial Interface	None
MIPI D-PHY Specification v0.65, v0.81, v0.90	-

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3.15. Power consumption

The following current consumption records are measured on TurboX C40x DK, and any specific equipment configuration or use different from DK may increase power consumption.

Table 3-22. Power Consumption

Test Condition: Room temperature (25°C). Measure power for 60 sec. **Test case**	**QCS404/QCS405 PMS405 & 1GB LPDDR3 WCN3999 (mA)**
Sleep mode	< 2.4
Airplane mode with display OFF, keyword detection OFF	33.5
Bluetooth paired (sniff + scan) Adder (from WCN399x, does not chane with QCS part)	34.1
WLAN DTIM3/DTIM1 Adder	44.1/44.9
Local MP3 audio playback in tunnel mode (excluding speaker PA)	51.3
WLAN PNO (preferred network order) scan (60s) Adder	48.2
WLAN [2.4 GHz 1x1 config] streaming MP3 [128 kps] audio playback in tunnel mode (excluding speaker PA)	201.2
Bluetooth A2DP Rx local audio playback (excluding speaker PA)	101.1
Bluetooth HFP voice call with Fluence Pro v2.1	34.7
Current leak while power off	< 0.2

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Appendix 1. Notices

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FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM

Manual v01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Yes, For details, see pages 5-16 of this document

2.6 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body.

2.7 Antennas

This radio transmitter FCC ID: **2AOHHTURBOX-C405-D** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna Manufacturer	Antenna Chain	Antenna type	Input impedance (Ohm)	Maximum antenna gain
BOSE	0	PCB	50	2.34 dBi/2.4-2.5GHz 2.33 dBi/5.15-5.85GHz
	1	PCB	50	2.6 dBi/2.4-2.5GHz 3.11 dBi/5.15-5.85GHz
Molex	0	FPC	50	3.2 dBi/2.4-2.5GHz 4.25 dBi/5.15-5.85GHz
	1	FPC	50	3.2 dBi/2.4-2.5GHz 4.25 dBi/5.15-5.85GHz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID: **2AOHHTURBOX-C405-D**"

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B

ISED Statement

This device complies with Industry Canada license -exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause interferenc e, and (2) This device must accept any interference, including interference that may cause un desired operation of the device.

Le présentappareilestconforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitationestautorisée aux deux conditions suivantes: (1) l'appa reil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareildoit accepter tout brouilla geradioélectriquesubi, mêmesi le brouillageest susceptible d'encompromettre le fonctionnem ent.

Radiation Exposure Statement

This equipment complies with Canada radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations

Cet équipement est conforme Canada limites d'exposition aux radiations dans un environnement non contrôlé. Cet équipement doit être installé et utilisé à distance minimum de 20cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following condition: The transmitter module may not be co-located with any other transmitter or antenna. As long as the condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:

Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne. Tant que les 1 condition ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the ISED cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

Any company of the host device which install this modular with limit modular approval should perform the test of radiated emission and spurious emission according to RSS-247 and RSSGen requirement, only if the test result comply with RSS-247 and RSS-Gen

requirement, then the host can be sold legally.

Note Importante:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l' ISED ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada. toute entreprise de l'hôte qui installent ce dispositif modulaire avec limite approbation devrait effectuer l'essai des modules et des rayonnements non essentiels des émissions rayonnées selon RSS-247 et le cnr - gen, seulement si le résultat d'essai conforme RSS-247 et le cnr - gen, puis l'hôte peut être vendu légalement.

End Product Labeling

The final end product must be labeled in a visible area with the following: Contains IC: 23465-TURBOXC405.

Plaque signalétique du produit final

Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: Contient des IC: 23465-TURBOXC405.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

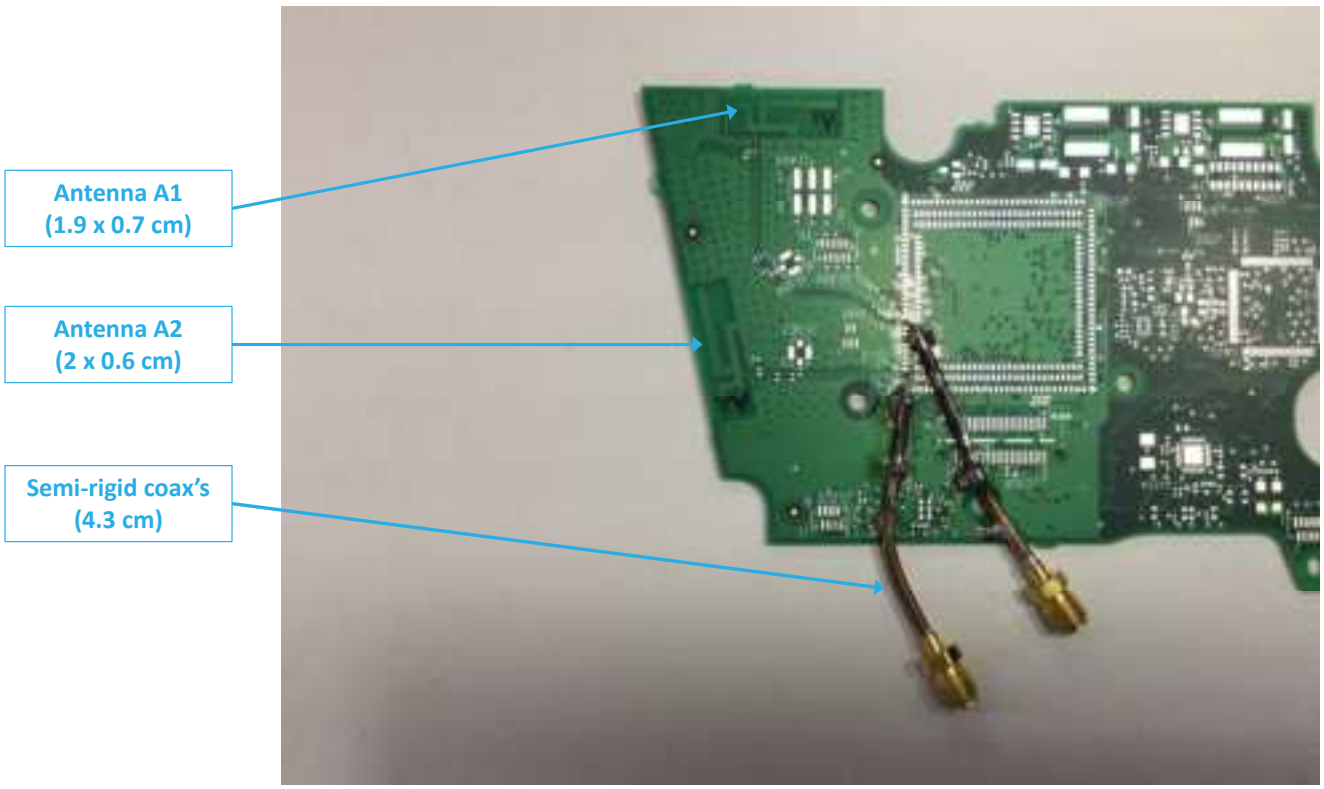
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

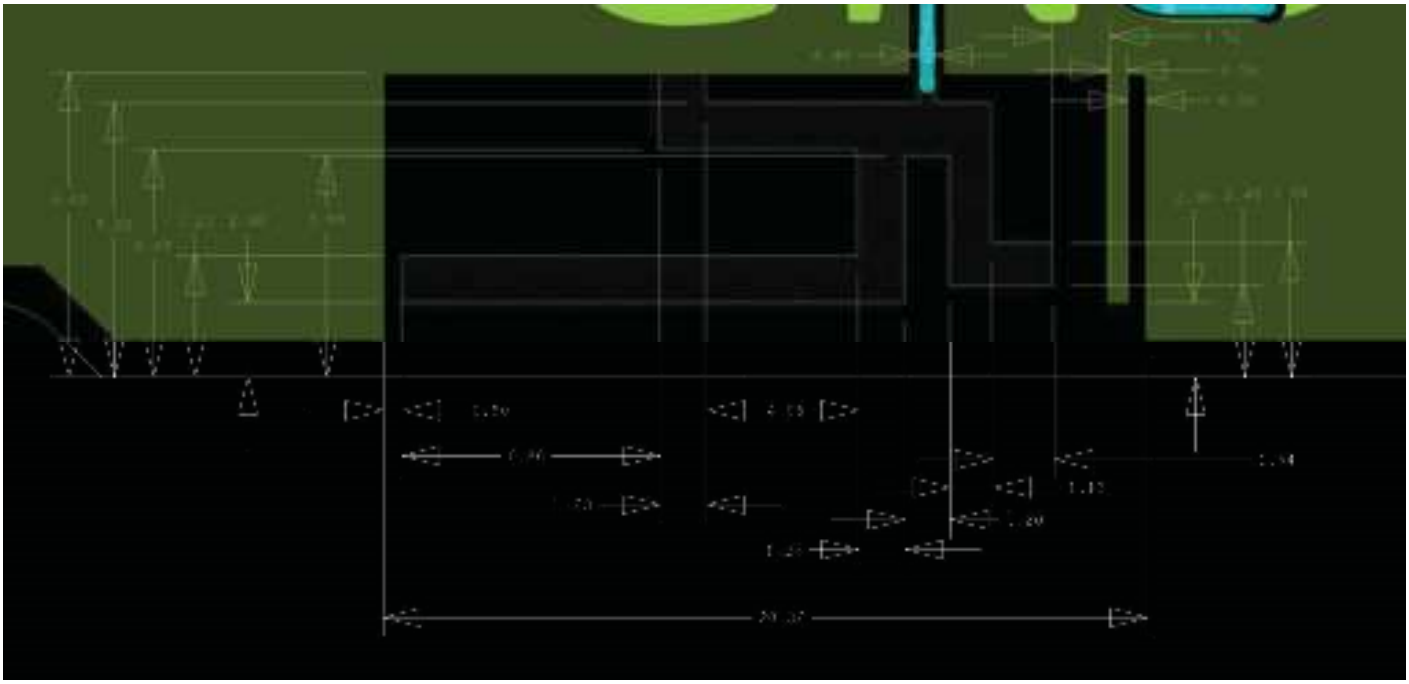
L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Trace Antenna Specs
Main PCBA = zoomed

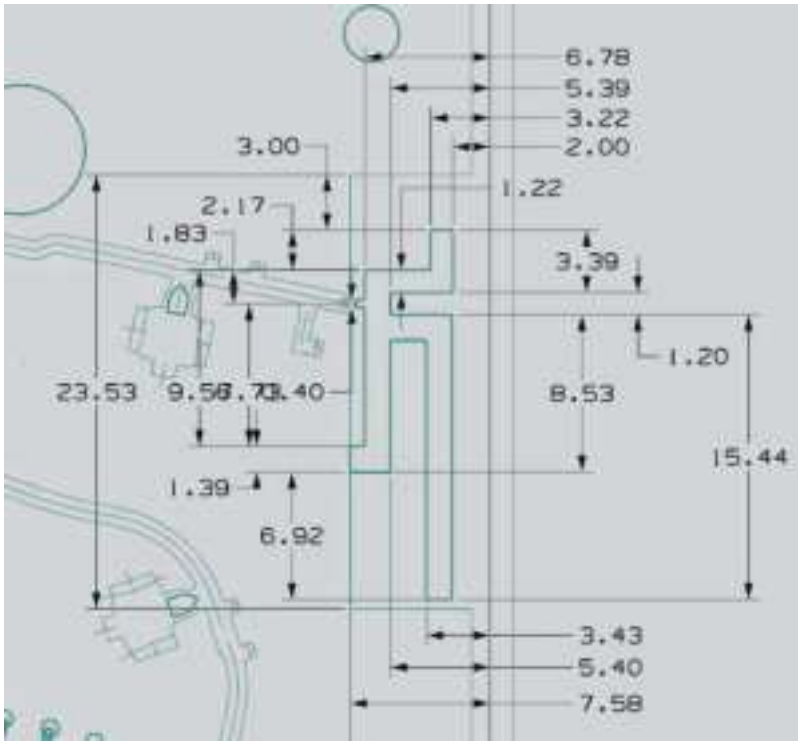


Antenna Pattern Detail – Ant-A1



Note:
1. Dimensions in mm.

Antenna Pattern Detail – Ant-A2



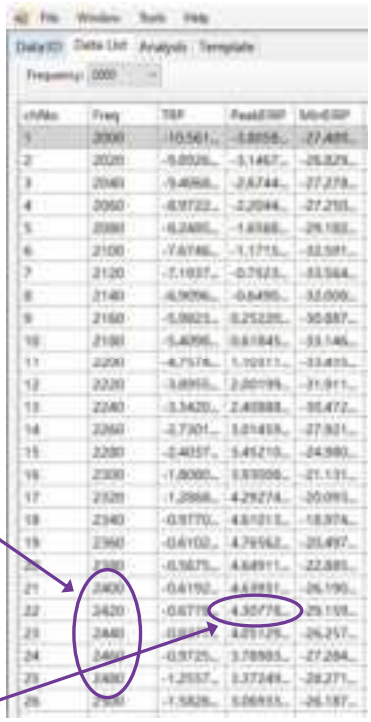
Note:
1. Dimensions in mm.

Bose Antenna Specs
Peak Antenna Gain – 2.4 GHz Band / Ant-A1

2.4 GHz Band

Gain_pk = 4.04-1.7 = +2.34 dBi
(1.7 dB correction factor applied)

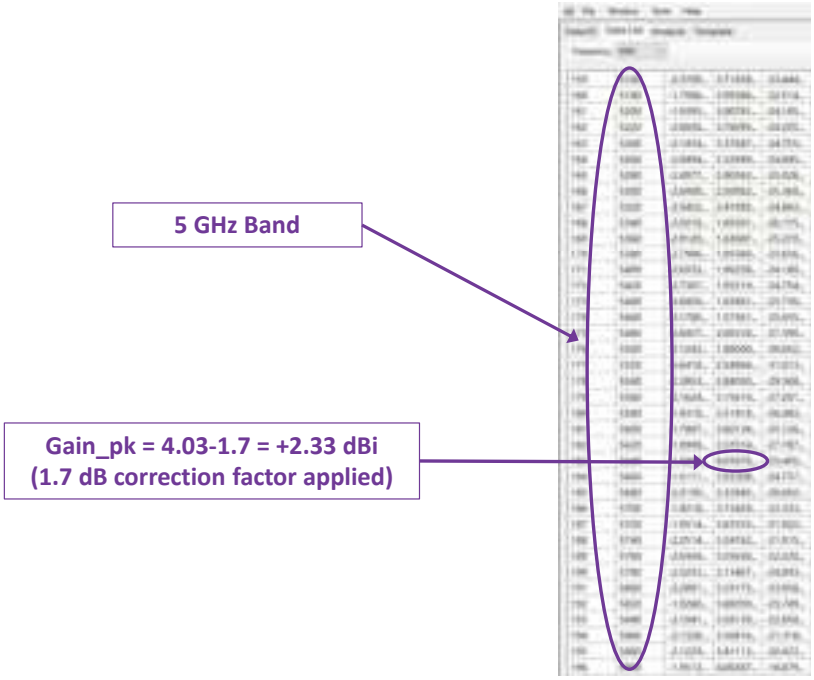
Peak Antenna Gain – 2.4 GHz Band / Ant-A2



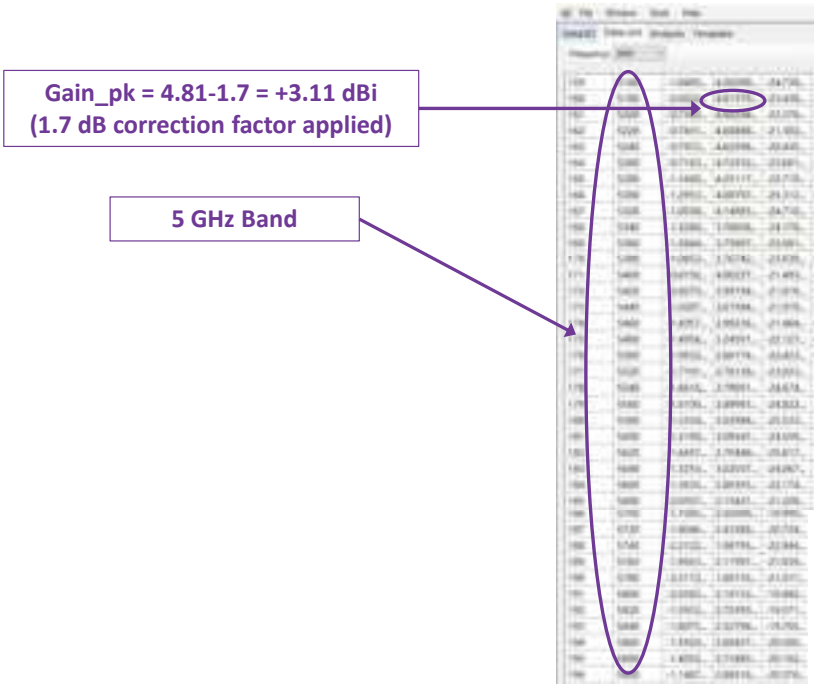
2.4 GHz Band

Gain_pk = 4.30-1.7 = +2.60 dBi
(1.7 dB correction factor applied)

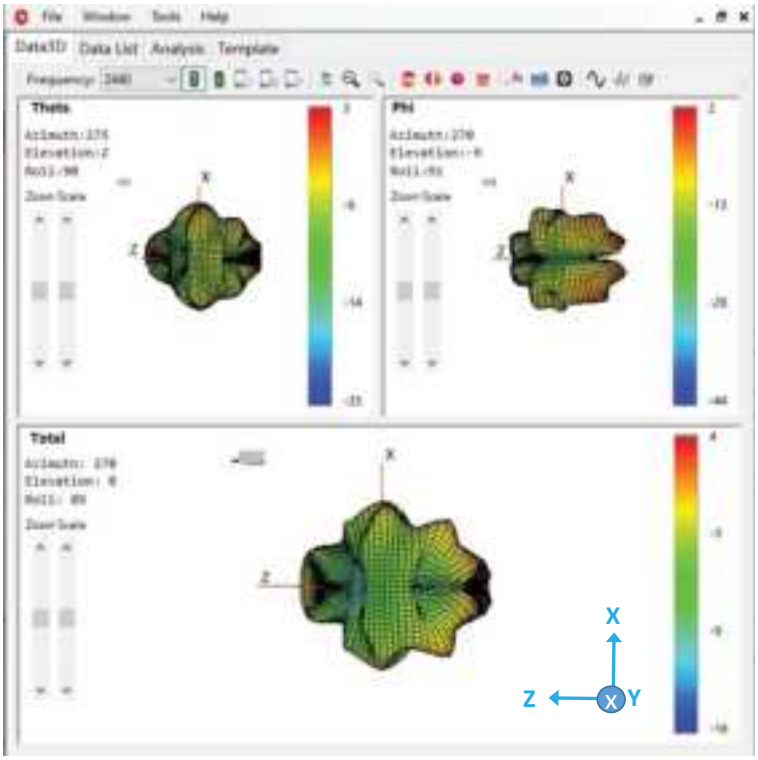
Peak Antenna Gain – 5 GHz Band / Ant-A1



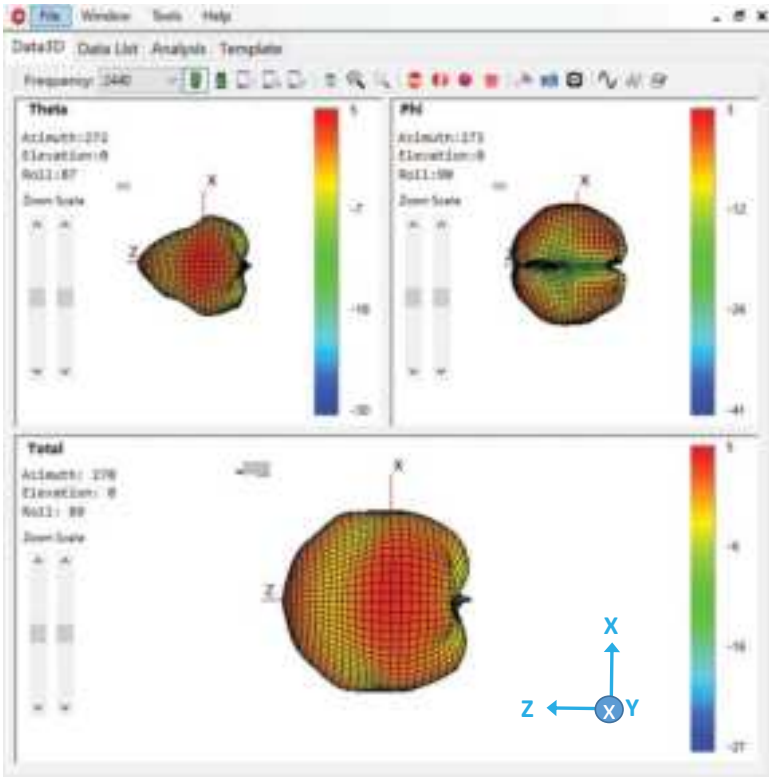
Peak Antenna Gain – 5 GHz Band / Ant-A2



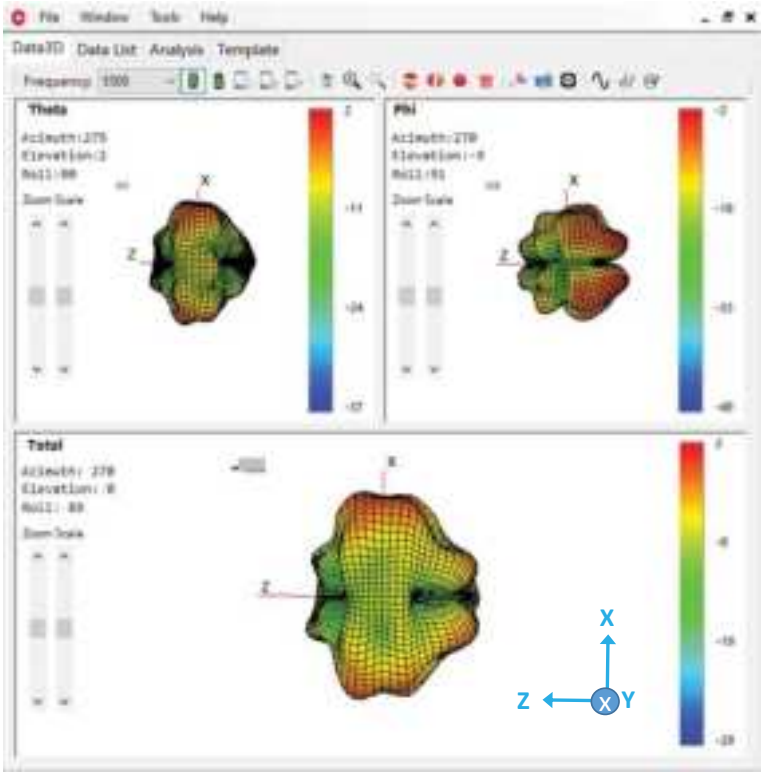
3D Antenna Gain – 2440 MHz / Ant-A1 / PCBA Front View (“ZX” Plane)



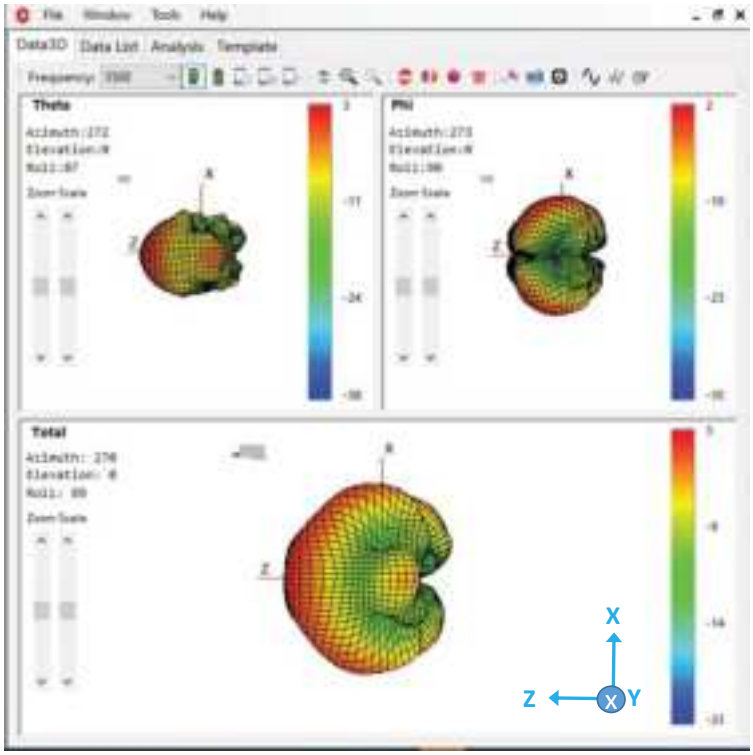
3D Antenna Gain – 2440 MHz / Ant-A2 / PCBA Front View (“ZX” Plane)



3D Antenna Gain – 5500 MHz / Ant-A1 / PCBA Front View (“ZX” Plane)



3D Antenna Gain – 5500 MHz / Ant-A2 / PCBA Front View (“ZX” Plane)



Bose Antenna Specs
PCB Info

	Copper foil(OZ)	Dielectric	Calculated final thickness(um)	DK	Single-ended	L
		Solder mask	15			
L1	1/3OZ+plating		41		50	
		prepreg 0.08mm(2113*1)	85	4		
L2	1OZ		30			
		core 0.12mm(consist 2116)	125	4		
L3	1OZ		30		50	
		prepreg 0.488mm(prepreg 7628*1/core 20+/-2mil(consist 7628)/prepreg 7628*1)	889	4.2		
L4	1OZ		30			
		core 0.12mm(consist 2116)	125	4		
L5	1OZ		30			
		prepreg 0.08mm(2113*1)	85	4		
L6	1/3OZ+plating		41		50	
		Solder mask	15			

Note:
1. Antenna pattern on layer-1. Antenna ground reference on layer-3.