Section 2.1049 Measurements Required: Occupied Bandwidth

In compliance with Section 2.1049(h), a single TDMA carrier was modulated by a pseudo-random data bit stream for all 3 time slots, and the PCS-TDMA Dual Radio Module (PDRM) 44WR53, subject of a separate application under AS5CMP-30, in combination with the PCS-TDMA Multi Carrier Linear Amplifier (PMCLA) 44WA28, subject of this application under AS5CMP-31, output power level was set to provide +30.8 dBm (1.2 Watts) at the transmit antenna terminal. In compliance with Part 24.238(c), occupied bandwidth measurements were made at both the lower and the upper block edge for each PCS frequency block as shown below. Measurements were made both at the antenna terminal and at the input to the PMCLA to demonstrate that the amplifier does influence and does alter the occupied bandwidth.

PCS Frequency	PCS	Carrier Center
Block	Channel No.	Frequency - MHz
A (le)	2	1930.08
A (ue)	498	1944.96
D (le)	502	1945.08
D (ue)	665	1949.97
B (le)	668	1950.06
B (ue)	1165	1964.97
E (le)	1168	1965.06
E (ue)	1332	1969.98
F (le)	1335	1970.07
F (ue)	1498	1974.96
C (le)	1502	1975.08
C (ue)	1998	1989.96

le = lower block edge frequency; and ue = upper block edge frequency

The occupied bandwidth limitations and emission mask for a 30 kHz TDMA carrier, i.e., digital transceiver, is specified in Part 22.917(d)(1-3) as:

Displacement from the	Required Attenuation Below the Carrier	
Carrier Center Frequency		
Greater than 20 kHz up to 45 kHz	At least 26 dBc	
Greater than 45 kHz up to 90 kHz	At least 45 dBc	
Greater than 90 kHz up to 1st harmonic	At least 60 dBc	
_	Or 43 + 10 log (Carrier Power in Watts) dBc	
	Or whichever is the lesser attenuation	

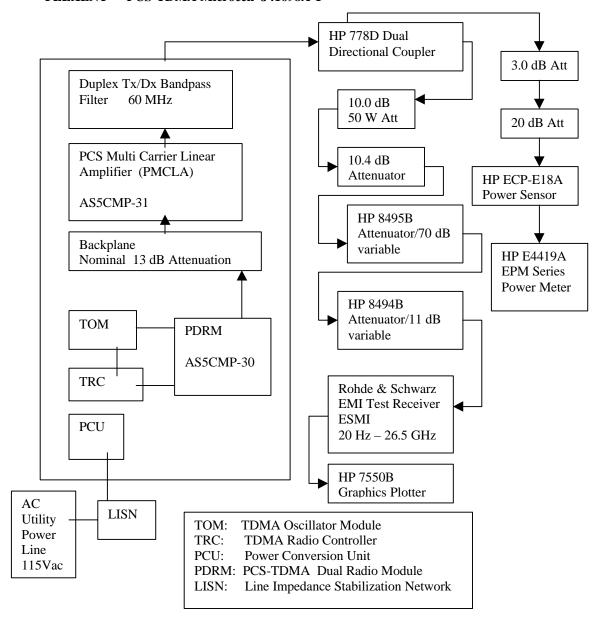
The limitation for each PCS frequency block edge is specified in Part 24.238(a) as: "the power of any emission shall be attenuated below the transmitter power (P in Watts) by at least 43 + 10 log (P) dBc." For the PMCLA output power at the antenna terminal +30.8 dBm (1.2 W), the required block edge emission attenuation is then 43.8 dBc. Part 24.238(b) specifies that the measurement instrumentation resolution bandwidth be set to 1% of the fundamental emission bandwidth. For the 30 kHz TDMA carrier, the spectrum analyzer resolution bandwidth was set to 300 Hz. The standard measurement procedure is to align the center of the carrier with the top of the spectrum analyzer display reticle (i.e., 0 dBm) and reference required "attenuation below the carrier" to the 0 dBm reference. Attenuation below the carrier is then read directly off the 0 dBm to -110 dBm scale. Using the 300 Hz resolution bandwidth requires displacing (offsetting) the 30 kHz modulated carrier from the 0 dBm reference line by:

RESULTS:

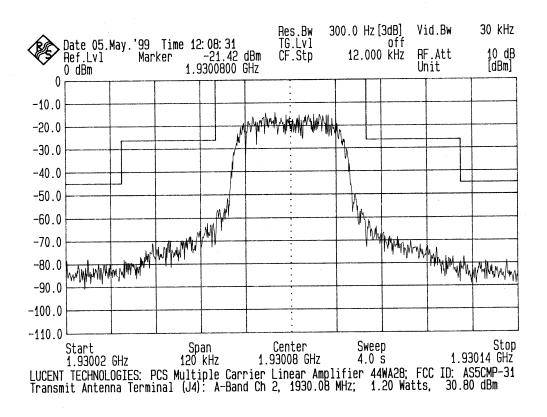
The attached occupied bandwidth plots demonstrate full compliance with the requirements of Part 24.238, for the required frequencies specified above. The block edge limitation of 43.8 dBc, for a carrier power level of +30.8 dBm, is less stringent than the 45 dBc emission mask. On this basis, and that all carriers are well within the required emission mask, the PCS-TDMA Multi Carrier Linear Amplifier (PMCLA) 44WA28 demonstrated full compliance with Part 24.238 for occupied bandwidth requirements. It also demonstrated it does not affect or influence the occupied bandwidth of the associated PCS-TDMA Dual Radio Module transceiver.

Test set-up for measuring the occupied bandwidth of the PCS-TDMA Dual Radio Module transceiver.

FLEXENT™ PCS-TDMA Microcell J41698A-1

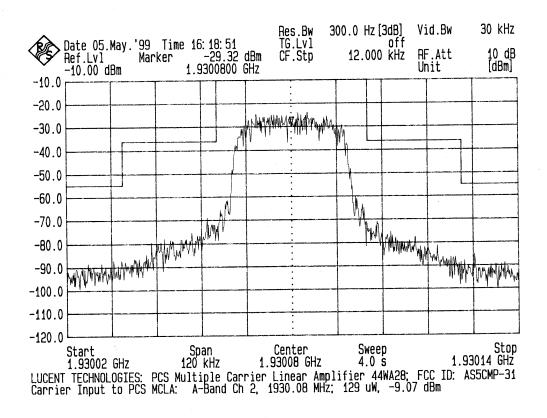


OCCUPIED BANDWIDTH PLOTS:



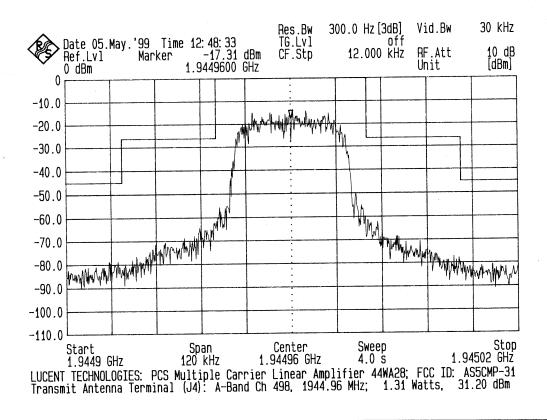
PCS A-Block: Lower Edge Channel Channel 2, 1930.08 MHz

OCCUPIED BANDWIDTH PLOTS:



PCS A-Block: Lower Edge Channel Channel 2, 1930.08 MHz

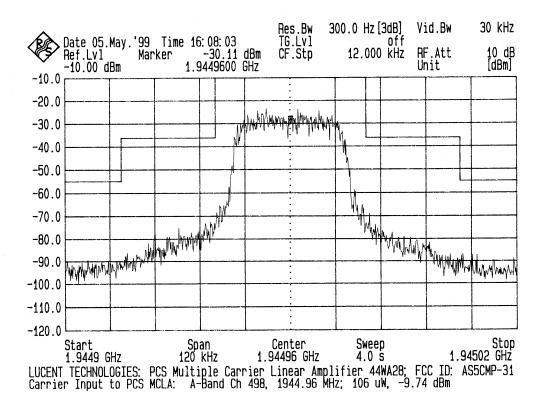
OCCUPIED BANDWIDTH PLOTS:



PCS A-Block: Upper Edge Channel

Channel 498, 1944.96 MHz

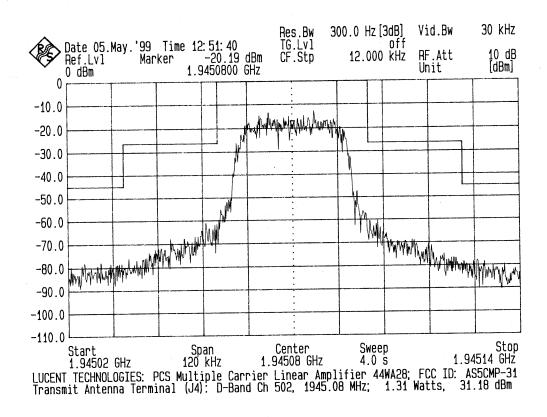
OCCUPIED BANDWIDTH PLOTS:



PCS A-Block: Upper Edge Channel

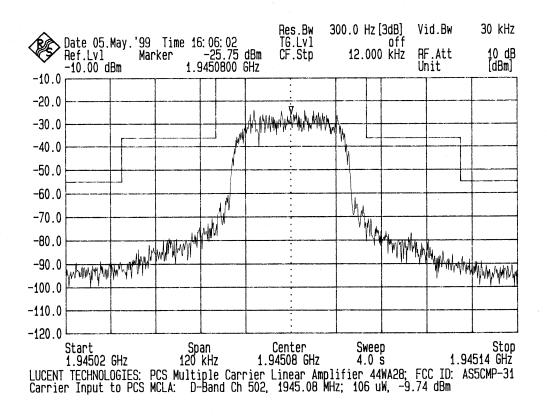
Channel 498, 1944.96 MHz

OCCUPIED BANDWIDTH PLOTS:



PCS D-Block: Lower Edge Channel Channel 502, 1945.08MHz

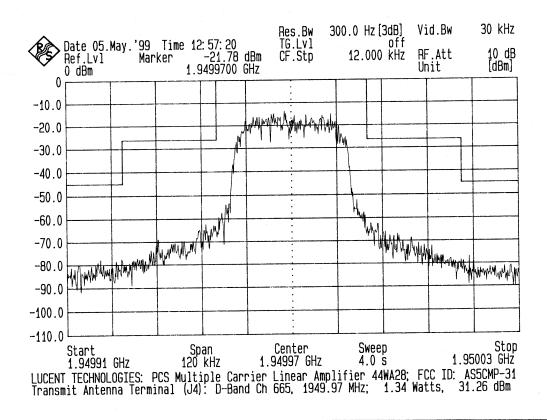
OCCUPIED BANDWIDTH PLOTS:



PCS D-Block: Lower Edge Channel

Channel 502, 1945.08MHz

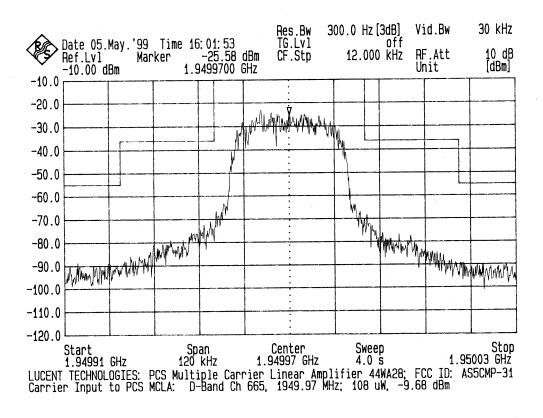
OCCUPIED BANDWIDTH PLOTS:



PCS D-Block: Upper Edge Channel

Channel 665, 1949.97 MHz

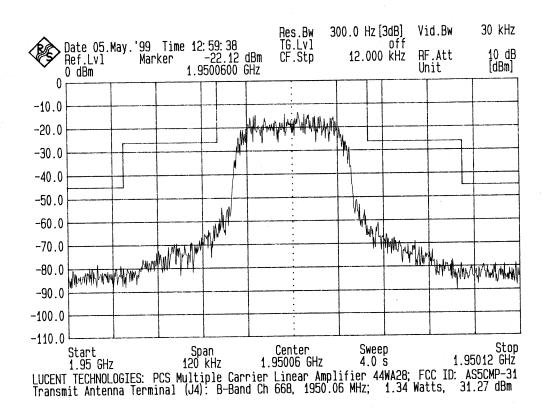
OCCUPIED BANDWIDTH PLOTS:



PCS D-Block: Upper Edge Channel

Channel 665, 1949.97 MHz

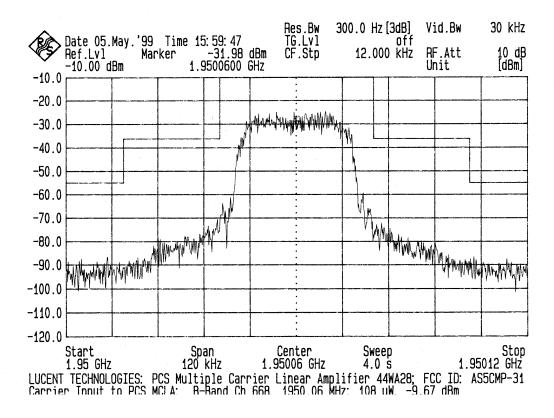
OCCUPIED BANDWIDTH PLOTS:



PCS B-Block: Lower Edge Channel

Channel 668, 1950.06 MHz

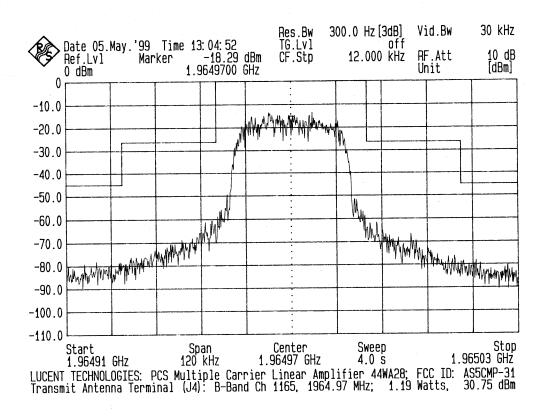
OCCUPIED BANDWIDTH PLOTS:



PCS B-Block: Lower Edge Channel

Channel 668, 1950.06 MHz

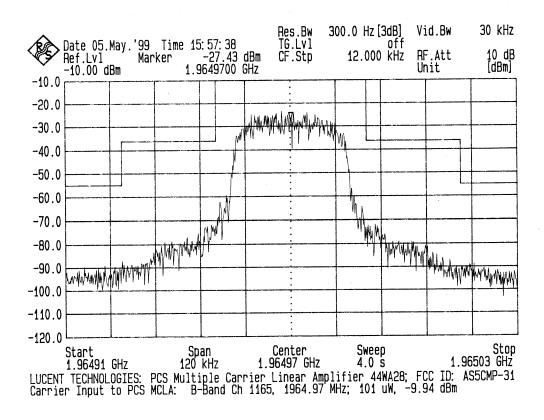
OCCUPIED BANDWIDTH PLOTS:



PCS B-Block: Upper Edge Channel

Channel 1165, 1964.97 MHz

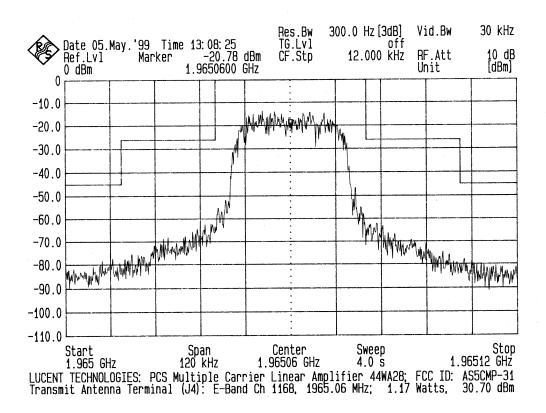
OCCUPIED BANDWIDTH PLOTS:



PCS B-Block: Upper Edge Channel

Channel 1165, 1964.97 MHz

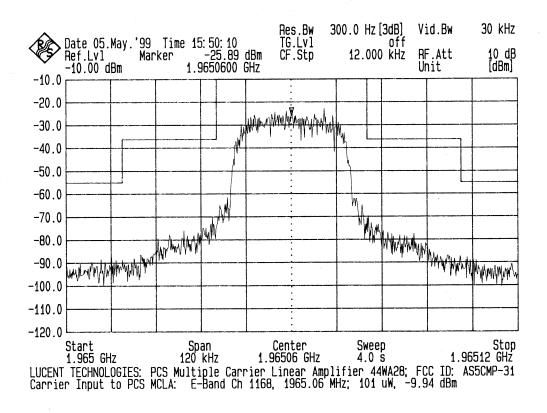
OCCUPIED BANDWIDTH PLOTS:



PCS E-Block: Lower Edge Channel

Channel 1168, 1965.06 MHz

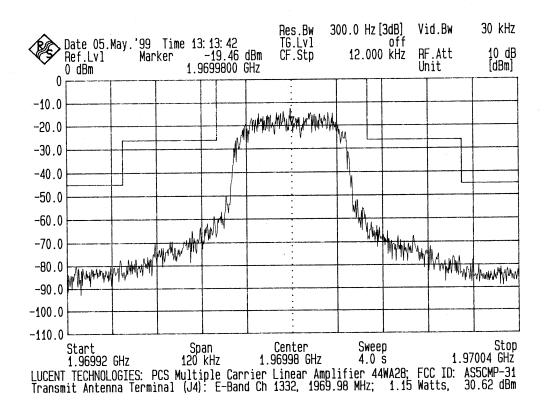
OCCUPIED BANDWIDTH PLOTS:



PCS E-Block: Lower Edge Channel

Channel 1168, 1965.06 MHz

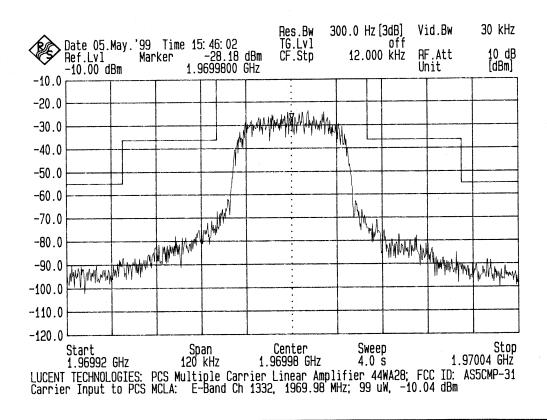
OCCUPIED BANDWIDTH PLOTS:



PCS E-Block: Upper Edge Channel

Channel 1332, 1969.98 MHz

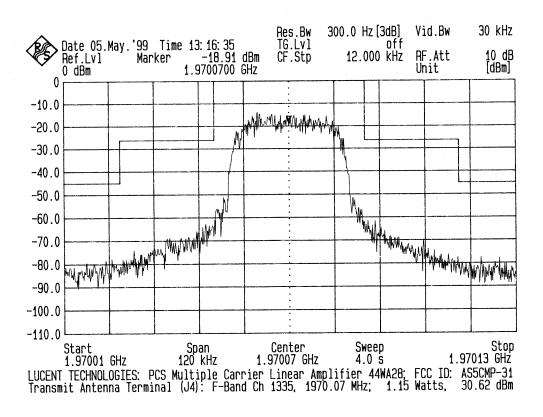
OCCUPIED BANDWIDTH PLOTS:



PCS E-Block: Upper Edge Channel

Channel 1332, 1969.98 MHz

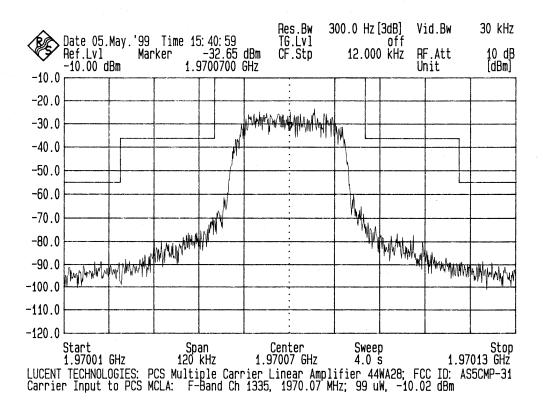
OCCUPIED BANDWIDTH PLOTS:



PCS F-Block: Lower Edge Channel

Channel 1335, 1970.07 MHz

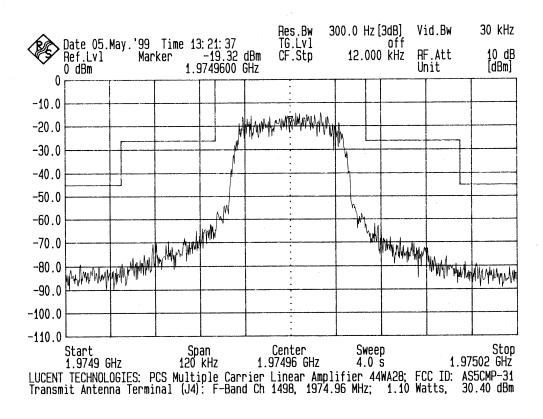
OCCUPIED BANDWIDTH PLOTS:



PCS F-Block: Lower Edge Channel

Channel 1335, 1970.07 MHz

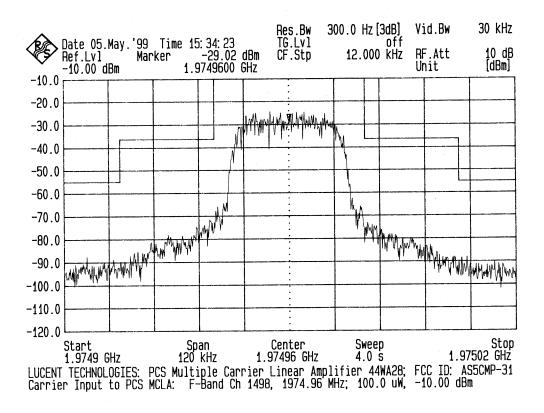
OCCUPIED BANDWIDTH PLOTS:



PCS F-Block: Upper Edge Channel

Channel 1498, 1974.96 MHz

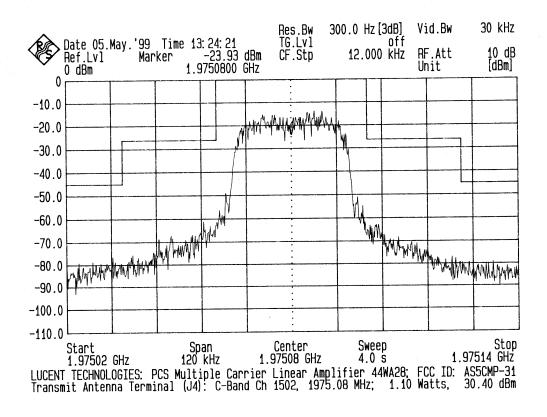
OCCUPIED BANDWIDTH PLOTS:



PCS F-Block: Upper Edge Channel

Channel 1498, 1974.96 MHz

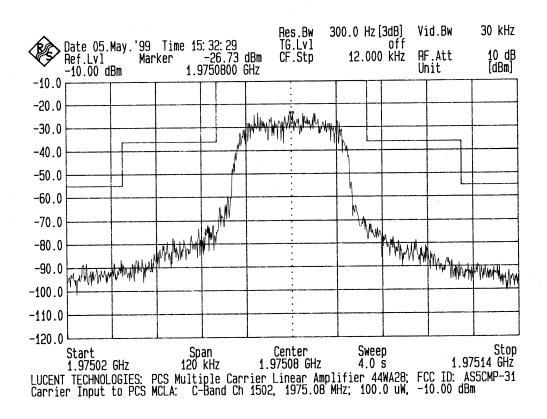
OCCUPIED BANDWIDTH PLOTS:



PCS C-Block: Lower Edge Channel

Channel 1502, 1975.08 MHz

OCCUPIED BANDWIDTH PLOTS:

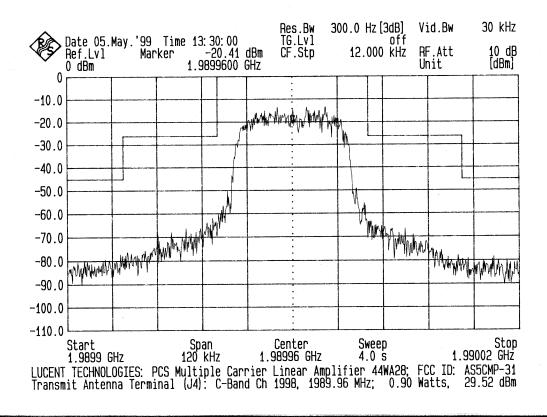


PCS C-Block: Lower Edge Channel

Channel 1502, 1975.08 MHz

EXHIBIT 16

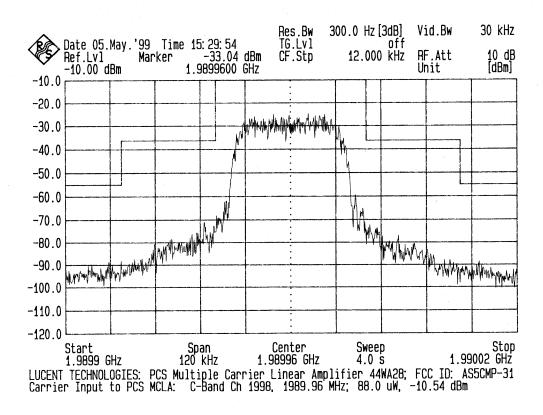
OCCUPIED BANDWIDTH PLOTS:



PCS C-Block: Upper Edge Channel

Channel 1998, 1989.96 MHz

OCCUPIED BANDWIDTH PLOTS:



PCS C-Block: Upper Edge Channel

Channel 1998, 1989.96 MHz