APPROVAL SHEET

QCC743M LGA Module

Halogens Free Product

P/N:RFIQM0743010NB001

Customer：_____

Customer ‘s Part No.：_____

Approval No.：_____

Issue Date：_____

*Contents in this sheet are subject to change without prior notice.

INPAQ
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品名：**RFIQM0743010NB001** **History List**

版本 REV.	修訂者 EDITOR	修訂頁次 PAGE	修訂內容 ITEMS OF CHANGE	申請日期 DATE	生效日期 VALID DATE	ECN 編號 ECN NO.
A0	Huiwenchan	ALL	Temporary Release	2024/10/30	According to the date of PLM Release	N/A

Device description

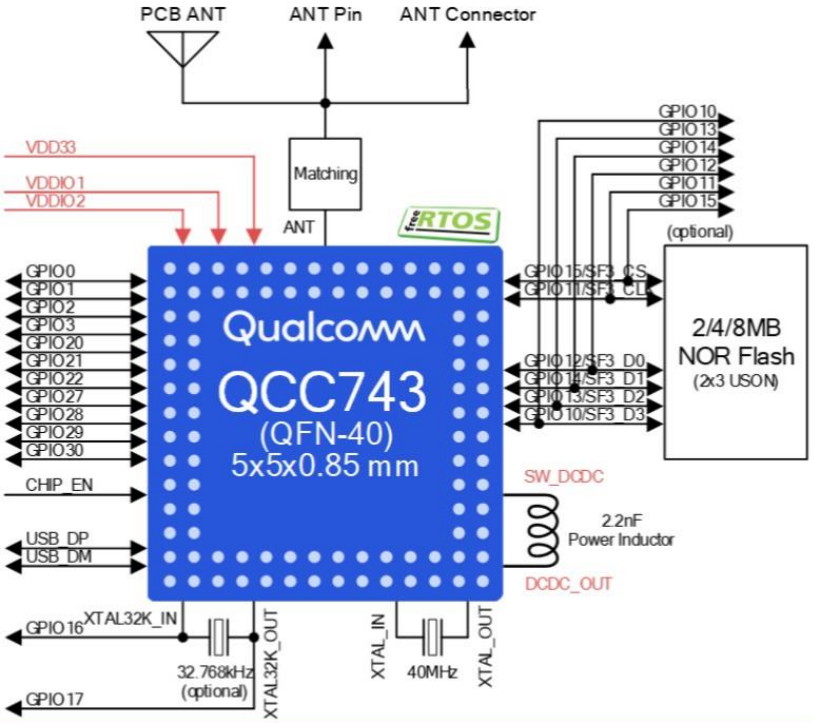
Powered by Qualcomm all-in-one 1x1 2.4 GHz Wi-Fi 6/ Bluetooth/802.15.4 combo all-in-one SoC QCC743, Qualcomm QCC743M LGA module is purposely designed to pack processing capabilities, Wi-Fi/Bluetooth/802.15.4 combo connectivity, and on-module memory into a single 32-pin LGA form factor

Key features

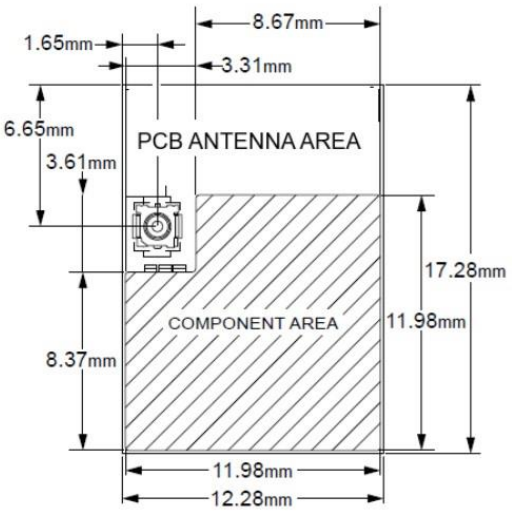
Pin compatible designs

- QCC743M LGA module PCB antenna: 12.28 x 17.28 x 2.2 mm, 1.27 mm pitch, 32-pin, 4-side LGA (4-layer PCB)

QCC743M block diagram and package outline drawings



GPIO Count	RTC	External Flash
11	Yes	Yes
13	No	Yes
19	No	No



QCC743M LGA Module
PCB Antenna

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DESIGNED BY：黃瑞郎	APPROVED BY：陳振榮		
TITLE：RFIQM0743010NB001		DOCUMENT NO.	ENS070033820-000803723839 / SPEC REV. A0

Contents

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TITLE：RFIQM0743010NB001		DOCUMENT NO. ENS070033820-000803723839	SPEC REV. A0

1 Introduction

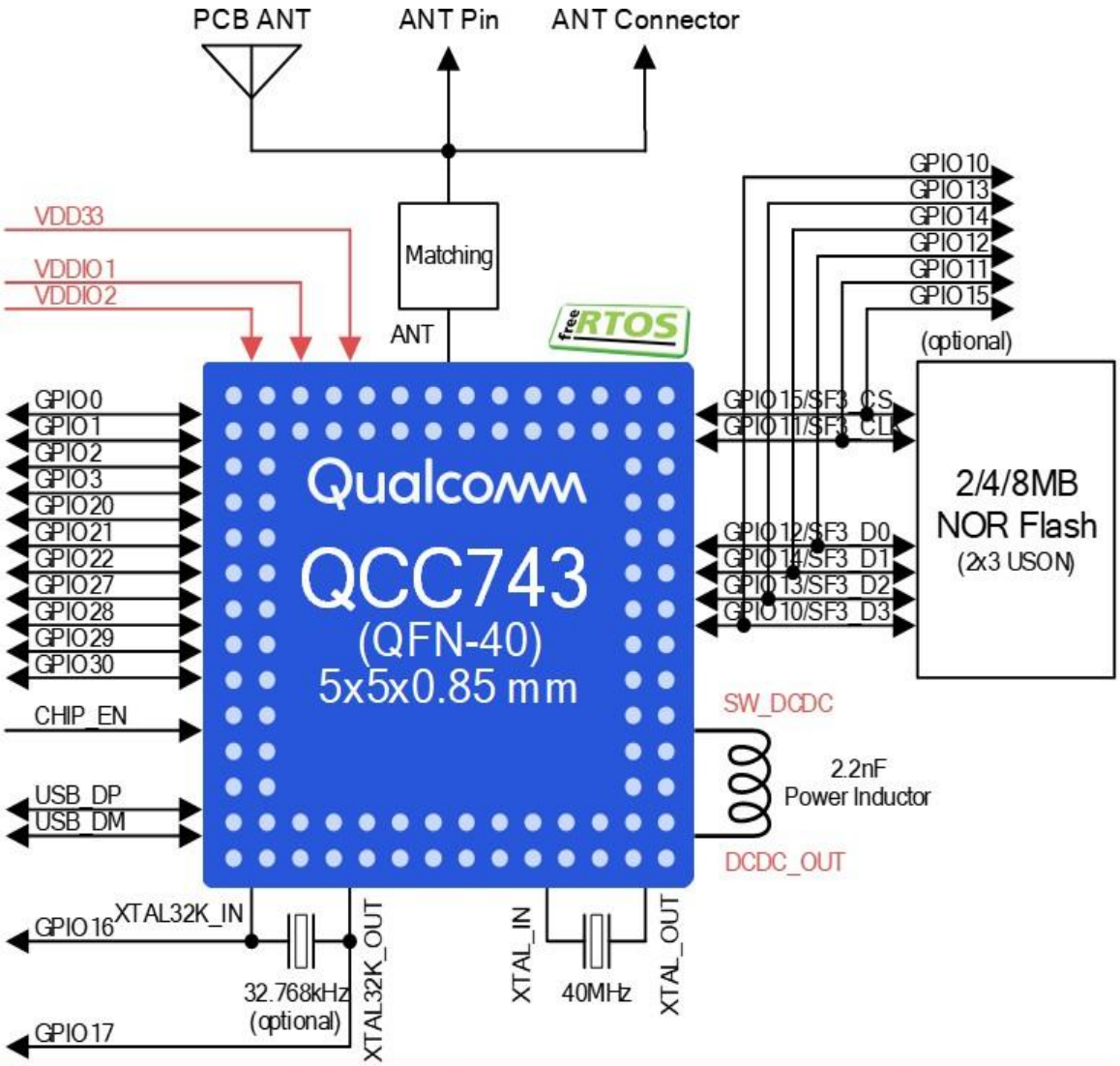
1.1 Product overview

Powered by Qualcomm high performance 1x1 2.4 GHz Wi-Fi 6/Bluetooth 5.3/802.15.4 combo all-in-one SoC QCC743, Qualcomm QCC743M LGA module is purposely designed to pack processing capabilities, Wi-Fi/Bluetooth/
802.15.4 combo connectivity, and on-module memory into a single 32-pin LGA form factor. QCC743M has an integrated powerful 32-bit RISC-V processor with FPU and DSP running up to 325 MHz, on-chip 484 KB SRAM and 128 KB ROM. Its all-in-one design and capability contribute to reduced costs and enhanced performance, making it an attractive choice for IoT edge devices requiring a single chip solution.

QCC743M operates in hostless mode, capable of running both the protocol stack all the way to application level as well as IoT applications without requiring an external MCU. Built on FreeRTOS, its software SDK is open-sourced on codelinaro coupled with VS Code IDE market extension to facilitate rapid IoT application development. It can also be used as an IoT connectivity transceiver in hosted mode with an external host running all upper protocol stacks and applications.

1.2 QCC743M functional block diagram

QCC743M integrates 2/4/8MB 2x3 USON NOR Flash and optional 32kHz RTC crystal. The design also supports PCB antenna or simply provides antenna pin to allow customized antenna implementation on the motherboard. The block diagram is shown below.



GPIO Count	RTC	External Flash
11	Yes	Yes
13	No	Yes
19	No	No

1.3 QCC743M features

Features	Capability
Microcontroller	32-bit RISC-V processor up to 325 MHz
On-chip Memory	▪ 484 KB SRAM ▪ 128 KB ROM ▪ 1/2/4 KB OTP ▪ 4 Kb eFuse
Security System	▪ Security System encryption engine ▪ Secure services (boot, debug, OTA, OTFAD, and so on)
Standard	▪ 802.11b/g/n/ax ▪ Bluetooth Classic/Low Energy 5.3 dual mode ▪ IEEE 802.15.4
Wi-Fi	▪ Max Tx Power (HE40 and MCS9): +16 dBm ▪ Rx Sensitivity (HE40 and MCS9): -67 dBm ▪ Active Tx Power (HE40 and MCS9): TBD ▪ Active Rx Power (HE40 and MCS9): TBD
802.15.4	▪ Max Tx Power: TBD ▪ Rx Sensitivity: TBD
Bluetooth	▪ Max Tx Power ▫ EDR (3Mbps): +8 dBm ▫ EDR (2Mbps): +8 dBm ▫ BR (1Mbps): +10 dBm ▫ BLE (2Mbps): +10 dBm ▫ BLE (1Mbps): +10 dBm ▫ BLE Coded PHY (500 kbps): +10 dBm ▫ BLE Coded PHY (125 kbps): +10 dBm ▪ Active Tx Power: TBD ▪ Rx Sensitivity ▫ EDR (3Mbps): -90 dBm ▫ EDR (2Mbps): -96 dBm ▫ BR (1Mbps): -94 dBm ▫ BLE (2Mbps): -97 dBm ▫ BLE (1Mbps): -99 dBm ▫ BLE Coded PHY (500 kbps): -102 dBm ▫ BLE Coded PHY (125 kbps): -105 dBm ▪ Active Rx Power: TBD

Features	Capability
Peripherals	19 configurable I/O: ▪ Serial Flash ▪ SD/MMC ▪ SDIO 2.0 ▪ QSPI ▪ SPI ▪ I2C ▪ UART ▪ I2S ▪ CAN bus (ISO11898) ▪ MIPI-DBI ▪ DVP ▪ PWM ▪ ADC ▪ DAC ▪ JTAG
Voltage	▪ Input voltage: 2.97 V~3.63 V ▪ I/O voltage: 1.8 V/3.3 V
Environmental	▪ Temperature ▫ Operating: -40°C ~ 105°C ▫ Storage: -40°C ~ 85°C ▪ Humidity ▫ Relative: < 90% Non-condensing ▫ Storage: < 90% Non-condensing

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pin type) parameters

Symbol	Description
Pin attribute	
AI	Analog input (does not include pin circuitry)
AO	Analog output (does not include pin circuitry)
DI	Digital input (CMOS)
DO	Digital output (CMOS)

2.2 Pin assignments

2.2.1 Pin map

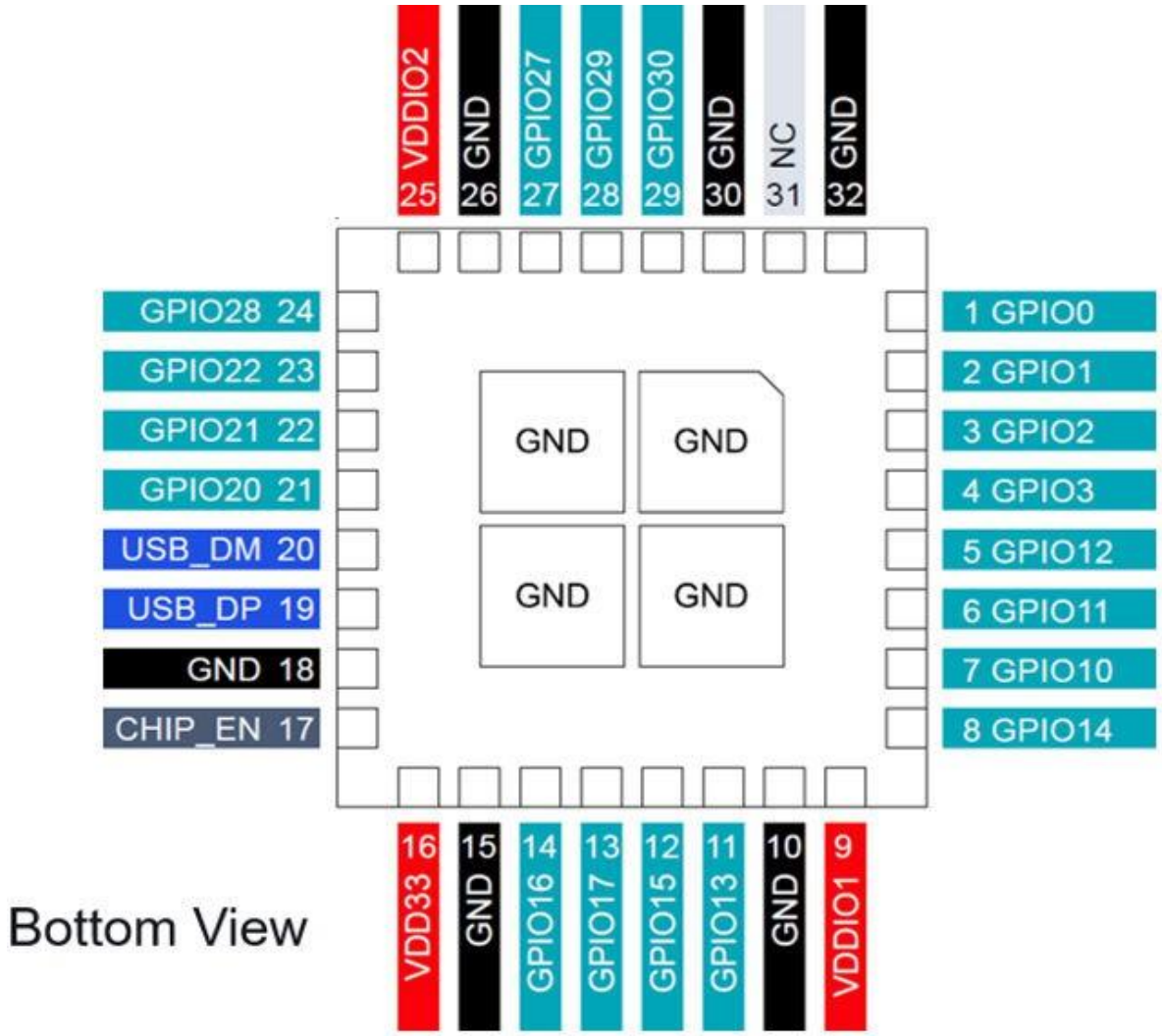


Figure 2-1QCC743M LGA module PCB antenna

2.3 Pin definition

Pin	Pin name	Type	Power domain	Description
16	VDD33	PWR	–	Power input (2.97V~3.63V)
9	VDDIO1	PWR	–	Host I/O voltage input GPIO0~15
25	VDDIO2	PWR	–	Host I/O voltage input GPIO20~30
10, 15, 18, 26, 30, 32	GND	GND	GND	Ground
31	ANT	AI/AO	–	Pin antenna for QCC743M LGA module antenna pin
	NC	–	–	NC for QCC743M LGA module antenna connector and QCC743M LGA module PCB antenna
19	USB_DP [a]	AI/AO	–	USB data plus
20	USB_DM [b]	AI/AO	–	USB data minus
17	CHIP_EN	DI	–	Chip power on
1	GPIO0	DI/DO	VDDIO1	General purpose I/O
2	GPIO1	DI/DO	VDDIO1	General purpose I/O
3	GPIO2	DI/DO	VDDIO1	General purpose I/O
4	GPIO3	DI/DO	VDDIO1	General purpose I/O
5	GPIO12	DI/DO	VDDIO1	General purpose I/O
6	GPIO11	DI/DO	VDDIO1	General purpose I/O
7	GPIO10	DI/DO	VDDIO1	General purpose I/O
8	GPIO14	DI/DO	VDDIO1	General purpose I/O
11	GPIO13	DI/DO	VDDIO1	General purpose I/O
12	GPIO15	DI/DO	VDDIO1	General purpose I/O
13	GPIO17	DI/DO	VDD33	General purpose I/O
14	GPIO16	DI/DO	VDD33	General purpose I/O
21	GPIO20	DI/DO	VDDIO2	General purpose I/O
22	GPIO21	DI/DO	VDDIO2	General purpose I/O
23	GPIO22	DI/DO	VDDIO2	General purpose I/O
24	GPIO28	DI/DO	VDDIO2	General purpose I/O
27	GPIO27	DI/DO	VDDIO2	General purpose I/O
28	GPIO29	DI/DO	VDDIO2	General purpose I/O
29	GPIO30	DI/DO	VDDIO2	General purpose I/O

a USB_DP functionality will be supported in future chip-spin.

b USB_DM functionality will be supported in future chip-spin.

2.4 GPIO pin mux table

GPIO	QSPI	SDIO	SDH	SPI	I2C (0/1)	UART (0/1)	I2S	PWM	CAN	ADC	DAC	DVP	DBI	JTAG
GPIO0	–	–	–	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX	CH9	–	CAM1_VSYNC	–	TMS
GPIO1	–	–	–	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX	CH8	–	CAM1_HSYNC	–	TCK
GPIO2	–	–	–	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX	CH2	–	–	–	TDO
GPIO3	–	–	–	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	CH3	–	CAM1_DAT0	–	TDI
GPIO10	SCL	DAT2	DAT1	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH1P	TX/RX	CH7	–	CAM1_DAT1	C_SDA0	TDO
GPIO11	CS	DAT3	DAT0	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	–	–	CAM1_DAT2	C_DCn	TDI
GPIO12	SDA0	CMD	CLK	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH6	–	CAM1_DAT3	C_SCL	TMS
GPIO13	SDA1	CLK	CMD	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	CH5	–	CAM1_CLK	C_CSn	TCK
GPIO14	SDA2	DAT0	DAT3	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	CH4	A_PWM_P	CAM1_DAT4	C_SDA0	TDO
GPIO15	SDA3	DAT1	DAT2	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH3N	TX/RX	–	A_PWM_N	CAM1_DAT5	C_DCn	TDI
GPIO16	–	–	–	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH0P	TX/RX	–	–	CAM1_DAT6	–	TMS
GPIO17	–	–	–	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH0N	TX/RX	–	–	CAM1_DAT7	–	TCK
GPIO20	–	–	–	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH0/ACH0	–	–	–	TMS
GPIO21	–	–	–	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	ACH1	–	–	–	TCK
GPIO22	–	–	–	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	ACH2	A_PWM_P	–	–	TDO
GPIO27	–	–	–	MOSI	SDA	RTS/CTS/TX/RX	DO	CH3P/CH1N	TX/RX	CH10/ACH4	A_PWN_N	–	–	TDI
GPIO28	–	–	–	CS	SCL	RTS/CTS/TX/RX	BCLK	CH0P/CH2P	TX/RX	CH11/ACH5	A_PWM_P	–	–	TMS
GPIO29	–	–	–	CLK	SDA	RTS/CTS/TX/RX	FS	CH1P/CH2N	TX/RX	ACH6	–	–	–	TCK
GPIO30	–	–	–	MISO	SCL	RTS/CTS/TX/RX	DI	CH2P/CH3P	TX/RX	ACH7	–	–	–	TDO

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings provided in this section reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating.

Pin	Parameter	Min	Max	Unit
VDD33	Power input voltage	-0.3	3.63	V
VDDIO1, VDDIO 2	I/O port voltage	-0.3	3.63	V
ESD Protection (HBM)	–	–	2,000	V
Storage temperature	–	-40	135	°C

3.2 Operating conditions

Pin	Parameter	Min	TYP	Max	Unit
VDD33	Power input voltage	2.97	3.3	3.63	V
VDDIO1, VDDIO 2 (3.3V)	I/O port voltage	2.97	3.3	3.63	V
VDDIO1, VDDIO 2 (1.8V)	I/O port voltage	1.62	1.8	1.98	V

3.3 Radio performance

The radio performance for Wi-Fi, Bluetooth and 802.15.4 are shown in the table below:

3.3.1 802.11b/g/n/ax

Standard	PHY	Modulation	MCS Index	Data ate (Mbps)		Max Tx Power (dBm)		Rx Sensitivity (dBm)	
				HT20	HT40	HT20	HT40	HT20	HT40
802.11b	CCK (DSSS)	DBPSK	–	1	–	22	–	–	–
	CCK (DSSS)	DQPSK	–	2	–	–	–	–	–
	CCK (DSSS)	B/DQPSK	–	5.5	–	–	–	–	–
	CCK (DSSS)	Q/DQPSK	–	11	–	22	–	–	–
802.11g	OFDM	BPSK	–	6	–	21	–	–	–
	OFDM	BPSK	–	9	–	–	–	–	–
	OFDM	QPSK	–	12	–	–	–	–	–
	OFDM	QPSK	–	18	–	–	–	–	–
	OFDM	16QAM	–	24	–	–	–	–	–
	OFDM	16QAM	–	36	–	–	–	–	–
	OFDM	64QAM	–	48	–	–	–	–	–
	OFDM	64QAM	–	54	–	19	–	–	–
802.11n	OFDM	BPSK	MCS0	7.2	15	20	20	-93	-89.5
	OFDM	QPSK	MCS1	14.4	30	–	–	-91	-88
	OFDM	QPSK	MCS2	21.7	45	–	–	-89	-86
	OFDM	16QAM	MCS3	28.9	60	–	–	-86.5	-83.5
	OFDM	16QAM	MCS4	43.3	90	–	–	-83	-80.5
	OFDM	64QAM	MCS5	57.8	120	–	–	-79	-76.5
	OFDM	64QAM	MCS6	65	135	–	–	-77.5	-75
	OFDM	64QAM	MCS7	72.2	150	19	18	-76	-73
802.11ax	OFDMA	BPSK	MCS0	8.6	17.2	20	20	-93	-89.5
	OFDMA	QPSK	MCS1	17.2	34.4	–	–	-91	-88
	OFDMA	QPSK	MCS2	25.8	51.6	–	–	-89	-86.5
	OFDMA	16QAM	MCS3	34.4	68.8	–	–	-86	-83.5
	OFDMA	16QAM	MCS4	51.6	103.2	–	–	-83	-80
	OFDMA	64QAM	MCS5	68.8	137.6	–	–	-79	-76.5
	OFDMA	64QAM	MCS6	77.4	154.9	–	–	-77.5	-75
	OFDMA	64QAM	MCS7	86	172.1	–	–	-75.5	-73
	OFDMA	256QAM	MCS8	103.2	206.5	–	–	-72	-69
	OFDMA	256QAM	MCS9	114.7	229.4	18	16	-70	-67

3.3.2 Bluetooth

Standard	Topology	PHY	Modulation	Data Rate	Max Tx Power (dBm)	Rx Sensitivity (dBm)
BT Classic	P2P	BR	GFSK	1Mbps	+10	-94
		EDR	π/4 DQPSK	2Mbps	+8	-96
		EDR	8DPSK	3Mbps	+8	-90
BLE	P2P Broadcast Mesh	LE 2M	GFSK	2Mbps	+10	-97
		LE 1M	GFSK	1Mbps	+10	-99
		LE Coded (S=2)	GFSK	500Kbps	+10	-102
		LE Coded (S=8)	GFSK	125Kbps	+10	-105

3.3.3 802.15.4

This information will be included in future revisions of this document.

3.4 Power consumption

QCC743M can operate in four power states as shown below to maximize power saving:

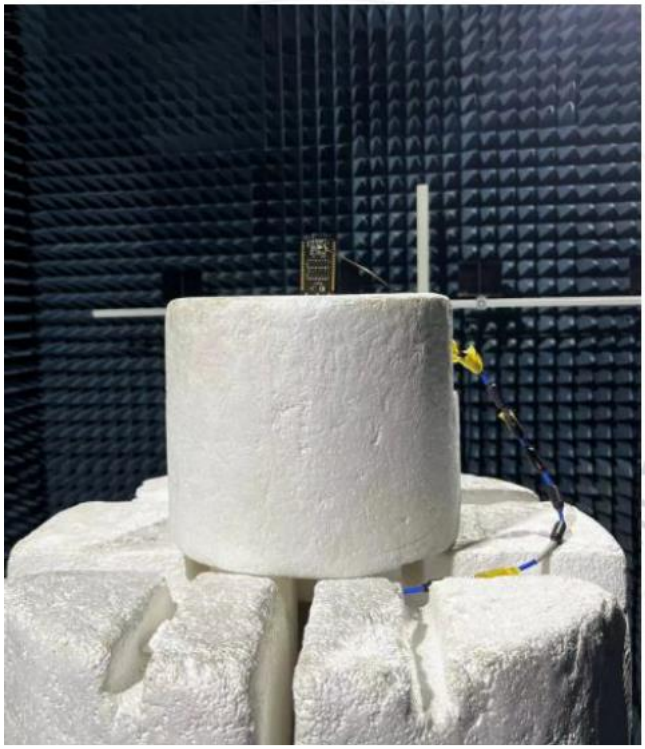
- Active – Continuous transmitting or receiving on connection to AP
- Idle – No active transmitting or receiving. CPU is in idle state.
- Deep Sleep – Wi-Fi/USB/CPU/Peripherals power off. This is DTIM power saving mode
- Hibernation – No connection to AP.
- Shut down – the chip is completed shut down
- The power consumption for each state is listed in the table below:

Operation Mode	State	Typical	Unit	Comments
Active	MCU Active & Rx Active	38	mA	MCU 160MHz, XCLK 40MHz, BCLK 80MHz, Flash 40MHz
	Tx Active	266	mA	MCS0, Tx Power = +18 dBm
Power Saving	Deep Sleep	64	µA	Wi-Fi/USB/CPU/Peripherals Power Off. This is DTIM PS mode
	Hibernation	2.1	µA	4KB RAM retained
	Shut Down	0.15	µA	–
DTIM	DTIM 1	476	µA	Xtal32k
		524	µA	RC 32k
	DTIM 3	179	µA	Xtal32k
		227	µA	RC 32k
	DTIM 5	119	µA	Xtal32k
		167	µA	RC 32k
	DTIM 10	75	µA	Xtal32k
		123	µA	RC 32k

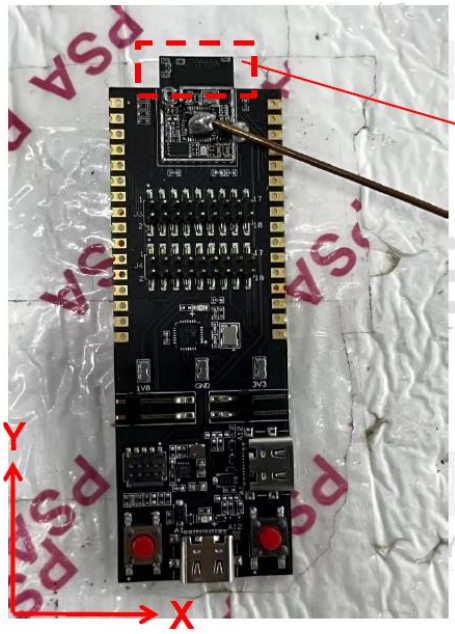
4 Antenna Electrical specifications

4.1 Measurement Information

4.1.1 Experimental Setup



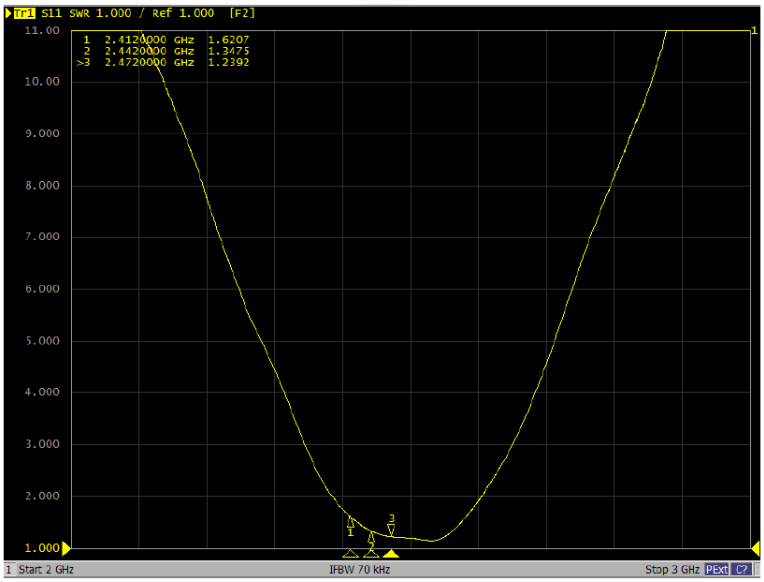
4.1.2 Antenna Solution Detail



Printed antenna design
Tiny height: 5mm
Good performance

4.2 Antenna Characteristics: Passive and Active

4.2.1 VSWR



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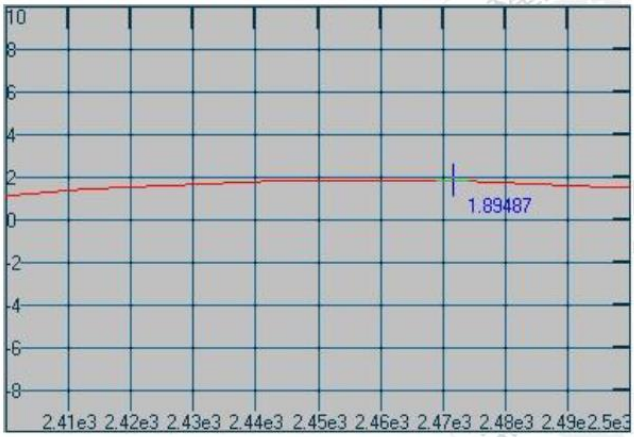
TITLE：RFIQM0743010NB001		DOCUMENT NO. ENS070033820-000803723839	SPEC REV. A0

4.2.2 Antenna Efficiency and Peak Gain

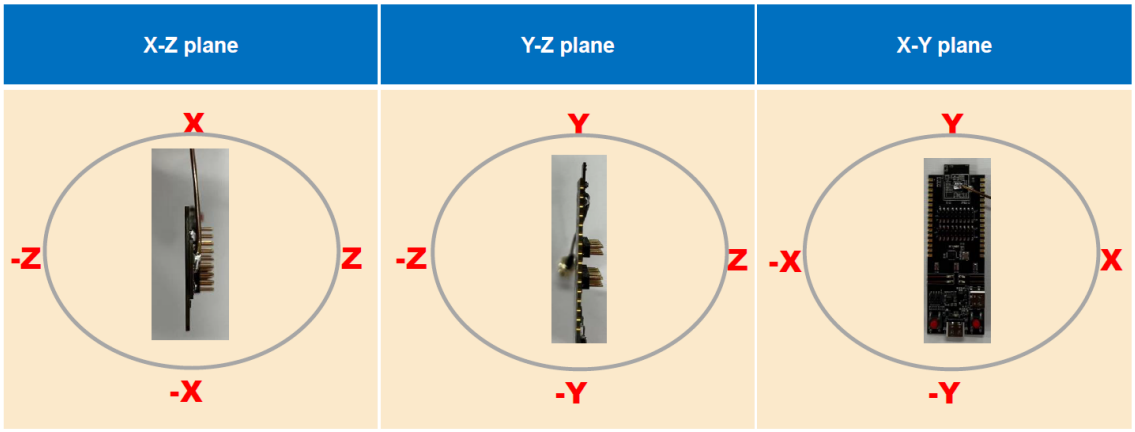


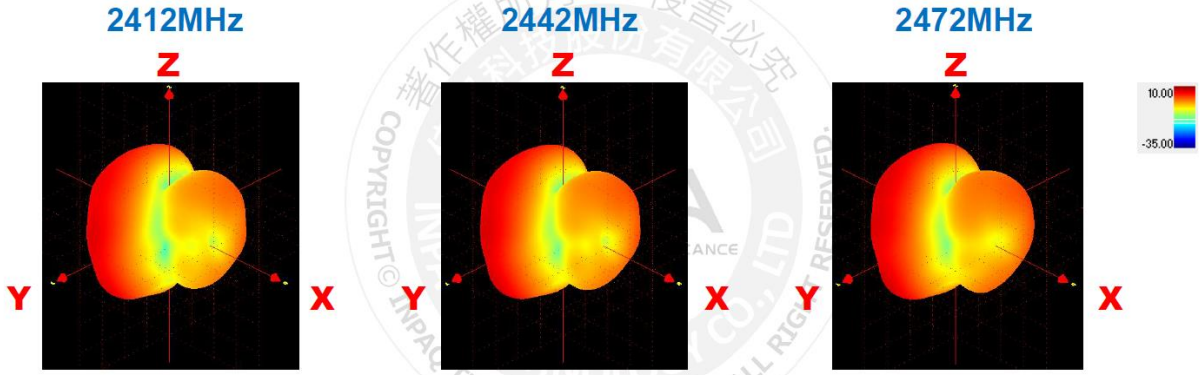
Maximum Peak Gain at 2472 MHz : 1.89dBi

Maximum Efficiency at 2472 MHz : 44.32%

Frequency(MHz)	Efficiency(%)	Peak gain(dBi)
2412	37.99	1.47
2417	38.78	1.54
2422	39.55	1.61
2427	40.33	1.67
2432	41.10	1.74
2437	41.88	1.81
2442	42.59	1.87
2447	42.91	1.87
2452	43.14	1.88
2457	43.44	1.88
2462	43.74	1.89
2467	44.03	1.89
2472	44.34	1.89
2484	43.93	1.74

4.2.3 3D Pattern & 3 views of antenna & 2D Radiation Patterns

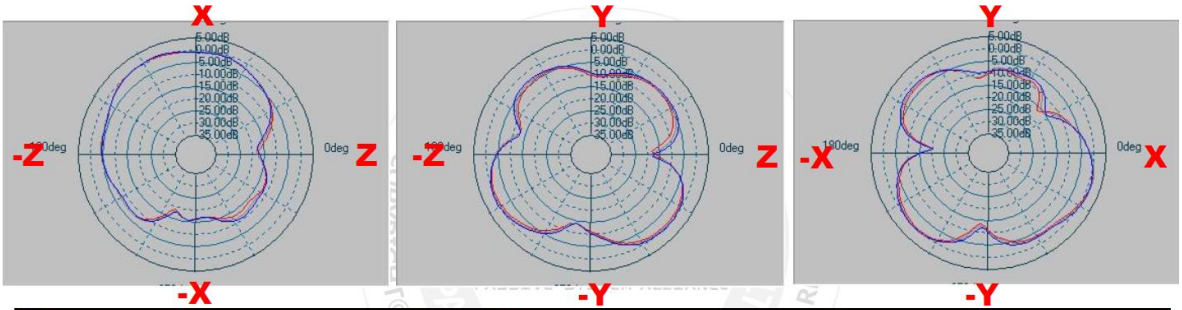




Peak gain 1.47dBi
Ave. gain -4.20dBi

Peak gain 1.87dBi
Ave. gain -3.70dBi

Peak gain 1.89dBi
Ave. gain -3.53dBi



	ZX plane		ZY plane		XY plane	
Frequency [MHz]	Max Value [dBi]	Average [dBi]	Max Value [dBi]	Average [dBi]	Max Value [dBi]	Average [dBi]
2412	-0.26	-5.17	-0.67	-5.02	1.27	-4.28
2442	-0.06	-5.01	-0.12	-4.45	1.49	-3.78
2472	-0.10	-5.18	0.17	-4.11	1.13	-3.68

5 Mechanical information

5.1 Device physical dimensions

1.1.1 QCC743M LGA module PCB antenna

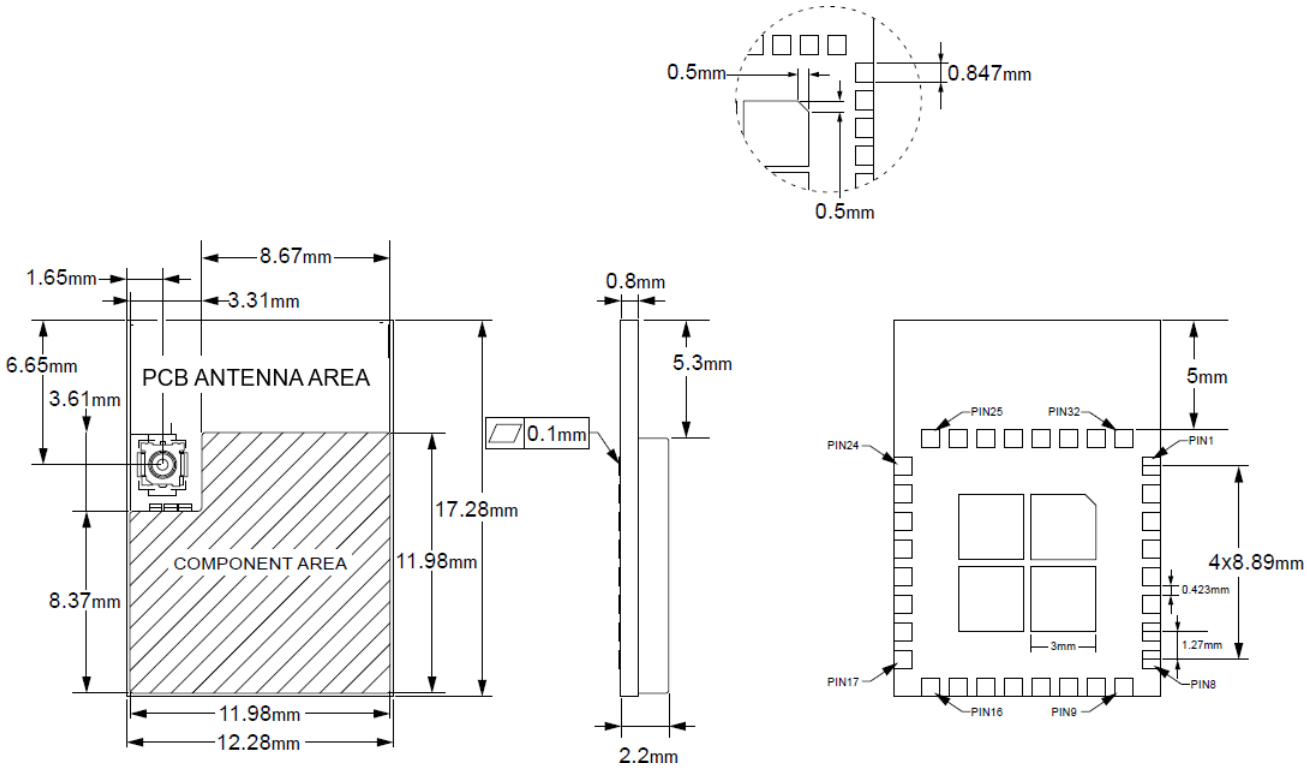


Figure 4-1QCC743M LGA module PCB antenna dimension

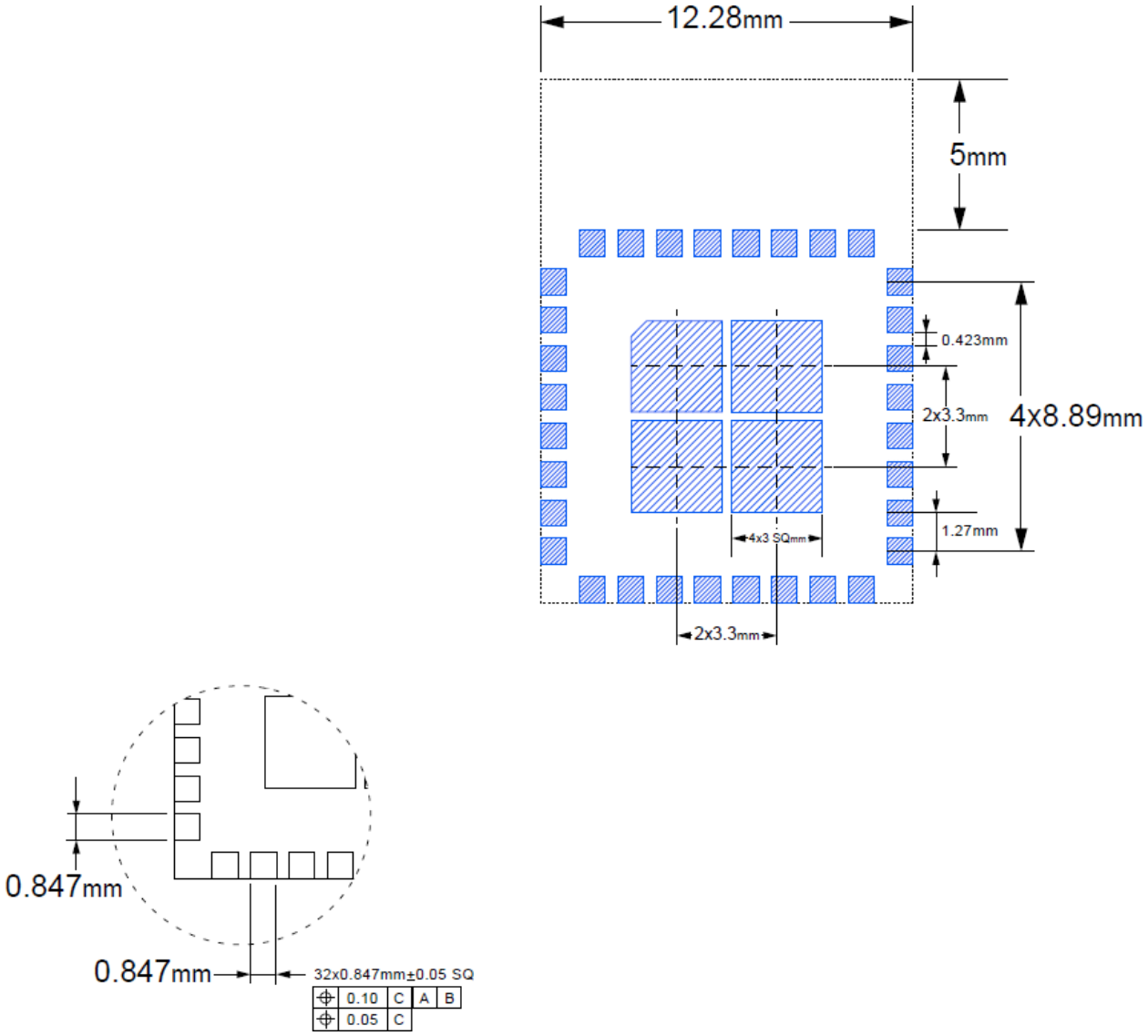


Figure 4-2QCC743M LGA module PCB antenna landing pad

UNLESS OTHER SPECIFIED TOLERANCES ON： X＝N/A X.X＝N/A X.XX＝N/A ANGLES＝N/A HOLEDIA＝N/A			INPAQ TECHNOLOGY CO., LTD.
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DRAWN BY：詹惠雯	CHECKED BY：詹惠雯		
DESIGNED BY：黃瑞郎	APPROVED BY：陳振榮		
TITLE：RFIQM0743010NB001		DOCUMENT NO.	ENS070033820-000803723839 SPEC REV. A0

5.2 Part marking

This information will be included in future revisions of this document.

5.3 Device ordering information

This information will be included in future revisions of this document.

6 Carrier, storage, and handling information

This information will be included in future revisions of this document.

7 Manufacturing guidelines

7.1 Power layout guideline

QCC743M is powered by either 3V battery or DC 3.3V. Power pin connection capacitor is as close as possible to chip and pin. Decoupling the power supply from the chip using a capacitor. Use capacitors to prevent noise from coupling back to the power plane.

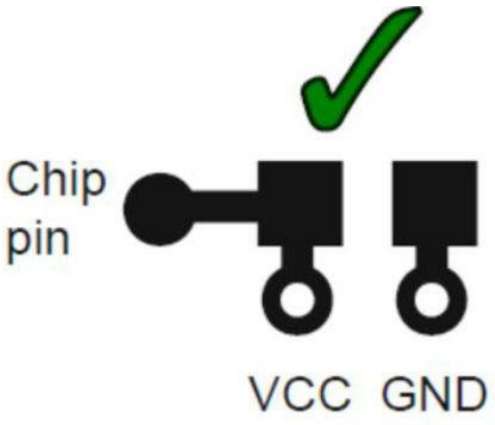

Figure 6-1 Power layout guideline

7.2 RF layout guideline

To optimize antenna performance, place QCC743M in the corner of the PCB as shown below. Do not cover copper and trace the antenna clearance area. Keep the antenna area as far away as possible from the power supply and metal components. Connect all GND pins directly to a solid GND plane. Place GND vias as close as possible to the GND pin. Use a good layout method to avoid excessive noise coupling with signal lines or supply voltage lines.

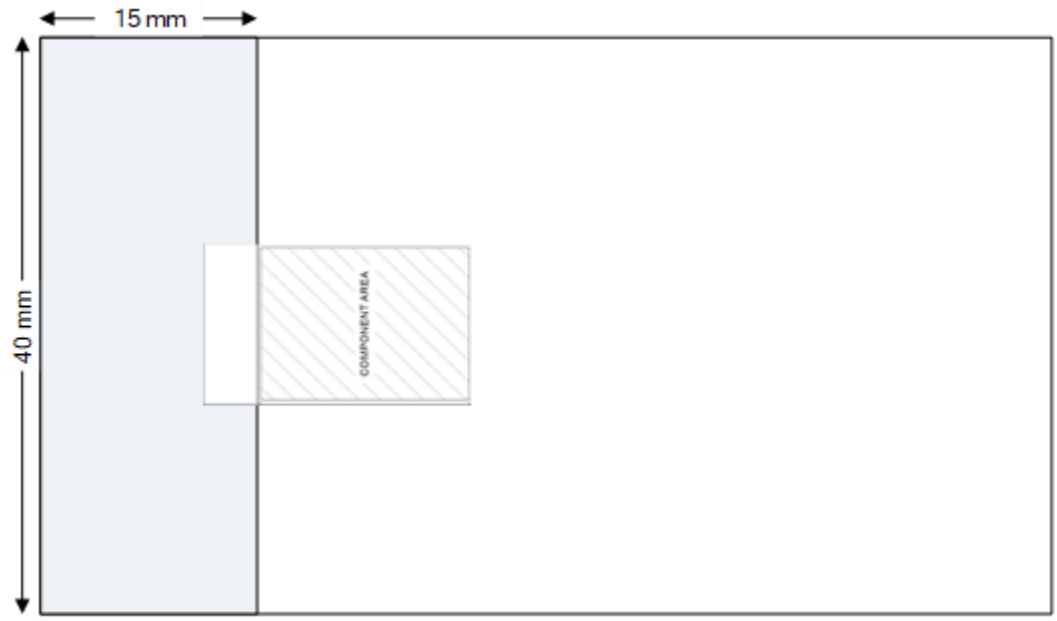

Figure 6-2 RF layout guideline

7.3 Soldering guideline

QCC743M can be SMT on the board following the temperature curve graph:

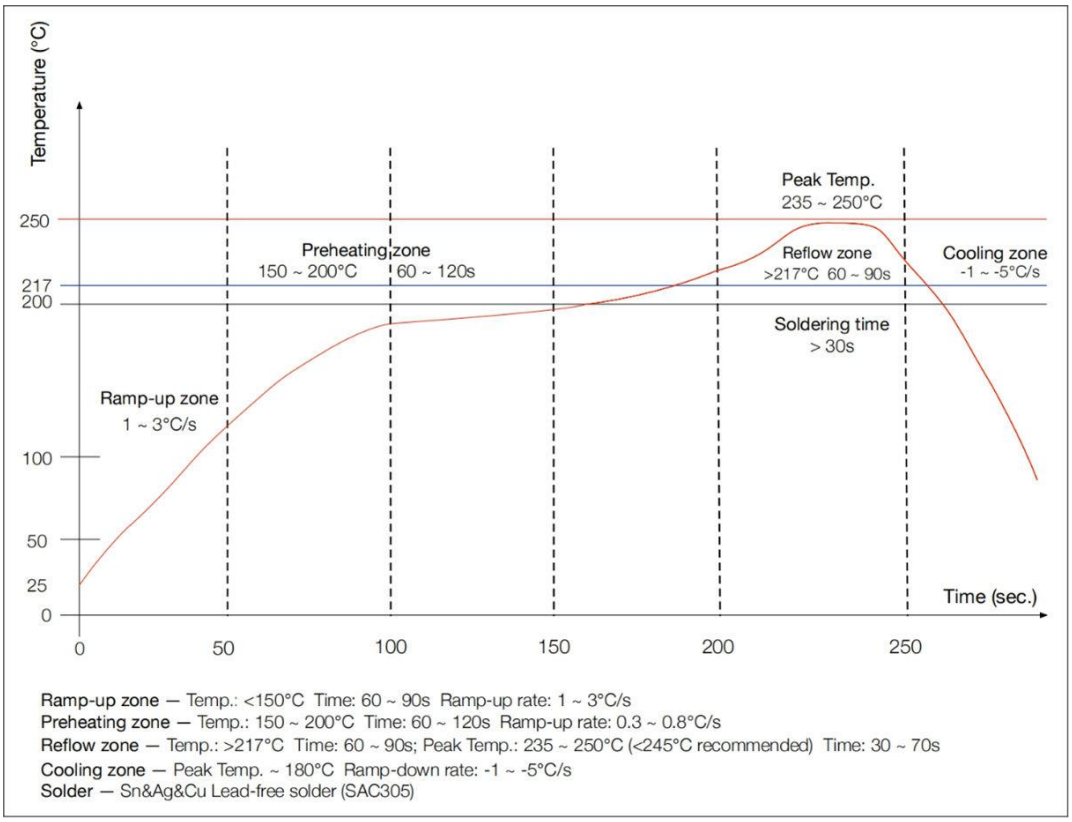

Figure 6-3 QCC743M soldering guideline

8 Part reliability

This information will be included in future revisions of this document.

Revision history

Revision	Date	Description
AA	Aug 2024	Initial release

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