SECTION 5 CIRCUIT DESCRIPTION

5.1 GENERAL TRANSCEIVER DESRIPTION

5.1.1 INTRODUCTION

The EFJohnson Stealth 25 Digital Radio is a microcontroller-based radio that uses a Digital Signal Processor (DSP) to provide the following modes of operation:

Narrowband Analog - FM modulation with a maximum deviation of 2.5 kHz. This mode is usually used in systems where the channel spacing is 12.5 kHz. Call Guard (CTCSS or DCS) subaudible squelch signaling can be used in this mode.

Wideband Analog - FM modulation with a maximum deviation of 5 kHz. This mode is usually used in systems where the channel spacing is 25 kHz or 30 kHz. Call Guard (CTCSS or DCS) subaudible squelch signaling can be used in this mode.

Project 25 Digital - The voice is digitized, error corrected, optionally encrypted and transmitted using C4FM modulation according to the Project 25 standard. This mode can be used in channel spacings of 12.5 kHz.

DES/DES-XL - This mode is compatible with the Motorola DES and DES-XL protocols. Voice is digitized, encrypted, and transmitted using FSK modulation. This mode can be used in channel spacings of 25 kHz. The DSP processes the received signals and generates the appropriate output signals. The microcontroller controls the hardware and provides an interface between hardware and DSP.

5.1.2 PC BOARDS

The 5300-series mobile contains the following PC board assemblies:

RF Board - Contains the receiver, synthesizer, and exciter sections.

PA Board - Contains the transmitter power amplifier, power control, and main DC power switching sections.

Logic Board - Contains the digital signal processing (DSP), control logic, and audio processing sections.

Interface Board - A small board that provides the electrical connections between the logic and RF/PA boards. It also contains the audio amplifier and volume control circuits for internal and external speakers.

Display Controller - Contains a microcontroller which provides an interface between the controller on the logic board and the front panel display and switches.

Display Board - Contains the liquid crystal display, option switch keypad, and display drivers. In addition, it contains the backlight for the display and keypad.

5.1.3 CIRCUIT PROTECTION (FUSES)

Circuit protection is provided as follows:

- A 15-ampere fuse in the power cable provides overall transceiver protection.
- A 2-ampere fuse on the RF board protects circuits on that board.
- F700 (2-ampere) on the display controller board protects the Sw B+ output of the microphone connector.
- F1 on the logic board protects the Sw B+ output of universal interface connector J5.
- The various voltage regulators provide circuit protection by automatically limiting current.

5.1.4 ANALOG MODE DESCRIPTION

Receive Mode

The RF signal is routed from the antenna connector to the RF Board where it is filtered, amplified, and mixed with the first local oscillator frequency generated by the synthesizer. The resulting IF signal is also filtered and amplified and sent to the ABACUS chip.

The signal is then mixed with the second local oscillator frequency to create a second IF signal of 450 kHz. The second IF signal is then sampled at 14.4 Msps and downconverted to baseband. The baseband

signal is then decimated to a lower sample rate that is selectable at 20 kHz. This signal is then routed via a serial interface using a differential current output to the ADSIC U3 on the logic board.

On the logic board ADSIC U3 digitally filters the input signal, performs frequency discrimination to obtain the message signal, and then routes the message signal to DSP (Digital Signal Processor) U12. The DSP first performs a carrier-detection squelch function on the radio. If a signal is determined to be present, the audio portion of the signal is resampled to an 8 kHz rate and then filtered appropriately. The filtered signal is then routed back to a D/A in the ADSIC to produce an analog signal for output to the audio power amplifier (PA) and then the speaker. Any detected signaling information is decoded and the resulting information is sent to the microcontroller.

Transmit Mode

The signal from the microphone is amplified by the audio PA and is then routed to ADSIC U3 where it is first digitized at a 16 ksps rate and then sent to DSP U12. The DSP performs the required filtering, adds the desired signaling, converts the sample rate to 48 ksps and then sends the resulting signal back to a D/A in the ADSIC to produce the analog modulation signal for the VCO. The modulated VCO signal is then sent to the RF PA for amplification.

5.1.5 PROJECT 25 DIGITAL MODE

Introduction

In Project 25 Digital Mode, the carrier is modulated with four discrete deviation levels of ± 600 Hz and ± 1800 Hz. Digitized voice is created using an IMBE™ vocoder.

Receive Mode

The signal is processed in the same way as an analog mode transmission until after the squelch function is performed. If a signal is detected to be present, DSP U12 resamples the signal from 20 kHz to 24 kHz. This is done so that the sample rate is an integer multiple (5x) of the data rate of the digital modulation which is 4800 symbols/sec (9600 bits/sec).

The resampled signal is then processed by a demodulator routine to extract the digital information. The resulting bit stream (9600 bps) is sent to a routine that performs unframing, error-correction, and voice decoding. The result of these operations is a reconstructed voice signal sampled at 8 kHz. The sampled voice signal is sent to a D/A in ADSIC U3 to produce an analog signal for output to the audio power amplifier and speaker.

Transmit Mode

The microphone signal is processed as in the analog mode until it reaches DSP U12. At this point the audio signal is processed by a voice encoding routine to digitize the information. The resulting samples are then converted to a bit stream that is placed into the proper framing structure and error protected. The resulting bit stream has a bit rate of 9600 Hz.

This bit stream is then encoded, two bits at a time, into a digital level corresponding to one of the four allowable frequency deviations. This produces 16-bit symbols with a rate of 4800 Hz. The symbols are resampled to a rate of 48 kHz and filtered to comply with channel bandwidth requirements. The filtered signal is then sent to a D/A in ADSIC U3 to produce the analog modulation signal for the VCO. The modulated VCO signal is then mixed up to the final transmit frequency and then sent to the RF board power amplifier section.

5.2 RF BOARD

NOTE: The RF Board is not field serviceable. Therefore, it must be replaced if it is defective.

5.2.1 RF BOARD OVERVIEW

The receiver front end consists of a preselector, RF amplifier, second preselector, and mixer (see Figure 5-1). Both preselectors on the VHF and UHF board are varactor-tuned, two-pole filters controlled by the microcontroller unit through the D/A IC. The 800 MHz board uses stripline technology for the preselector. The RF amplifier is a dual-gate gallium-arsenide IC. The mixer is a double-balanced, transformer-coupled active mixer. Injection is provided by the VCO through an injection filter. See Table 5-1 for local oscillator (LO) and first IF information.

The frequency generation function is performed by the PLL (Phase-Locked-Loop) consisting of synthesizer U204 and VCO circuit Q202/U201. Reference oscillator U203 generates and supplies a reference signal of 16.8 MHz to synthesizer. The synthesizer contains a programmable reference divider, programmable A and B dividers, a programmable prescaler counter (P), and a programmable fractional N divider with two programmable values (N numerator and N denominator).

All of these dividers are programmed through the serial interface which connects the synthesizer to the controller microprocessor. The 16.8 MHz reference oscillator frequency is divided down to a synthesizer reference frequency of 2.1, 2.4, or 2.225 MHz. This signal is fed to the phase detector which generates the steering voltage for the VCO. The output of the VCO circuit is coupled back and divided by AP+B and then divided by the fractional divider and fed into the second input of the phase detector. The VCO buffer has two outputs. One input goes to the input of Rx mixer chip U2, and the other is applied to the input of power amplifier module U105.

The receiver back end consists of a two-pole crystal filter, IF amplifier, a second two-pole crystal filter, and the ABACUS digital back-end IC. The two pole filters are wide enough to accommodate 5 kHz modulation. Final IF filtering is done digitally in the ADSIC.

Table 5-1 LO and First IF Frequencies

	VHF	UHF	800 MHz
LO Frequency range	181.15 - 219.15 MHz	329.65 - 446.65 MHz	776.65 - 796.65 MHz
First IF Frequency	45.15 MHz	73.35 MHz	73.35 MHz

The ABACUS digital back-end chip consists of an amplifier, second mixer, IF analog-to-digital converter, a baseband down-converter, and a 2.4 MHz synthesis circuit to provide a clock to the ADSIC on the logic board. The second LO is generated by discrete components external to the ABACUS. The output of the ABACUS is a digital bit stream that is current driven on a differential pair to reduce noise generation.

The transmitter consists of an RF power amplifier IC that amplifies an injection signal from the VCO. Transmit power is controlled by two custom ICs that monitor the output of a directional coupler and adjust the power amplifier control voltages correspondingly. The signal passes through a Rx/Tx switch that uses

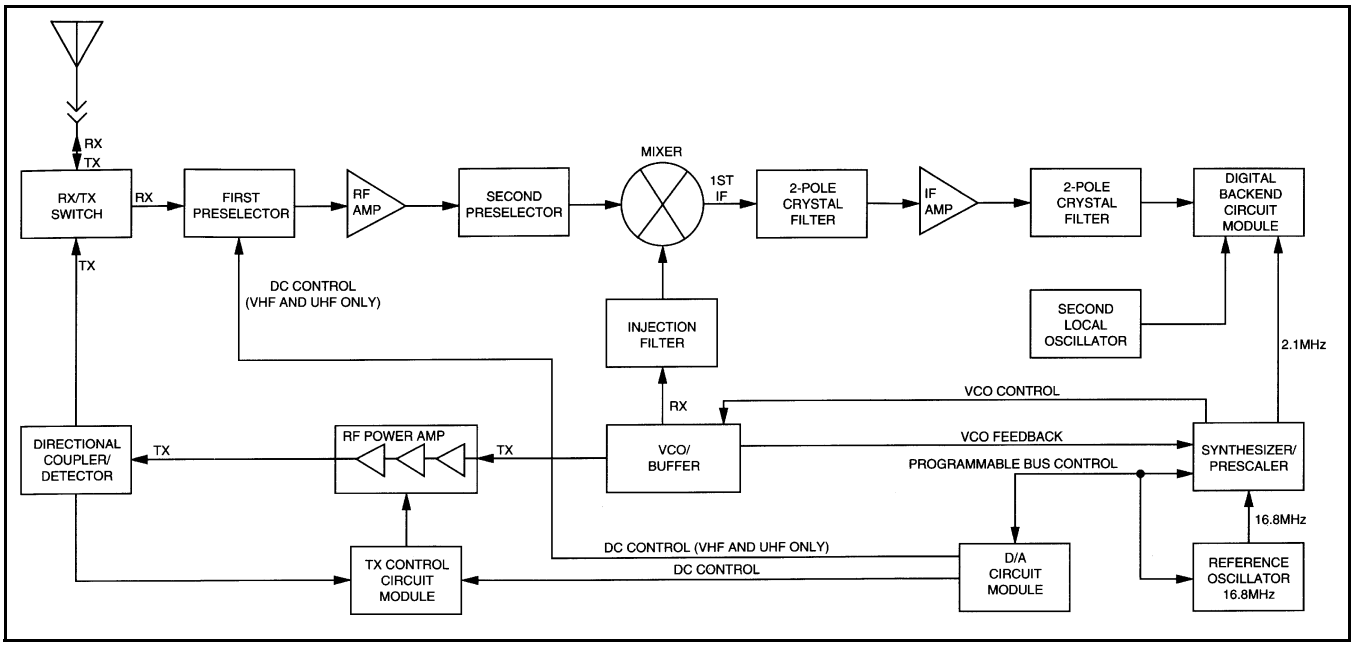


Figure 5-1 RF Board Block Diagram

PIN diodes to automatically provide an appropriate interface to transmit or receive signals.

5.2.2 FREQUENCY GENERATION UNIT

The Frequency Generation Unit (FGU) consists of these three major sections: (1) high stability reference oscillator, (2) fractional-N synthesizer, and (3) VCO buffer. A 5-volt regulator supplies power to the FGU. The regulator output voltage is filtered and then distributed to the transmit and receive VCOs and the VCO buffer IC. The mixer LO injection signal and transmit frequency are generated by the receive VCO and transmit VCO, respectively. The receive VCO uses an external active device, and the transmit VCO active device is a transistor inside the VCO buffer.

The receive VCO is a Colpitts-type oscillator. The receive VCO signal is received by the VCO buffer where it is amplified by a buffer inside the IC. The amplified signal is routed through a low-pass filter and injected as the first LO signal into the mixer. In the VCO buffer, the receive VCO signal is also routed to an internal prescaler buffer. The buffered output is applied to a low-pass filter. After filtering, the signal is routed to a prescaler divider in the synthesizer.

The divide ratios for the prescaler circuits are determined from information stored in an EEPROM. The microprocessor extracts data for the division ratio as determined by the position of the channel-select switch and routes the signal to a comparator in the synthesizer. A 16.8 MHz reference oscillator applies the 16.8 MHz signal to the synthesizer. The oscillator signal is divided into one of three pre-determined frequencies. A time-based algorithm is used to generate the fractional-N ratio.

If the two frequencies in the synthesizer's comparator differ, an error voltage is produced. The phase detector error voltage is applied to the loop filter. The filtered voltage alters the VCO frequency until the correct frequency is synthesized.

In the transmit mode, the modulation of the carrier is achieved by using a two-port modulation technique. The modulation for low frequency tones, such as CTCSS and DCS, is achieved by injecting the tones into the A/D section of the fractional-N divider, generating the required deviation. Modulation of the high frequency audio signals is achieved by modulating the varactor through a frequency compensation network.

The transmit VCO signal is amplified by an internal buffer, routed through a low-pass filter, and then sent to the transmit power amplifier module. The reference oscillator supplies a 16.8 MHz clock to the synthesizer where it is divided down to a 2.1 MHz clock. This divided down clock is fed to the ABACUS IC.

5.2.3 ANTENNA SWITCH

A pair of diodes is used to electronically steer the RF signal between the receiver and transmitter. In transmit mode, RF is routed through a transmit switching diode and sent to the antenna. In receive mode, RF is received from the antenna, routed through a receive switching diode and applied to the RF amplifier.

5.2.4 RECEIVER FRONT END

The RF signal from the antenna is sent through a bandpass filter. The bandpass filter is electronically tuned by the microcontroller via the D/A IC by applying a control voltage to the varactor diodes in the filter. The D/A output range is extended through the use of a current mirror. Wideband operation of the filter is achieved by retuning the bandpass filter across the band.

The output of the bandpass filter is applied to a wideband amplifier. After being amplified by the RF amplifier, the RF signal is further filtered by a second broadband, fixed tuned, bandpass filter to improve spurious rejection.

The filtered RF signal is routed via a broadband 50-ohm transformer to the input of a broadband mixer/buffer. The mixer uses GaAs FETs in a double-balanced Gilbert Cell configuration. The RF signal is mixed with a first LO signal of about –10 dBm supplied by the FGU. Mixing of the RF and the first LO results in an output signal which is the first IF frequency according to Figure 5-1. The first IF signal output is routed through a transformer and impedance matching components and is then applied to a two-pole crystal filter. The two-pole crystal filter removes unwanted mixer products.

5.2.5 RECEIVER BACK END

The output of the crystal filter is matched to the input of the IF buffer amplifier transistor. The output of the IF amplifier is applied to a second crystal filter through a matching circuit. This filter supplies further attenuation at the IF sidebands to increase radio selectivity.

In the ABACUS IC the first IF frequency is amplified and then downconverted to 450 KHz, the second IF frequency. At this point, the analog signal is converted into two digital bit streams via a sigma-delta A/D converter. The bit streams are then digitally filtered and mixed down to baseband and filtered again. The differential output data stream is then sent to ADSIC U3 on the logic board where it is processed to produce the recovered audio.

The ABACUS IC on the RF board is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing and signal type, is controlled by the microcontroller. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information and fill bits dependent on sampling speed. A fractional-N synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The 2nd LO/VCO is a Colpitts oscillator. The VCO has a varactor diode to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter.

5.2.6 EXCITER

The exciter consists of three major sections: Harmonic Filter, RF Power Amplifier, and the ALC (Automatic Level Control) circuit.

The RF signal from the PA module is routed through a coupler, then through the harmonic filter, then to the antenna switch. The RF power amplifier module is a wide-band multi-stage amplifier. The nominal input and output impedance of the power amplifier is 50 ohms. The DC bias for the RF power amplifier is controlled by a switching transistor. The microcontroller uses the D/A IC to produce a ready signal for the transmit ALC IC. The synthesizer sends a LOC signal to the transmit ALC IC. When both the ready signal and LOC signal are available to the transmit ALC IC, the switching transistor for the RF power amplifier is turned on.

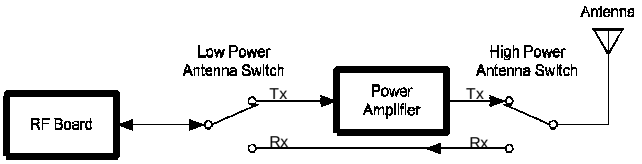
A coupler module samples the forward power and the reverse power of the PA output voltage. Reverse power is present when there is other than 50-ohm impedance at the RF output connector. Sampling is achieved by coupling some of the forward and/or reverse power for rectification and summing. The resulting DC voltage is then applied to the transmit ALC IC as an RF strength indicator.

The transmit ALC circuit is the core of the power control loop. Circuits in the transmit ALC module compare the RF strength indicator to a reference value and generate a bias signal that is applied to the base of a transistor. This transistor varies the DC control voltage applied to the RF PA controlling the RF power.

5.3 VHF PA BOARD

5.3.1 ANTENNA SWITCHES

The RF signal from the RF board is fed by a coaxial cable to the PA board. Since both the receive and transmit signals are present on the input of the PA board, special antenna switching is required on the PA board to route the receive signal around the amplifier section to the antenna. Both a high power and a low power antenna switch are used as shown below.



The low power switch consists of pin diodes CR512 and CR513 and other components. The Q7 output of shift register U601 is high in the transmit mode and low in the receive mode. Therefore, in the transmit mode, Q507 and Q514 are on and Q508 and Q513 are off. This forward biases CR513 and reverse

biases CR512. The transmit signal from the RF board then has a low impedance path through C533 and CR513 to driver Q509, and the high impedance provided by CR512 blocks it from the receive path.

In the receive mode, the opposite occurs, so CR513 is reverse biased and CR512 forward biased. The receive signal from the high power antenna switch (see following) then has a low impedance path through C544, CR512, and C534 to the RF board, and is blocked from the power amplifier by CR513.

The high power antenna switch consists of CR501, CR502, and CR503. This switch effectively switches the antenna between the power amplifier and the receive bypass path to the RF board (see preceding illustration).

Transistor Q501 is on in the transmit mode and off in the receive mode. Therefore, in the transmit mode, all three diodes are forward biased (CR501 and CR502 are biased by voltage applied from the collector of Q510). The transmit signal then has a low impedance path through CR502 to the low-pass filter and is blocked from the bypass path by L504/C511 and L505/C515 which present a high impedance at the transmit frequency. In the receive mode, all three diodes are reverse biased. Therefore, the receive signal from the antenna is blocked from the power amplifier by CR502 and has a low impedance path through L504 and L505 to the RF board.

5.3.2 AMPLIFIERS (Q509, Q510)

Impedance matching between the low power antenna switch and Q509 is provided by L511 and several capacitors and sections of microstrip. Class C biasing is provided by L510 and ferrite bead EP503, and negative feedback for stabilization is provided by R557 and R543. Supply voltage to Q509 is controlled by the power control circuit to regulate the power output of the transmitter. Conditioning and isolation of the DC supply to Q509 is provided by L509, L514, EP501, and C540-C542.

Impedance matching between Q509 and final amplifier Q510 is provided by several capacitors and sections of microstrip. Class C biasing of Q510 is provided by L515, EP502, R559, and R560. The current for this stage flows through L516, R561, and L517. The voltage drop across R561 is sensed by the power control circuit to detect an over-current condition.

From Q510 the transmit signal is fed through another impedance matching network to a directional coupler, to the high power antenna switch (see preceding section), and then to the low-pass filter. This filter attenuates harmonics occurring above the transmit frequency band to prevent adjacent channel interference. The directional coupler detects the forward component of the output power for use by the power control circuit.

5.3.3 POWER CONTROL

Introduction

The power control circuit maintains a constant power output as changes occur in temperature and voltage. It does this by sensing forward power and then varying the drive to Q510 to maintain a constant output power. The drive to Q510 is controlled by varying the supply voltage to driver Q509. The current to final amplifier Q510 is also sensed, but power output is affected by this input only if current becomes excessive. Power output is then cut back to approximately 25% of full power.

The power output level is set in 127 steps by D/A converter U801 which is controlled by the microcontroller. This allows power to be adjusted using the PCTune software and computer and also different power levels to be programmed. In addition, it allows the microcontroller to cut back power if the power amplifier temperature is excessive. Temperature is sensed via thermistor RT501.

U500A, Q500/Q502 Operation

The forward power signal from the directional coupler is applied to pin 2 of amplifier U502A. This is a DC signal that increases proportionally to forward power. The other input to U502A is a DC reference voltage from a D/A converter formed by shift register U801 and several resistors. The voltage from this D/A converter sets the voltage on pin 3 which sets the power output of the transmitter.

U502A is a difference amplifier which amplifies the difference between the reference voltage on pin 3 and the forward power signal on pin 3. The turn-on time of U502A is controlled by the time constant of C528 and R534, and negative AC feedback to prevent oscillation is also provided by C528. This circuit operates as follows: Assume the output power attempts to increase. The DC voltage applied to U502A, pin 2 then increases which causes the output voltage on pin 1 to decrease. Transistors Q505 and Q506 then turn off slightly which decreases the supply voltage to driver Q509. The output power then decreases to maintain a constant power output. R541 and R542 limit the voltage gain of Q505 and Q506 to approximately two.

Delayed PTT

Transistor Q504 is used to delay power output for a short time after the transmitter is keyed. This allows the synthesizer and exciter to stabilize so that the transmitter does not transmit off-frequency. The signal which controls Q504 is from microcontroller U9 on the logic board. In the receive mode this output is low, so Q504 is off. Pin 2 of U500A is then pulled high by the 7.2-volt supply applied through R537 and CR506. This causes the output on pin 1 of U502A to go low which shuts off power to Q509. Then when the transmitter is keyed, the Q504 control signal goes high after a short delay. Q504 then turns on and diode CR506 is reverse biased. Only the forward power signal is then applied to pin 2 of U502A.

Over-Current Shutdown

Current to final amplifier Q510 is monitored by sensing the voltage drop across R561. Pins 3 and 6 of U506 are connected across this resistor. As current increases, the output voltage on U506, pin 8 decreases. This causes the output voltage of voltage follower U507A to decrease. This signal is applied to Schmitt trigger U502B. When the voltage on pin 6 rises above the reference on pin 5, the output on pin 7 goes low. This lowers the power control voltage applied to U502A, pin 3 which lowers the power output to approximately 25% of full power.

5.4 DC POWER DISTRIBUTION

5.4.1 POWER ON OPERATION

When the On-Off/Volume knob is pressed to turn power on (this is a push on/push off switch), the following sequence of events occurs:

1. The power switch closes and grounds the emitter of Q8 on the logic board.

2. If ignition switch sense is used, the 13V signal from the ignition switch is applied to the base of Q8 and pin 48 of microcontroller U9. If ignition sense is not used, pull-up resistor R145 is installed.

3. Q8 then turns on which grounds the base of Q512 on the PA board and turns it on. This turns on main power switching transistor Q511 and applies power to the switched portions of the transceiver.

5.4.2 POWER OFF OPERATION

When power is turned off, the following sequence of events occur:

1. If the power switch is pressed, it opens and the base of Q8 is no longer grounded. This also applies a high signal to pin 45 of microcontroller U9 which then detects the power-off condition.

2. If ignition switch control of power is used, turning the ignition switch off causes the signal applied to the base of Q8 to go low. This signal is also inverted by Q5 and applied to pin 48 of microcontroller U9.

3. Q8 then turns off. However, when the controller detects the power-down request, it holds Q2 on to delay power turn-off until all the required save operations are complete.

4. The controller then turns off Q2 and both Q511 and Q512 on the PA board turn off which turns off transceiver power.

5.5 LOGIC BOARD

5.5.1 LOGIC BOARD OVERVIEW

The Logic Board contains ADSIC U3, Digital Signal Processor U12 (TMS320C50), static RAM U5/U6, FLASH memory U2, and a programmable logic IC U1. In addition, it contains microcontroller U9, audio circuits, and a 5V power supply.The logic board connects with the interface board via J9 and the display controller board via J1.

The ADSIC performs the frequency discrimination and receiver filtering functions. It also performs analog-to-digital (A/D) and digital-to-analog (D/A) conversion. Functions previously performed in hardware like filtering and limiting are performed by software running in the DSP chip. The DSP performs demodulation and modulation, voice encoding and decoding, audio filtering, and squelch signaling. The software for the radio is stored in FLASH memory that is loaded in to static RAM at turn-on. The programmable logic IC controls which device (Flash, SRAM, or UART) is connected to the DSP address and data bus.

5.5.2 DIGITAL SIGNAL PROCESSING OVERVIEW

The DSP section consists of a DSP chip (U12), the ADSIC (U3), two 128K x 8-bit Static RAM chips (U5, U6), one 512K x 16-bit FLASH ROM memory chip (U2), a UART chip (U20), a programmable logic IC (U1), and a glue-logic chip (U4). The FLASH ROM contains the program code executed by the DSP. Depending on the operational mode selected for the radio, different sections of the program code in the FLASH ROM are copied into SRAM for faster execution.

The ADSIC is a support chip for the DSP. It provides the interface between the DSP and the analog signal paths, and between the DSP and the ABACUS chip on the RF Board. Configuration of the ADSIC is handled primarily by the microcontroller. The DSP has access to a few memory-mapped registers on the ADSIC.

In receive mode, the ADSIC interfaces the DSP with the ABACUS IC on the RF board. The ADSIC collects the I and Q samples from the ABACUS and performs channel filtering and frequency discrimination on the signals. The resulting demodulated signal is routed to the DSP via the serial port for further processing. After the DSP processing, the signal is sent to the ADSIC Speaker D/A by writing to a memory-mapped register. The ADSIC then converts the processed signal from the DSP to an analog signal and then outputs this signal to the speaker power amplifier on the interface board.

In transmit mode the ADSIC Microphone A/D digitizes the analog signal from the microphone. The DSP reads these values from a memory-mapped register in the ADSIC. After processing, the DSP sends the modulation signal to the ADSIC via the serial port. In the ADSIC, the VCO D/A converts the sampled modulation signal into an analog signal and then routes this signal to the VCO on the RF board.

5.5.3 RECEIVE SIGNAL PATH

The ABACUS IC on the RF board provides a digital back end for the receiver section. It provides a digital output of I (in phase) and Q (quadrature) samples which represent the IF signal at the receiver back end. These samples are routed to the ADSIC where the signal is filtered and frequency discriminated to recover the modulating signal.

The recovered signal is sent to the DSP chip for processing. The ADSIC interface to the ABACUS is comprised of four signals SBI, DIN, DIN*, and ODC. The ODC signal is a clock the ABACUS provides to the ADSIC. Most internal ADSIC functions are clocked by this ODC signal at a rate of 2.4 MHz and are available as soon as the power is supplied to the circuitry. This signal initially may be 2.4 or 4.8 MHz after power-up. It is programmed by the ADSIC through the SBI signal to 2.4 MHz when the ADSIC is initialized by the microcontroller through the SPI bus. For any functionality of the ADSIC to exist, including initial programming, the reference clock must be present.

SBI is a programming data line for the ABACUS. This line is used to configure the operation of the ABACUS and is driven by the ADSIC. The microcontroller programs many of the ADSIC operational features through the SPI interface. There are 36 configuration registers in the ADSIC of which 4 contain

configuration data for the ABACUS. When these particular registers are programmed by the microcontroller, the ADSIC in turn sends this data to the ABACUS through the SBI.

DIN and DIN* are the data lines in which the I and Q data words are transferred from the ABACUS. These signals make up a differentially encoded current loop. Instead of sending TTL-type voltage signals, the data is transferred by flowing current one way or the other through the loop. This helps reduce internally generated spurious emissions on the RF board. The ADSIC contains an internal current loop decoder which translates these signals back to TTL logic and stores the data in internal registers.

The ADSIC performs digital IF filtering and frequency discrimination on the signal, sending the baseband demodulated signal to the DSP. The internal digital IF filter is programmable with up to 24 taps. These taps are programmed by the microcontroller through the SPI interface.

The DSP processes this data through the SSI serial port. This is a six-port synchronous serial bus. The ADSIC transfers the data to the DSP on the TxD line at a rate of 2.4 MHz. This is clocked synchronously by the ADSIC which provides a 2.4 MHz clock on SCKT. In addition, a 20 kHz interrupt is provided on TFS to signal the arrival of a data packet. This means a new I and Q sample data packet is available to the DSP at a 20 kHz rate which represents the sampling rate of the received data. The DSP then processes this data to extract audio, signaling, and other information based on the 20 kHz interrupt.

In addition to the SPI programming bus, the ADSIC also contains a parallel configuration bus. This bus is used to access registers mapped into the DSP memory. Some of these registers are used for additional ADSIC configuration controlled directly by the DSP. Some of the registers are data registers for the speaker D/A. Analog speaker audio is processed through this parallel bus where the DSP outputs the speaker audio digital data words to this speaker D/A. In addition, an analog waveform is generated which is output to SDO (Speaker Data Out).

In conjunction with speaker D/A, ADSIC contains a programmable attenuator to set the rough signal attenuation. However, the fine levels and differences between signal types are adjusted through the DSP software algorithms. The speaker D/A attenuator setting is programmed by the microcontroller through the SPI bus.

The ADSIC provides an 8 kHz interrupt to the DSP on IRQB for processing the speaker data samples. This 8 kHz signal must be enabled through the SPI programming bus by the microcontroller and is necessary for any audio processing to occur.

5.5.4 TRANSMIT SIGNAL PATH

The ADSIC contains an analog-to-digital (ADC) converter for the microphone. The microphone path in the ADSIC also includes an attenuator that is programmed by the microcontroller through the SPI bus. The microphone input in the ADSIC is on pin MAI (U3-19). The microphone ADC converts the analog signal to a series of data words and stores them in internal registers. The DSP accesses this data through the parallel data bus. As with the speaker data samples, the DSP reads the microphone samples from registers mapped into its memory space. The ADSIC provides an 8 kHz interrupt to the DSP on IRQB for processing the microphone data samples.

The DSP processes these microphone samples and generates and mixes the appropriate signaling and filters the resultant data. This data is then transferred to the ADSIC on the DSP SSI port. The ADSIC generates a 48 kHz interrupt so that a new sample data packet is transferred at a 48 kHz rate and sets the transmit data sampling rate at 48 ksps. These samples are then input to a transmit D/A which converts the data to an analog waveform. This waveform is the modulation signal from the ADSIC and is connected to the VCO on the RF Board.

5.5.5 DSP CHIP (U12)

DSP chip U12 has a 16-bit data bus and a 16-bit address bus. It has 10K words of internal SRAM from which 0.5K are used only to store data and 9.5K are used either for data or for program storage. The DSP bus can access through its buses the following external devices:

SRAM U5 and U6 - These two chips are 128K x 8 chips. U5 stores the lower byte of the word while U6 stores the higher byte. Those chips are selected by

asserting CE2 high and CE1* low. The programmable logic IC is responsible for controlling the select lines of these ICs.

FLASH ROM U2 - This chip is 512K x 16 words in size. It is selected by asserting CE* low. The programmable logic IC is responsible for controlling the select line of this IC.

ADSIC U3 - The ADSIC contains several registers which can be read from or written to by the DSP. The ADSIC IC has an output which drives a data/address bus enable signal for the programmable logic IC.

UART U7 - This chip converts data from the DSP into serial data. It is used to interface with the optional encryption board.

Programmable Logic U1 - This IC arbitrates access to the DSP's address/data bus between the flash (U2), SRAMs (U5,U6), and UART (U7). The DSP can modify the memory configuration by writing to a series of registers in the programmable logic IC. In order to reduce power consumption, the programmable logic IC can be 'disconnected' from the DSP's address/data bus using the bus enable input on the programmable logic IC (pin 44).

The DSP uses memory as data space, program space, and I/O space as follows. Refer to Figure 5-2 for more information.

Program Space - Internal SRAM, external SRAM, and FLASH memory.
Data Space - Internal SRAM and external SRAM.
I/O Space - Programmable logic IC, ADSIC, and the UART.

The DSP accesses the difference spaces by setting the corresponding lines PS*, DS*, IS* low. Only one of these three signals can be low at a given time. When the DSP accesses internal SRAM, none of these lines is activated.

The programmable logic IC (PLD) acts as the primary arbitrator of the DSP's memory map. The FLASH ROM and the SRAM are both mapped in the program space and cannot both be active at the same time. The DSP may control which type of memory is mapped in program space by enabling the programmable logic IC (PLD), then manipulating a register in the PLD. In addition, the DSP can manipulate other registers to control paging of both the Flash and the SRAM. Paging refers to the swapping of 64K word blocks of Flash or SRAM into or out of the DSP's memory map.

FLASH ROM U2 is used to permanently store the program to be executed in the DSP. However, it is slow to access, so to fully utilize the speed of the DSP, the program stored in the FLASH ROM must be copied into the SRAM. As the size of the SRAM is half the size of the FLASH ROM, only the code required for the current mode of operation is copied in the SRAM. As previously mentioned, the FLASH ROM and the SRAM cannot be active at the same time. Therefore, the internal data memory is used as a temporary buffer to transfer the program from the FLASH ROM to the SRAM.

The following hardware interrupts are used on the DSP:

Interrupt	Description
INT1*	8 kHz interrupt for speaker DAC and microphone ADC from ADSIC
INT2*	125 kHz signal from ADSIC
INT3*	2 kHz timer interrupt from the Controller on the Keypad Board.
INT4*	Interrupt from the UART
NMI*	Not used

Connector J3 allows connection to an emulator for debugging purposes. The emulator connects to some dedicated pins on the DSP.

5.5.6 UART (U20)

UART U20 performs parallel to serial and serial to parallel conversion. The serial format used is a 9-bit format with start and stop bits. The serial transmission speed is 19200 bps. The UART appears as eight registers visible in the I/O space of the DSP starting at every multiple of 0008h from 0000h to 07FFh. U1 performs the address decoding by selecting the UART (pin 39) when both IS* and A15 are low. Crystal Y2 along with the internal oscillator of the UART provides the clock required to generate the correct bit rate on the serial output of the UART.

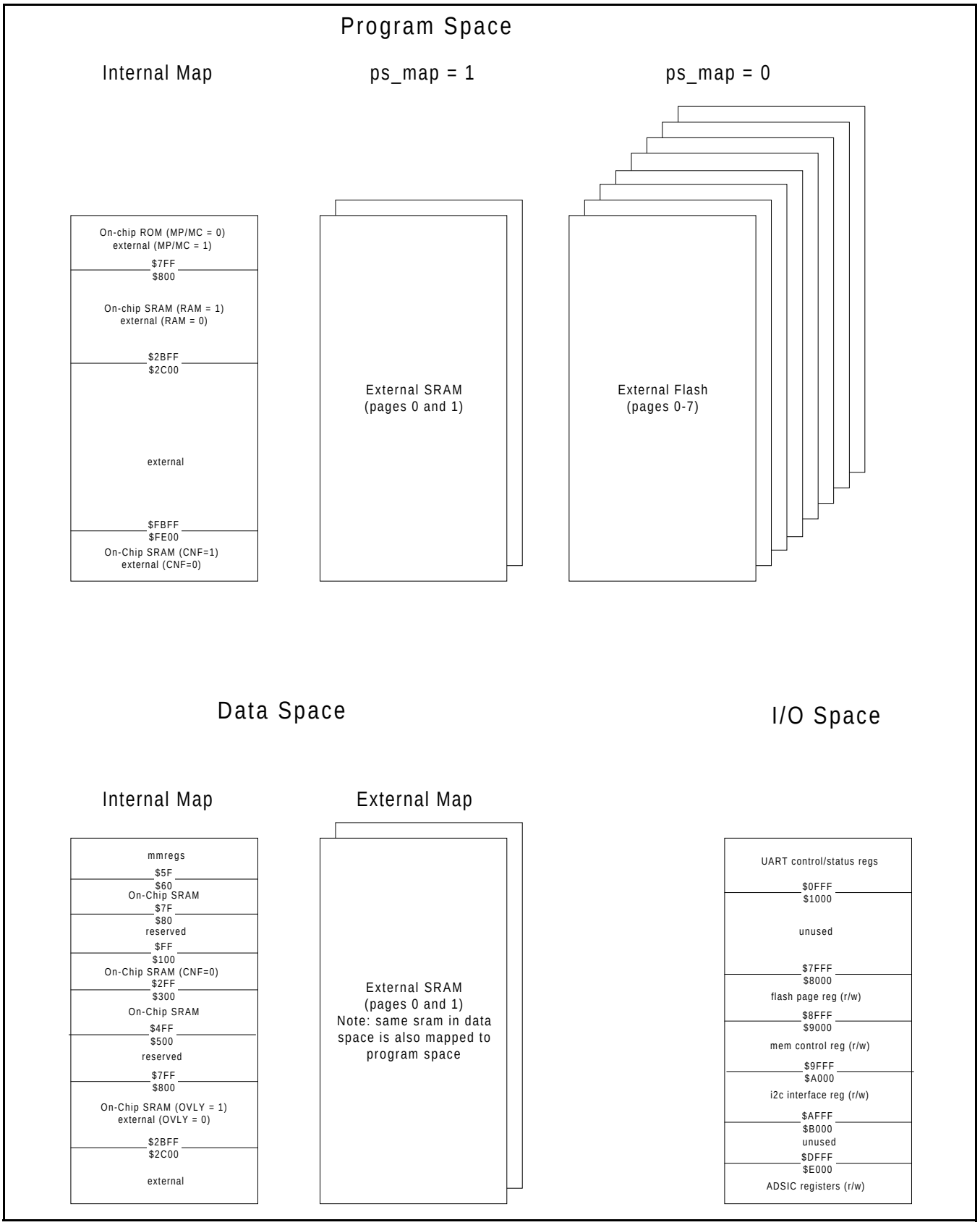


Figure 5-2 Memory Utilization

When the UART receives a new serial word or is ready to accept a new word to send from the DSP, it generates an interrupt on INTRN. This pin is connected to one of the hardware interrupt lines on the DSP. The DSP responds by reading the status register in the UART and by answering accordingly.

5.5.7 ADSIC

The ADSIC is a complex custom IC which performs many analog-to-digital, digital-to-analog, and purely digital functions as previously described. The ADSIC has four internal registers accessible by the DSP. They are selected through the use of address lines A15, A14, A13, A2, A1, A0, IS* (IS* needs to be inverted with U4 to be compatible with the logic level required by the ADSIC), RD*, and WR*. Two of these registers are read-only while the two others are write-only. Therefore, they can be accessed as two locations in the I/O spaces. Due to the decoding performed, those locations appear at the following addresses: Fxx0h, Fxx1h, Fxx8h, Fxx9h, Exx0h, Exx1h, Exx8h, and Exx9h.

Crystal Y1 along with the internal oscillator in the ADSIC provide a 20 MHz clock. This clock signal is used internally by the ADSIC and is also multiplied by two to provide a 40 MHz clock to the DSP. The frequency of the clock can be electronically shifted a small amount by controlling varicap D1 through the OSCW pin (U3-97). This removes interference created on some channels by the clock.

The ADSIC and DSP exchange the sampled receive data and the sampled VCO modulation signal through a serial port. This serial port consists of pins SCKR*, RFS, RxD, TxD, SCKT, and TFS on the ADSIC. U21 and U1 modify the relative phase of TxD and TFS to be compatible with the timing required on the serial port of the DSP.

SDO is the output of the internal speaker DAC. MAI is the input of the internal microphone attenuator and is followed by the microphone ADC.

The ADSIC is configured partially by the DSP through its data and address bus (see preceding). However, most of the configuring is provided through an SPI compatible serial bus. This SPI serial bus consists of pins SEL*, SPD, and SCLK. The other side of this bus is connected to microcontroller U9.

5.5.8 MICROCONTROLLER U9 OVERVIEW

The microcontroller provides an interface between the hardware and DSP U12. When the user presses or rotates a control such as the Select switch, an option button, or the PTT switch, the microcontroller signals the change to the DSP. Conversely, when the DSP needs to change the display or an LED, it signals the microcontroller which then performs the action. The microcontroller also controls peripheral ICs such as the synthesizer, reference oscillator, display processor, and ADSIC.

The microcontroller uses a serial bus to communicate with the DSP and another RS-485 bus to communicate with the front panel/remote control unit. The RS-485 bus is used for external communication with a computer running the programming or tuning software. Finally, the microcontroller maintains certain operating parameters in the associated EEPROM which is controlled via a two-wire serial bus.

5.5.9 MICROCONTROLLER DESCRIPTION

Microcontroller U9 is a Motorola 68HC08XL36 chip. It includes 28K bytes of internal ROM memory and 1K byte of internal SRAM. It does not have an external bus and therefore cannot access any external program memory.

The clock to the microcontroller is provided by Y3 and an internal oscillator. The frequency of the clock can be slightly offset by polarizing the base of Q1 through software control. This prevents RF interference on some channels caused by the clock.

The microcontroller contains an SPI-compatible synchronous serial bus. This bus consists of pins MISO (U1-53), MOSI (U1-52), SPSCK (U1-50), and a chip enable for each device with which it communicates. The devices which communicate with the microcontroller through this bus are as follows:

- PA temperature sense ADC U21
- ADSIC chip U3
- Reference Oscillator (RF Board)
- Front-End DAC (RF Board)
- Synthesizer chip (RF Board)
- Shift register U801 (PA board)
- Optional DES board

The microcontroller communicates with the DSP chip through a custom serial bus. This serial port includes pins PTA3 (U9-8), PTA4 (U9-9), PTA5 (U9-10), PTA6 (U9-11), and PTA7 (U9-12).

The microcontroller SCI asynchronous serial bus is converted to an RS-485 bus by U14. The RS-485 bus is then used for communication with the front panel/remote control unit controller and the external computer running the programming or tuning software. The SCI bus consists of RxD (U9-42) and TxD (U9-43). The RS-485 driver (U14) converts U9 signals at a logic level of 0 and 5 V to three-state RS-485 logic levels.

Serial EEPROM U10 is used to store some important radio parameters. The EEPROM is read to or written from using I/O lines PTC6 and PTC7 of the microcontroller. PTC6 is the data line, and PTC7 is the clock line.

5.5.10 RECEIVE AUDIO CIRCUIT

In receive mode, the analog receive waveform created by the ADSIC is fed to summing amplifier U19A. This amplifier sums this signal with the audio tones generated by the microcontroller on pin 46. The output of the summing amplifier is then fed to buffer amplifiers U19B and U18B, and to U17A/U17B which provide a differential output.

The output signal from U19B is fed to volume control IC U4 on the interface board and then to audio amplifier U1. The output signal from U18B provides the External PA output to the accessory cable, and the output signal from U17A/U17B is fed to the display controller board. It is then converted back to a single-ended signal and fed to the Rx Audio pin of the front panel microphone jack. If a remote control unit is used, the U17A/U17B output signal is also routed to the audio amplifier in the remote control unit.

5.5.11 TRANSMIT AUDIO CIRCUIT

In transmit mode, the audio for transmission can be selected from the microphone connected to the front panel microphone jack or the microphone connected to a remote control unit. U15A and U15B convert a differential input to a single-ended output, and analog switch U18A selects the desired microphone signal.

The microphone signal is then buffered by U15C and fed to analog switch U18B and to the microphone output pin of the universal interface connector. U18B which selects either the microphone or universal interface microphone input signal. Additional buffering is provided by U15D and the signal is then fed to the A/D input of the ADSIC.

5.5.12 VOLTAGE REGULATION

The 5-volt supply is produced by switching DC-DC converter U11. This device is powered by the switched 7.2V supply, and the switching frequency is approximately 160 kHz. A switching regulator provides improved efficiency compared to a standard linear regulator. The 5-volt supply power provides a large percentage of the total power consumed by the radio. The peak-to-peak residual ripple on the 5-volt supply is approximately 50 mV.

The DC-DC converter has a soft-start feature (R27, C141) to prevent chattering of the output regulated voltage due to “bouncing” of the on/off switch. The converter has current limiting that limits output current to 1.5 A. The under voltage protection turns the converter off if the input (switched B+) voltage drops below 5.45 V.

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