Askey 802.11a/b/g, 802.11b/g WLAN card Functional Description

The Askey 802.11a/b/g, 802.11b/g WLAN card Designs are based on Atheros AR5002X chip set which implements IEEE 802.11a, IEEE 802.11b, and IEEE 802.11g WLAN solutions or the AR5002G chipset for IEEE 802.11b/g-only solutions. The chipsets consist of the following:

- AR5212—An all-CMOS, IEEE 802.11a/802.11b/802.11g MAC/baseband processor, and CardBus/PCI bus interface.
- AR5112 Radio-on-a-Chip (RoC)

An all-CMOS IEEE 802.11a/802.11b/802.11g, single-chip radio transceiver that converts RF signals to the baseband range for use by the AR5212. The AR5112 offers fully integrated transmitter, receiver, and frequency synthesizer functions; eliminating the need for external voltage controlled oscillators (VCOs) and surface acoustic wave (SAW) filters.

- AR2112 Radio-on-a-Chip (RoC)

An all-CMOS IEEE 802.11b/802.11g, single-chip radio transceiver that converts RF signals to the baseband range for use by the AR5212. The AR2112 offers fully integrated transmitter, receiver, and frequency synthesizer functions; eliminating the need for external voltage controlled oscillators (VCOs) and surface acoustic wave (SAW) filters.

When combined into a single design, the AR5002X (AR5112 and AR5212) chip set enables a low-cost, compact multi-mode solution that easily fits on a PC Card or Mini PCI design.

For IEEE 802.11g-only implementations, the WLAN card may be used by not populating the IEEE 802.11a radio section, replacing the AR5002X chip set with a AR5002G (AR2112 and AR5212) chip set. By doing this, a single PCB may be used for triple band designs, and single band designs.

AR5002 STA Block Diagram

The AR5002X chipset provides a highly integrated IEEE 802.11a, IEEE 802.11b, and IEEE 802.11g solution, as shown by the block diagram in Figure 1-1.

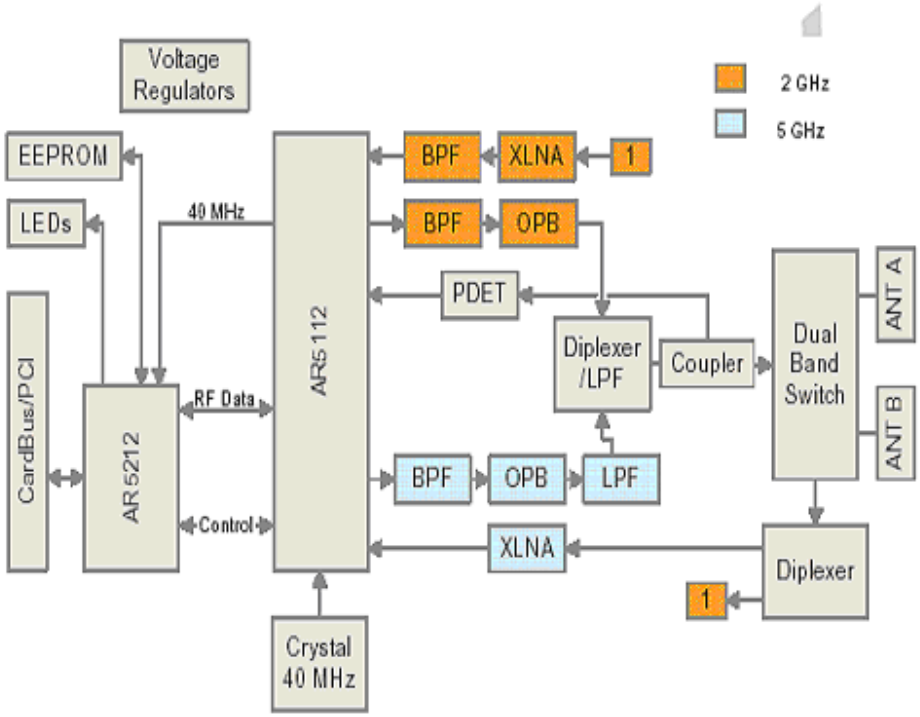

Figure 1-1. **AR5002 STA Radio Block Diagram**

The AR5212 is the origin and destination for all the front-end signals. Both transmit (Tx) and receive (Rx) signals are transferred by the AR5112 to either a 5 GHz front-end, or to a 2.4 GHz front end.
The 5 GHz and the 2.4 GHz front ends share a single set of antennae, dual band switch, Rx diplexer, Tx diplexer/low pass filter, coupler, and power detect circuitry.

The 5 GHz transmit signal is boosted with an output booster (OPB). The OPB drives a diplexer and a coupler/detector (PDET) assembly. The diplexer ' s function is to combine the 5 GHz and 2.4 GHz signals, while the coupler/ detector ' s function is to sample the transmit signal and rectify it. The rectified signal is proportional to the output power and is used for power leveling and control.
The RF transmit signal then passes through a dual band switch. This switch enables the connection of the input to either one of the two antennae.
The 5 GHz receive signal is transferred in a reverse order from the antennae through the switch and receive diplexer. It is then boosted using a low noise amplifier (LNA) and fed back into the AR5112.
The transmit and receive 2.4 GHz signals follow a similar path as the 5 GHz signals in the 2.4 GHz front-end.

CardBus/PCI Interface

The CardBus/PCI interface of the AR5212 is PCI 2.3 and PC Card 7.1 compatible. In the WLAN card design, this interface seamlessly connects to

the CardBus or Mini PCI interface provided by the host.

MAC/Baseband Processor (AR5212)

The AR5212 is a highly integrated chip containing a CardBus/PCI interface, media access control (MAC) and a baseband processor (PLCP/PHY). The AR5212 runs on 2.5 V (digital and analog) core and 3.3 V I/O, and is packaged in a 15x15x1.5 mm 196 plastic ball grid array (PBGA).

40 MHz Crystal

The 40 MHz crystal provides the core clock for the AR5212 and ARx112, (AR5112/AR2112). This crystal is attached to the ARx112, which then internally forms an oscillator. The ARx112 then provides the output of the oscillator to its internal frequency synthesizer, and to the AR5212.
The maximum frequency tolerance allowed by the IEEE 802.11a standard is +/ – 20 ppm. Therefore, the crystal device needs to meet this requirement over all operating conditions. Atheros recommends a crystal device with an overall tolerance of 18 ppm that includes initial tolerance, tolerance over operating temperature range and aging tolerance.
The crystal device used in the Reference Design is calibrated at 19.5 pF load. When designing the crystal circuit, care should be taken to include the board stray and other capacitances, such as those inherent with the oscillator circuits, in the overall calculation of the load capacitance.
A significant shift in frequency can occur if the overall load capacitance presented to the crystal device is not the same as what the crystal was cut for. Excessive load capacitance on the crystal circuit, compared to the actual load that the crystal was designed for, shifts the frequency down. Conversely, lower load capacitance causes an increase in the frequency of the circuit.
When the final circuit boards are available, the overall crystal circuit load capacitance should be calibrated by requesting known frequency crystals at a particular load from the crystal vendor.

RF Front End Section

This section provides information and design guidelines for the transmit and receive paths between the antennae and the ARx112.

General Guidelines

All RF, Rx, and Tx traces are to be 50Ω unless otherwise noted, and must have no sharp bends (90 °) unless otherwise noted.
Atheros recommends that all RF components, traces, and the ARx112 be on the same side of the board.
Vias should be avoided in the RF traces as much as possible. Do not use any test points on any RF trace or component.
Minimize lengths of all RF traces because FR4 material is inherently lossy at RF frequencies. Minimizing the trace lengths reduces the overall signal loss.
It is more important to keep the Tx path short than it is to keep the Rx path short. A loss in signal strength in the Tx path has no opportunity to be recovered, but the Rx signal can be amplified on-board to compensate for losses. The Tx path must be optimized from the output of the OPB to the

antenna ports, and the Rx path must be optimized from the antenna ports to the input to the external low noise amplifier (LNA).
First make the Tx path as short as possible, then shorten the Rx path.

5 GHz Single-Chip Radio Transceiver (AR5112)

The AR5112 chip is an integrated CMOS radio transceiver that supports the IEEE 802.11a, IEEE 802.11b, and IEEE 802.11g standard. The AR5112 supports connection to an external output booster for high performance. The transceiver core, digital logic, and VCO are powered by 2.5 V. The tolerances on the 2.5 V supply need to be +/ – 5%. The I/Os are powered by 3.3 V. The AR5112 is packaged in a 64-pin, 9x9x1 mm lead-less plastic chip carrier (LPCC).

Serial Digital Interface to the ARx112

The AR5212 provides a serial digital interface to the ARx112 for programming its internal registers, such as gain and bias control registers. This interface consists of the signals RFSHIFT, RFDATAOUT0-RFDATAOUT3, RFDATAIN5, RFRESET_L, and RFLOAD.

Analog Receive Interface

The analog receive interface is made up of four analog signals: ADC_QN, ADC_QP, ADC_IP, and ADC_IN. These are two differential pair signal sets that connect directly between the AR5212 and the ARx112.
All four signals must be routed with care to make sure that all have equal routed lengths. Each differential pair also should be routed together to minimize loop area and reduce noise coupling. The width of these traces is not as critical and may be as thin as 5 mils wide.

Analog Transmit Interface

The analog receive interface is made up of four analog signals: DAC_QN, DAC_QP, DAC_IP, and DAC_IN. These are two differential pair signal sets that connect directly between the AR5212 and the ARx112.
All four signals must be routed with care to make sure that all have equal routed lengths. Each differential pair also should be routed together to minimize loop area and reduce noise coupling. The width of these traces is not as critical and may be as thin as 5 mils wide.

ARx112 Tx Matching

Due to the high operating frequencies and the internal ARx112 wire bonds, the input and output impedances appear inductive.
External biasing is needed on pins next to the RF outputs. Due to bonds and practical lengths of external traces, no RF chokes are required for the biasing. Still, bypass capacitors need to be placed close to the chip.
The 5 GHz and 2.4 GHz balanced Tx outputs from the AR5112 are matched to external baluns using lumped-element matching circuits. The baluns are designed for balanced-to-unbalanced impedance transformations of 100:50 and 50:50 for the 5 GHz and 2.4 GHz paths, respectively.

5 GHz Tx Band Pass Filter (BPF)

The output of the 5 GHz balun is directed to a multi-layer ceramic band-pass filter. This filter is intended to reduce spurious emissions from the AR5112 before they reach the external 5 GHz power amplifier, and has a typical insertion loss of 1.5 dB and 25 dB of rejection at 3.8 GHz.

5 GHz Power Booster (OPB)

The 5 GHz power booster is intended to provide a linear gain boost to the AR5112 transmitter outputs, thereby improving overall system performance.

5 GHz Tx Low Pass Filter (LPF)

The 5 GHz low pass filter between the output of the OPB and the Diplexer/ Low Pass Filter,

2.4 GHz Tx Band Pass Filter (BPF)

The output of the 2.4 GHz balun is directed to a semi-lumped low pass filter and multi-layer ceramic band-pass filter combination. These filters are intended to reduce spurious emissions from the ARx112 before they reach the external 2.4 GHz output booster.

2.4 GHz Power Booster (OPB)

The 2.4 GHz power booster is intended to provide a linear gain boost to the ARx112 transmitter outputs, thereby improving overall system performance.

Tx Diplexer

The Tx diplexer is a frequency selective, three-port circuit that combines the 5 GHz and 2.4 GHz transmit signals at their respective power booster outputs before they proceed to the rest of the Tx chain. It serves as a partial low-pass filter to reject 2.4 GHz harmonics, and as a band-pass filter for the 5 GHz Tx path, providing both low frequency signal rejection and additional 5 GHz harmonic rejection.

Coupler

The directional coupler is a dual-band printed microstrip structure that samples the transmit signal energy and directs it to a diode detector. Because wave propagation in microstrip is not TEM, the phase velocities of the even and odd modes are different. This fact causes degradation in the coupler's directivity. EM simulations were used in the coupler design to introduce “fingers” that equalize the coupler/detector phase velocities.
The output of the coupler is directed to the dual-band switch where the transmit signal is directed to the antennas.

Dual Band Switch

The dual band switch is a DC-6 GHz, pHEMT GaAs MMIC device. It is a DPDT configuration that provides Tx/Rx and antenna diversity switch functions in a single package.

Dual Band Antennae

The 802.11a/802.11b/802.11g antennae (Ant-A, Ant-B) are dual band antenna

capable of providing a single antenna pair solution for 2 GHz and 5 GHz applications.
In CardBus implementations, the antenna is printed on the PCB.
In Mini PCI implementations, external antennae are attached to the Mini PCI card via coaxial cables attached to a small form factor coaxial connector. Antenna performance in this situation varies from antenna to antenna and should be studied carefully for optimum performance.

Antenna Location

To have relatively independent operation of the antennae, for diversity, it is recommended to space them as far apart from each other as possible. This is of greater importance for 802.11b. If sufficient distance is not kept between the antennae, then the mutual coupling will be too strong.

Radiation Patterns in Laptops

With a finite ground plane, the radiation peak is not necessarily in the horizontal direction, and will typically be elevated. In CardBus implementations, the card is inserted in the host ' s slot, the pattern deviates significantly from omnidirectional. In this case, many nulls and sidelobes may appear. Diversity, however, can offset most of the nulls. However, on average, some sectors may be worse than others.

Rx Diplexer

The Rx diplexer is a frequency selective, three-port circuit that separates the 5 GHz and 2.4 GHz receive signals at the Rx output port of the dual-band switch. It serves as a partial filter for rejecting external signals. It employs a semi-lumped design (3 discrete components and one printed inductive element), which provide high-pass filtering for the 5 GHz path, and low-pass filtering for 2.4 GHz path.

External Low Noise Amplifiers (XLNA)

The XLNAs for the 2.4 GHz and 5 GHz receive chains are designed to improve overall system sensitivity by minimizing front end noise figure.

2.4 GHz Rx Band Pass Filter (BPF)

The 2.4 GHz receive chain employs a multi-layer ceramic BPF. This filter, which is intended to reject undesired out-of-band signals, is placed after the XLNA in order to minimize overall system noise figure.

AR5112 Rx Matching

The 5 GHz and 2.4 GHz receive chains use single-ended, lumped-element matching circuits to match the AR5112 Rx inputs to the external front end circuitry.

Light Emitting Diodes (LEDs)

The LED drivers have the capability to source 12 mA, and the GPIO drivers are capable of sourcing or sinking 12 mA of current. Furthermore, under software control, GPIOs can also be configured to generate interrupts.

EEPROM

The EEPROM used is a 2048 x 8, or 1024 x 16 (16 Kb) device used to store the AR5002 configuration information, PC Card tuples, and any OEM-specific data.

The EEPROM contents include PCI configuration data with a read/write protection key, Card Information Structure (CIS) (or tuples) for PC Card, and vendor-specific data. Upon the de-assertion of reset, if the EPRM_EN_L signal of the AR5212 is active, the EEPROM contents are loaded.

The EEPROM can be read at any time under software control. EEPROM reads and writes transfer 16 bits of data. To transfer a full 32 bit double word, the software needs to perform the necessary two read or write operations.

Voltage Regulator

One voltage regulator provides 2.5 V, the core voltage for the AR5212. It converts 3.3 V to 2.5 V to supply the AR5212 PLL, ADC/DAC, and digital core. This regulator also supplies the core 2.5 V to the ARx112.