APPENDIX 6

TRANSMITTER TUNE-UP PROCEDURE

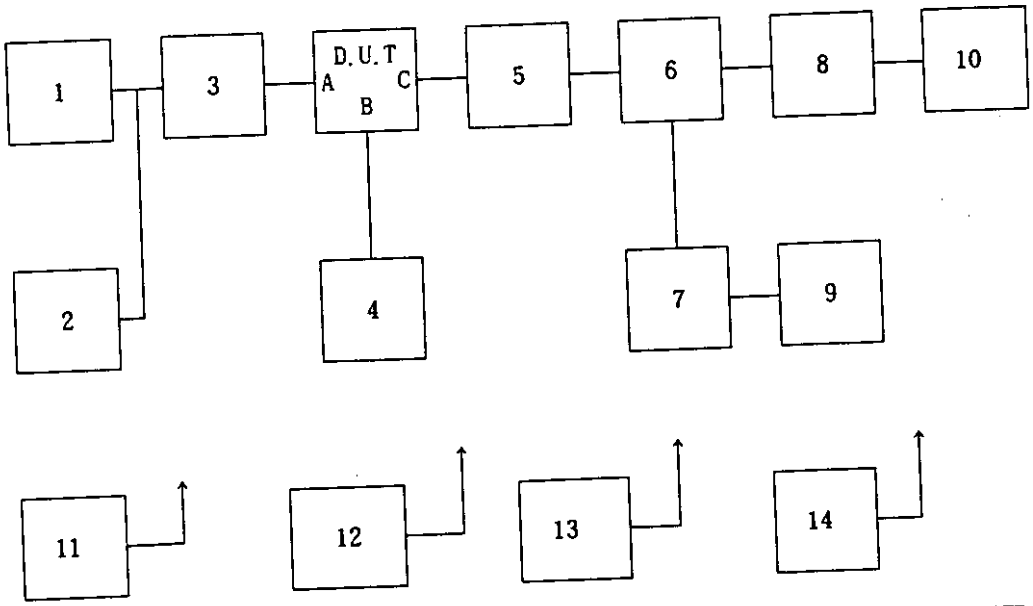
THREE (3) PAGE TUNE-UP PROCEDURE
FOLLOWS THIS SHEET

F. TRANSMITTER TUNE-UP PROCEDURE

1. TRANSMITTER TUNE UP PROCEDURE

1-1. TEST SET UP

1-2. REFER TO THE DIAGRAM SHOWN BELOW.



D.U.T : DEVICE UNDER TEST

A : MIC INPUT

B : POWER INPUT LEADS

C : ANTENNA JACK

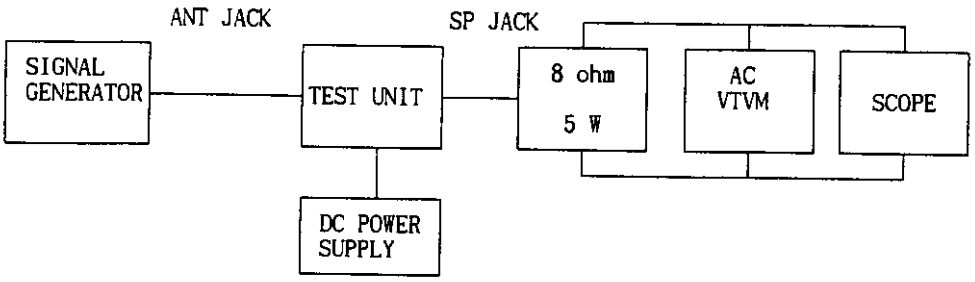
ITEM NO	DESCRIPTION	MANUFACTURER	MODEL NO.
1	AUDIO OSCILLATOR	KIKUSUI	417A
2	FREQUENCY COUNTER	TAKEDA RIKEN	TR5125
3	AUDIO ATTENUATOR	TECH INSTRUMENTS	TE-111
4	REGULATED DC SUPPELY	KIKUSUI	7133A
5	RF WATTMETER	BIRD	4311-200
6	COUPLER	TOKYO DENPA	WV-1
7	OSCILLOSCOPE	HEWLETT-PACKARD	1710B
8	RF ATTENUATOR	FUJISOKU	FAT-515N
9	FREQUENCY COUNTER	TAKEDA RIKEN	TR5125
10	SPECTRUM ANALYZER	HEWLETT-PACKARD	8554B/8552A/8566B
11	OSCILLOSCOPE	HEWLETT-PACKARD	1710B
12	FREQUENCY COUNTER	TAKEDA RIKEN	TR5125
13	RF VOLTMETER	ANRITSU	M316A
14	DC VOLTMETER	TAKEDA RIKEN	TR6355

G. RECEIVER TUNE-UP PROCEDURE

1. RECEIVER CIRCUIT ALIGNMENT

1-1. TEST SET UP

1-2. REFER TO THE DIAGRAM SHOWN BELOW.



RECEIVER ALIGNMENT SET UP

2. SENSITIVITY ALIGNMENT

2-1. SET THE SIGNAL GENERATOR TO PROVIDE 27.185MHz, 1KHz 30% MOD. 1uV RF INPUT. PLASE THE CHANNEL SELECTOR IN CHANNEL 19 POSITION.

2-2. ADJUST L101,L201, L202 FOR MAXIMUM AUDIO OUTPUT ACROSS THE 8 ohm DUMMY LOAD RESISTER. THIS ALIGNMENT SHOULD BE PERFORMED BY GRADUALLY DECREASING THE SIGNAL OUTPUT SIGNAL TO A MINIMUM LEVEL REQUIRED FOR TUNING TO AVOID INACCURATE ALIGNMENT DUE TO AGC ACTION

3. SQUELCH CIRCUIT ALIGNMENT

3-1. SET THE SIGNAL GENERATOR TO PROVIDE 60dB, 1KHz, 30% MOD ANTENNA INPUT.

3-2. ROTATE THE SQUELCH CONTROL IN FULL CLOCKWISE DIRECTION.

3-3. TEMPERARILY ADJUST VR101 FOR MAXIMUM AUDIO OUTPUT, AND NOTE THE AUDIO OUTPUT LEVEL. THEN ADJUST RV550 SO THAT AUDIO OUTPUT JUST APPEARED.

3-4. NEXT, REDUCE THE ANTENNA INPUT SIGNAL LEVE TO 800uV-4000uV AND MAKE SURE THE AUDIO OUTPUT DECREASES TO ZERO.

3-5. REDUCE ANTENNA SIGNAL INPUT LEVEL TO ZERO, AND ADJUST THE SQ CONTROL UNTIL THE NOISE OUTPUT DECREASES TO JUST DISAPPEAR.

2. VCO VOLTAGE ADJUSTMENT

SELECT THE OPERATING CHANNEL ON CH 1.
CONNECT DC VOLTMETER(14) BETWEEN GROUND AND VCO POINT (BETWEEN R516 AND R608).
MAKE THE SET UNDER TX MODE.
TUNE THE VCO VOLTAGE TUNING IFT L601 TO OBTAIN 2.0 V READING OF DC VOLTMETER.
CHECK THE VOLTAGE OF CHANNEL 40 WHETHER THE READING IS IN BETWEEN 2.5 TO 5.5 V DC UNDER RX MODE.
REMOVE DC VOLTMETER .

3. TRANSMITTER ALIGNMENT

3-1. CONNECT THE RF VOLTMETER (13) ON THE BASE OF Q704.
TRANSMIT ON CHANNEL 19 .
ADJUST L701, L702 FOR MAXIMUM READING ON RF VOLTMETER .
REPEAT AS NEEDED.
REMOVE RF VOLTMETER .

3-2. WITH THE RF POWER METER READING ON RF WATTMETER (5).
REPEAT IF NEEDED.

3-3. REPEAT STEPS 1 AND 2 IF NEEDED.

3-4. OUTPUT POWER READING ON RF WATTMETER (5) SHOULD BE FROM 3.6 TO 4.0 W.
IF POWER EXCEEDS 4.0 WATTS INCREASE R711 TO REDUCE POWER AND REPEAT ALIGNMENT AGAIN.

4. FINAL CHECK

IN TRANSMIT ON ALL 40 CHANNELS

4-1. OUTPUT POWER SHOULD BE FROM 3.6 TO 4.0 WATTS .

4-2. FREQUENCY SHOULD BE WITHIN +400 Hz OF CHANNEL CENTER FREQUENCY .

4-3. STRENGTH OF SPURIOUS SIGNALS AS OBSERVED ON SPECTRUM ANALYZER (10) SHOULD BE LESS 60 dB THAN THE TRANSMITTING FREQUENCY.

APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

All 40 channels of transmitting, and receiving, frequencies are provided by PLL (Phase Locked Loop) (IC501) circuitry.

The purpose of the PLL is to provide a multiple number of frequencies from a VCO (Voltage Controlled Oscillator) with quartz crystal accuracy and stability locked to crystal oscillator reference frequency.

The reference crystal oscillator frequency is 10.24 MHz.

APPENDIX 8

1. Circuits For Suppression Of Spurious Radiation

The tuning circuit between frequency synthesizer and final amp Q702 and 3-stage "PI" network C718, C719, L711, C721, L712, C725, C722, L713, C723 in the Q704 output circuit serve to suppress spurious radiation. This network serves to impedance match Q704 to the antenna and to reduce spurious content to acceptable levels in the frequency synthesizer.

2. Circuits For Limiting Modulation

A portion of the modulating voltage is rectified by D401 which controls Q403 and Q404 to attenuate the mic amp IC401. The resulting feedback loop keeps the modulation below 100 percent for the inputs approximately 40 dB greater than that required to produce 50% modulation. The modulation attack time is about 50 mS and the modulation release time is about 300 mS.

3. Circuits for Limiting Power

During factory alignment, the series resistor of TX power amp Q704 is selected to limit the available power to slightly less than 4 watts. The tuning is adjusted so that the actual power is from 3.6 to 3.9 watts. There are no other additional controls for adjusting the TX output power.

DEVICES AND CIRCUITS TO SUPPRESS SPURIOUS RADIATION AND LIMIT MODULATION
FCC ID: BBOHH28

APPENDIX 8

LC7185-8xxx

CMOS LSI

CB TRANSCEIVER PLL FREQUENCY SYNTHESIZER AND CONTROLLER

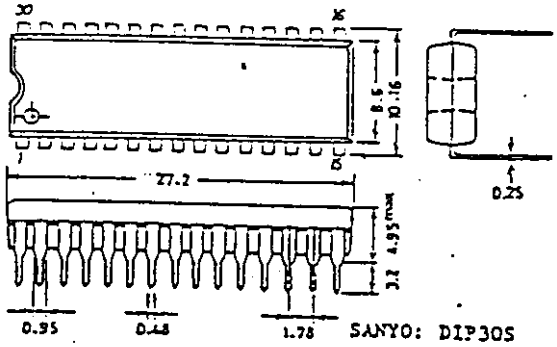
Overview

This 27MHz band, PLL frequency synthesizer LSI chip is designed specifically for CB transceivers. The internal ROM can be changed to suit the frequency specifications of various countries (hence the 8xxx designation). The LC7185-8xxx incorporates PLL circuitry and a controller for CB applications on a single CMOS chip. The controller handles the PLL circuitry, frequency data ROM, channel preset/recall RAM, and LED display drivers. It also supports channel scan, channel preset/recall, and emergency channel call.

Features

- A built-in programmable divider for the 16MHz VCO
- Transmission is inhibited when the PLL is unlocked (degital lock monitor).
- Direct channel 9 or 19 selection (sliding switch)
- A 7-segment, 2-character LED display
- "PA" is displayed in public announcement mode.
- Output beep-tone control circuitry
- Up to 5 channel settings can be stored in memory.
- 4 x 3 key matrix implementation
- DIP30S (shrink) package

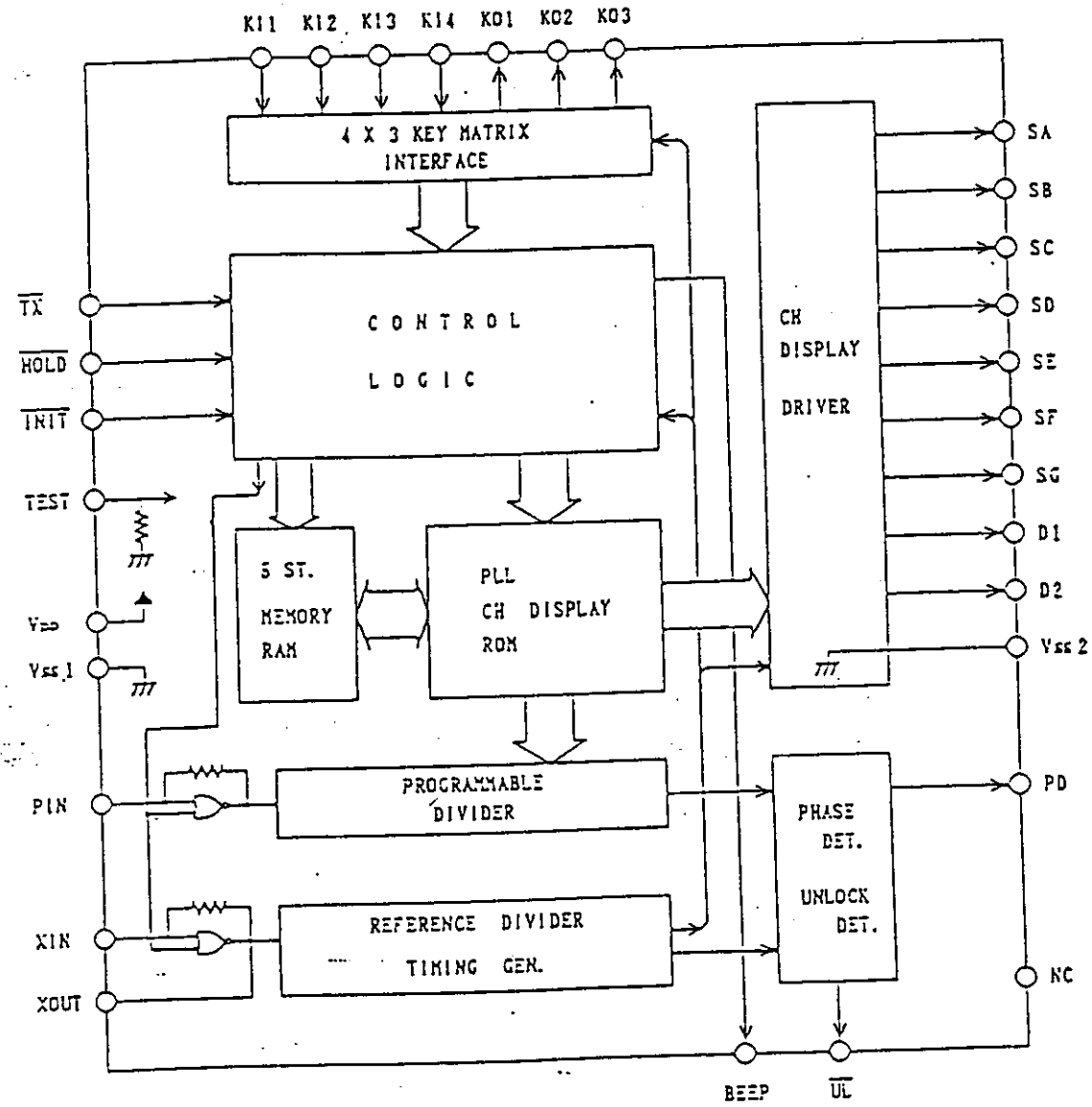
Case Outline 3061-D30SNIC
(unit:mm)



SANYO: DIP30S

Specifications and information herein are subject to change without notice.

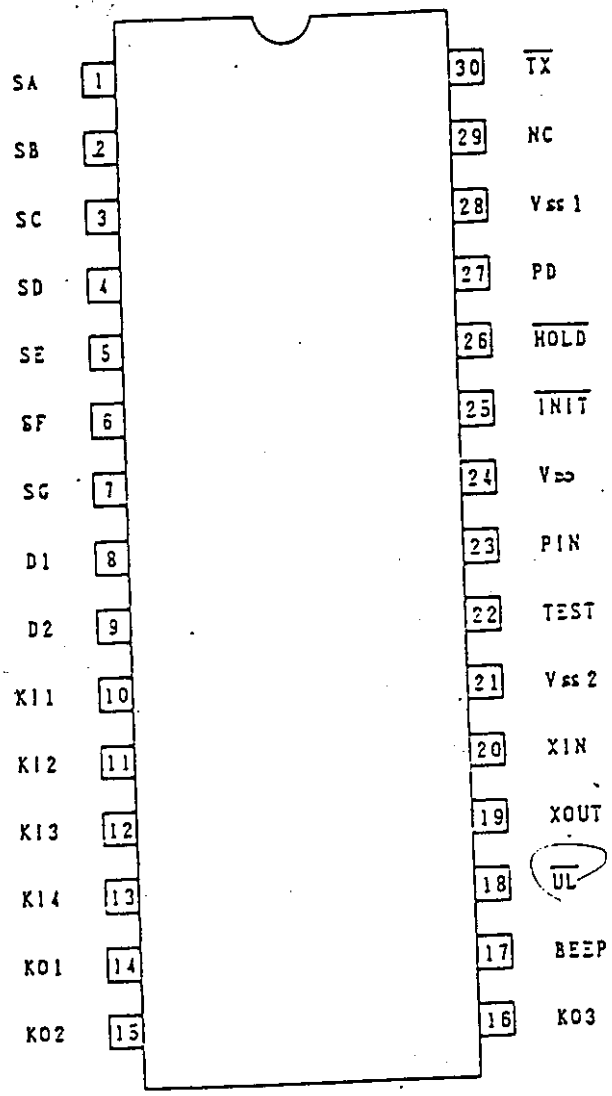
Block Diagram



Pin Descriptions

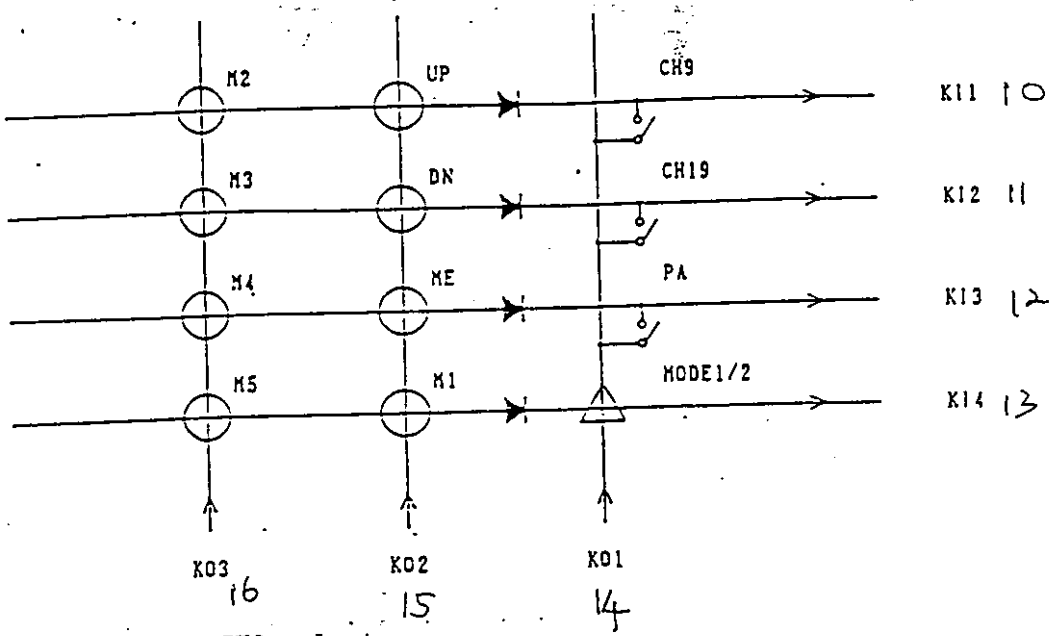
$\overline{TX}$: Transmit/receive select
$\overline{HOLD}$: Hold mode select
$\overline{INIT}$: Reset line
TEST: Test point (input)
V_{DD}, V_{SS1}, V_{SS2}: Power supply
PIN: Programmable divider input
XIN, XOUT: Crystal oscillator input, output (e.g. 10.240MHz)
$\overline{UL}$: Unlock detected output
PD: Charge pump output
NC: NC Pin
SA to SG: Segment drivers (for display)
D1, D2: Digit output (for display)
KI1 to 4: Key inputs
KO1 to 3: Key scan outputs
BEEP: Beep-tone control output

Pin Assignment: DIP30S (shrink) package



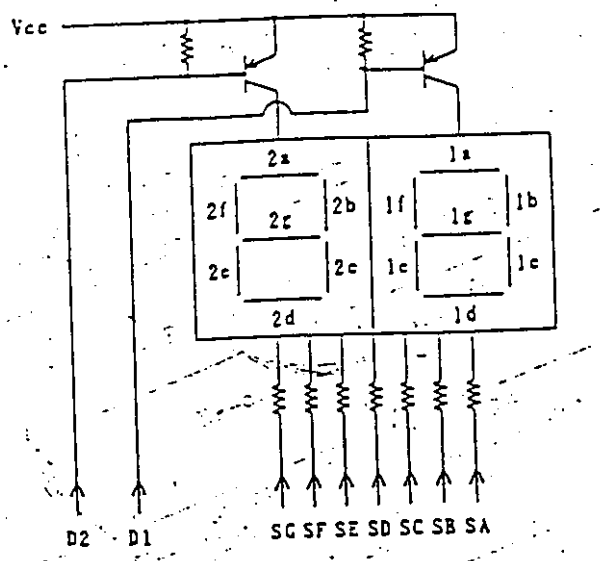
top view

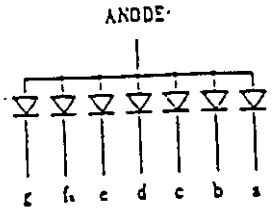
Key Matrix



CH9: Emergency CH9 select
CH19: Emergency CH19 select
PA: Public announcement display
MODE 1/2: Display mode
UP: Channel up/scan
DN: Channel down/scan
ME: Channel memory enable
M1 to M5: Channel memory recall
UP/DN/ME/M1 to M5: Momentary switch
CH9/CH19/PA: Sliding switch
MODE 1/2: Diode

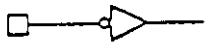
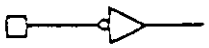
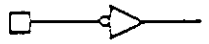
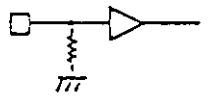
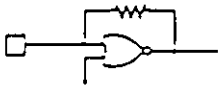
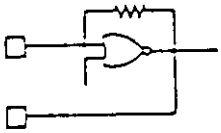
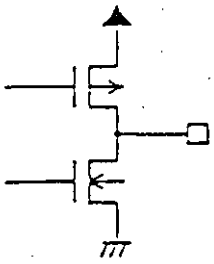
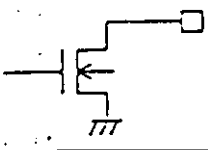
KD Display Configuration (Common anode/7 segment)





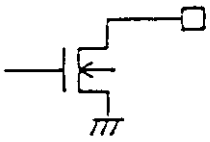
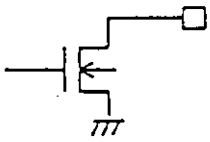
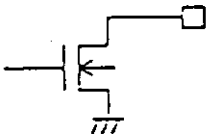
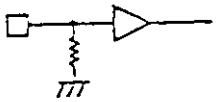
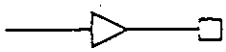
	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

Pin Description

Pin Name	Pin No.	Type	Description
$\overline{TX}$	30		Transmit/receive select $\overline{TX}$="0" ... Transmit, $\overline{TX}$="1" ... Receive
$\overline{HOLD}$	26		Hold mode select $\overline{HOLD}$="0" ... Hold mode select ="1" ... Normal mode select
$\overline{INIT}$	25		Reset line $\overline{INIT}$="0" ... Reset
TEST	22		Test point (input) Tie to ground or leave floating
V_{DD}	24		Power supply (+) Normal mode: 5.0 to 8.0V Hold mode: ≥3.0V
V_{SS2}	21		Channel display LED driver Ground
PIN	23		Programmable divider input 150mVrms min Hold mode: Programmable divider is disabled.
XIN XOUT	20 19		Crystal oscillator Frequency: 10.24MHz Hold mode: Oscillator is disabled.
PD	27		Charge pump output from the phase comparator . f_V is obtained by dividing the PIN frequency input by N (programmable divider value) . f_R is the reference signal (reference divider output) $f_V > f_R$ or leading: Positive pulses . $f_V < f_R$ or lagging: Negative pulses $f_V = f_R$ and phase matched: High impedance Hold mode: High impedance
V_{SS1}	28		. PLL circuit and controller Ground
NC	29		. No-connection
$\overline{UL}$	18		Unlock detected output Low level: See Unlock Detected Output ($\overline{UL}$) for detail. Open: Locked

Continued on next page.

Continued from preceding page.

Pin Name	Pin No.	Type	Description
BEEP	17		Beep-tone control output Open: See Beep-tone Control Output for detail. Low level: Hold mode
SA to SG	1 to 7		Segment drivers for the display (Common anode/7 segments)
D1 D2	8 9		Digit output (150Hz) for the display (Common anode/7 segments) Hold mode: Tr goes off.
KI1 to KI4	10 to 13		Key inputs Input from the key matrix
KO1 to KO3	14 to 16		Key scan output (75Hz) Output to the key matrix Hold mode: Low (scanning stops)

Operation

(1) Channel selection (up/down)

The unlock detected line ($\overline{UL}$) is asserted (low) when the UP (or DN) key is pressed and deactivated 25ms after the key is released (see diagram below). The beep-tone control line (BEEP) is asserted (open) for 50msec after each new channel is selected (see diagram below).

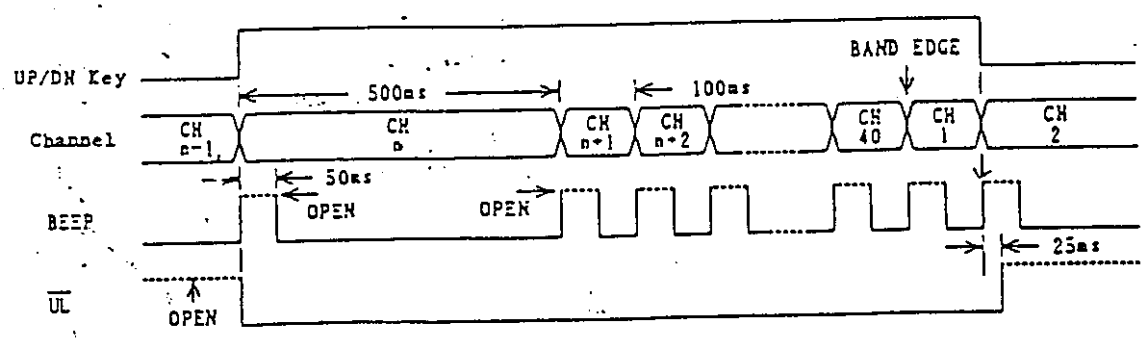
1) Manual scanning (up/down)

Pressing the UP key increments by one channel and pressing the DN key decrements by one channel.

When scanning reaches the end of the band, it automatically wraps around to the beginning.

2) Auto scanning (up/down)

Holding the UP (or DN) key down for 500msec or longer starts auto scanning. For both up and down scanning, each channel takes 100msec to scan.

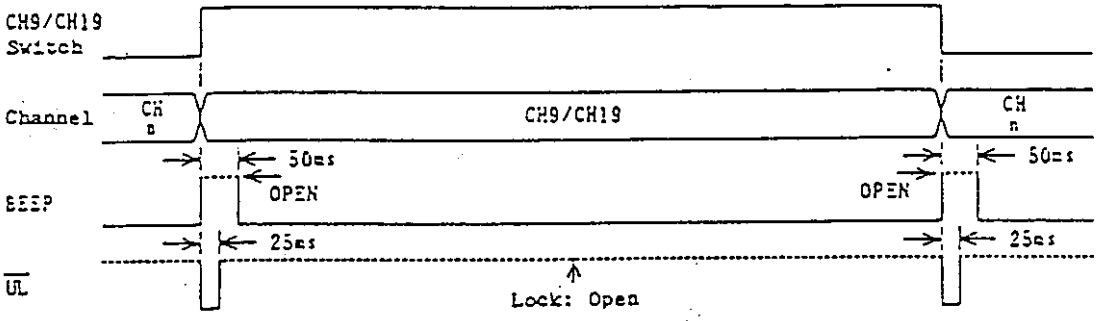


(2) Selecting an emergency channel (CH9/CH19)

If the CH9 or CH19 switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Asserts the beep-tone control line for 50msec
- Disables the UP/DN, M1 to M5, and ME switches
- Causes either "9" or "19" to blink on the display
- Keep the emergency channel open until the CH9 or CH19 switch is turned off.

After the CH9 or CH19 switch is turned back off the beep-tone control line is asserted for 50msec and the LC7185 reopens the previous channel.
Note the CH9 has a higher priority over CH19. As a result, if both switches are turned on, CH9 will be opened.
As shown in the diagram, the $\overline{UL}$ line is asserted for 25ms after the CH9 or CH19 switch is turned off or on.

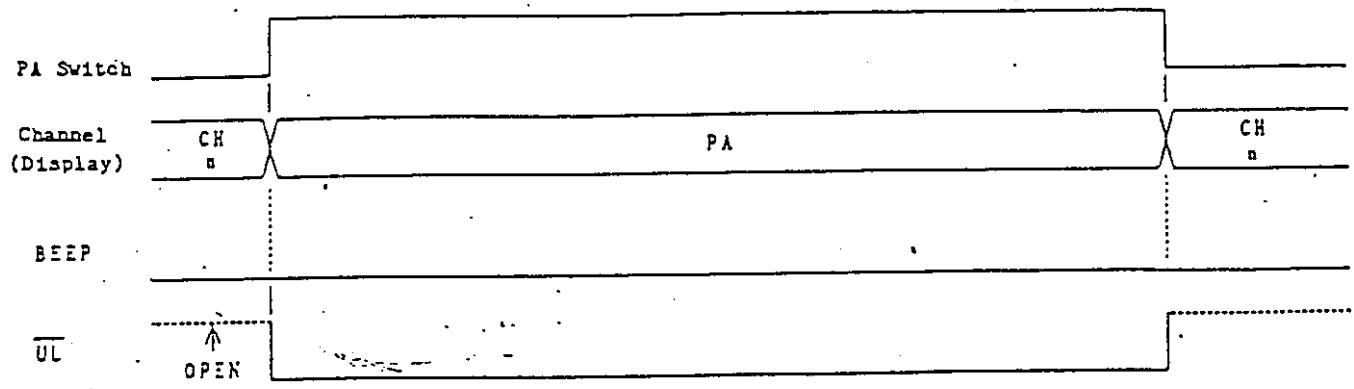


(3) Public Announcement (PA) mode

When the PA switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Disables all keys
- Causes "PA" to be displayed
- Stays in PA mode until the PA switch is turned off.

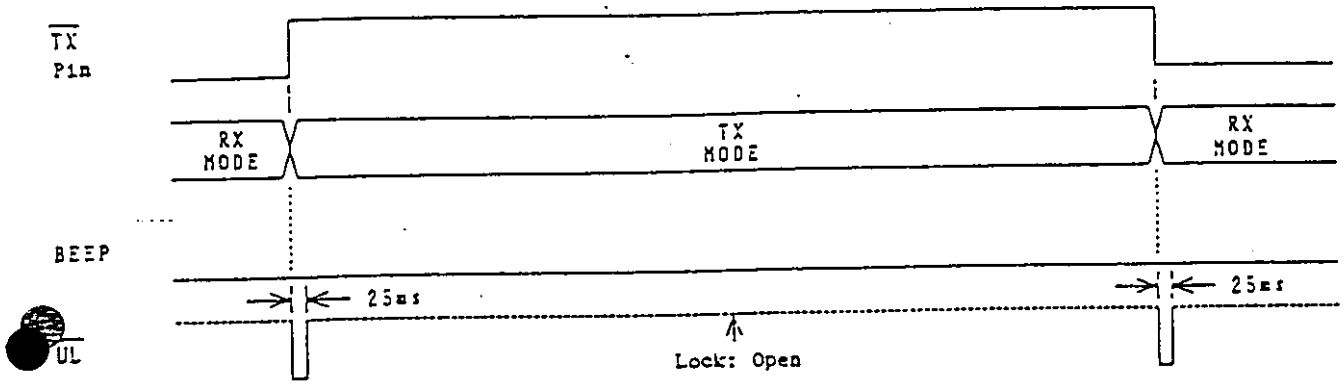
When the PA switch is turned back off, the LC7185 leaves PA mode and reopens the previous channel.
As shown in the diagram, the $\overline{UL}$ line is asserted while the PA switch is turned on.



(4) Transmit/Receive Selection

When the $\overline{TX}$ line is asserted, the LC7185 enters TX mode. The LC7185 will only leave this mode if the PA switch is pressed or the $\overline{TX}$ line is deactivated.

As shown in the diagram, the $\overline{UL}$ line is asserted for 25ms after the TX line is asserted or deactivated.



(5) Channel Preset/Recall Facility

1. The LC7185 allows up to 5 channels to be preset (assigned to M1 to M5).
   . After a reset, M1 to M5 are assigned to CH33.

2. Recalling preset channels
   . A preset channel is recalled by pressing one of the preset memory keys (M1 to M5)* to which the channel was previously assigned.
   . Presetting channel (assigning keys) are covered in the next section. There are two different display modes as shown below.

Mode 1 (without diode)

Each time a key is pressed (e.g. M1), the new channel is displayed.

Example: Display 21 ⟶ 15

Key [M1]

Mode 2 (with diode)

Each time a key is pressed (e.g. M1), a key mnemonic (e.g. "P1") is displayed for 400msec, then the new channel is displayed.

Example: Display 21 ⟶ P1 ⟶ 15 (400ms)

Key [M1]

3. Presetting channels

Presetting a channel is done in the following way. First select the channel to be preset, then hold down the ME key and press the preset memory key (M1 to M5)* to which you would like to assign the current channel.

In the following cases, a channel will not be preset:

. 9 seconds elapse after the ME key is pressed and one of M1 to M5 is pressed.
. Emergency channels CH9 or CH19 are currently selected
. The $\overline{TX}$ line is asserted.
. The PA switch is turned on (PA mode).
. The $\overline{HOLD}$ line is asserted (hold mode).

There are two different display modes as shown below.

Mode 1 (without diode)

The current channel is displayed throughout the preset process.

Example: Display 15 ⟶ 15

Key [ME] [M1]

Mode 2 (with diode)

When the ME key is held down, "PE" is flashed on the display. Once a preset memory key is pressed (e.g. M1), the key mnemonic (e.g. "P1") is displayed for 400msec before the current channel is redisplayed.

Example: Display 15 ⟶ PE ⟶ P1 ⟶ 15 (400msec)

Key [ME] [M1]

* Note that if two or more keys are pressed at the same time, priority is assigned as follows:

M1>M2>M3>M4>M5

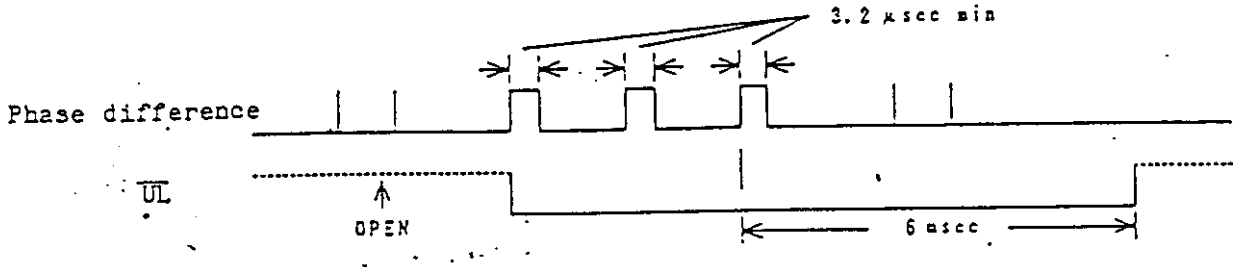
(6) Beep-tone Control Output

After each of the following events, the BEEP line is asserted for 50msec:

. A reset (e.g. battery replacement)
. Any key press associated with the channel memory
. Any emergency channel switch activation
. A new channel is selected.
. Leaving hold mode

(7) Unlock Detected Output ($\overline{UL}$)

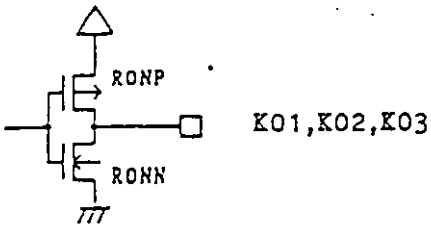
In the following cases, the $\overline{UL}$ line is asserted for the duration indicated.



. When the phase difference between the programmable and reference divider outputs exceeds 3.2μsec. The $\overline{UL}$ line is held low for 6msec after the last out-of-range phase sample is detected, as shown below.
. After a new transmit/receive or channel selection. The $\overline{UL}$ line is asserted for 25msec.
. While the PA switch is turned on.

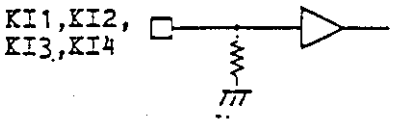
(8) Key Matrix

It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines.
But KO1, KO2 and KO3 lines don't need diodes.

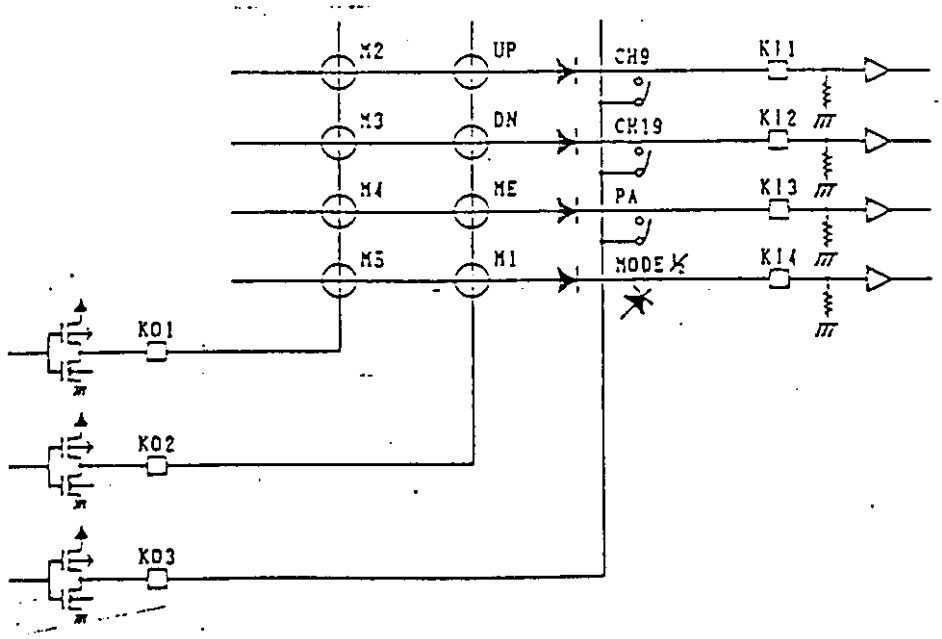


R_{ONP}, R_{ONN}: ON impedance

	min	typ	max	[kohm]
R_{ONP}	0.5	1.0	2.0	
R_{ONN}	30	50	70	
R_{PdN}	30	50	70	



P_{PdN}: Pull-down resistor



Hold Mode

The LC7185 enters hold mode when the $\overline{HOLD}$ line is asserted. In this mode, the channel preset/recall RAM is not affected.

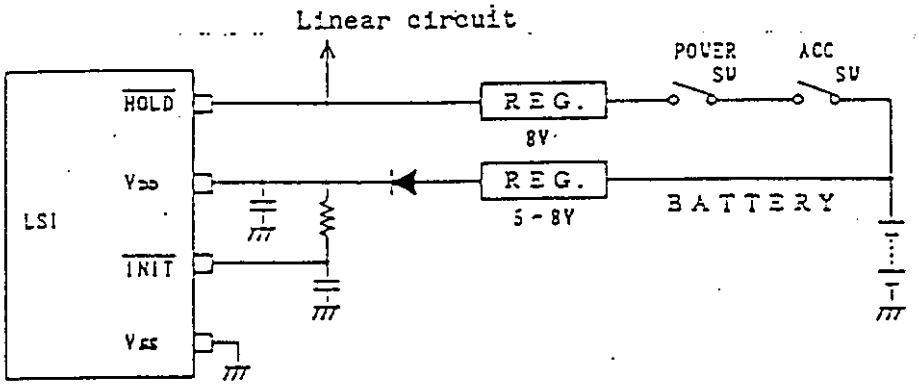
(1) System status

The LC7185 will remain in hold mode until the $\overline{HOLD}$ line is deactivated or a reset occurs ($\overline{INIT}$ line is asserted). The programmable divider, crystal oscillator, and reference divider are all inhibited. Signal output levels are shown below.

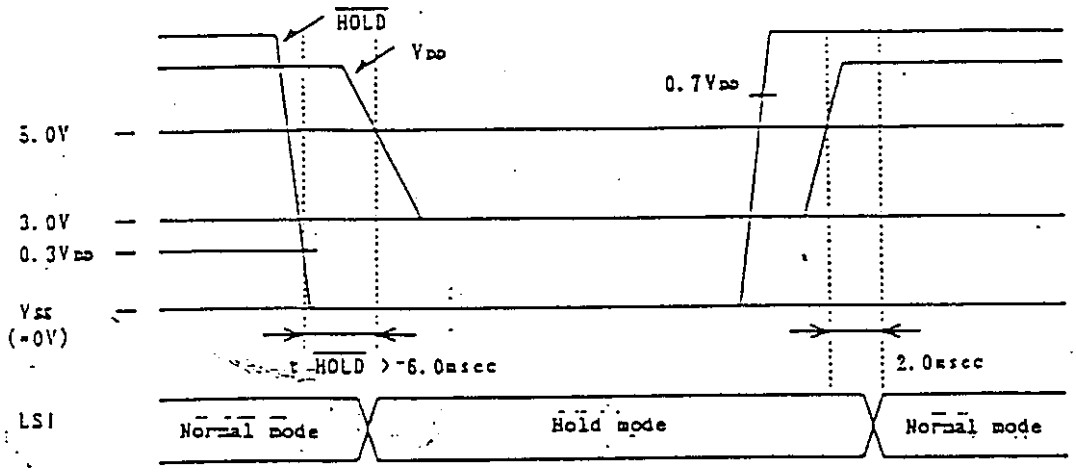
PD: High impedance
$\overline{UL}$: V_{SS} (ground)
D1, D2: High impedance
BEEP: V_{SS}
KO1 to KO3: V_{SS}
When the LC7185 leaves hold mode, the previously selected channel is reopened.

(2) Reset

To reset the chip, assert the $\overline{INIT}$ line,
Reset state:
. CH9 is selected.
. Preset memory keys are all set to CH33.



(3) Timing Requirements for Hold Mode

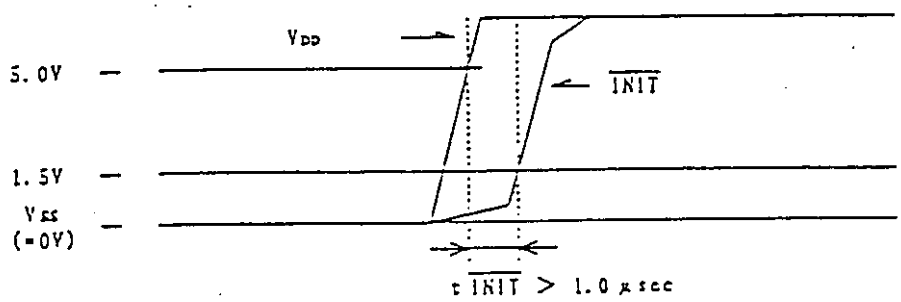


V_{DD} must remain at 5.0V or higher (crystal oscillator requirement) for 6.0msec (t_{HOLD}) after the HOLD line is asserted (HOLD<0.3V_{DD}). After this V_{DD} may go as low as 3.0V.
There are no constraints on timing when the chip is leaving hold mode.
The signals can be activated in one of two orders.

1) If HOLD is already deactivated (>0.7V_{DD}), the LC7185 leaves hold mode within 2.0msec after V_{DD} rises to >5.0V.
2) If V_{DD} is >5.0V, the LC7185 enters normal mode within 2.0msec after HOLD is deactivated.

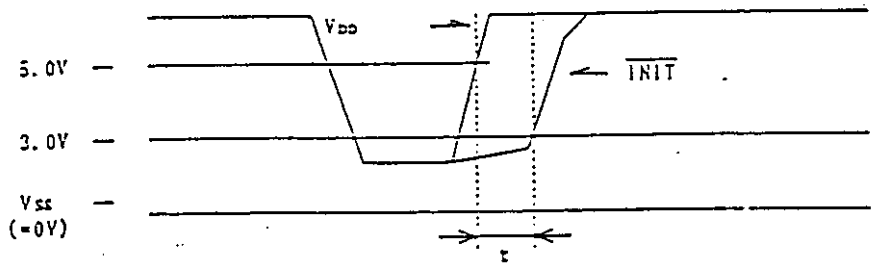
(4) Reset Timing

1) Reset timing (e.g. battery replacement)



Note: $t_{\overline{INIT}}$ should be greater than 1.0usec.

2) Reset caused by a sudden voltage (V_{DD}) drop



Note: If V_{DD} drops momentarily down to less than 3.0V and rises up to more than 5.0V (t>1.0usec), a reset may be generated.

Frequency Table (U.S.A.; LC7185-8750)

CHANNEL	FREQENCY (MHz)	RX ($\overline{TX}$=1)		TX ($\overline{TX}$=0)	
		N	Fvco	N	Fvco
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

Vco (TX) = RF ÷ 2
Vco (RX) = RF − 10.695MHz (IF)
CH1 : Vco (TX) = 26.965 ÷ 2 = 13.4825
Vco (RX) = 26.965 − 10.965 = 16.27

Electrical Characteristics

Absolute maximum ratings at Ta=25°C, V_{SS}=0V

		V_{SS}=0V	min	typ	max	unit
Supply Voltage	$V_{DD}max$	V_{DD}	-0.3		9.0	V
Input Voltage	$V_{IN(1)}max$	$\overline{HOLD}$,$\overline{TX}$	-0.3		15	V
	$V_{IN(2)}max$	Input pins other than $V_{IN(1)}max$	-0.3		V_{DD}+0.3	V
Output Voltage	$V_{O(1)}max$	SA,SB,SC,SD,SE,SF,SG, D1,D2	-0.3		15	V
	$V_{O(2)}max$	$\overline{UL}$,BEEP	-0.3		15	V
	$V_{O(3)}max$	PD	-0.3		V_{DD}+0.3	V
	$V_{O(4)}max$	Output pins other than mentioned above	-0.3		V_{DD}+0.3	V
Output Current	$I_{O(1)}max$	SA,SB,SC,SD,SE,SF,SG	0		30	mA
	$I_{O(2)}max$	D1,D2			10	mA
	$I_{O(3)}max$	$\overline{UL}$	0		20	mA
	$I_{O(4)}max$	BEEP	0		10	mA
Allowable Power Dissipation	Pd max	(Ta≤85°C)			350	mW
Operating Temperature	Topg		-40		+85	°C
Storage Temperature	Tstg		-55		+125	°C

Allowable operating conditions at Ta=-40 to +85°C, V_{SS}=0V

Supply Voltage	V_{DD}		5.0		8.0	V
"H"-Level Input Voltage	$V_{IH(1)}$	$\overline{HOLD}$,$\overline{TX}$	0.7V_{DD}		12	V
	$V_{IH(2)}$	$\overline{INIT}$	3.0		V_{DD}	V
	$V_{IH(3)}$	KI1,KI2,KI3,KI4	0.6V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	$\overline{HOLD}$,$\overline{TX}$	0		0.3V_{DD}	V
	$V_{IL(2)}$	$\overline{INIT}$	0		1.5	V
	$V_{IL(3)}$	KI1,KI2,KI3,KI4	0		0.4V_{DD}	V
Output Voltage	$V_{OUT(1)}$	SA,SB,SC,SD,SE,SF,SG, D1,D2	0		13	V
	$V_{OUT(2)}$	$\overline{UL}$,BEEP	0		8	V
Input Frequency	$f_{IN(1)}$	XIN(sine wave, capacitor coupled)	1.0	10.24	15	MHz
	$f_{IN(2)}$	PIN(sine wave, capacitor coupled)	10		30	MHz
Input Amplitude	$V_{IN(1)}$	XIN(sine wave, capacitor coupled)	0.5		1.5	Vrms
	$V_{IN(2)}$	PIN(sine wave, capacitor coupled)	0.15		1.5	Vrms
Required Oscillating Frequency	X'tal	XIN,XOUT(CI≤50ohms)	5.0	10.24	15	MHz

Electrical characteristics at under allowable operating conditions

Internal Feedback Resistance	Rf(1)	XIN		1.0		Mohm
	Rf(2)	PIN		500		kohm
Pull-down Resistor	R_{PdN}	KI1,KI2,KI3,KI4,TEST	30	50	70	kohm
"H"-Level Input Current	$I_{IH(1)}$	$\overline{HOLD}$,$\overline{TX}$ V_I=12V			5.0	uA
	$I_{IH(2)}$	$\overline{INIT}$ V_I=V_{DD}			5.0	uA
	$I_{IH(3)}$	XIN V_I=V_{DD}			20	uA
	$I_{IE(4)}$	PIN V_I=V_{DD}			40	uA

Continued on next page.

Continued from preceding page.

			min	typ	max	unit
"L"-Level Input Current	$I_{IL(1)}$	$\overline{HOLD}$, $\overline{TX}$, $V_I=V_{SS}$			5.0	uA
	$I_{IL(2)}$	$\overline{INIT}$ $V_I=V_{SS}$			5.0	uA
	$I_{IL(3)}$	XIN $V_I=V_{SS}$			2.0	uA
	$I_{IL(4)}$	PIN $V_I=V_{SS}$			4.0	uA
"H"-Level Output Voltage	$V_{OH(1)}$	KO1,KO2,KO3 I_O=1mA	V_{DD} -2.0	V_{DD} -1.0	V_{DD} -0.5	V
	$V_{OH(2)}$	PD I_O=1mA	V_{DD}-1.0			V
"L"-Level Output Voltage	$V_{OL(1)}$	KO1,KO2,KO3 I_O=20uA	0.6	1.0	1.4	V
	$V_{OL(2)}$	PD I_O=0.5mA			1.0	V
	$V_{OL(3)}$	BEEP I_O=2mA			1.0	V
	$V_{OL(4)}$	SA,SB,SC,SD,SE,SF,SG I_O=20mA			1.0	V
	$V_{OL(5)}$	D1,D2 I_O=5mA			1.0	V
	$V_{OL(6)}$	$\overline{UL}$ I_O=10mA			1.0	V
Output Leakage Current	$I_{OFF(1)}$	SA,SB,SC,SD,SE,SF,SG, D1,D2 V_O=13V			5.0	uA
	$I_{OFF(2)}$	$\overline{UL}$,BEEP V_O=8V			5.0	uA
"H"-Level Tristate Leakage Current	I_{OFFH}	PD $V_O=V_{DD}$		0.01	10.0	nA
"L"-Level Tristate Leakage Current	I_{OFFL}	PD $V_O=V_{SS}$		0.01	10.0	nA
Supply Current	$I_{DD(1)}$	Normal mode *1(PLL operates)		10	15	mA
	$I_{DD(2)}$	Hold mode V_{DD}=3.0V			5	uA
		*2(memory backup) V_{DD}=8.0V			15	uA

*1 $f_{IN(2)}$=20MHz(PIN)
$V_{IN(2)}$=0.15Vrms
X'tal=10.240MHz
$\overline{TX}=\overline{HOLD}=\overline{INIT}=V_{DD}$
Other inputs=V_{SS}
Other outputs=open

*2 $\overline{HOLD}=V_{SS}$
$\overline{TX}=\overline{INIT}=V_{DD}$
Other inputs=V_{SS}
Other outputs=open

APPENDIX 10

FINAL RF AMPLIFIER DATA SHEETS

FOUR (4) PAGES FOR 2SC2078 FOLLOW THIS SHEET

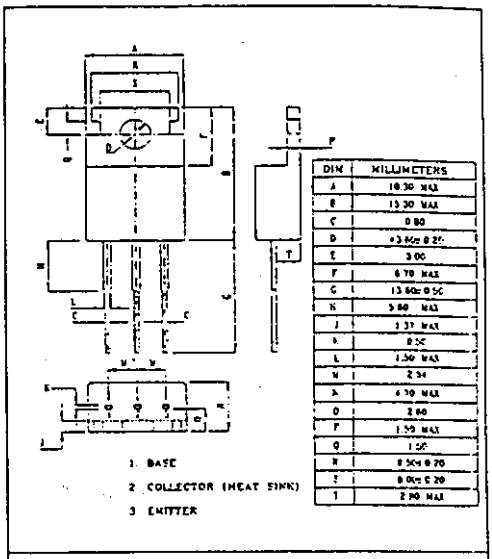
B TRANSCEIVER TX FINAL AMPLIFIER APPLICATION.
F TRANSCEIVER APPLICATION.

EATURES

Recommended for Output Stage Application of M 4W Transmitter.

High Power Gain.

Wide Area of Safe Operation.



TO-220AB

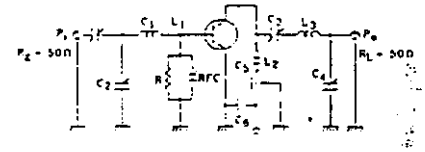
AXIMUM RATINGS(Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
ollector-Base Voltage	V_{CBO}	80	V
ollector-Emitter Voltage (R_{BE}=50Ω)	V_{CER}	80	V
tter-Base Voltage	V_{EBO}	4	V
ollector Current	I_C	4	A
mitter Current	I_E	-4	A
ollector Power Dissipation (Tc=25℃)	P_C	10	W
unction Temperature	T_j	150	℃
torage Temperature Range	T_{stg}	-55~150	℃

ECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
llector Cut-off Current		I_{CBO}	V_{CB}=30V, I_E=0	-	-	10	μA
eakdown ge	Collector-Emitter	$V_{(BR)CER}$	I_C=10mA, R_{BE}=50Ω	80	-	-	V
	Emitter-Base	$V_{(BR)EBO}$	I_E=1.0mA, I_C=0	4	-	-	V
Current Gain		h_{FE}	V_{CE}=5V, I_C=0.5A	100	-	200	
llector-Emitter turation Voltage		$V_{CE(sat)}$	I_C=3A, I_B=0.3A	-	-	1.5	V
ansition Frequency		f_T	V_{CE}=5V, I_C=500mA	100	-	-	MHz
llector Output Capacitance		C_{ob}	V_{CB}=10V, I_E=0, f=1MHz	-	40	-	pF
tput Power (Fig.1)		P_o	V_{CC}=12V, P_i=0.3W, f=27MHz	4	-	-	W

Fig.1 P_o TEST CIRCUIT



C_1 : ~100pF, C_2, C_3 : ~150pF, C_4 : ~300pF, C_5 : 1000pF
C_6 : 0.01μF, R : 250Ω
L_1 : 0.8mmφ UEW, 7T, 8mm I.D L_2 : 0.8mmφ UEW, 5T, 8mm I.D
L_3 : 0.8mmφ UEW, 10T, 8mm I.D RFC : 0.35mmφ UEW, 17T, 5mm I.D

KTC2078

EPITAXIAL PLANAR NPN TRANSISTOR.

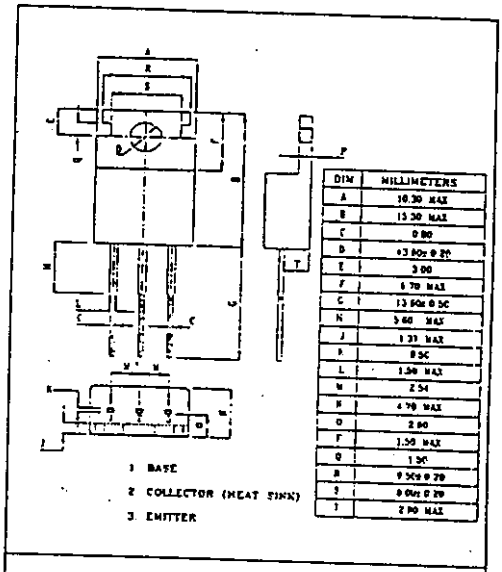
B TRANSCEIVER TX FINAL AMPLIFIER APPLICATION.
F TRANSCEIVER APPLICATION.

EATURES

Recommended for Output Stage Application of M 4W Transmitter.

High Power Gain.

Wide Area of Safe Operation.



TO-220AB

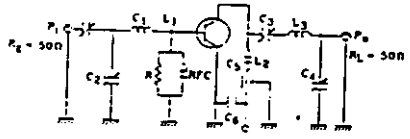
AXIMUM RATINGS(Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
ollector-Base Voltage	V_{CBO}	80	V
ollector-Emitter Voltage (R_{BE}=50Ω)	V_{CER}	80	V
mitter-Base Voltage	V_{EBO}	4	V
ollector Current	I_C	4	A
mitter Current	I_E	-4	A
ollector Power Dissipation (Tc=25℃)	P_C	10	W
unction Temperature	T_J	150	℃
torage Temperature Range	T_{stg}	-55~150	℃

ECTRICAL CHARACTERISTICS (Ta=25℃)

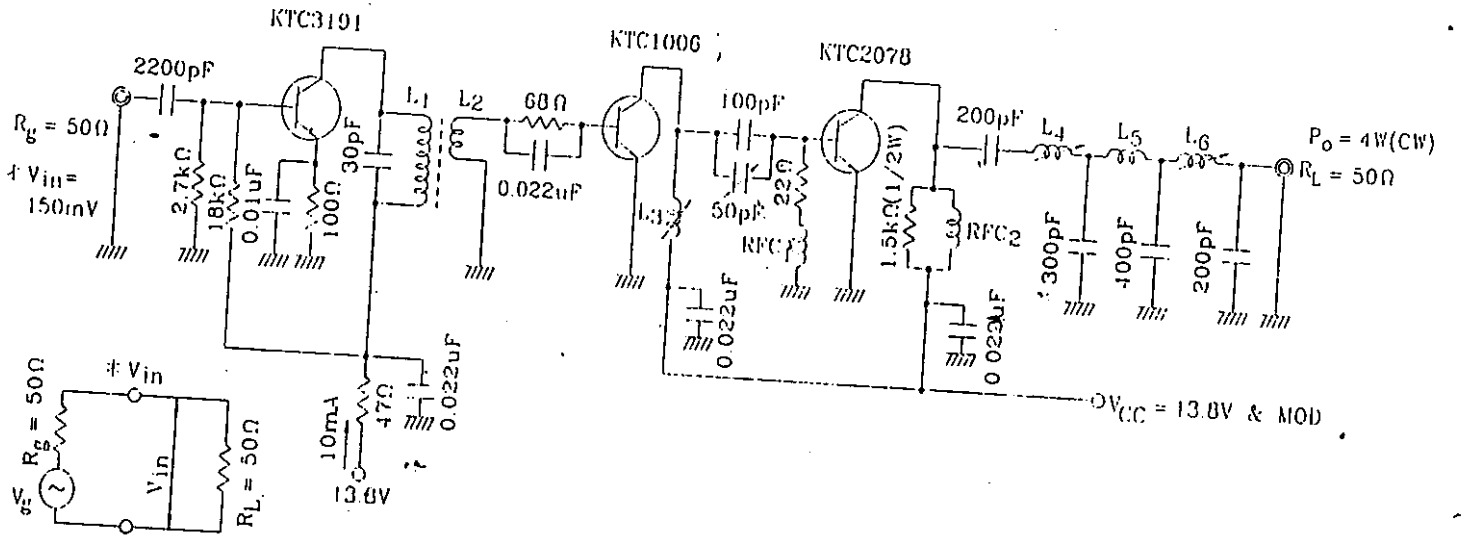
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
llector Cut-off Current		I_{CBO}	V_{CB}=30V, I_E=0	-	-	10	μA
eakdown Voltage	Collector-Emitter	$V_{(BR)CER}$	I_C=10mA, R_{BE}=50Ω	80	-	-	V
	Emitter-Base	$V_{(BR)EBO}$	I_E=1.0mA, I_C=0	4	-	-	V
Current Gain		h_{FE}	V_{CE}=5V, I_C=0.5A	100	-	200	
llector-Emitter turation Voltage		$V_{CE(sat)}$	I_C=3A, I_B=0.3A	-	-	1.5	V
ansition Frequency		f_T	V_{CE}=5V, I_C=500mA	100	-	-	MHz
llector Output Capacitance		C_{ob}	V_{CB}=10V, I_E=0, f=1MHz	-	40	-	pF
tput Power (Fig.1)		P_o	V_{CC}=12V, P_i=0.3W, f=27MHz	4	-	-	W

Fig.1 P_o TEST CIRCUIT



C_1 : ~100pF, C_2, C_3 : ~150pF, C_4 : ~300pF, C_5 : 1000pF
C_6 : 0.01μF, R : 250Ω
L_1 : 0.8mm φ UEW, 7T, 8mm I.D L_2 : 0.8mm φ UEW, 5T, 8mm I.D
L_3 : 0.8mm φ UEW, 10T, 8mm I.D RFC : 0.35mm φ UEW, 17T, 5mm I.D

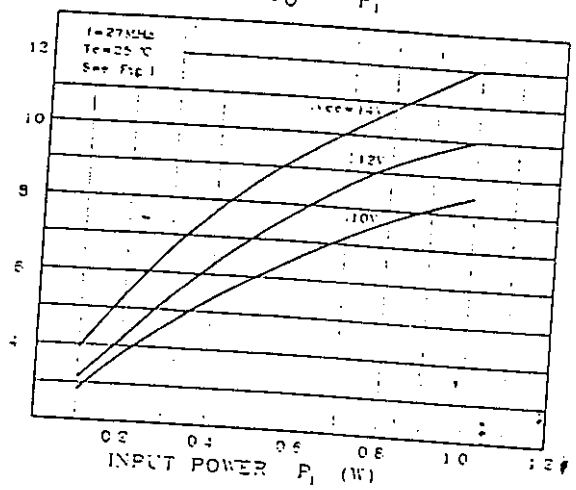
Fig.2 27MHz 4W OUTPUT AM TRANSCEIVER CIRCUIT



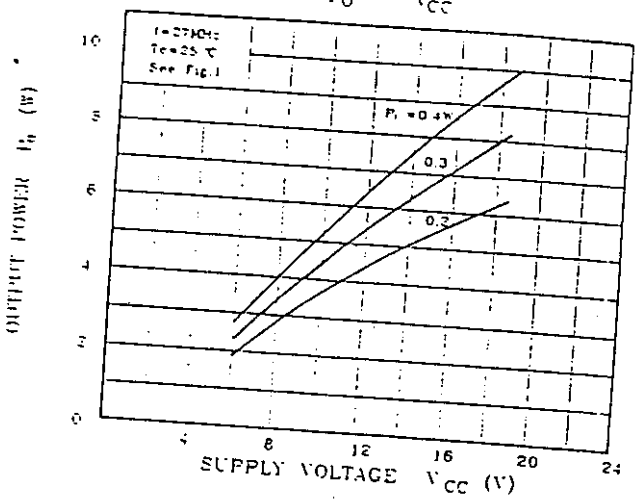
L_1 : 4mmø BOBBIN WITH FERRITE CORE, 0.08mmø UEW, 8 TURNS
L_2 : 4mmø BOBBIN WITH FERRITE CORE, 0.08mmø UEW, 2 TURNS
L_3, L_6 : 6.5mmø BOBBIN WITH FERRITE CORE, 0.6mmø Sn PLATED COPPER WIRE 6 $\frac{1}{2}$ TURNS
L_4 : 6.5mmø BOBBIN WITH FERRITE CORE, 0.6mmø Sn PLATED COPPER WIRE 8 $\frac{1}{2}$ TURNS
L_5 : 0.6mmø Sn PLATED COPPER WIRE, 6.5mm I.D, 8 $\frac{1}{2}$ TURNS
RFC_1 : 4.7uH,7BA-480k (TOKO)
RFC_2 : 0.2mmø, UEW, 30 TURNS

RESISTOR : 1/4W CARBON
CAPACITOR : CERAMIC

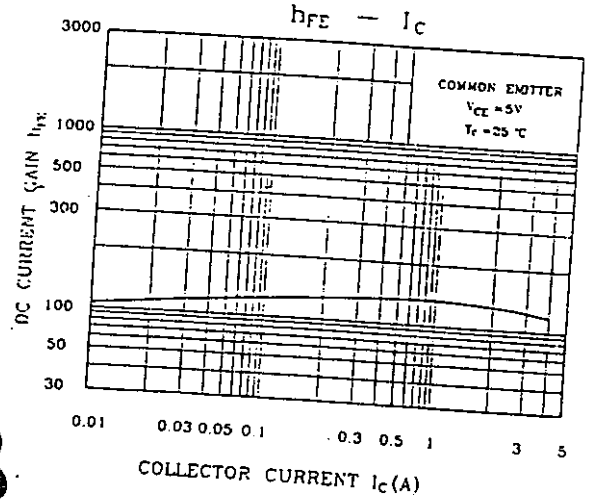
$P_O - P_I$



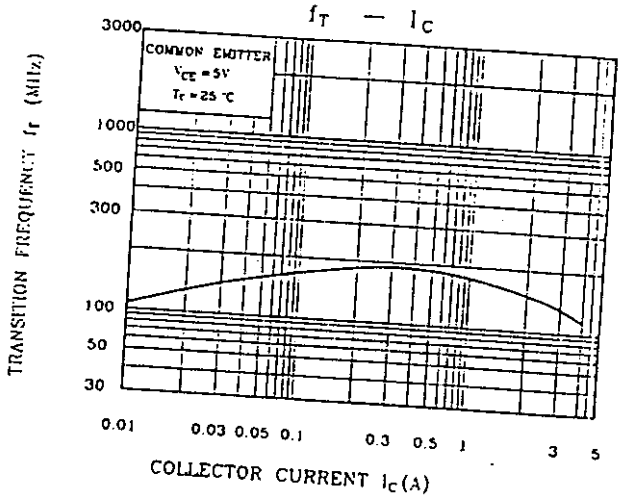
$P_O - V_{CC}$



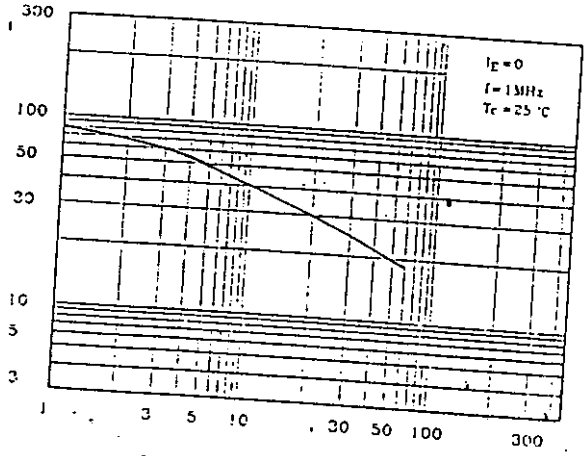
$h_{FE} - I_C$



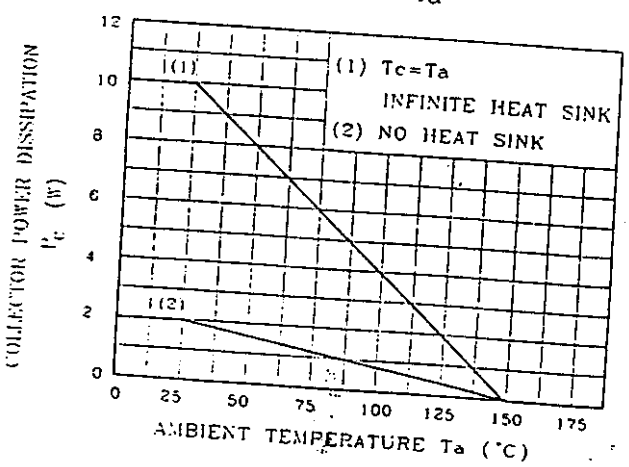
$f_T - I_C$



$C_{ob} - V_{CB}$



$P_C - Ta$



APPENDIX 3

FUNCTION OF DEVICES

HH28

ONE (1) PAGE LIST OF ACTIVE SEMICONDUCTORS
AND FUNCTIONS FOLLOW THIS SHEET

C . SEMICONDUCTORS AND FUNCTION

REF. NO	DESCRIPTION	RX	TX	REMARK
Q101	KTC3875S	RF ATTENUATOR	×	KEC
Q102	KTC3880S	RF AMP	×	KEC
Q103	KTC3880S	1'ST MIXER	×	KEC
Q201	KTC3880S	2'ND MIXER	×	KEC
Q202	KTC3880S	IF AMP	×	KEC
Q203	KTC3880S	IF AMP	×	KEC
Q204	KTA1504S	A.N.L.	×	KEC
Q403	KTA1504S	×	A. L. C.	KEC
Q404	KTC3875S	×	A. L. C.	KEC
Q500	KTC3875S	LED CONTROL	LED CONTROL	KEC
Q501	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q502	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q503	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q510	KTC3875S	CHARGE PUMP	CHARGE PUMP	KEC
Q511	KTC3875S	CHARGE PUMP	CHARGE PUMP	KEC
Q513	KRC110S	SQ CONTROL	X	KEC
Q550	KTC3875S	SQ CONTROL	×	KEC
Q553	KTA1504	SQ CONTROL	×	KEC
Q601	KTC3880S	BUFFER	BUFFER	KEC
Q602	KTC3875S	×	SWITCHING	KEC
Q603	KTC3880S	VCO	VCO	KEC
Q701	KTC3880S	×	DOUBLER	KEC
Q702	KTC3880S	×	PRE AMP	KEC
Q703	KTC1006	×	RF DRIVER	KEC
Q704	KTC2078	×	RF POWER AMP	KEC
Q900	KTC3875S	BATT LOW	BATT LOW	KEC
Q901	KTC3875S	BATT LOW	BATT LOW	KEC
Q902	KTC3875S	REGULATOR(9.1V)	REGULATOR(9.1V)	KEC
Q903	KRA102S	B+ CONTROL	×	KEC
Q904	KRA102S	×	B+ CONTROL	KEC
IC401	KIA7217AP	×	AF AMP	KEC
IC501	LC7185	PLL	PLL	SANYO
IC551	LM386	AF AMP	×	NATIONAL

*** MANUFACTURER INFORMATION ***

* K.E.C ---------- KOREA ELECTRONICS SEMICONDUCTOR CO., LTD.
* SANYO ---------- JAPAN SANYO SEMICONDUCTOR CO., LTD.
* NATIONAL ---------- NATIONAL SEMICONDUCTOR CO., LTD.

APPENDIX 4

SCHEMATIC DIAGRAM

ONE (1) SCHEMATIC DIAGRAM FOLLOWS THIS SHEET

TABLE 1

TRANSMITTER CONDUCTED SPURIOUS

Channel	Spurious Frequency MHz	dB Below Unmod Carrier Ref. Low	High
1	53.930	86	83
1	80.895	75	82
1	107.860	88	89
1	134.825	95	93
1	161.790	96	96
1	188.755	95	95
1	215.720	93	94
1	242.685	94	93
1	269.650	91	94
21	54.430	89	86
21	81.645	76	85
21	108.860	90	93
21	136.075	95	92
21	163.290	94	93
21	190.505	93	93
21	217.720	95	95
21	244.935	95	94
21	272.150	93	94
40	54.810	91	91
40	82.215	76	86
40	109.620	89	90
40	137.025	92	92
40	164.430	96	95
40	191.835	96	93
40	219.240	96	94
40	246.645	92	96
40	274.050	94	91
	Required:	60	60

All other spurious were more than 20 dB below required 60 dB suppression.

E. FIELD STRENGTH MEASUREMENTS OF SPURIOUS RADIATION (Paragraph 2.993(a)(b,2) of the Rules)

Field intensity measurements of radiated spurious emissions from the HH28 transmitter were made with a Tektronix 494P spectrum analyzer and dummy load located in an open field 3 meters from the test antenna. Output power was 3.5 watts. The supply voltage was 13.8 volts. The transmitter and test antennae were arranged according to OCE 42 to maximize pickup. No external accessory jacks are provided. Both vertical and horizontal test antenna polarization were employed.

Measurements were made from 10 MHz to 10 times the maximum operating frequency of 26.965 or 269.650 MHz.

Reference level for the spurious radiations was taken as an ideal dipole excited by 3.5 watts, the output power of the transmitter according to the following relationship:*

$$E = \frac{(49.2 \times P_t)^{1/2}}{R}$$

where E = electric-field intensity in volts/meter

P_t = transmitter power in watts

R = distance in meters

for this case $E = \frac{(49.2 \times 3.5)^{1/2}}{3} = 4.4$ V/m

Since the spectrum analyzer is calibrated in decibels above one milliwatt (dBm):

4.2 volts/meter $= 4.2 \times 10^6$ uV/m

dBu/m $= 20 \text{ Log}_{10}(4.2 \times 10^6)$

$= 133$ dBu/m

Since 1 uV/m $= -107$ dBm, the reference becomes

$133 - 107 = 26$ dBm

Representing a conversion for convenience, from dBu to dBm. The measurement system was capable of detecting signals 100 dB or more below the carrier reference level. Data, including antenna factor and line loss corrections, are shown in Table 2.

*Reference Data for Radio Engineers, International Telephone and Telegraph Corporation, Sixth Edition.

F. FIELD STRENGTH MEASUREMENTS (Continued)

TABLE 2

TRANSMITTER CABINET RADIATED SPURIOUS
Channel 1, 26.965 MHz; 3.5 watts, 13.8 Vdc

	dB Below Carrier Reference	
Frequency, MHz	(V)	(H)
53.930	81	91
80.895	102	102
107.860	100	89
134.825	91	89
161.790	84	81
188.755	95	91
215.720	98	95
242.685	95	94
269.650	93	94
Required:	60	60

Any unlisted spurious were more than 80 below carrier reference from 4.5 to 269.65 MHz.

F. FREQUENCY STABILITY
(Paragraph 2.995(a)(1) of the Rules)

Measurement of frequency stability versus temperature was made at temperatures from -30°C to +50°C in 10° increments. At each temperature, the unit was exposed to the test chamber ambient a minimum of 60 minutes after indicated chamber temperature ambient had stabilized to within ±2° of the desired test temperature. Following a 30 minute soak at each temperature, the unit was turned on, keyed and frequency measured within 2 minutes. Test temperature was sequenced in the order shown in Table 3, starting with -30°C.

A Thermotron S1.2 temperature chamber was used. The transmitter output stage was terminated in a dummy load. Primary supply was 13.8 volts. Frequency was measured with a HP 5385A digital frequency counter connected to the transmitter through a power attenuator. Measurements were made on Channel 9, 27.065 MHz. No transient keying effects were observed.

G. FREQUENCY STABILITY (Continued)

TABLE 3

Temperature	Output Frequency, MHz
-29.0	27.064770
-19.8	27.064931
- 9.4	27.065018
0.1	27.065059
9.9	27.065061
20.4	27.065035
30.5	27.065008
40.3	27.065007
50.0	27.065050
Maximum frequency error:	27.065000
	27.064770
	- .000230 MHz

FCC Rule 95.625(b) specifies .005% or a maximum of ± .001353 MHz.

G. FREQUENCY STABILITY AS A FUNCTION OF SUPPLY VOLTAGE (Paragraph 2.995(d)(2) of the Rules)

Oscillator frequency as a function of power supply voltage was measured with a HP 5385A digital frequency counter as supply voltage provided by an HP 6264B variable dc power supply was varied ±15% from the nominal 13.8 volt rating. A Keithley 197 digital voltmeter was used to measure supply voltage at transmitter primary input terminals. Measurements were made at 20°C ambient.

TABLE 4

Supply Voltage	Output Frequency, MHz
15.87	27.065036
15.19	27.065037
14.49	27.065034
13.80	27.065035
13.11	27.065037
12.42	27.065036
11.73	27.065039
11.04 (rated battery end-point)	27.065037
Maximum frequency error:	27.065000
	27.065037
	+ .000037 MHz

FCC Rule 95.625(b) specifies .005% or a maximum of ± .001353 MHz. No effects on frequency related to keying the unit were observed.

H. ADDITIONAL REQUIREMENTS FOR TYPE ACCEPTANCE
(Paragraph 95.669 of the Rules)

The HH28 meets the applicable provision of 95.669(a).

External controls are limited to the following per 95.669(a):

1. Primary power connection
2. Microphone
3. RF output power connection
4. Not applicable, no accessory jacks
5. On-off switch (combined with receiver volume control)
6. Not applicable, AM only
7. Not applicable, AM only
8. Transmitting frequency selector
9. Transmit-receive switch
10. See #1
11. Not applicable

The serial number of each unit will be implemented in accordance with 95.671.

A copy of Part 95, Subpart D, of the FCC rules for the Citizens Band Radio Service, current at the time of packing of the transmitter, must be furnished with each CB transmitter marketed per 95.673.

I. PLL RESTRICTIONS
(Per Public Notice of April 27, 1978)

The HH28 meets the following conditions specified in the April 27, 1978 notice:

1. All frequency-determining elements, including crystals, PLL integrated circuits and channel selector switches are permanently wired and soldered in place.

2. The PLL integrated circuit division ratio selection is BCD coded. All the 40 channels are mask programmed into the CPU and can not be changed.

3. Channel selection is controlled by the masked program of the CPU and has only 40 positions for use in the US.

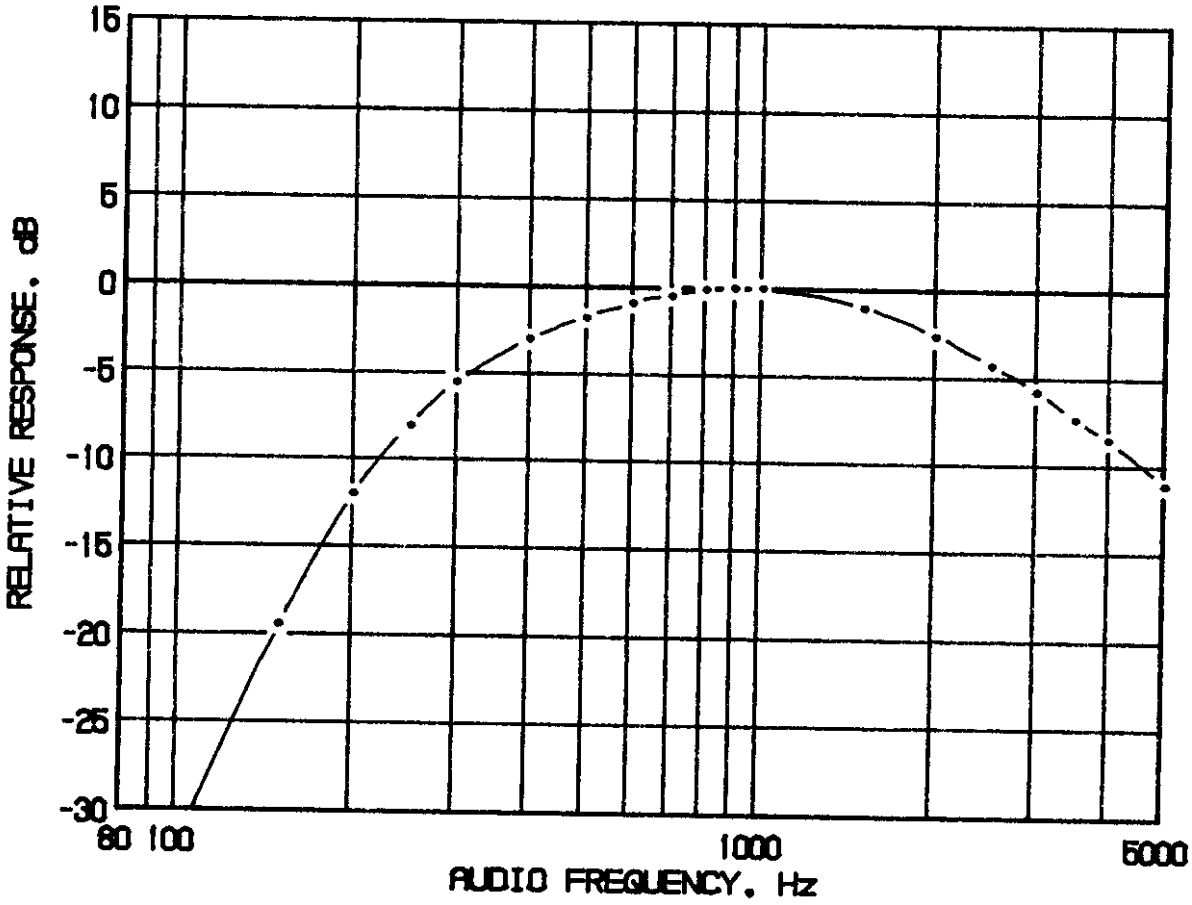
4. All the undedicated leads in the CPU and Pll integrated circuits are disabled and not serviceable by the user.

J. FINAL AMPLIFIER DATA

1. A copy of the final RF amplifier data sheet is included in Appendix 10.

FIGURE 1

TRANSMITTER FREQUENCY RESPONSE

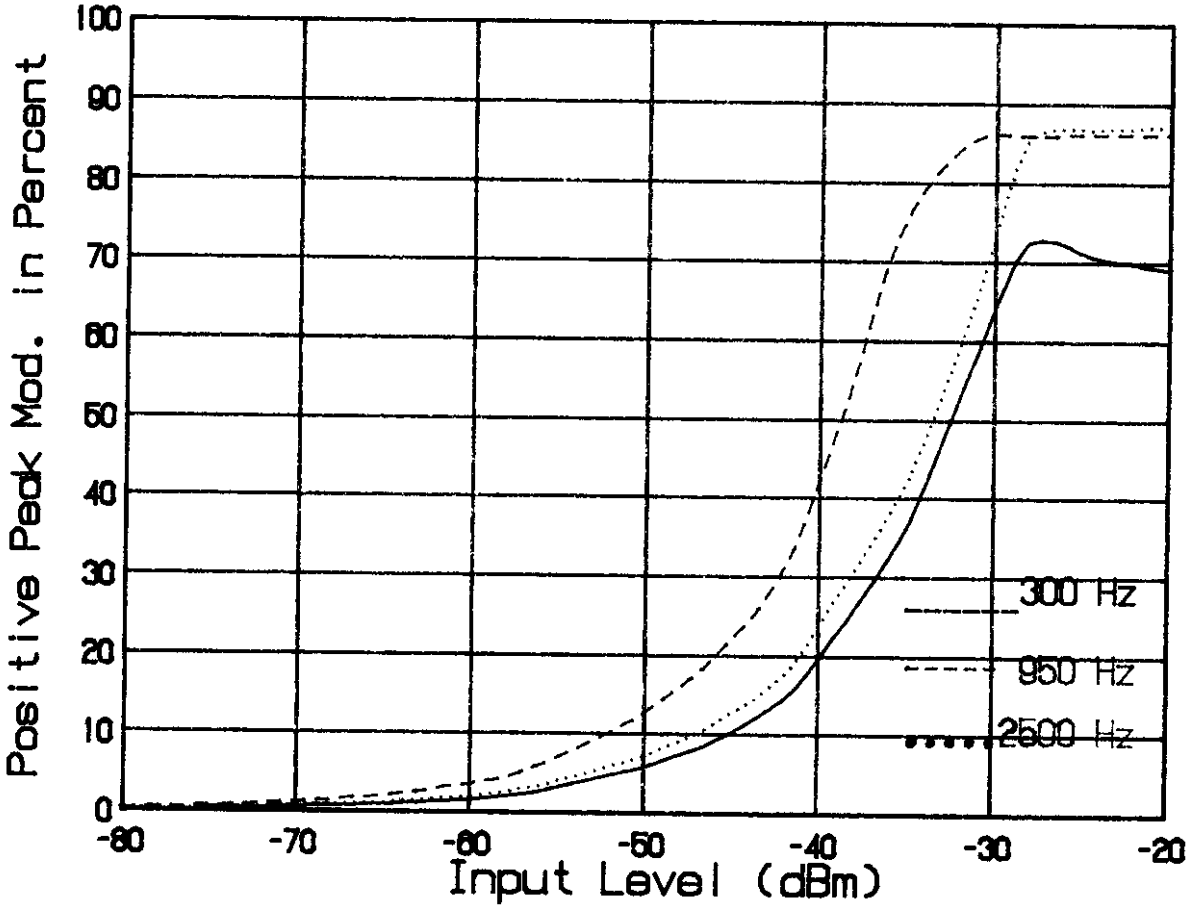


TRANSMITTER FREQUENCY RESPONSE
FCC ID: BBOHH28

FIGURE 1

FIGURE 2a

AM MODULATION LIMITING - POSITIVE PEAKS



MODULATION LIMITING CHARACTERISTICS

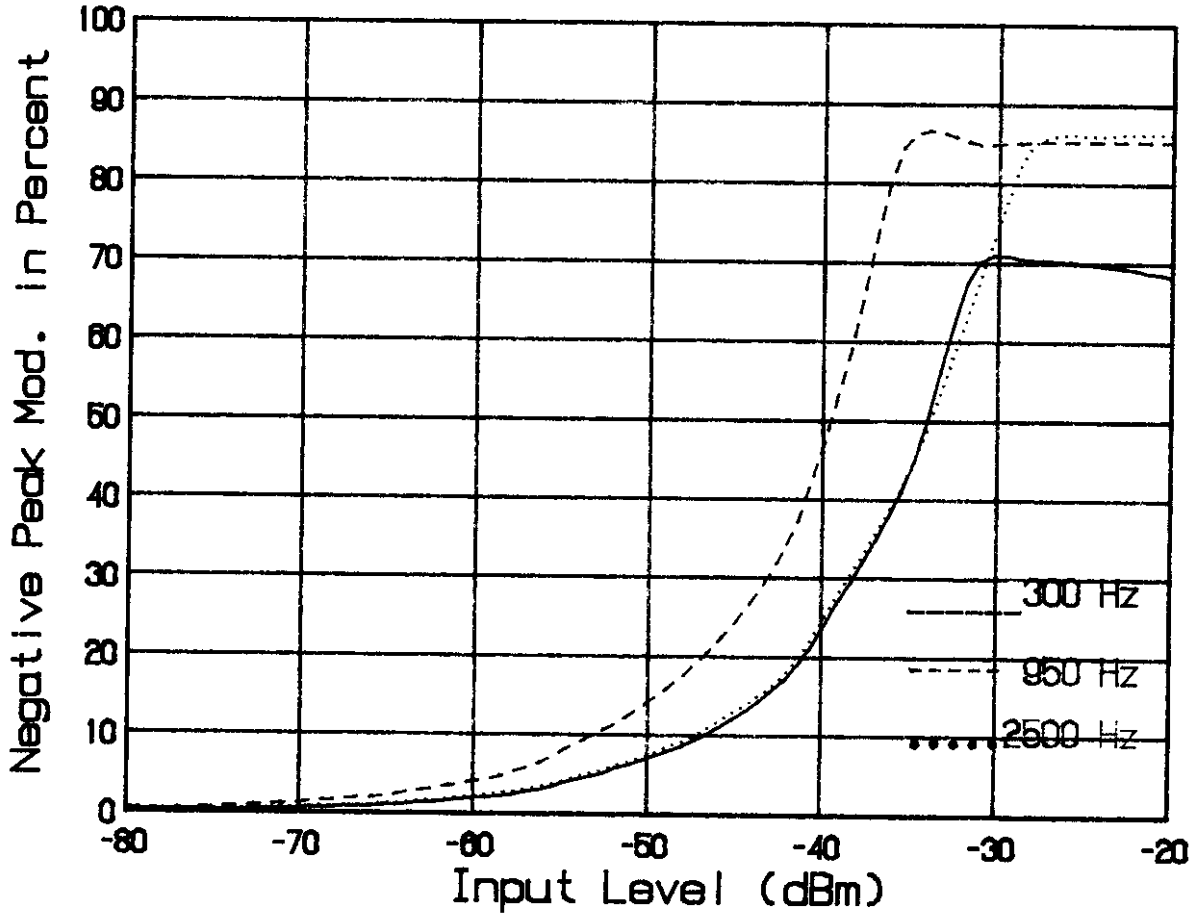
Percent modulation as a function of input level at microphone jack in dBm for 300 Hz, 950 Hz, and 2500 Hz tones.

MODULATION LIMITING POSITIVE PEAKS
FCC ID: BBOHH28

FIGURE 2a

FIGURE 2b

AM MODULATION LIMITING - NEGATIVE PEAKS



MODULATION LIMITING CHARACTERISTICS

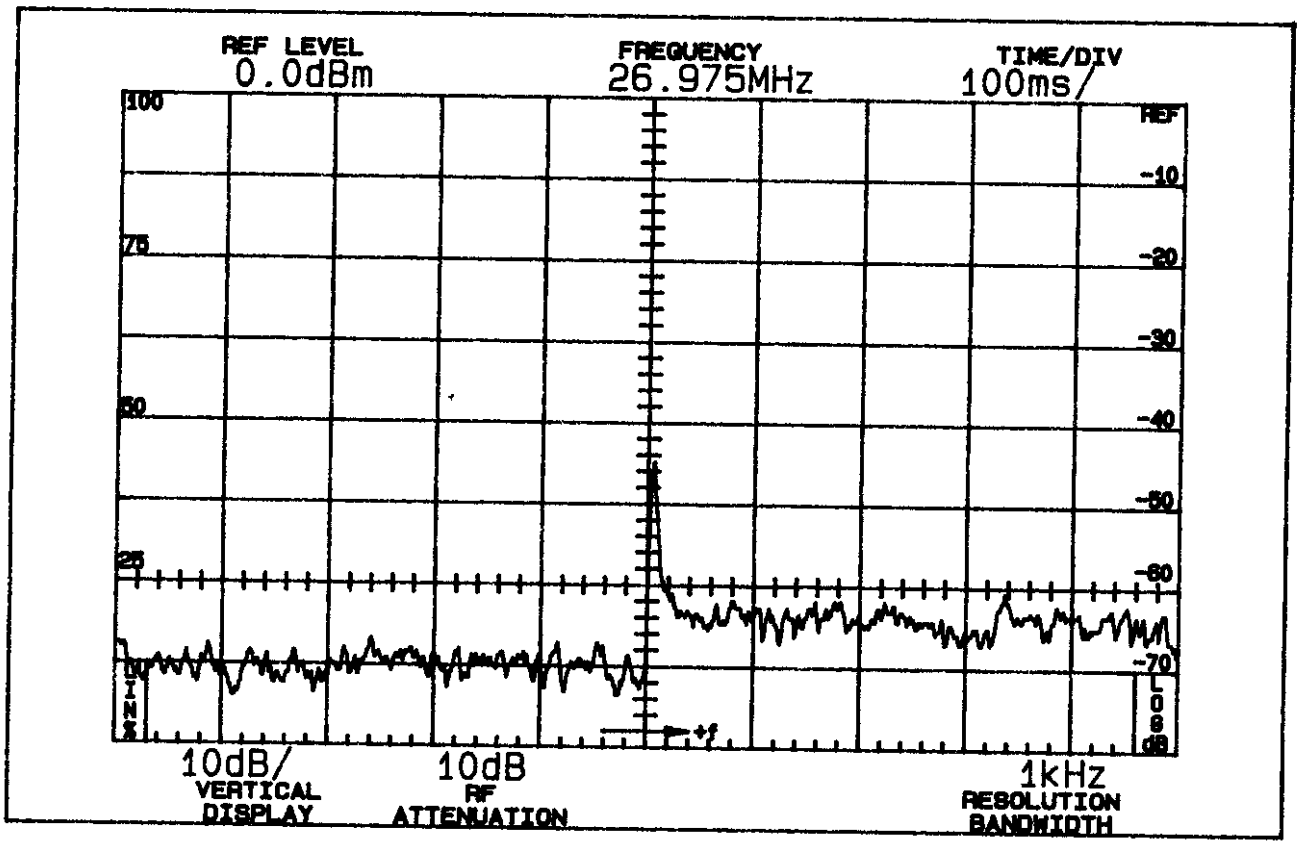
Percent modulation as a function of input level at microphone jack in dBm for 300 Hz, 950 Hz, and 2500 Hz tones.

MODULATION LIMITING NEGATIVE PEAKS
FCC ID: BBOHH28

FIGURE 2b

FIGURE 3a

MODULATION LIMITER ATTACK TIME



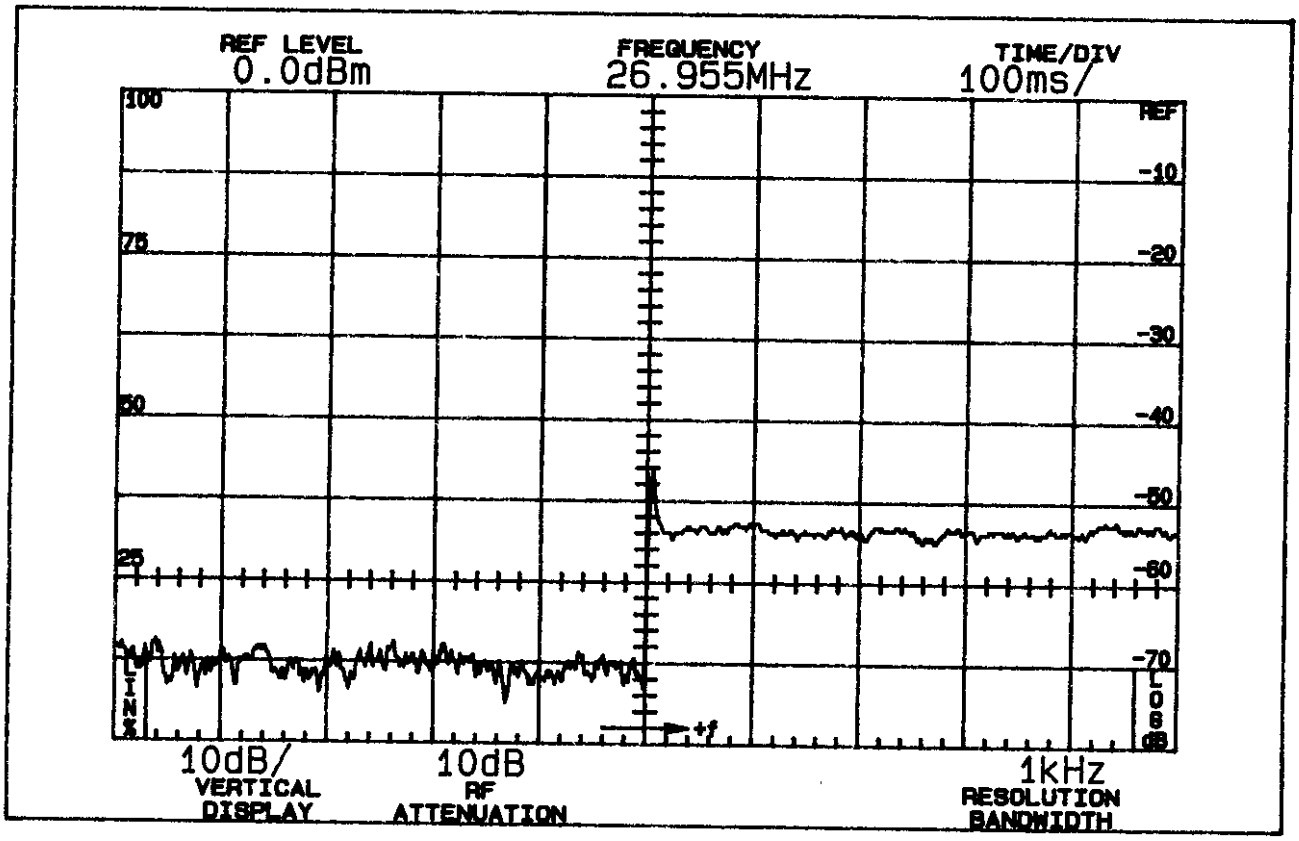
Measurement Conditions: 16 dB over 50% modulation level at 950 Hz with 2500 Hz tone, upper fourth order sideband; horizontal scale 100 ms/div.

UPPER FOURTH-ORDER SIDEBAND
LIMITER ATTACK TIME
FCC ID: BBOHH28

FIGURE 3a

FIGURE 3b

MODULATION LIMITER ATTACK TIME



Measurement Conditions: 16 dB over 50% modulation level at 950 Hz with 2500 Hz tone, lower fourth order sideband; horizontal scale 100 ms/div.

LOWER FOURTH-ORDER SIDEBAND
LIMITER ATTACK TIME
FCC ID: BBOHH28

FIGURE 3b

C. MODULATION CHARACTERISTICS (Continued)

4. Occupied Bandwidth - AM
(Paragraph 2.989(c) of the Rules)

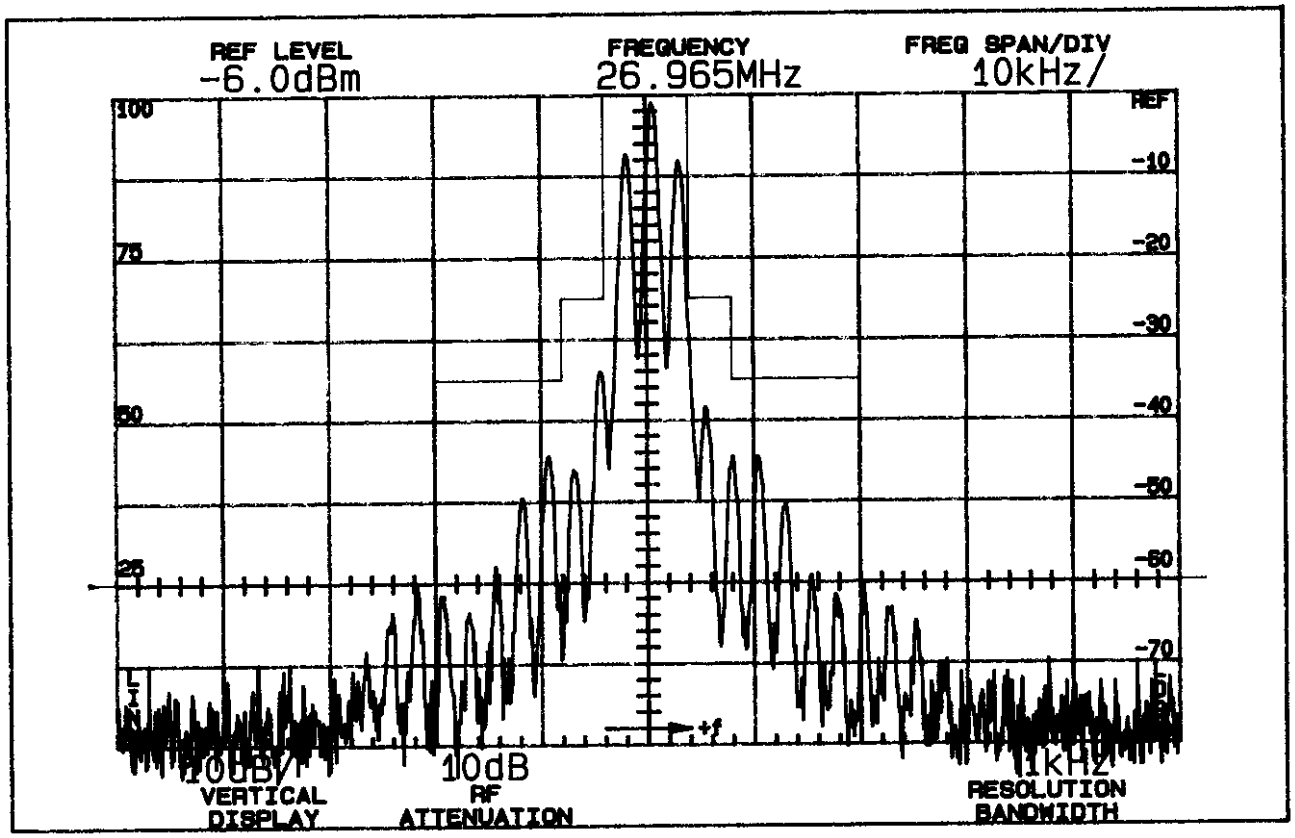
Figures 4a and 4b are plots of the sideband envelope of the transmitter at low and high power settings respectively taken from a Tektronix 494P spectrum analyzer. Modulation corresponded to conditions of 2.989(a) and consisted of 2500 Hz tone at an input level 16 dB greater than that necessary to produce 50% modulation at 950 Hz, the frequency of maximum response. Measured modulation under these conditions was 95%.

The plots are within the limits imposed by Paragraph 95.631(b)(1,3) for double sideband AM modulation. The horizontal scale, frequency, is 10 kHz per division and the vertical scale, amplitude, is a logarithmic presentation equal to 10 dB per division.

NOTE: Reference of 0 dBc is unmodulated transmitter power.

FIGURE 4a

OCCUPIED BANDWIDTH



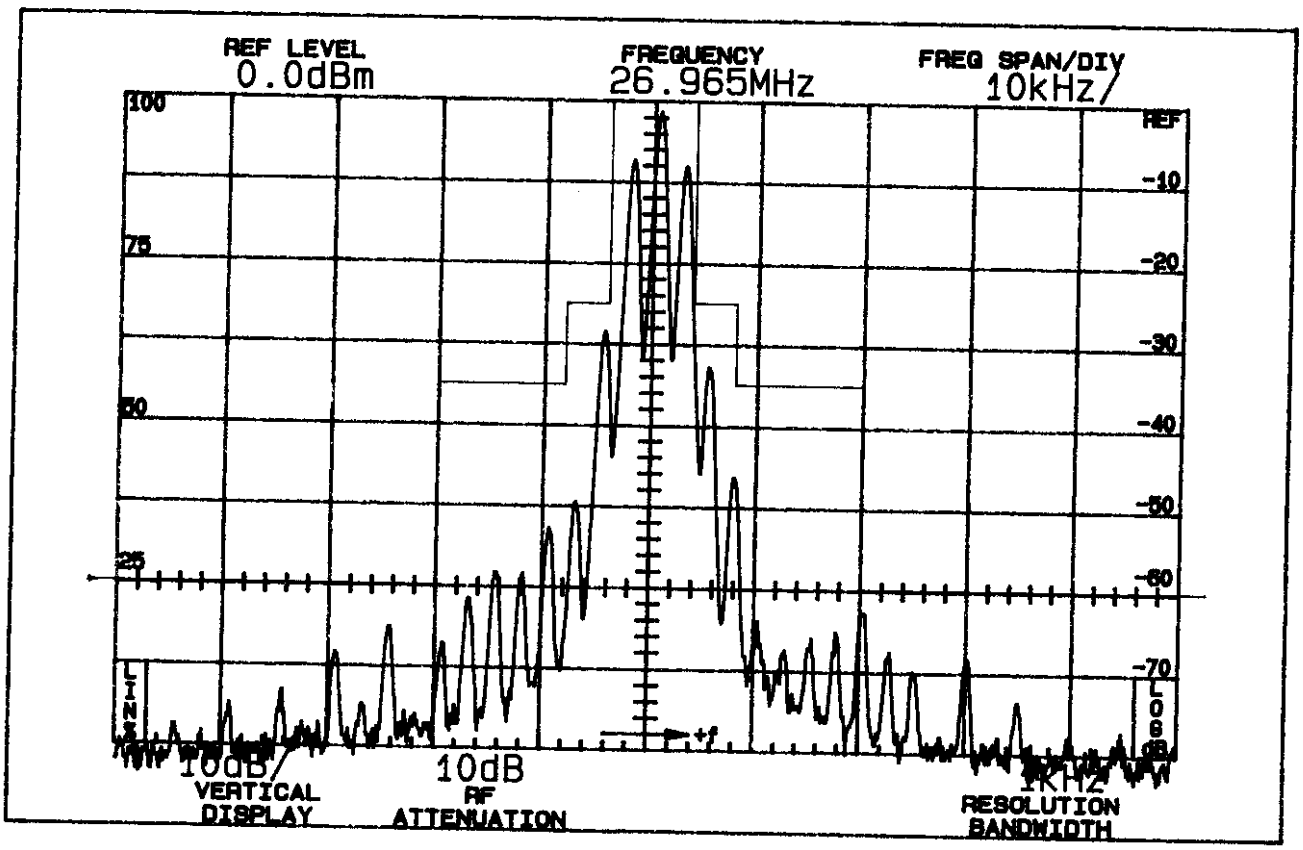
	ATTENUATION IN dB BELOW MEAN OUTPUT POWER Required
On any frequency more than 50% up to and including 100% of the authorized bandwidth, 8kHz (4-8kHz)	25
On any frequency more than 100%, up to and including 250% of the authorized bandwidth (8-20kHz)	35
On any frequency removed from the assigned frequency by more than 250% of the authorized bandwidth	60

OCCUPIED BANDWIDTH
FCC ID: BBOHH28

FIGURE 4a (Low Power)

FIGURE 4b

OCCUPIED BANDWIDTH



	ATTENUATION IN dB BELOW MEAN OUTPUT POWER Required
On any frequency more than 50% up to and including 100% of the authorized bandwidth, 8kHz (4-8kHz)	25
On any frequency more than 100%, up to and including 250% of the authorized bandwidth (8-20kHz)	35
On any frequency removed from the assigned frequency by more than 250% of the authorized bandwidth	60

OCCUPIED BANDWIDTH
FCC ID: BBOHH28

FIGURE 4b (High Power)

D. SPURIOUS EMISSIONS AT THE ANTENNA TERMINALS
(Paragraph 2.991 of the Rules)

The HH28 transmitter was tested in the AM mode for spurious emissions at the antenna terminals while the equipment was modulated with a 2500 Hz signal, 16 dB above minimum input signal for 50% modulation at 950 Hz, the frequency of highest sensitivity.

Measurements were made with Tektronix 494P spectrum analyzer coupled to the transmitter output terminal through Narda 765-20 50 ohm power attenuator.

In order to improve measurement system dynamic range, a series trap tuned to the carrier frequency was used on the Narda attenuator output. The trap, which had negligible shunt attenuation at the second harmonic and high frequencies, provided 26 dB attenuation of the fundamental. The trap was not used during close-in (within 10 MHz of the carrier) spurious measurements.

During the tests, the transmitter was terminated in the Narda 765-20 dummy load. Power was monitored on a Bird 43 Thru-Line wattmeter; dc supply was 13.8 volts throughout the tests.

Spurious emission was measured at both power settings on Channels 1, 21, and 40 throughout the RF spectrum from 10 to 300 MHz. Any emissions that were between the 60 dB attenuation required and the 100 dB noise floor of the spectrum analyzer were recorded. Data are shown in Table 1.