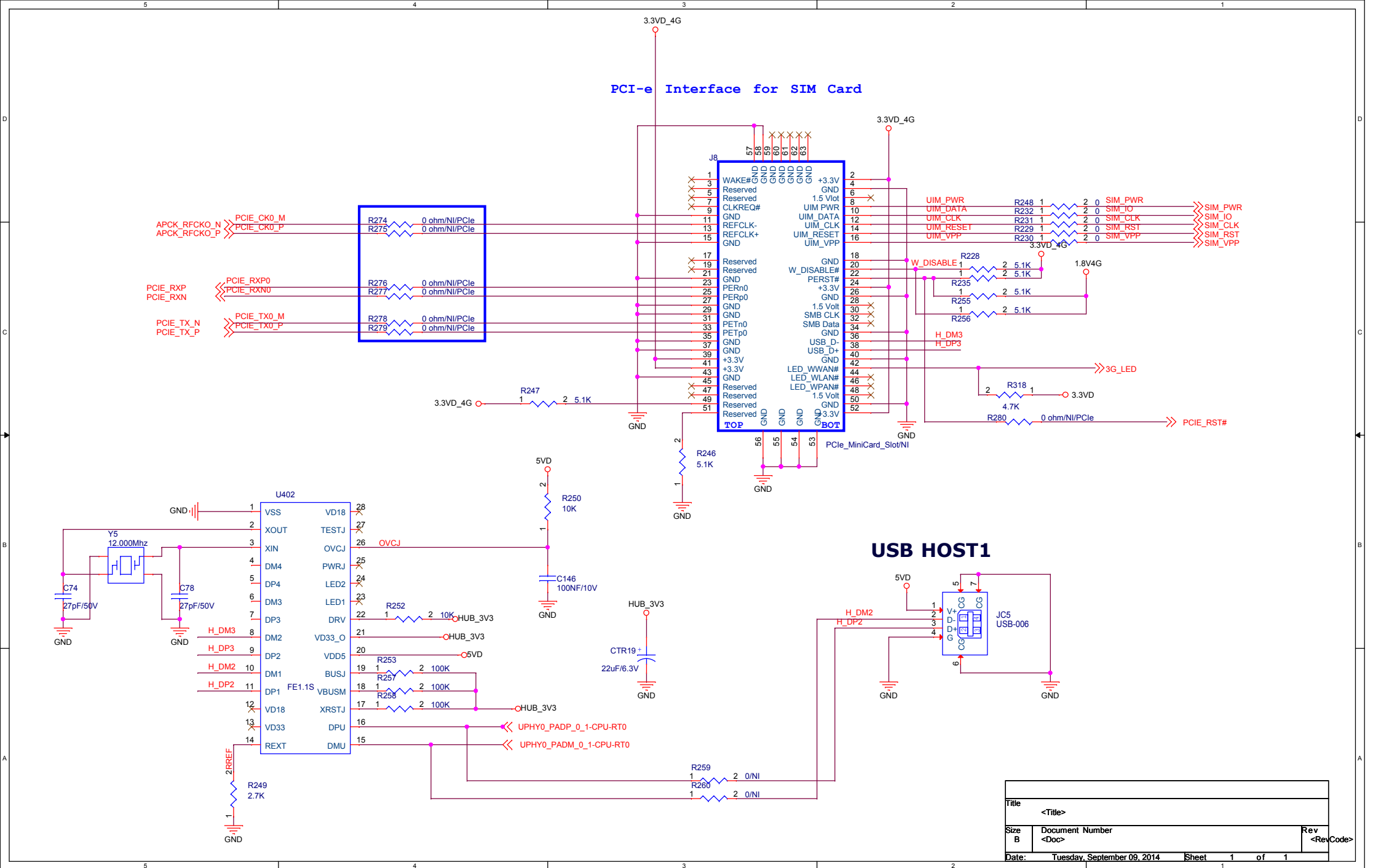
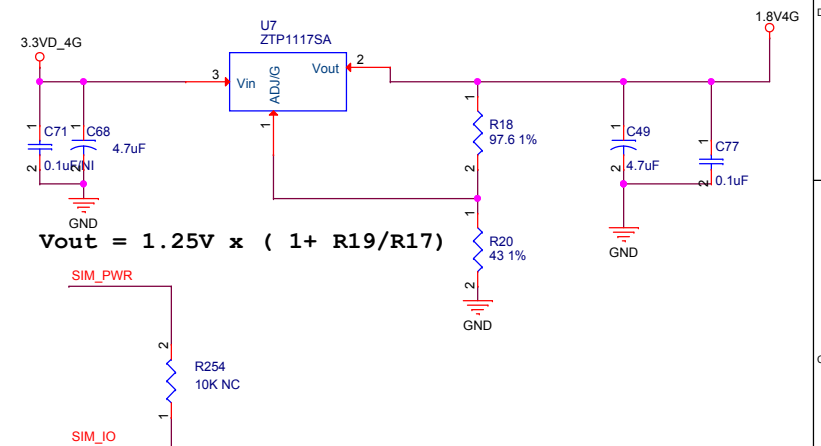
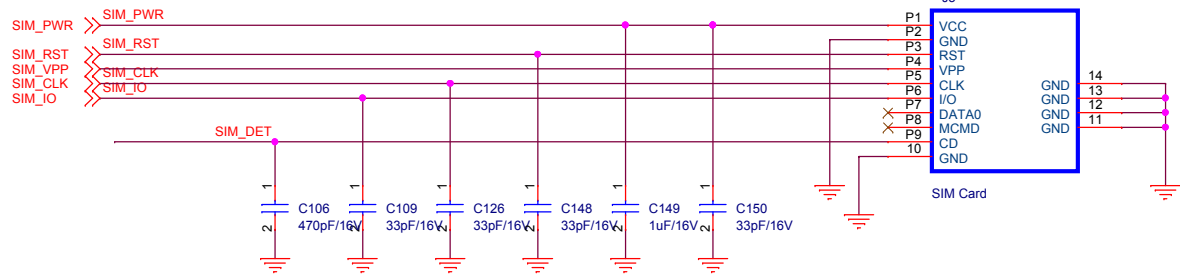




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Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, September 09, 2014	Sheet 1 of 1



Title		
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Size B	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, August 12, 2014	Sheet 1 of 1

[11] MDATA[0:15]

Close to RT6352

1. 1.8V for DDR2
2. 2.5V for DDR1

1.8VD

1.8VD

1.8VD

1.8VD

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1.8VD

1.8VD

1.8VD

F6 GND
F7 GND
F8 GND
F9 GND
F10 GND
F11 GND
F12 GND
G6 GND
G7 GND
G8 GND
G9 GND
G10 GND
G11 GND
G12 GND
K4 GND
F2 GND
H5 VDD25/DDR_IO_V18D
J5 VDD25/DDR_IO_V18D
K5 VDD25/DDR_IO_V18D
N6 VDD25/DDR_IO_V18D
P7 VDD25/DDR_IO_V18D

M5 DDR_IOC_V12D
N4 DDR_IOC_V12D
L5 DDR_IO_VREF

MT7620A

SOC_1.2VD

C72
0.1uF

GND

MA6/MCAS_N
MA5/MCS_N
MA4/MRAS_N
MWE_N/MCKE
MCAS_N/MWE_N

T4 MDQS0_1-CPU-RT0 1 R93 2 47 ohm DDR_MDQS0
N1 MDQS1_1-CPU-RT0 1 R94 2 47 ohm DDR_MDQS1

U4 MDQM0_1-CPU-RT0 1 R95 2 47 ohm DDR_MDQM0
N2 MDQM1_1-CPU-RT0 1 R96 2 47 ohm DDR_MDQM1

U6 MBA0_1-CPU-RT0 1 R97 2 47 ohm DDR_BA0
T6 MBA1_1-CPU-RT0 1 R98 2 47 ohm DDR_BA1
R7 MBA2_1-CPU-RT0 1 R99 2 47 ohm DDR_BA2

P2 DDR_CLK_N_1-CPU-RT0 1 R100 2 22 ohm CLK_N
P1 DDR_CLK_P_1-CPU-RT0 1 R99 2 22 ohm CLK_P

M3 MCAS_N_1-CPU-RT0 1 R104 2 47 ohm DDR_CASN
K3 MCS_N_1-CPU-RT0 1 R105 2 47 ohm DDR_CSN
L3 MRAS_N_1-CPU-RT0 1 R103 2 47 ohm DDR_RASN
U7 MCKE_1-CPU-RT0 1 R101 2 47 ohm DDR_MCKE
T7 MWE_N_1-CPU-RT0 1 R106 2 47 ohm DDR_WEN

J3 MODT_1-CPU-RT0 1 R102 2 47 ohm DDR_MODT

MADDR0
MADDR1
MADDR2
MADDR3
MADDR4
MADDR5
MADDR6
MADDR7
MADDR8
MADDR9
MADDR10
MADDR11
MADDR12
MADDR13

DDR_MDQS0
DDR_MDQS1
DDR_MDQM0
DDR_MDQM1

DDR_BA0
DDR_BA1
DDR_BA2

DDR_CASN
DDR_CSN
DDR_RASN
DDR_WEN
DDR_CSN

DDR_MODT

DDR_CASN
DDR_CSN
DDR_RASN
DDR_MCKE
DDR_WEN

DDR_MODT

DDR_CASN
DDR_CSN
DDR_RASN
DDR_MCKE
DDR_WEN

DDR_MODT

DDR_CASN
DDR_CSN
DDR_RASN
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DDR_RASN
DDR_MCKE
DDR_WEN

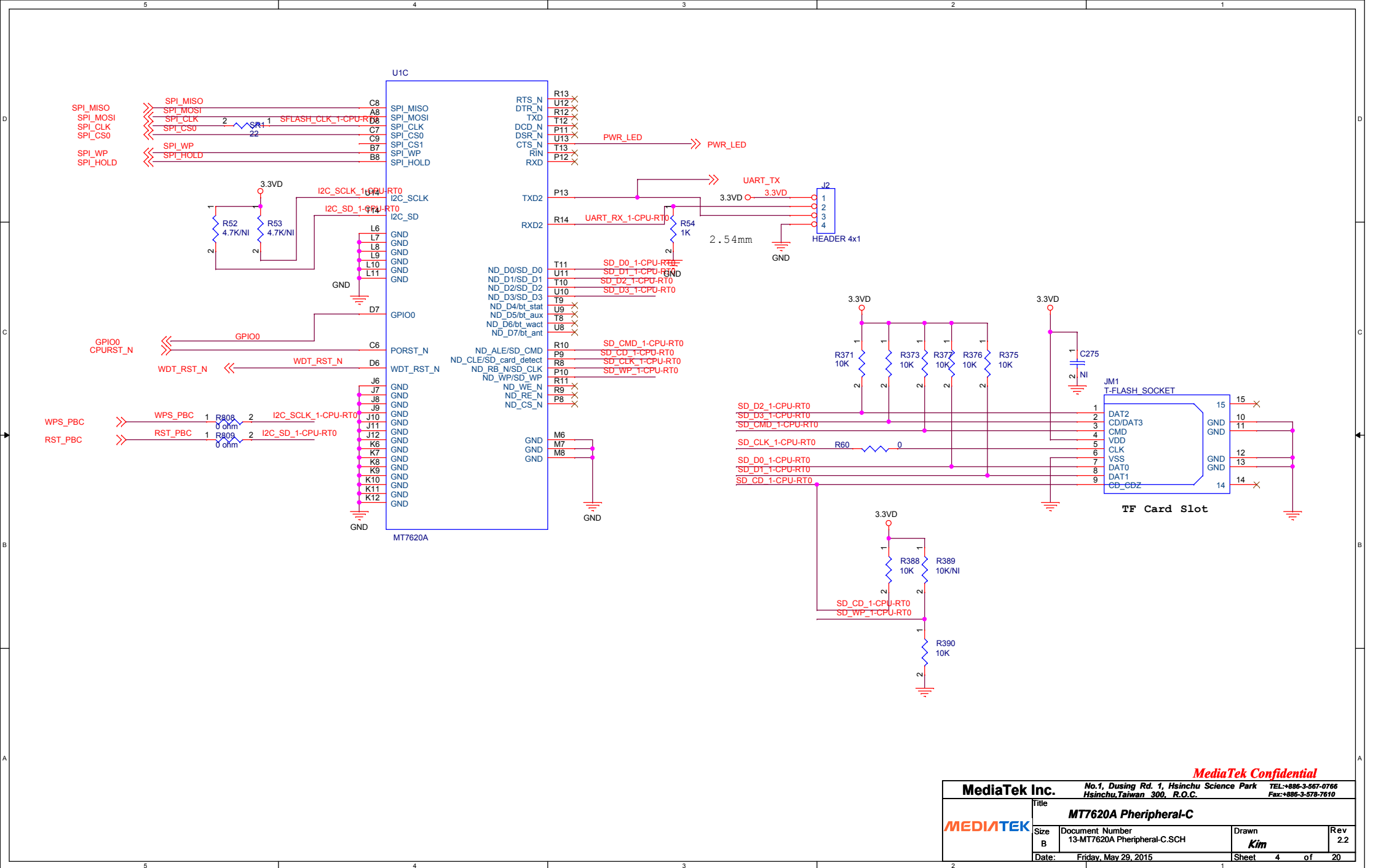
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DDR_CASN
DDR_CSN
DDR_RASN
DDR_MCKE
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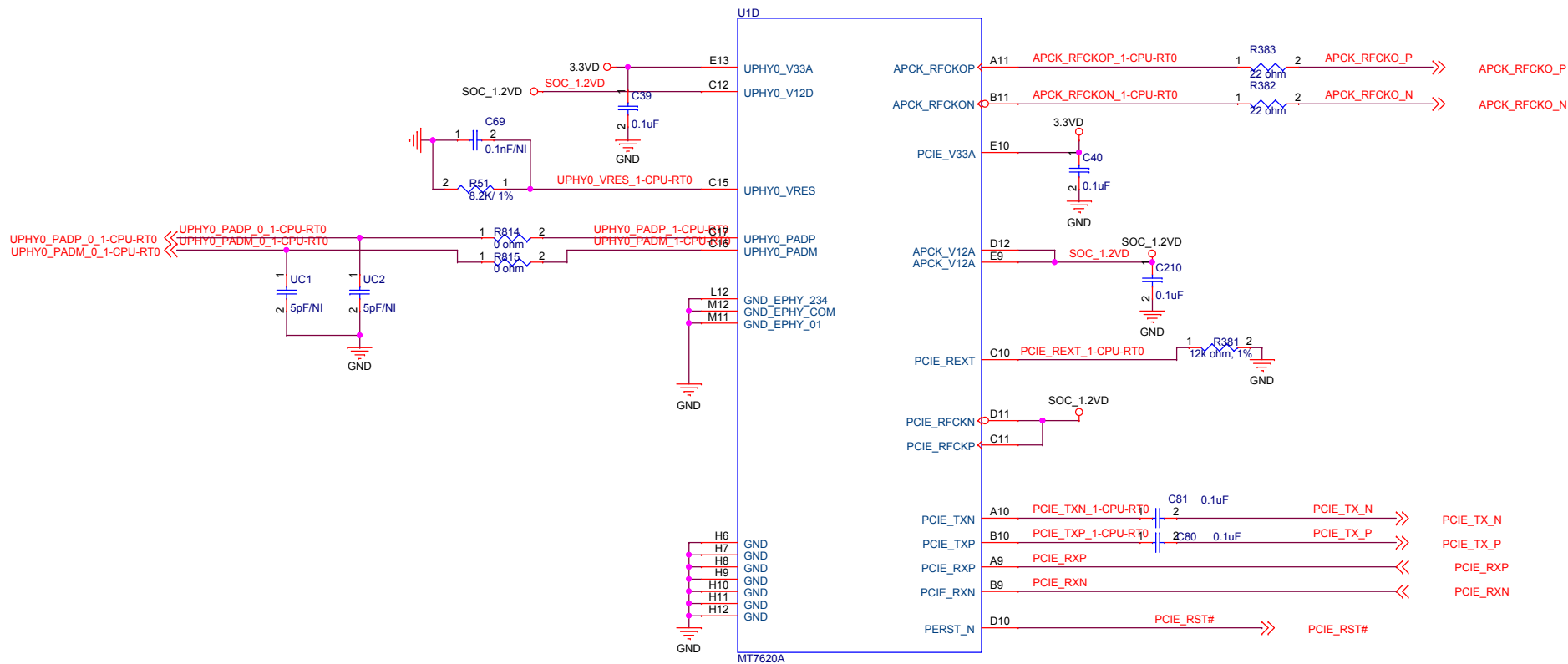
DDR_MODT

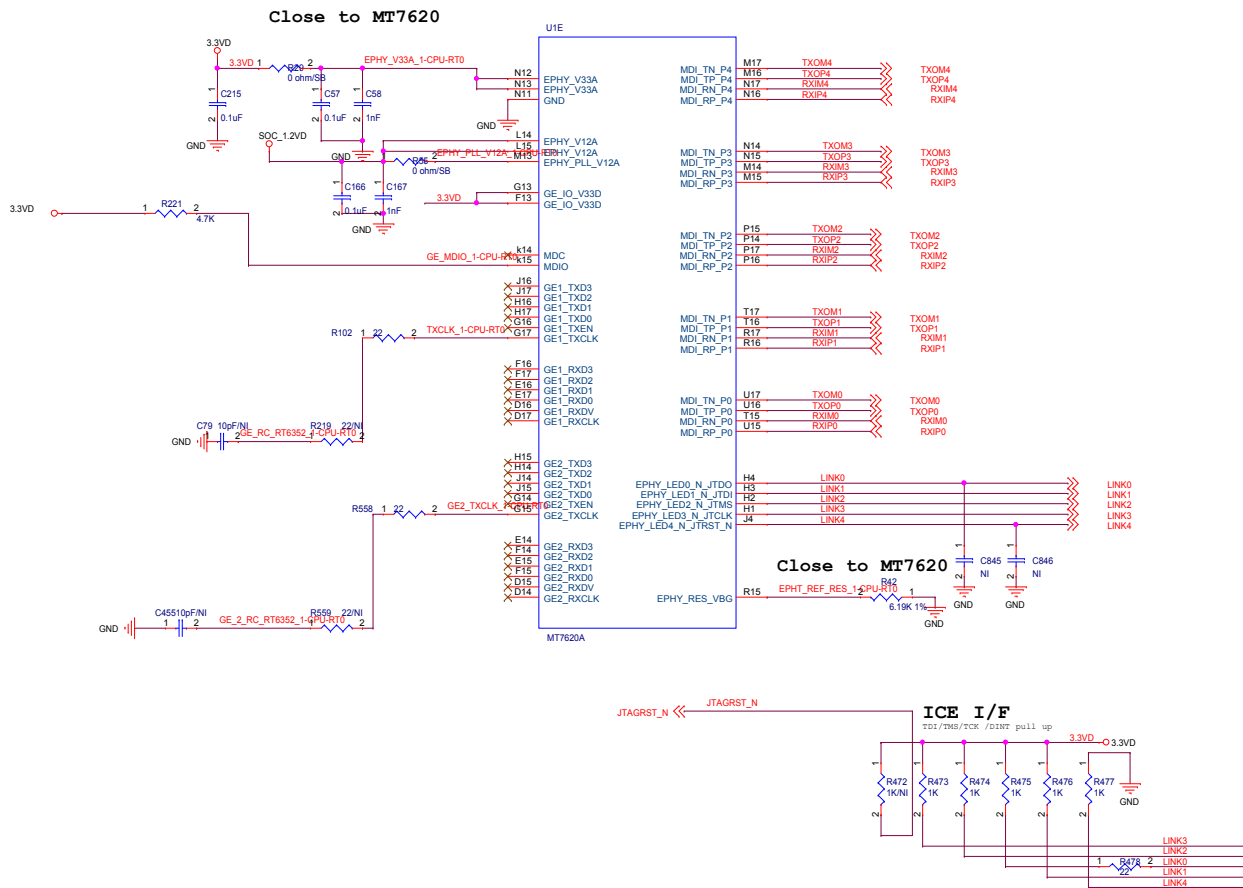
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DDR_RASN
DDR_MCKE
DDR_WEN

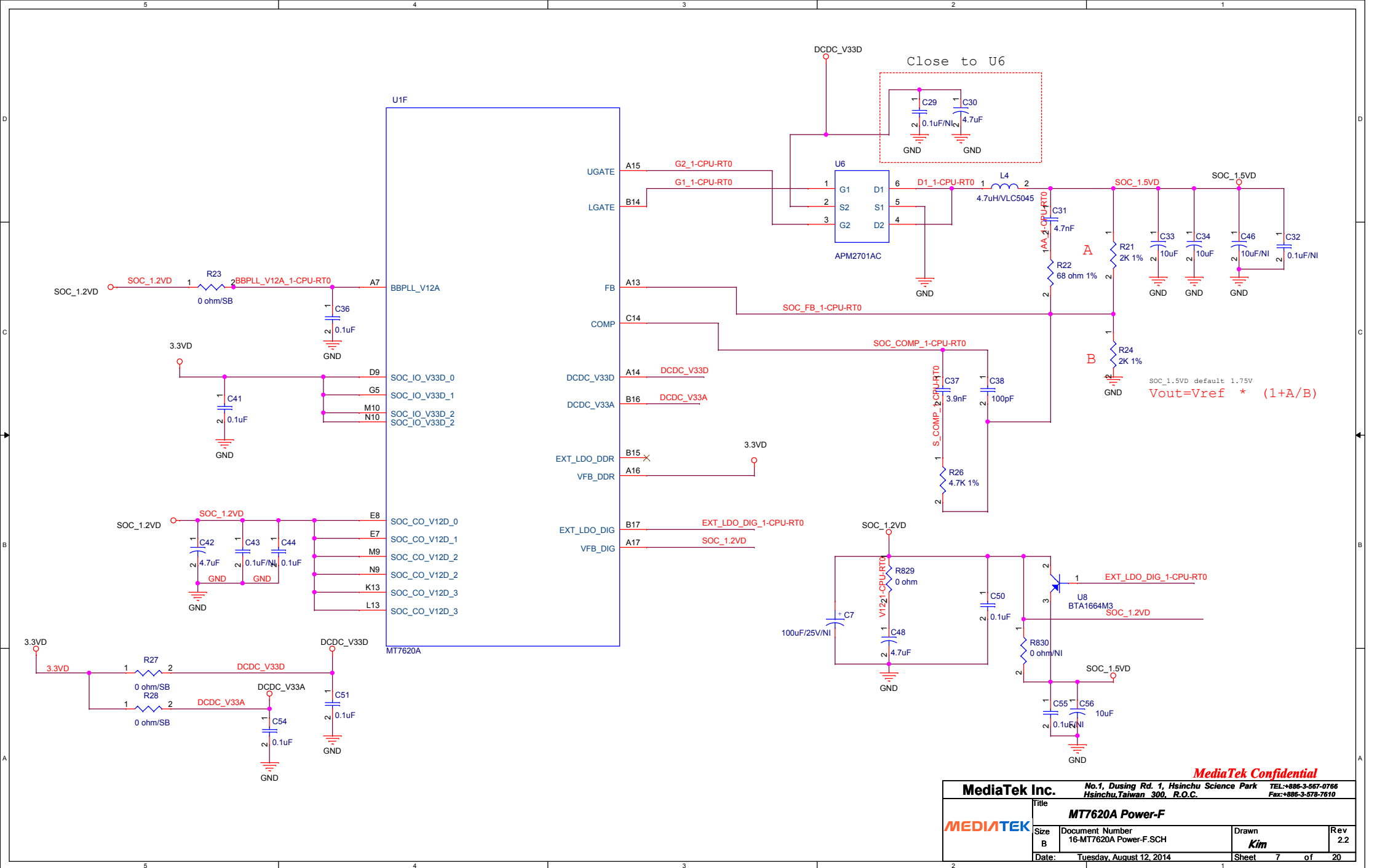
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MediaTek Inc.		No.1, Dusing Rd., Hsinchu Science Park Hsinchu, Taiwan 300, R.O.C.	
		TEL: +886-3-567-0766 Fax: +886-3-578-7610	
MEDIATEK	Title	MT7620A DDR I/F-C	
	Size	Document Number	Drawn
	B	13-MT7620A DDR2 I/F-C.SCH	Kim
	Date:	Tuesday, August 12, 2014	Sheet 3 of 20

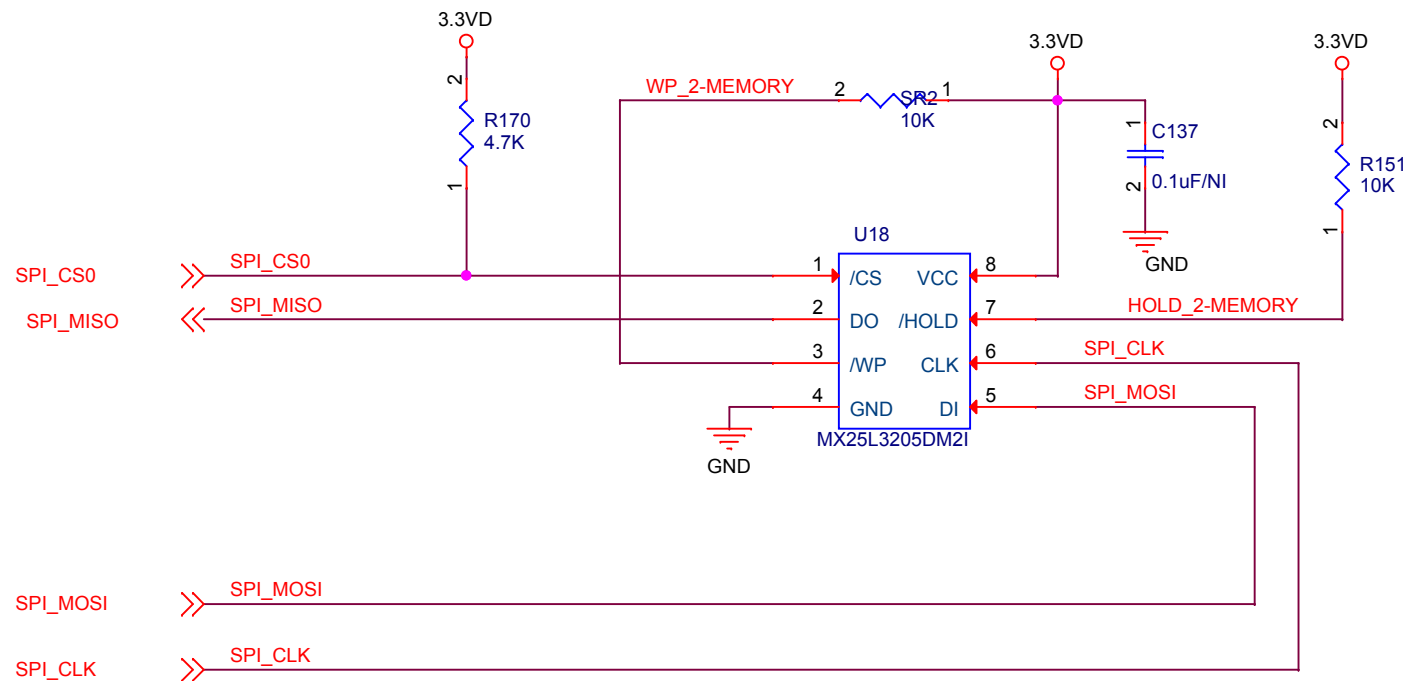


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MEDIA TEK	Title		MT7620A Peripheral-C		
	Size	Document Number	Drawn	Rev	
	B	13-MT7620A Peripheral-C.SCH	Kim	2.2	
	Date:	Friday, May 29, 2015	Sheet	4	of 20









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	Title SPI Flash				
	Size A	Document Number 21-SPI Flash.SCH		Drawn Kim	Rev 2.2
	Date: Tuesday, August 12, 2014		Sheet 10 of 20		

[3] MDATA[0:15]

MDATA[0:15]

[3] MADDR[0:13]

MADDR[0:13]

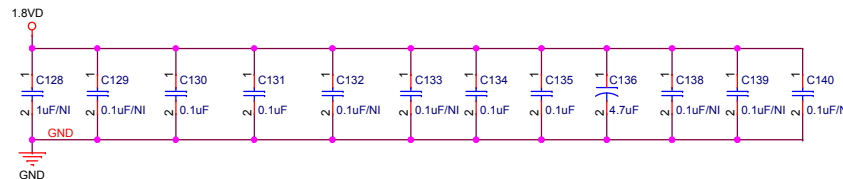
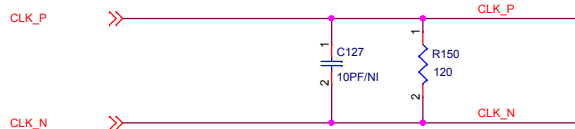
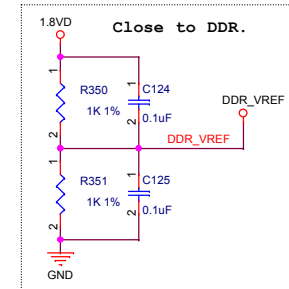
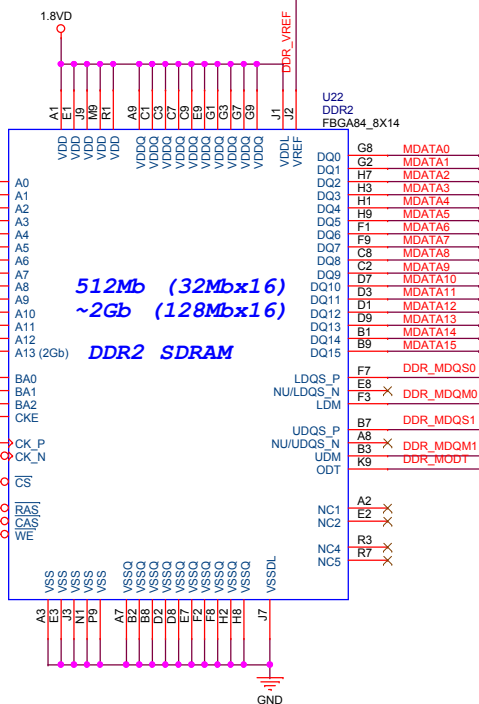
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DDR_BA1
DDR_BA2
DDR_MCKE

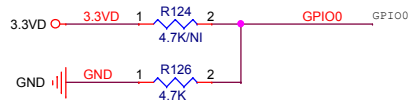
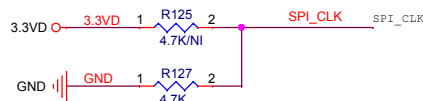
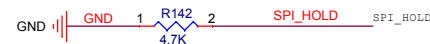
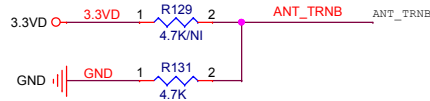
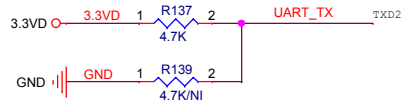
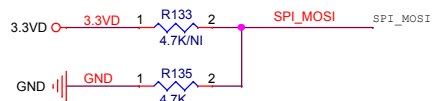
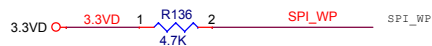
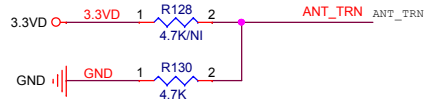
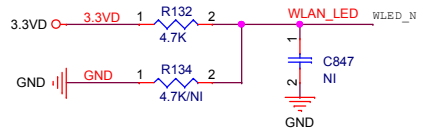
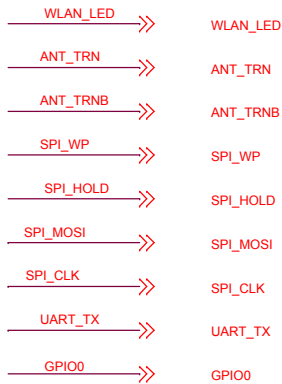
DDR_CSN
DDR_RASN
DDR_CASN
DDR_WEN

DDR_BA0
DDR_BA1
DDR_BA2
DDR_MCKE

CLK_P
CLK_N
DDR_CSN

DDR_RASN
DDR_CASN
DDR_WEN



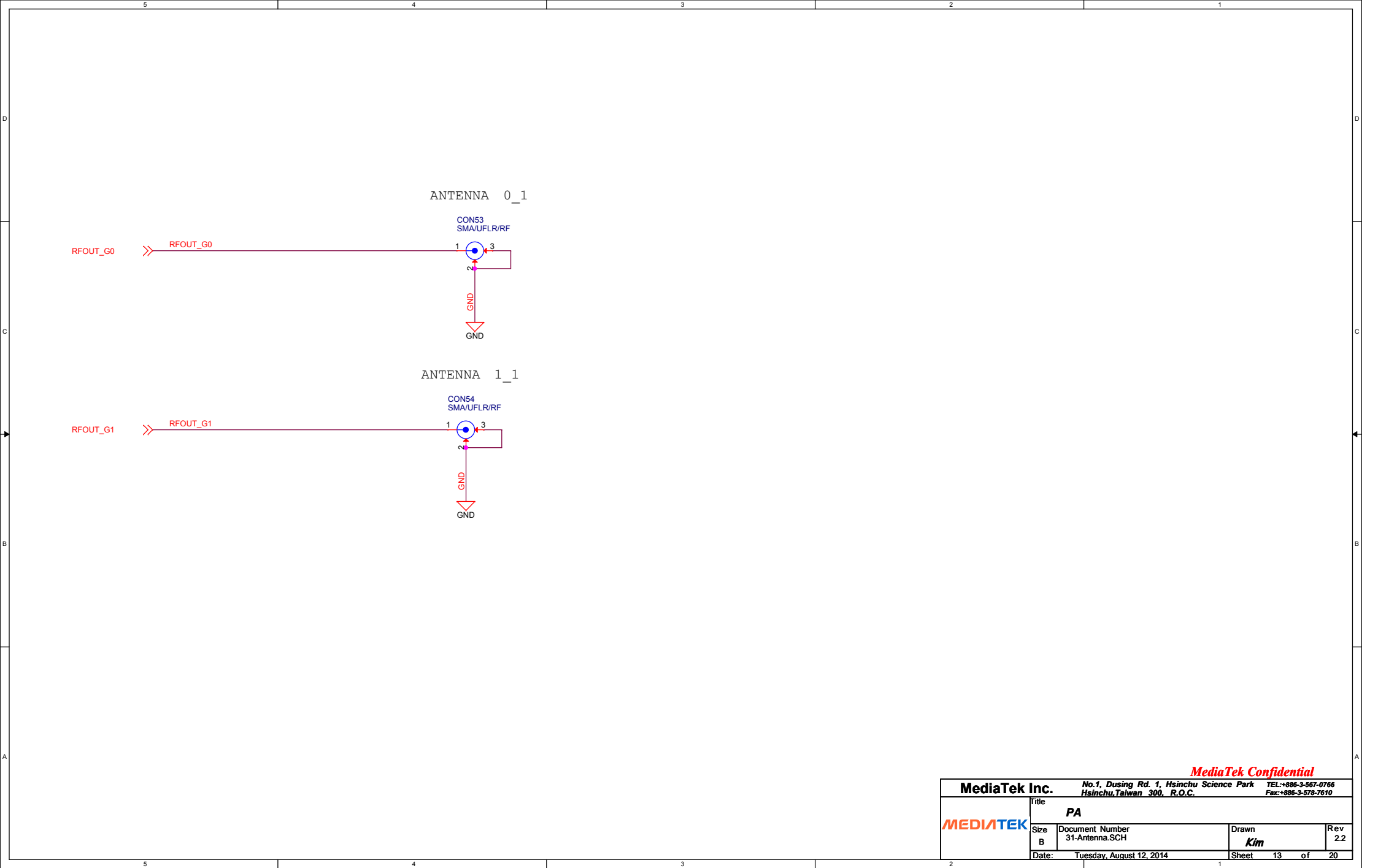


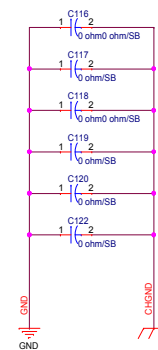
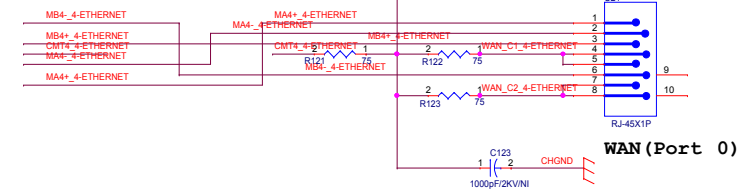
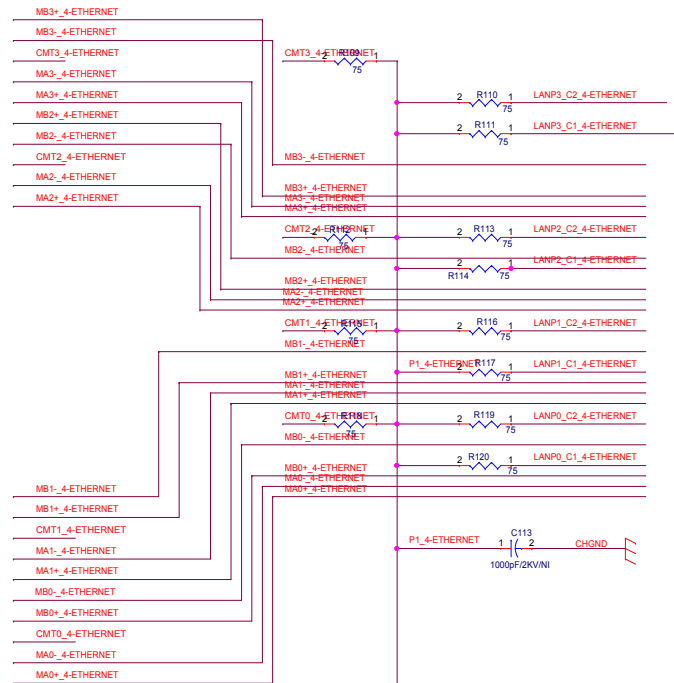
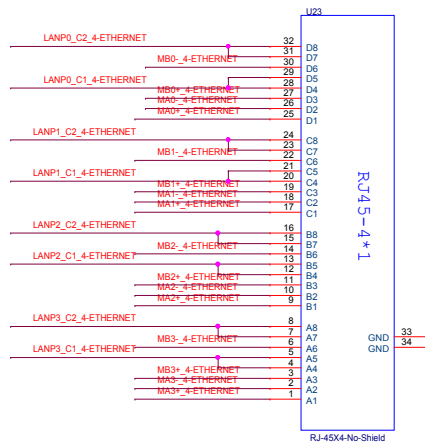
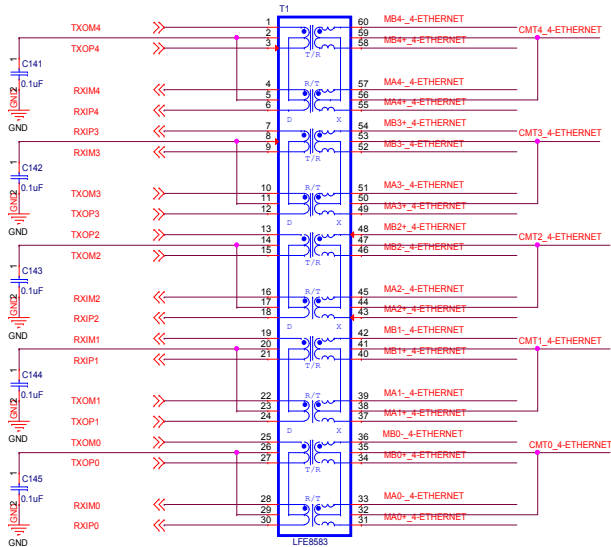
MT7620 Boot Up Strapping

Pin Name	Description	Value
WLED_N	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP 10: DDR2 (CPU/3) FBGA 11: SDRAM (CPU/5) (LVTTL 3.3 V) TSOP Package
{SPI_MOSI SPI_CLK, TXD2, GPIO0 }	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0001: Normal mode (boot from ROM+NAND flash 4 cycle address) 0010: Normal mode (boot from SPI 3Byte Addr) 0011: Normal mode (boot from SPI 4Byte Addr) 0100 :iNIC RGMII mode(boot from ROM) 0101: iNIC MII mode(boot from ROM) 0110: iNIC RVMII mode(boot from ROM) 0111: iNIC PHY mode(boot from ROM) 1000: iNIC USB mode(boot from ROM) 1001: iNIC PCIe mode(boot from ROM)

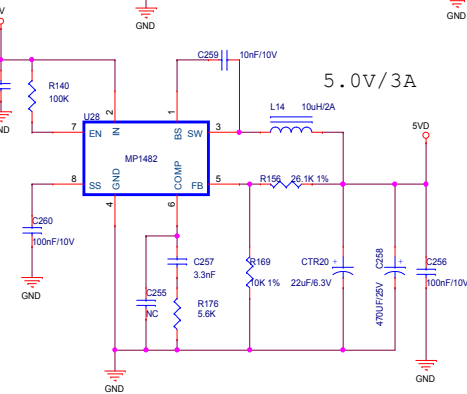
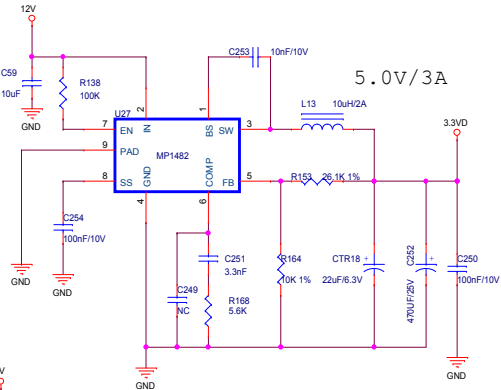
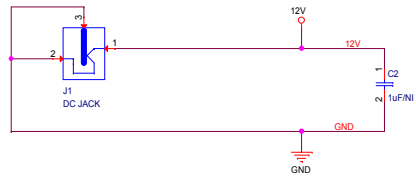
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MEDIATEK	Title	Config		
	Size	Document Number	Drawn	Rev
	B	23-Config.SCH	Kim	2.2
Date: Tuesday, August 12, 2014		Sheet 12 of 20		





12V DC ADAPTER



Reset Circuit

