# 7. THEORY OF OPERATION

Circuit Composistion And Operation Theory

The basic explanation for the circuit composition

FRS-250 SLV consists mainly of the two board controlling the analog circuit parts and the digital circuit parts for the other control. Since the RF fronted, TX poser stage and the PLL circuit are the problem on the circuit can be easily solved by changing the approprate modules.

## Receiver

FRS-250SLV Receiver part is composed in the double conversion system, which has the 1st IF Frequency of 21.4MHz and the 2nd IF frequency of 455KHz. With the fronted module which has an excellant band characteristice and skite characteristice, the 2 pole MCF used in the 1st IF, and the 4 pole ceramic filter in the 2nd IF, the reception interrupting factors such as the image and the sensiticity repression are reduced for the more stable reception.

RF Frontend

The signal received by the antenna will be transmitted to the frontend module through the antenna switching circuit consisted of C44, L7 and C301. The fronted module consists of the RF amplifier transistor Q1 and input/output band pass filter. Each input/output band passfilter has the bandwidth of approximately 20MHz, primarily diminishes the other signal rather then the 1st IF image and other signal within the reception band and amplifies only the nessary signal within the RF.

1st Mixer

The receiver signal which has been amplified in the RF fronted is provided to the base of the 1st mixer Q2. The 1st L/O signal provide from the PLL module is supplied to the emitter of Q2 and converted to the 1st IF 21.4MHz.

1st IF Filter and 1st IF Amplifier

The signal covered by Q2 to 21.4MHz, the 1st frequency, change its impedance through C61, L14 and then is infused to the fundmental MCF which has the center frequency of 21.4MHz and the band width of +/-3.75KHz.
Here, the signal reduces the image and other unwanted signal for the 2nd IF, and changes its impendance again through the R9 . Then the signal is infused to the Q3, the 1st IF amplifier.

The signal infused to the Q3 is amplified approximately by 20dB in othor to acquire the required reception sensitivity, and infused to the IC1 which functions as the 2nd mixer, the 2nd IF amplifier, and the FM detector.
2nd Mixer, 2nd IF, FM Detector

2nd Mixer, and IF, FM Dectector ( IC1 )

The receiver IF signal of 21.4MHz, which has been infused to IC1 is mixed with the 2nd L/O signal of 20.945MHz, and converted to 455KHz, the 2nd IF frequency. The receiver signal converted to the 2nd IF frequency passed through the CF1, the ceramic filter of 455KHz again. After the limiting inside the IC1 and the FM demodulating by the quarature detector inside the IC1, the signal offers the output through the 9th pin of the IC1.
The 2nd L/O signal of 20.945MHz which infused to the IC1 filters and uses directly the crystal of 20.945MHz. The squelch circuit is composed to detect the noises from the received signal demodulate in the 9th pin of the IC1. For this purpose, the noise filter is using the OP amplifier inside the IC1.

De-Emphasis and 300Hz HPF ( IC103 )

The audio signal which has been FM demodulate in the IC1 is supplies to the IC103 which function as the De-emphasis and 300Hz HPF.
Since the IC103A has the 300Hz HPF with the 1st characteristics and the De-emphasis characteristice with the cornor frequency of approximately 200Hz, and IC103B, and the IC103C has the 300Hz HPF with the 6th characteristices, they function as a normal De-emphasis and also reduce the signal such as CTCSS to unwanted noises from the speaker.

Audio Power Amplifier ( IC309 )

The received audio signal which has been adjusted to the appropriate volume in the Q105, and Q104 are suppiled to the 2nd pin of the IC309 and amplified approximately by 20dB.
Then, it turns up the speaker with the maximum output of 0.3Watts.
The 7th pin of the IC309 is the audio mute terminal. If a voltage supply to the 6th pin of the IC309 is supplied to this terminal, the IC309 stops functioning as the audio power amplifier regardless of the signal supplied to the 2nd pin of the IC309, and there is no sound from the speaker.

## Transmitter

The transmission part of the FRS-250SLV is designed to amplify the RF signal oscillated and modulated by the synthesizer to approximately 500mW by the power transistor of Q8.

Pre-emphasis and 300Hz HPF, Limiter ( IC104B, IC104A )

The voice signal input from the microphone is pre-emphasized at the IC104B, and at the same time, the components below 300Hz are reduce to minimize the infuence to the CTCSS tone.
The signal which comes out of the IC104B is limited to a certain amplitude at the IC104A for the voice signal not to exdeed the allowable band width assigned for transmission.

3KHz LPF ( IC104C, IC104D )

After passing the IC104A limiter, the signal is combined with the CTCSS tone at the digital circuits, passes the RV102, and is supplied to the 3KHz LPF has the 4th characteristices and adjusts the assigned frequency band width not to exceed the allowable range.

TX Power ( Q8 )

The transmitted signal of approximately 16dBm , combined at the PLL module is supplied to the base of the Q8 amplifier. The transmitted signal amplified to 27dBm here passes the TX LPF of the 2nd characteristiced of the L9 and the L8, and RX/TX switching takes place by the D6. After this, the signal is provided to the antenna.

## Frequency Synthesizer

Voltage Control Oscillator ( VCO )

The VCO of the FRS-250SLV oscillates 462.5625MHz to 467.7125MHz under the transmission condition and 441.1625MHz to 446.3125MHz under the reception condition. The VCO consists of the colpitts oscillator of the Q4, and contains the oscillator frequency of approximately 21.4MHz during the transmission / reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared to transmission, the D3 is directly biased by the Q11.
Therefore as a result, the C19 is added in parallel tothe resonance circuit of the VCO to oscillate a low frequency. During transmission, a relatively high frequency should be oscillate compared to reception. Therefore, the D3 is adversely biased by the Q11, and as a result, the C19 which is added inparallel to the resonance circuit of the VCO is removed to oscillate the desired transmission frequency.
The VCO is controlled by the IC2 PLL IC in order to oscillate accurate frequency. The output frequency of the VCO is supplied to the IC2 PLL IC immediately. At the IC2,

TCXO(12.8MHz) by the M1 is compared to the output frequency of the VCO. The VCO is controlled through the loop filter consisted of the R28, R29 and the C41, C33, C68 in order to oscillate the stable frequency wanted for the radio.
The VCO controlled voltage which ahs passed the loop filter is supplies to the D4 varactor diode, and the VCO an oscillate the PLL programmed frequency by the capacity varation in the D4. In addition, the L4 on the VCO circuit functions as frequency for the VCO to be properly controlled by the IC2 PLL IC.

RX/TX Buffer Amplifier ( Q7 )

The RF signal oscillate at the VCO is provide to the Q2 RX 1st mixer through the Q7 during the reception, and is provide to the Q9 power driver amplifier through the Q7 during the transmission.

PLL Frequency Synthesizer ( IC2 )

The PLL synthesier of the signal loop PLL circuit with the reference of 6.25KHz. The IC2 PLL IC includes all the functions such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.
At the reference oscillator, the 12.8MHz TCXO of the M1 is connected to the pin 11 of the IC2 to oscillate the frequency of 12.8MHz. The TCXO(12.8MHz) is the temperature compensation circuit to maintain the frequency withen the allowable error range even under a low temperature of -30℃.
The phase decetor send out the output power to the loop filter through 3rd pin of the IC2. If the oscillation frequency of the VCO is low compareed to the referencd frequency, the phase decetor sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase decetor sends out the output power in negative pules. Therefore, the VCO can maintain the frequency set.

The programmable diceder divider maintains the desired frequency with the control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below :

N = VCO oscillation frequency / reference frequency

If the desired frequency is 462.5625MHz

a) TX
N = 462.5625 MHz / 0.00625 MHz = 74010

b) RX
N = 441.1625 MHz / 0.00625 MHz = 70586

## CTCSS Processing

### RX CTCSS Tone Processing

The received CTCSS tone is sent out through 9th pin of the IC1, and supplies to the IC107 switching capacitor filter through the IC102 analog switch. The voice signal which can effected the reception of the CTCSS tone is decreased enough at the IC107.
The cut off frequency at the IC107 is adjusted by the IC106 CPU to suit the characteristice of the CTCSS tone.
The CTCSS tone received at the IC107 is supplies to the 35th pin of the IC106 CPU, and receives the desired CTCSS tone.

### TX CTCSS Tone Processing

The TX CTCSS tone composed at the IC106 CPU is , and the R179, R180, R181, and supplies to the IC107 switchied capacitor filter reduce enough the components in the high frequency which can effect the voice communication. And then, the TX CTCSS tone is combined with the TX voice signal through the IC102 analog switch, and supplies to the RV102 TX CTCSS Tone deviation control volume.

## CPU and Momery

Most of the control functions of the FRS-250SLV are controlled by the IC106 CPU.
The IC106 CPU has the internal ROM in the capacity of 48K byte, and the program for the operation of the IC106.
When the power of the FRS-250SLV turned on, the IC106 reads the data necessety for the operation from the IC108 EEPROM, and decide the operation channel, frequency, etc.
If the user alters any parameter of the radio, the IC106 updates the altered parameter to the IC108.