

Function Theorem

WUG2654 is an USB 2.0 interface to Wireless Adapter. The frequency range is from 2400 ~2500 MHz. It combines 802.11 b/g mode—11b mode of CCK modulation technology to producing 11Mbps data rate, and 11g mode of OFDM modulation technology to producing 54 Mbps data.

The transceiver is super heterodyne architecture.

At TX mode: all of digital signals will be modulated on MAC+B.B (U1), delivering I/Q signals to transceiver to up convert its frequency to RF frequency (ISM Band). The RF signals will be sent to Power Amplifier (U4)—to amplify its power—delivering through antenna.

At RX mode :The antenna receive RF signals then send to transceiver that down converted to IF signal to deliver I/Q signals to MAC_B.B to demodulate.

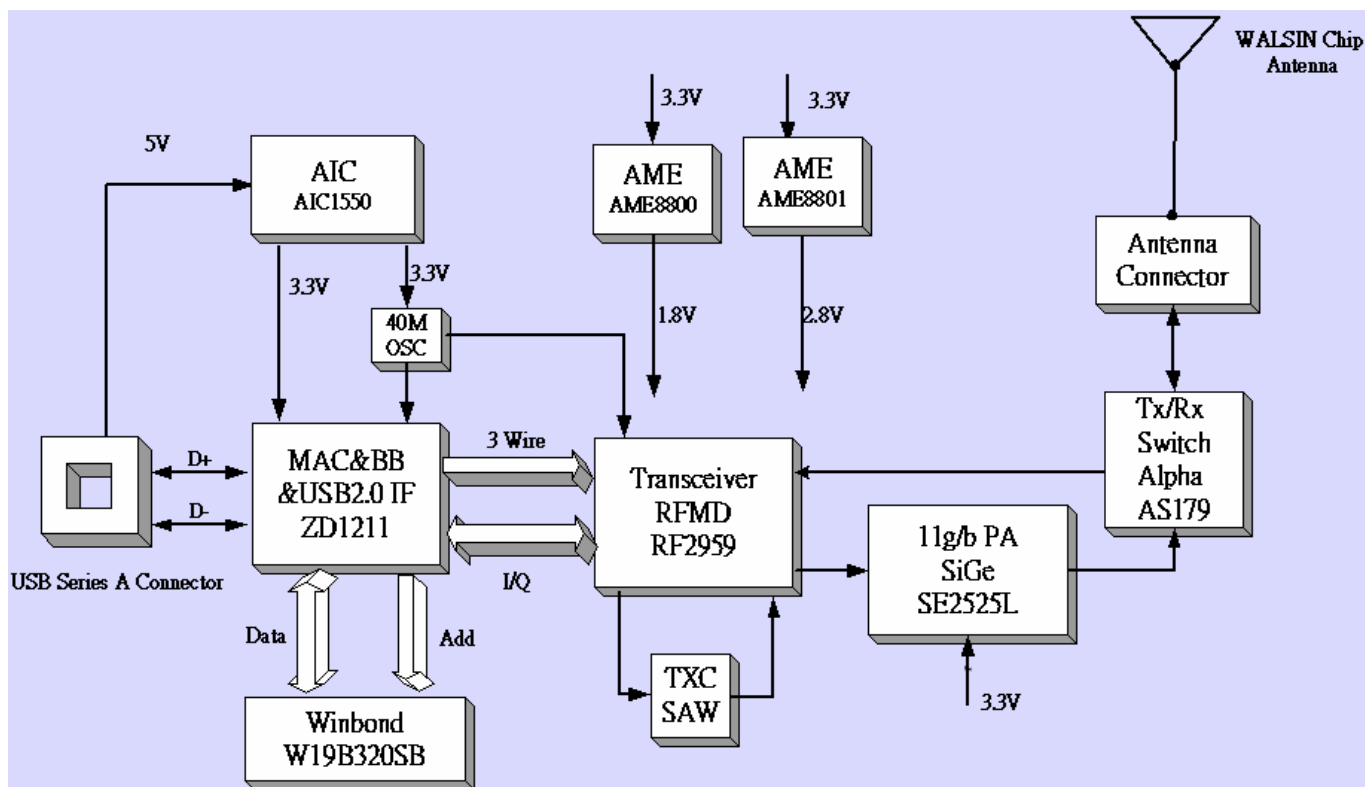


Figure 1 System Diagram

ZD1211: BBP+MAC+USB 2.0 I/F Controller

ZyDAS ZD1211 is a highly integrated, triple mode Wireless LAN (WLAN) MAC and base-band processor that is compatible with IEEE's 802.11g, and 802.11g standards. The ZD1211 includes two different modems; an Orthogonal Frequency Division Multiplexing (OFDM) modem, and a Direct Sequence Spread Spectrum / Complementary Code Keying (DSSS/CCK) modem. The OFDM modem is compatible with the IEEE 802.11g standards that supports multiple data rates of up to 54 Mbps. The DSSS/CCK

The diagram illustrates the internal architecture of the CC1101 SoC, enclosed in a large rectangular box. The components are interconnected as follows:

- External Interfaces (Top):**
 - ICE:** Connected to the Micro Controller via a bidirectional arrow.
 - Serial EEPROM:** Connected to the EEPROM Controller via a bidirectional arrow.
 - UART:** Connected to the UART block via a bidirectional arrow.
 - LEDs, GPIOs:** Connected to the GPIO block via a bidirectional arrow.
- Internal Blocks:**
 - Micro Controller:** The central processing unit, connected to the ICE and other peripherals.
 - EEPROM Controller:** Manages the Serial EEPROM.
 - UART:** Handles serial communication.
 - GPIO:** Controls LEDs and general-purpose input/output pins.
 - USB 2.0:** Provides a USB interface, connected to a 12MHz clock source.
 - FIFO:** A first-in-first-out buffer between the USB 2.0 and MAC Controller.
 - MAC Controller:** Manages the MAC layer, connected to the Baseband Processor.
 - Baseband Processor:** Handles the baseband processing, connected to the RF Interface.
 - RF Interface:** Connects the Baseband Processor to the external RF world.
 - PLL:** Phase-locked loop, connected to the 12MHz clock and the Power management block.
 - Power management:** Manages the power supply, connected to the PLL and Power on Reset.
 - Power on Reset:** Provides a reset signal to the Micro Controller.
- Power and Control Signals (Bottom):**
 - Clock 40MHz:** Provides the main system clock.
 - PDN40M/XPOR:** A power-down or reset signal.
 - Mode selection:** Selects the operating mode of the device.
 - Digital VDD:** Provides the digital supply voltage.
 - Digital Ground:** Provides the digital ground reference.
- RF and Analog Signals (Right):**
 - Analog VDD:** Provides the analog supply voltage.
 - Analog Ground:** Provides the analog ground reference.
 - RF Digital:** A bidirectional signal between the RF Interface and the external RF world.
 - RF Analog:** A bidirectional signal between the RF Interface and the external RF world.

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