

3161A-SL

**Wi-Fi Single-band 1X1 802.11b/g/n
SDIO Module Datasheet**



3161A-SL Module Datasheet

Office: 6 Floor, Building U6, Junxiang U8 Park,
Hangcheng Avenue, Bao'an District,
Shenzhen City, CHINA

Factory: No.8, Litong Road, Liuyang Economic & Technical
Development Zone, Changsha, Hunan, CHINA

TEL: +86-755-2955-8186

Website: www.fn-link.com

Customer Approval :	_____	Company
	_____	Title
	_____	Signature
	_____	Date
	_____	Fn-Link

Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2020/04/22	New version	Lxy	Szs
1.1	2020/05/30	Add 1line sdio application	Lxy	Szs

CONTENTS

1 Overview.....	1
1.1 Introduction.....	1
1.2 Features.....	1
1.3 General Specification.....	2
1.4 Recommended Operating Rating.....	2
2 Wi-Fi RF Specification.....	3
2.1 2.4GHz RF Specification.....	3
3 Pin Assignments.....	3
3.1 Pin Outline.....	4
3.2 Pin Definition.....	5
4 Dimensions.....	7
4.1 Module Picture.....	7
4.2 Marking Description.....	7
4.3 Module Physical Dimensions.....	8
4.4 Layout Recommendation.....	8
5 Host Interface Timing Diagram.....	10
5.1 SDIO Pin Description.....	10
5.2 SDIO CLK Timing Diagram.....	10
6 Reference Design.....	19
6.1 Low Power Dissipation Reference Design.....	19
6.2 Normal Power dissipation Reference Design.....	20
7 Ordering Information.....	21
8 The Key Material List.....	21
9 Power on Sequence.....	22
10 Design Attention.....	22
11 Recommended Reflow Profile.....	22
12 Packing Information.....	23
12.1 Reel.....	23
12.2 Carrier Tape Detail.....	24
12.3 Packaging Detail.....	24
12.4 Moisture sensitivity.....	25

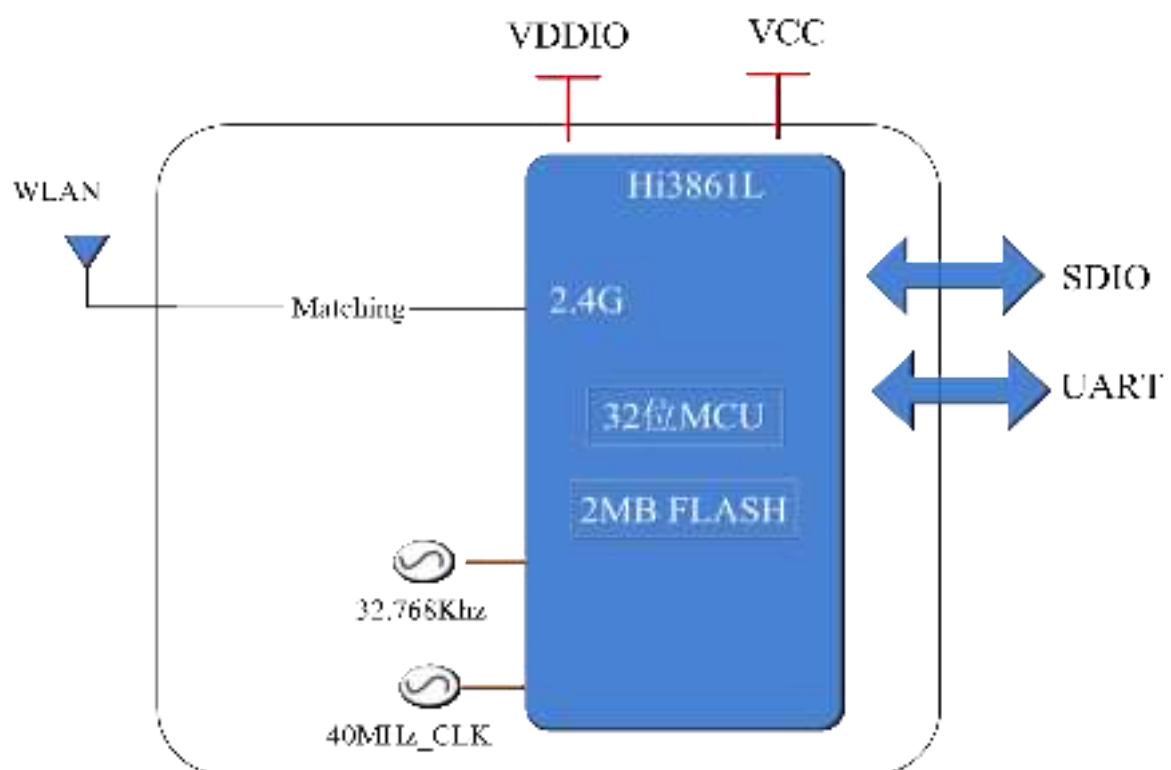
1 Overview

1.1 Introduction

3161A-SL is a highly integrated 2.4 GHz Wi-Fi module that support the IEEE 802.11b/g/n baseband and RF circuit. It supports 20 MHz standard bandwidth and 5 MHz/10 MHz narrow bandwidth, and provides a physical layer rate up to 72.2 Mbit/s. Wi-Fi baseband supports the orthogonal frequency division multiplexing (OFDM) technology and is backward compatible with the direct sequence spread spectrum (DSSS) and complementary code keying (CCK) technologies, offering various data rates defined in the IEEE 802.11 b/g/n protocol.

Module chipset integrates a high-performance 32-bit microprocessor, a hardware security engine, and various peripheral interfaces, including the SPI, UART, I2C, PWM, GPIO, and multi-channel ADC. In addition, it provides high-speed SDIO2.0 slave interfaces, with clock frequency up to 50 MHz. Its built-in SRAM and flash can operate independently and even programming is allowed on the flash.

Block Diagram:



1.2 Features

- Operate at ISM frequency bands (2.4GHz)

- Maximum rate of 72.2 Mbit/s@HT20 MCS7
- SDIO interface for Wi-Fi
- Low power dissipation
- High transmitting power
- High receiving sensitivity
- PHY supporting IEEE 802.11b/g/n
- MAC supporting IEEE802.11 d/e/h/i/k/v/w
- Module integrated 32K clock
- WFA WPA, WFA WPA2 personal, and WPS2.0 for Wi-Fi
- Built-in 352 KB SRAM and 288 KB ROM
- Main chipset Built-in 32bit MCU and 2 MB flash memory

1.3 General Specification

Model Name	3161A-SL
Product Description	Support Wi-Fi functionality
Dimension	L x W x H: 12 x 12 x 2.3 (typical) mm
Wi-Fi Interface	Support SDIO
Ambient temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C
RoHS	All hardware components are fully compliant with EU RoHS directive

1.4 Recommended Operating Rating

		Min.	Typ.	Max.	Unit
Ambient temperature		-40	25	85	deg.C
VCC		2.3	3.3	3.6	V
VDDIO		-	1.8V/3.3V	-	V
Power Consumption		VCC = 3.3V(Unit:mA)			
	Sleep Mode	5uA			
	TX Test mode (2.4G HT20@17dbm)	288			
	RX Test mode (2.4G HT20)	53			

Note: Suggested power input range in 3.3V.

2 Wi-Fi RF Specification

2.1 2.4GHz RF Specification

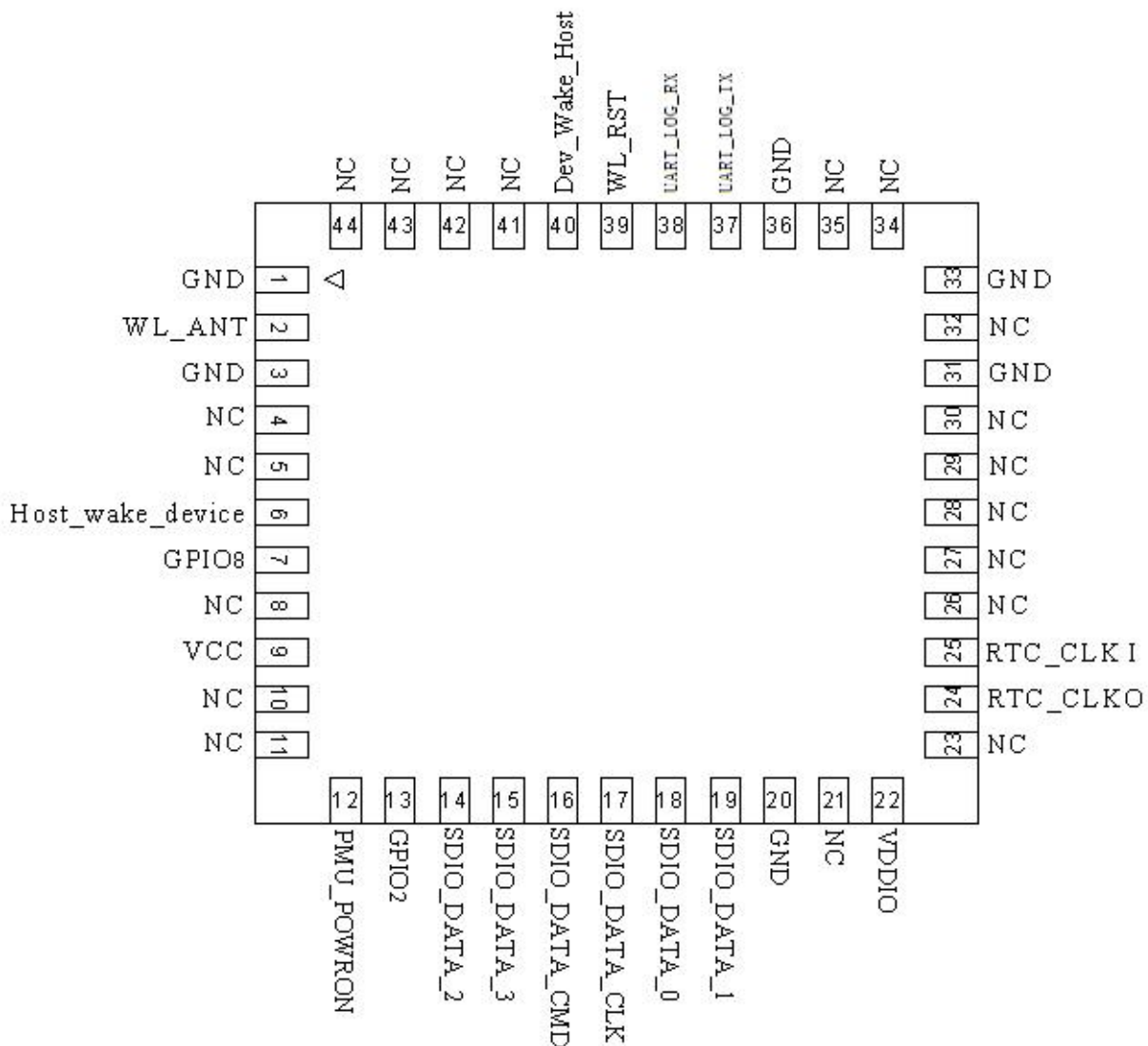
Feature	Description			
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant			
Frequency Range	2.400~2.4835GHz			
Number of Channels	Wi-Fi: US: channel 1~11; EU: channel 1~13; Japan: channel 1~14;			
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm
Test Items	Typical Value		EVM	
Output Power	802.11b /11Mbps : 16dBm ± 1.5 dB		EVM ≤ -10dB	
	802.11g /54Mbps : 16dBm ± 1.5 dB		EVM ≤ -25dB	
	802.11n /MCS7 : 16dBm ± 1.5 dB		EVM ≤ -28dB	
Test Items	Test Value		Standard Value	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -97 dBm	≤-94 dBm	
	- 2Mbps	PER @ -95 dBm	≤-92 dBm	
	- 5.5Mbps	PER @ -92 dBm	≤-89 dBm	
	- 11Mbps	PER @ -90 dBm	≤-87 dBm	
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -94 dBm	≤-89 dBm	
	- 9Mbps	PER @ -92 dBm	≤-88 dBm	
	- 12Mbps	PER @ -91 dBm	≤-87 dBm	
	- 18Mbps	PER @ -88 dBm	≤-86 dBm	
	- 24Mbps	PER @ -85 dBm	≤-84 dBm	
	- 36Mbps	PER @ -82 dBm	≤-80 dBm	
	- 48Mbps	PER @ -79 dBm	≤-77 dBm	
	- 54Mbps	PER @ -77 dBm	≤-75 dBm	
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -93 dBm	≤-89 dBm	
	- MCS=1	PER @ -90 dBm	≤-86 dBm	
	- MCS=2	PER @ -89 dBm	≤-84 dBm	
	- MCS=3	PER @ -85 dBm	≤-82 dBm	
	- MCS=4	PER @ -82 dBm	≤-79 dBm	

	- MCS=5	PER @ -78 dBm	≤-76 dBm
	- MCS=6	PER @ -76 dBm	≤-74 dBm
	- MCS=7	PER @ -73 dBm	≤-72 dBm
Maximum Input Level	802.11b: -10 dBm		
	802.11g/n: -20 dBm		
Antenna Reference	PCB antenna with 0~2 dBi peak gain		

3 Pin Assignments

3.1 Pin Outline

<TOP VIEW>



3.2 Pin Definition

NO	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	WL_ANT	I/O	RF I/O port	
3	GND	—	Ground connections	
4	NC	—	Floating (Don't connected to ground)	
5	NC	—	Floating (Don't connected to ground)	
6	Host wake device	I	Host Wake up Wi-Fi,GPIO06	VDDIO
7	GPIO8	I/O	GPIO or configured as SDIO interrupt pin. (If not used keep Floating)	VDDIO
8	NC	—	Floating (Don't connected to ground)	
9	VCC	P	Main power voltage source input 2.3V-3.6V	3.3V
10	NC	—	Floating (Don't connected to ground)	
11	NC	—	Floating (Don't connected to ground)	
12	PMU_POWRON	I	Enable pin for WLAN device Default ON: pull high ; OFF: pull low	VDDIO
13	GPIO2	I/O	SDIO data interrupt,or GPIO function.	VDDIO
14	SDIO_DATA_2	I/O	SDIO data line 2, GPIO09	VDDIO
15	SDIO_DATA_3	I/O	SDIO data line 3, GPIO10	VDDIO
16	SDIO_DATA_CMD	I/O	SDIO command line, GPIO11	VDDIO
17	SDIO_DATA_CLK	I	SDIO clock line, GPIO12	VDDIO
18	SDIO_DATA_0	I/O	SDIO data line 0, GPIO13	VDDIO
19	SDIO_DATA_1	I/O	SDIO data line 1, GPIO14	VDDIO
20	GND	—	Ground connections	
21	NC	—	Floating (Don't connected to ground)	
22	VDDIO	P	I/O Voltage supply input 1.8V/3.3V	VDDIO
23	NC	—	Floating (Don't connected to ground)	
24	RTC_CLK O	I/O	Floating(module have 32K clock), GPIO00	VDDIO
25	RTC_CLK I	I	Floating(module have 32K clock), GPIO01	VDDIO
26	NC	—	Floating (Don't connected to ground)	
27	NC	—	Floating (Don't connected to ground)	
28	NC	—	Floating (Don't connected to ground)	
29	NC	—	Floating (Don't connected to ground)	
30	NC	—	Floating (Don't connected to ground)	
31	GND	—	Ground connections	
32	NC	—	Floating (Don't connected to ground)	

33	GND	—	Ground connections	
34	NC	-	Floating (Don't connected to ground)	
35	NC	—	Floating (Don't connected to ground)	
36	GND	—	Ground connections	
37	UART_LOG_TX	—	UART0_LOG_TX,GPIO03 For firmware download, can floating this pin	VDDIO
38	UART_LOG_RX	—	UART0_LOG_RX,GPIO04 For firmware download, can floating this pin	VDDIO
39	WL_RST	I	Wi-Fi reset pin. GPIO07 Low: reset enable, Default High: reset disable	VDDIO
40	Dev_Wake_Host	O	Wi-Fi wake up host. GPIO05	VDDIO
41	NC	—	Floating (Don't connected to ground)	
42	NC	—	Floating (Don't connected to ground)	
43	NC	—	Floating (Don't connected to ground)	
44	NC	—	Floating (Don't connected to ground)	

P:POWER I:INPUT O:OUTPUT

3.3 Muti Pin definition

3861L all GPIO pin can configure as muti function,detail see below information.

Pin	NAME	F.0	F.1	F.2	F.3	F.4	F.5	F.6	F.7	F.8
24	GPIO00	GPIO00	UART1_TXD	SPI1_CLK	PWM3	I2C1_SDA	RTC_OSC_32K	RTC32K_XOUT	/	/
25	GPIO01	GPIO01	UART1_RXD	SPI1_RXD	PWM4	I2C1_SCL	/	RTC32K_XINT	/	/
13	GPIO02	GPIO02	UART1_RTS	SPI1_TXD	PWM2	/	SSI_CLK	/	/	/
37	GPIO03	UART0_LOG_TX	UART1_CTS	SPI1_CS1	PWM5	I2C1_SDA	SSI_DATA	GPIO03	/	/
38	GPIO04	UART0_LOG_RX	/	/	PWM1	I2C1_SCL	/	GPIO04	ADC1	/
40	GPIO05	UART1_RXD	GPIO05	I2S0_MCK	PWM2	/	BT_STATUS	SPI0_CS1	ADC2	/
6	GPIO06	UART1_TXD	GPIO06	I2S0_TX	PWM3	/	COEX_SWITH	SPI0_CLK	/	/
39	GPIO07	UART1_CTS	GPIO07	I2S0_CLK	PWM0	/	BT_ACTIVE	SPI0_RXD	ADC3	/
7	GPIO08	UART1_RTS	GPIO08	I2S0_WS	PWM1	/	WLAN_ACTIVE	SPI0_TXD	/	/
14	GPIO09	GPIO09	UART2_RTS	SPI0_TXD	PWM0	I2C0_SCL	I2S0_MCK	SDIO_D2	ADC4	/
15	GPIO10	GPIO10	UART2_CTS	SPI0_CLK	PWM1	I2C0_SDA	I2S0_TX	SDIO_D3	/	/
16	GPIO11	GPIO11	UART2_TXD	SPI0_RXD	PWM2	/	I2S0_RX	SDIO_CMD	ADC5	/
17	GPIO12	GPIO12	UART2_RXD	SPI0_CS1	PWM3	/	I2S0_CLK	SDIO_CLK	ADC0	/
18	GPIO13	GPIO13	UART2_RTS	UART0_LOG_TX	PWM4	I2C0_SDA	I2S0_WS	SDIO_D0	ADC6	SSI_DATA

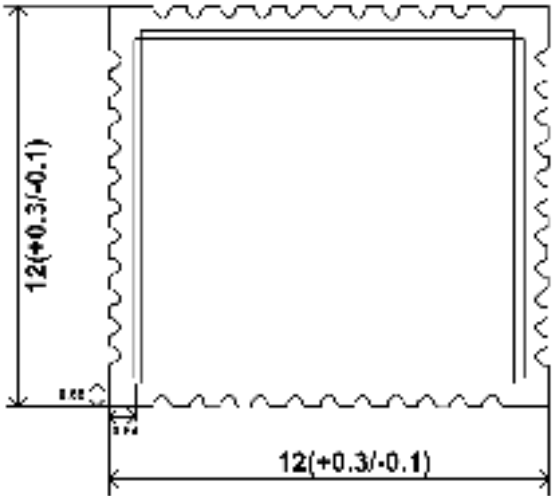
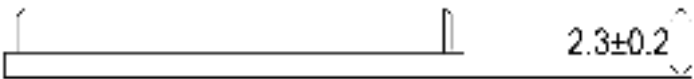
19	GPIO14	GPIO14	UART2_CTS	UART0_LOG_RX	PWM5	I2C0_SCL	/	SDIO_D1	/	SSI_CLK
----	--------	--------	-----------	--------------	------	----------	---	---------	---	---------

Notes:

1. IO 类型: Ispu/O.
2. 驱动电流 1mA.
3. 电压 3.3/1.8V.

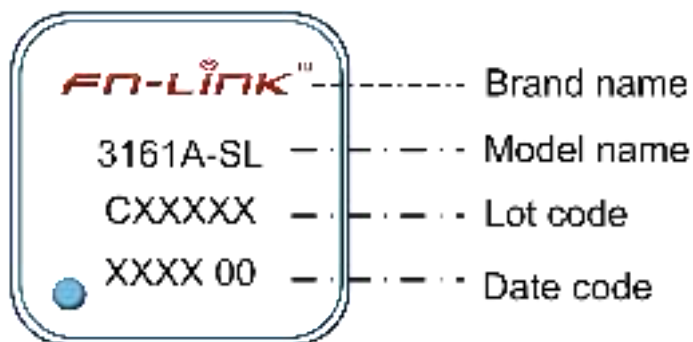
4 Dimensions

4.1 Module Picture

L x W : 12 x 12 (+0.3/-0.1) mm 	
H: 2.3 (±0.2) mm	
Weight	0.66g

4.2 Marking Description

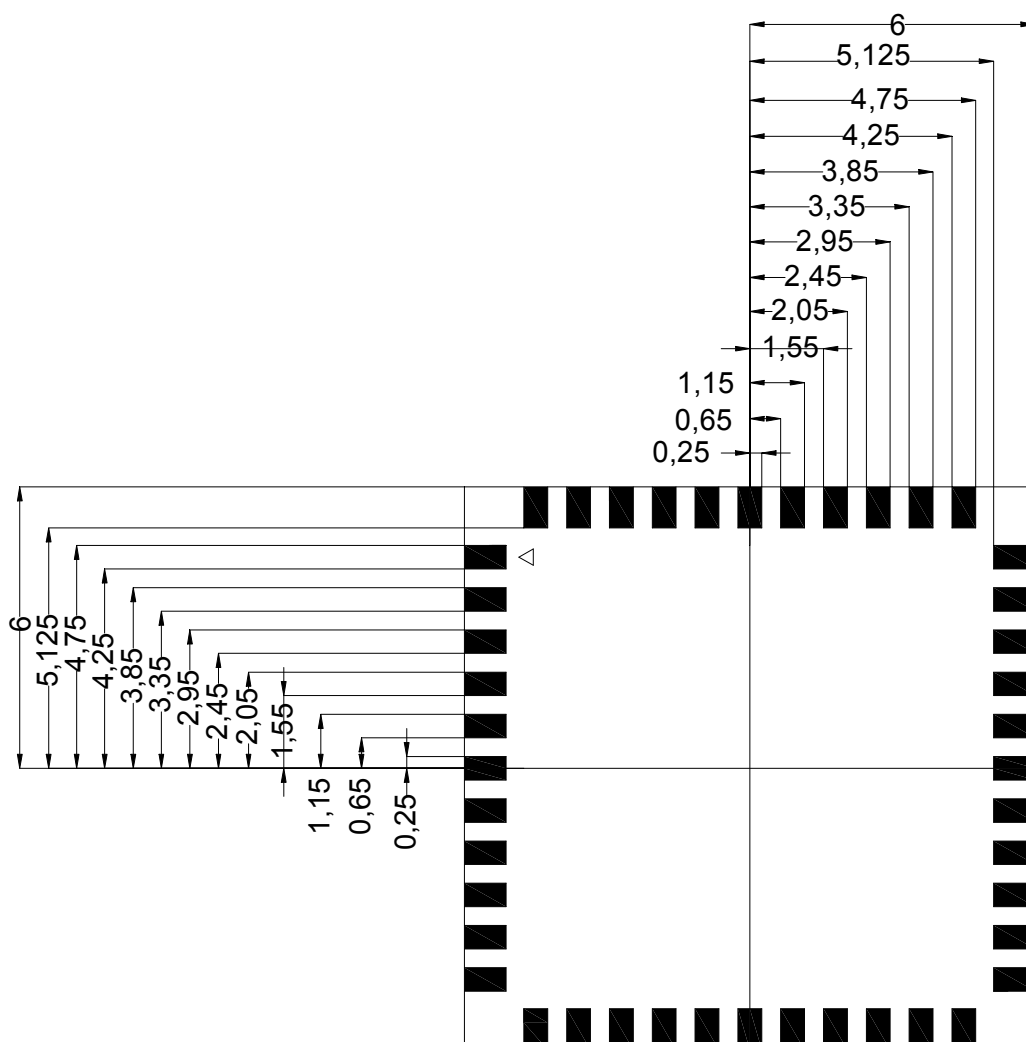
< TOP VIEW >



4.3 Module Physical Dimensions

(Unit: mm)

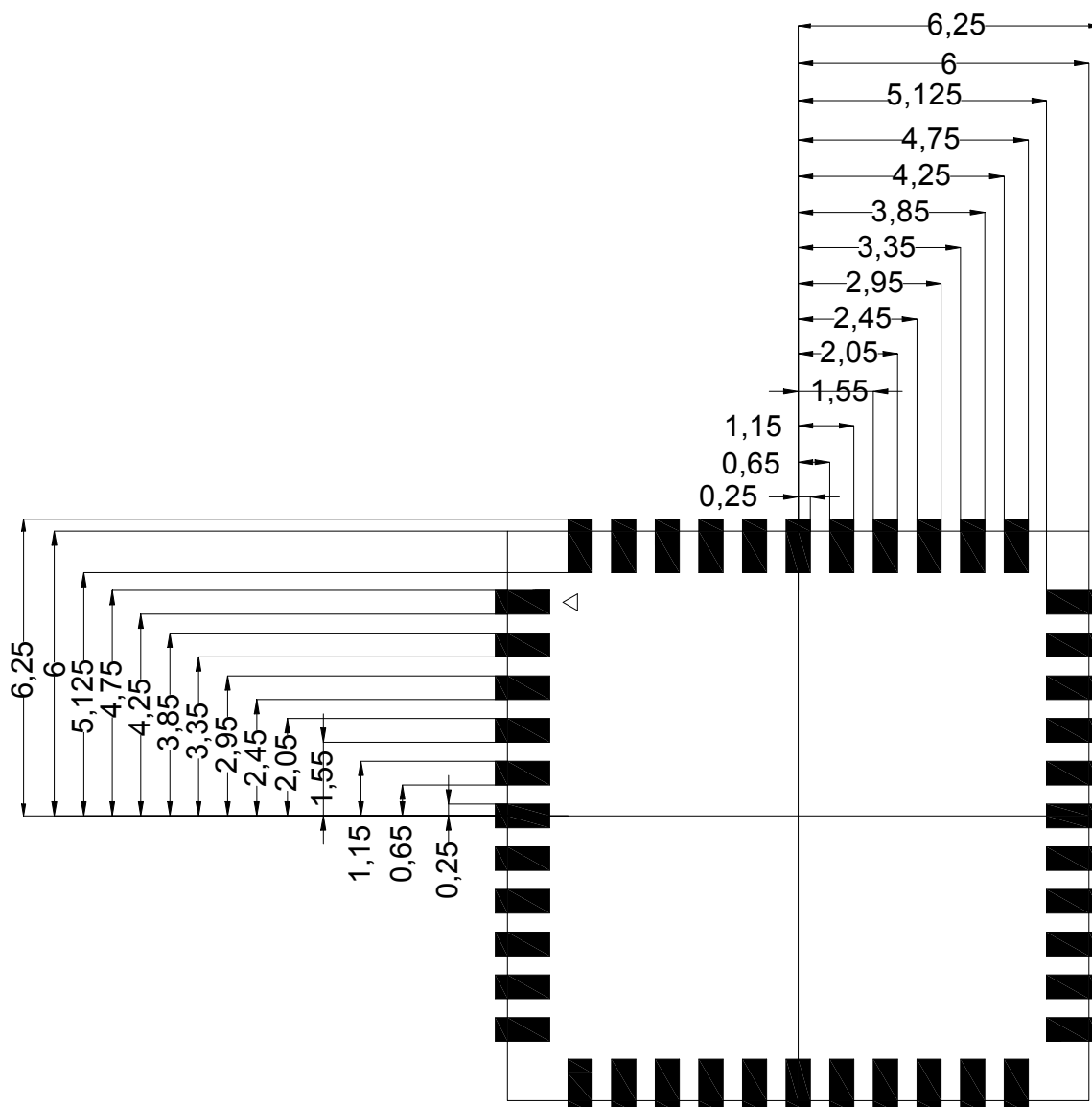
< TOP VIEW >



4.4 Layout Recommendation

(Unit: mm)

< TOP VIEW >



5 Host Interface Timing Diagram

5.1 SDIO Pin Description

The secure digital input/output (SDIO) interface supports three working modes:

Default speed mode (DS)

The maximum frequency of the interface clock is 25 MHz. The interface clock can work in 1-bit or 4-bit mode.

High speed mode (HS)

The maximum frequency of the interface clock is 50 MHz.

SDR25 mode

The maximum frequency of the interface clock is 50 MHz

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1
DATA2	Data Line 2
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

5.2 SDIO CLK Timing Diagram

DS Mode

The DS mode is the default mode after the SDIO is powered on. To ensure compatibility with various host components, the DS mode requires a low working rate and supports only the 25 MHz clock.

Clock parameters in DS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{pp}	-	25	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	17	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	17	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$

Clock parameters in DS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{pp}	-	25	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	14	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	14	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$

Figure 8-6 shows the output data timing in DS mode. t_{ISU} is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. t_{IH} is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode.

Figure 8-6 Input timing in DS mode

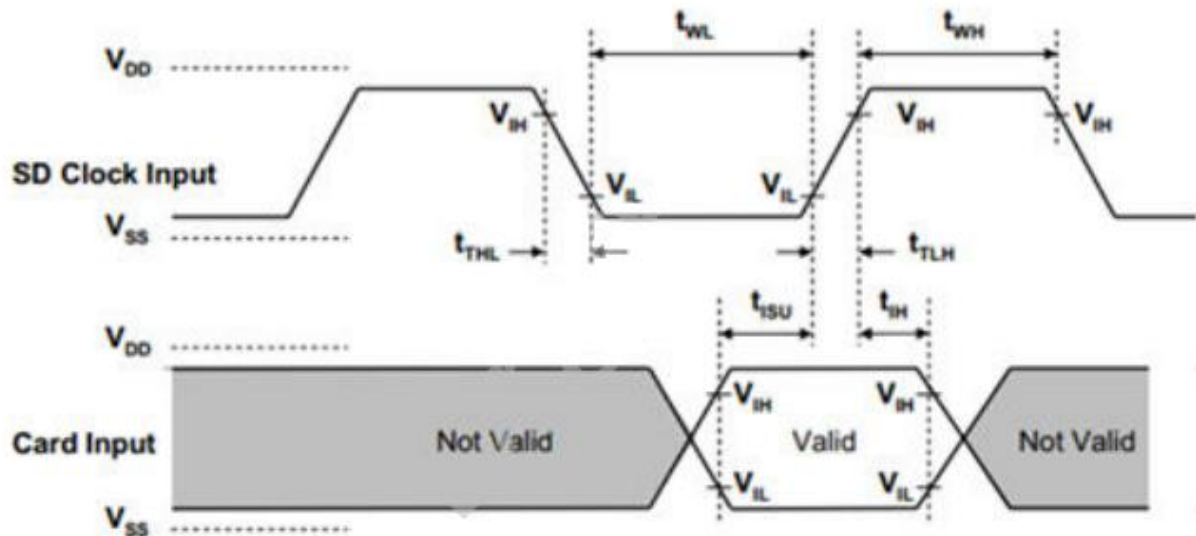


Figure 8-7 shows the input data timing in DS mode. Where, $t_{ODLY(max)}$ is the maximum delay of the output data relative to the clock falling edge, and $t_{ODLY(min)}$ is the minimum delay of the output data relative to the clock falling edge.

Figure 8-7 Output timing in DS mode

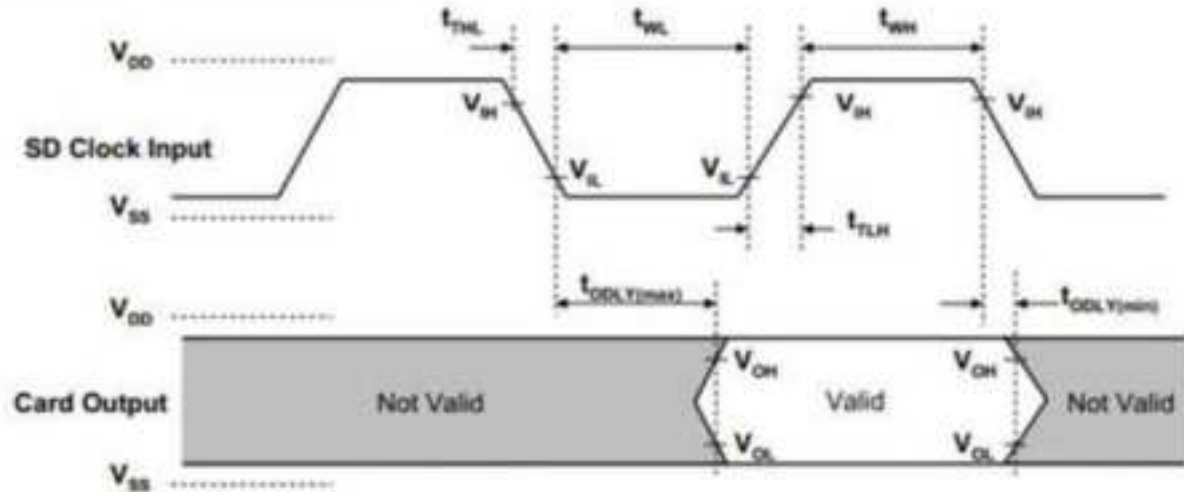


Table 8-12 describes the timing restrictions in DS mode.

Table 8-12 Timing restrictions in DS mode

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	11	ns	$C_L \leq 40 \text{ pF}$
Output Delay time during Identification Mode	t_{ODLY}	-	11	ns	$C_L \leq 40 \text{ pF}$

Note: In DS mode, the output data is referenced to the clock falling edge, and the input data is referenced to the clock rising edge.

HS Mode

The HS mode is entered after the SDIO is powered on and initialized because a higher working rate than the DS mode is required. In HS mode, the clock supports 50 MHz. For details about the restrictions on the clock, see **Table 8-13**.

Table 8-13 Clock parameters in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to $\min(V_{IH})$ and $\max(V_{IL})$)					
Clock frequency Data Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$

Table 8-14 Clock parameters in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{pp}	-	50	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$

Figure 8-8 shows the input data timing in HS mode. t_{ISU} is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. t_{IH} is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode

Figure 8-8 Input timing in HS mode

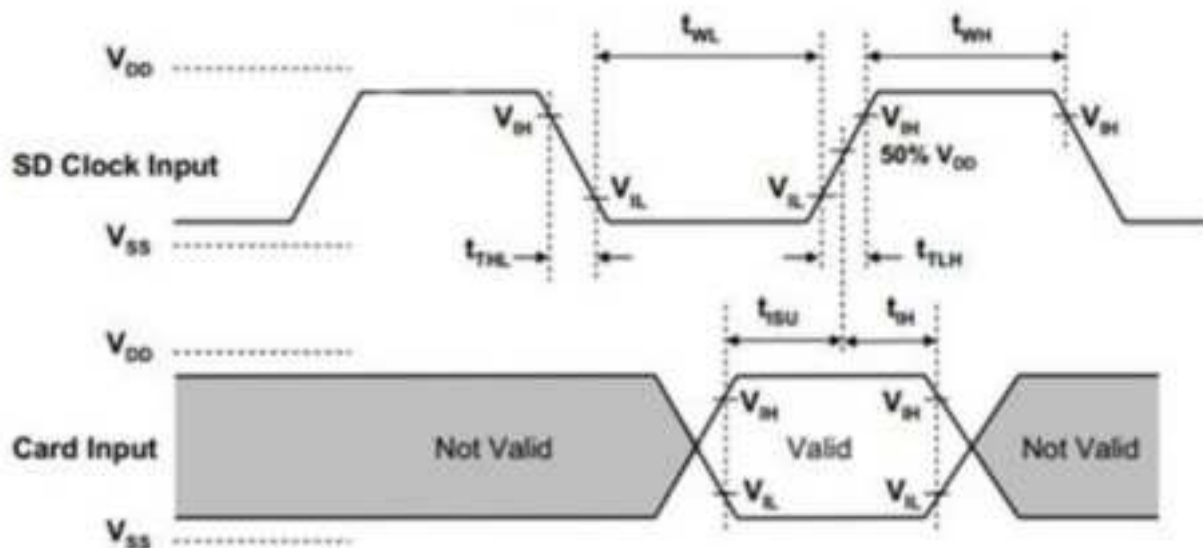


Figure 8-9 shows the input data timing in HS mode. Where, $t_{ODLY(max)}$ is the maximum delay of the output data relative to the clock rising edge, and t_{OH} is the minimum delay of the output data relative to the clock rising edge.

Figure 8-9 Output timing in HS mode

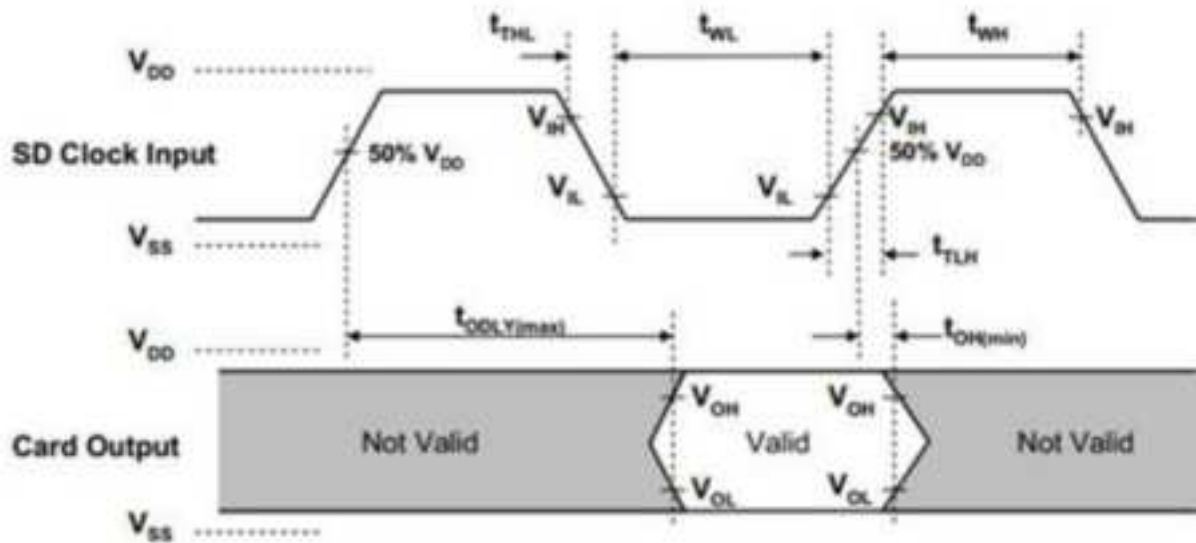


Table 8-15 describes the timing restrictions in HS mode.

Table 8-15 Timing restrictions in HS mode ($V_{DDIO} = 3.3\text{ V}$)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10\text{ pF}$
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10\text{ pF}$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40\text{ pF}$
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40\text{ pF}$
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-16 Timing restrictions in HS mode ($V_{DDIO} = 1.8\text{ V}$)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40 \text{ pF}$
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40 \text{ pF}$
Total System Capacitance for each line	C_L	-	40	pF	1 card

Note: The data signal timing in HS mode is different from that in DS mode. The output data and input data are referenced to the clock rising edge.

SDR25 Mode

The SDR25 mode is entered only after the voltage of the SDIO is switched. In this mode, the maximum interface clock frequency is 50 MHz. **Table 8-17** describes the clock restrictions.

Table 8-17 Clock parameters in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to $\min(V_{IH})$ and $\max(V_{IL})$)					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10 \text{ pF}$

Table 8-18 Clock parameters in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{pp}	-	50	MHz	$C_{CARD} \leq 10 \text{ pF}$
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10 \text{ pF}$

Table 8-19 Timing restrictions in SDR25 mode (VDDIO = 3.3 V)

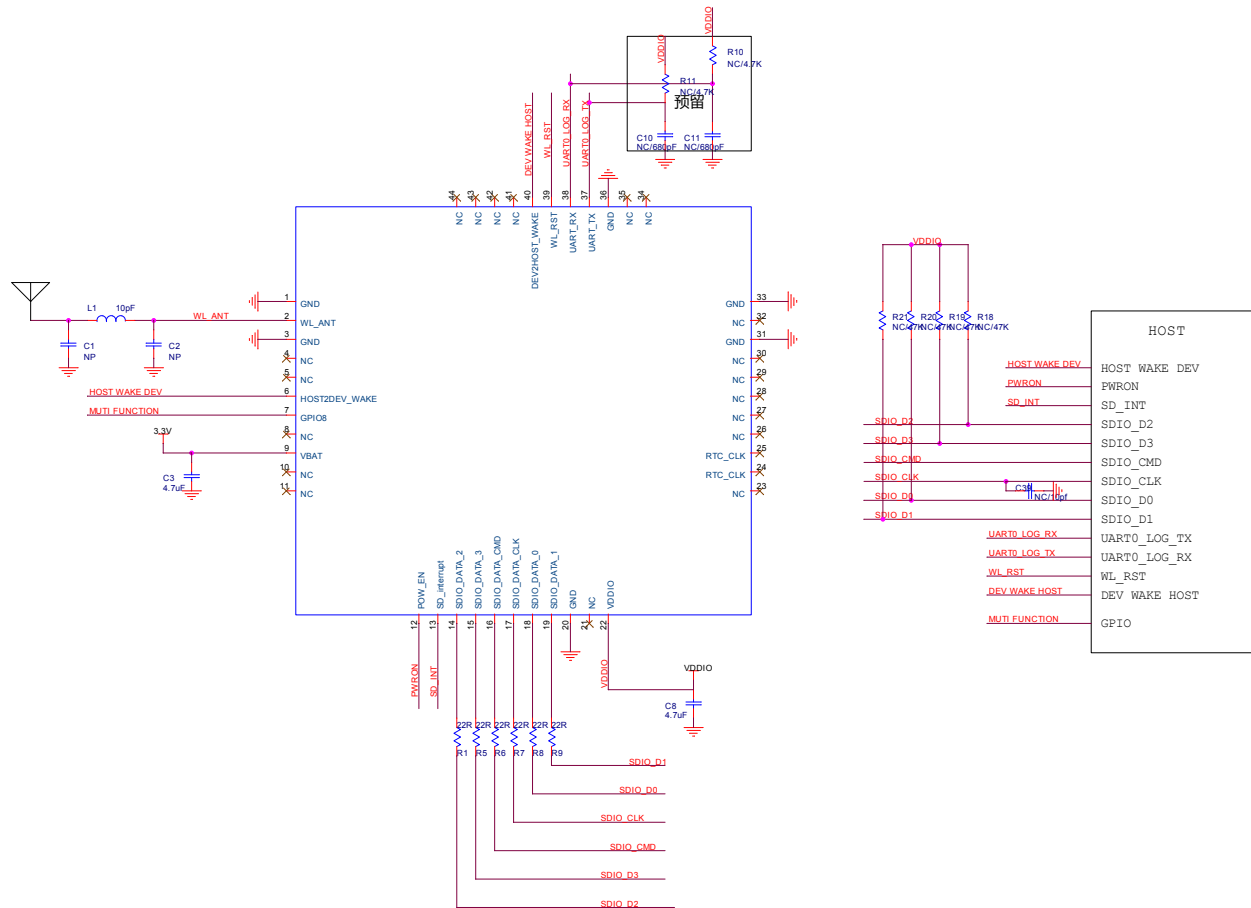
Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40 \text{ pF}$
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40 \text{ pF}$
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-20 Timing restrictions in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symb ol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10 \text{ pF}$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40 \text{ pF}$
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40 \text{ pF}$
Total System Capacitance for each line	C_L	-	40	pF	1 card

6 Reference Design

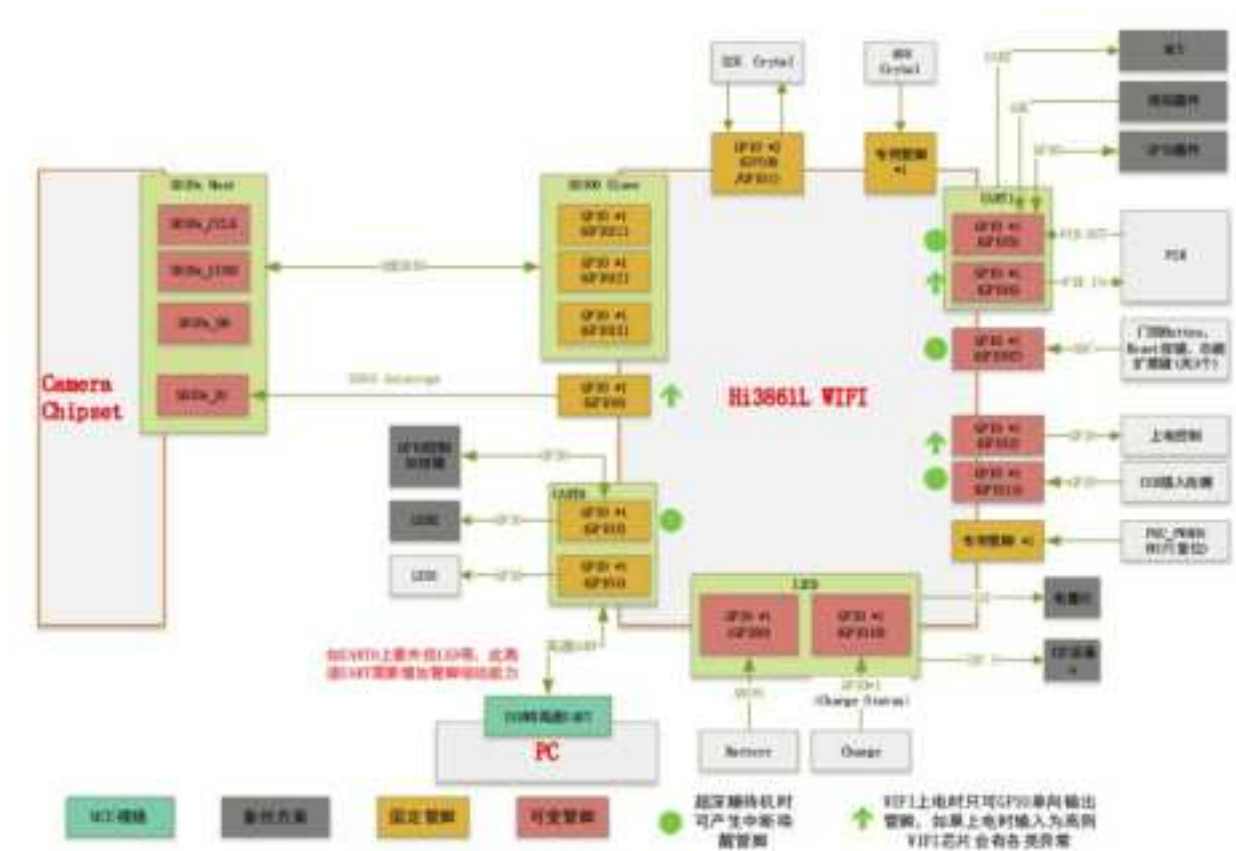
6.1 4line SDIO Reference Design



Notes:

1. 4line WLAN module application, all wake function may not supported;
2. Can using Power EN pin to shut down module for power saving;

6.2 1line SDIO Reference Design



设计注意事项:

1. Hi3861L 与 Hi18EV300 互连的以下管脚请完全拷贝海思设计, 禁止修改。

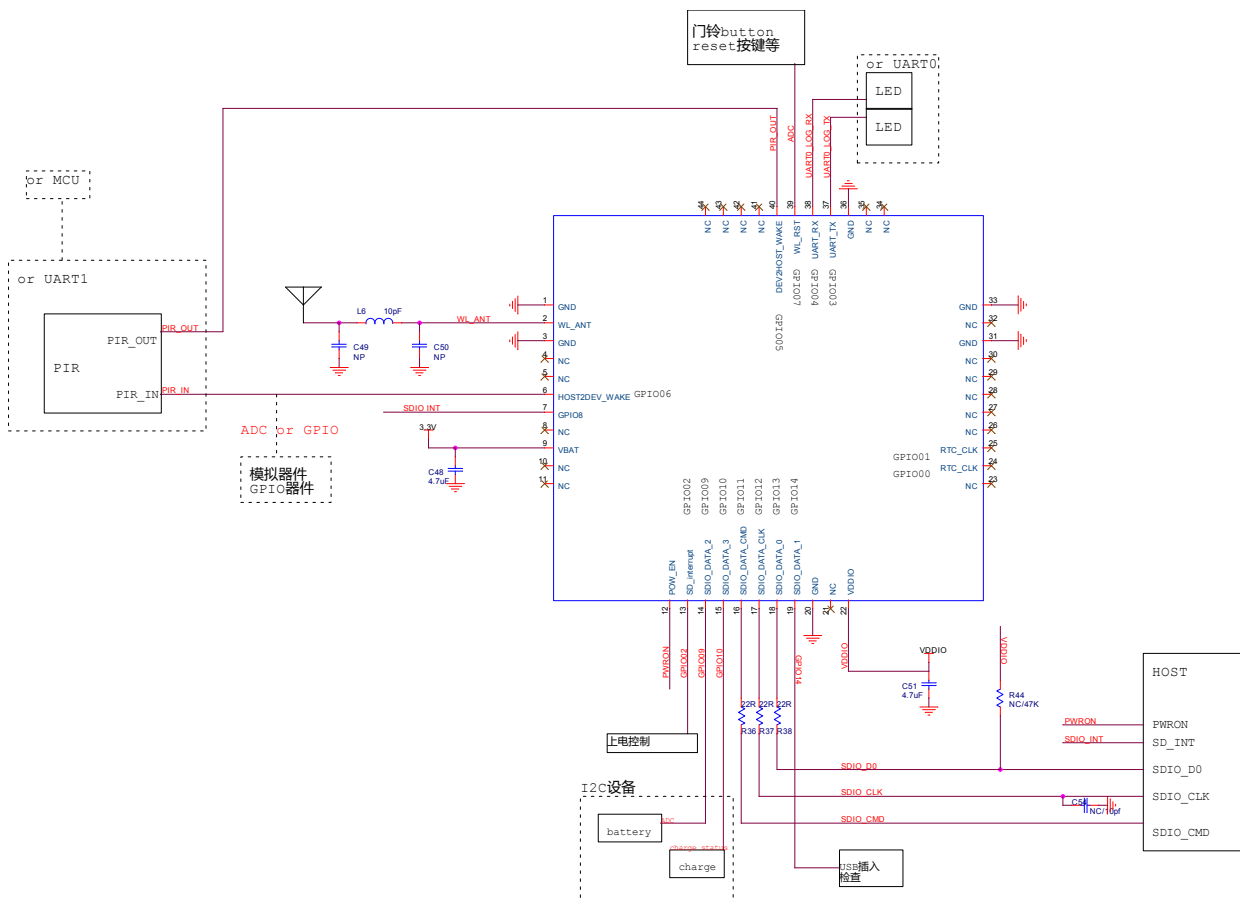
- GPIO8
- GPIO11
- GPIO12
- GPIO13

这些管脚会由软件上的 Hisyslink 组件直接控制, Hi3861L 的 SDIO 使用 1 线模式配置。

2. 3161A WIFI 上电复位 (POR: Power On Reset)期间, GPIO2/GPIO6/GPIO8 不能输入高电平, 否则芯片可能出现未知异常, 如出现 Flash 被写保护等问题。任何在上电器件可能出现高电平的应用都禁止接入到 GPIO2/GPIO6/GPIO8, 如 PIR 输入、按键输入、USB 插入检测。待 Hi3861L 上电完成 POR 后, 这些管脚可以输入高电平。

3. 如果要支持 WIFI 裸烧, UART 只能接在 GPIO3/GPIO4 上, 其中 TX 接 GPIO_3, RX 接 GPIO4。裸烧时建议选择支持高速 UART 的电脑以提升效率高速模式下 UART 的速率达 900Kbps-2Mbps, 比普通模式下 UART 的烧写速度更快。GPIO3/4 管脚上可以再外接 LED 灯、按键等管脚, 但要做好软硬件上的处理(如开关控制、外置管脚驱动能力等)。

4. 当 WIFI 待机时，外部设备可以通过 GPIO3/GPIO5/GPIO7/GPIO14 以中断方式唤醒 WIFI。
5. 由于管脚有限，在 GPIO7 上接了三个按键。使用方法为先使用 GPIO 中断，在获取到 GPIO 中断后，再复用成 ADC 进行电压采集，以区分按键。
6. WIFI IO 电平与 VDDIO 供电电压一致。当 VDDIO 采用 3.3V 供电时，WIFI IO 配置为 3.3V。



7 Ordering Information

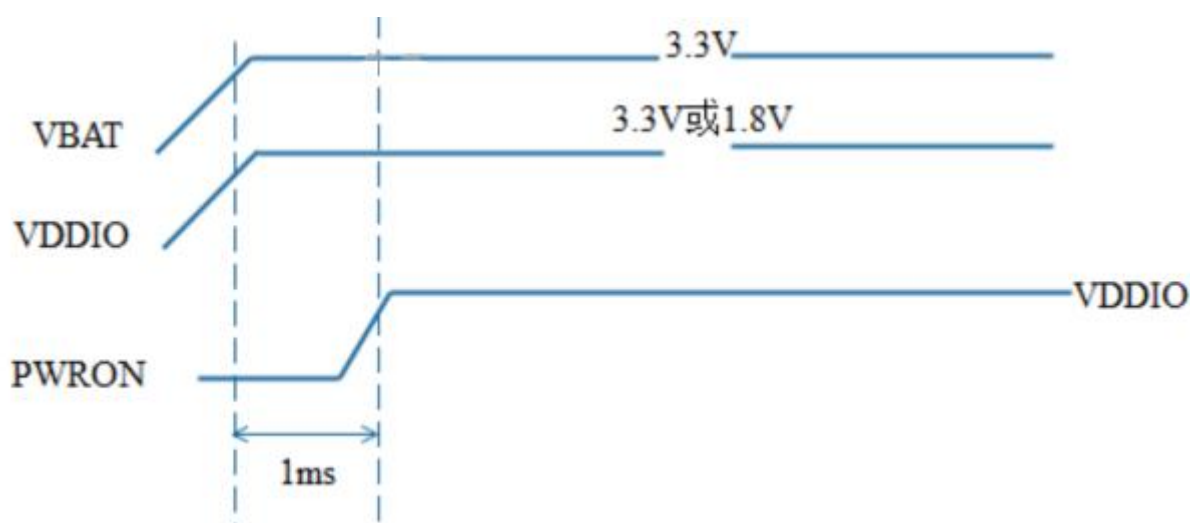
Part No.	Description
FG3161ASLX-00	Hi3861L, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,with shielding.
FG3161ASLX-01	Hi3861L, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,no shielding.

8 The Key Material List

Main	Inductor	2016 2.2uH ,±20%, DCR=0.125ohm, Isat=1.5A, Irms=1.5A, MPIE201610-2R2M-LF (麦捷微)
Main	Shielding	3161A-SL-V1.0 Shielding cover, no insulation glue, no

	cover	positioning foot (material: copper) Xintai
Main	Crystal	2520 40MHZ,13.8PF,7ppm,SR:50 Ω ,E2SB40E00000GE (HOSONIC)
Alt.	Crystal	2520 40MHz 15pF ±10ppm -40~85℃ Q40000V024 (东晶)
Main	RTC	3215 32.768KHZ 12.5PF 20PPM -40~85 ° C SF32K32768D31T-12.5 (泰晶)
Main	Chipset	Hi3861LRNIV100 WiFi IoT Soc,802.11b/g/n, WiFi Mesh, 内置 2M Flash, SDIO,UART,支持低功耗, QFN32, 5x5mm (海思)

9 Power on Sequence



- ※ VCC / VDDIO supreme electrical order requirements
- ※ In the process of power up, GPIO02 internal weak pull low ,the 40MHz crystal is selected..

10 Design Attention

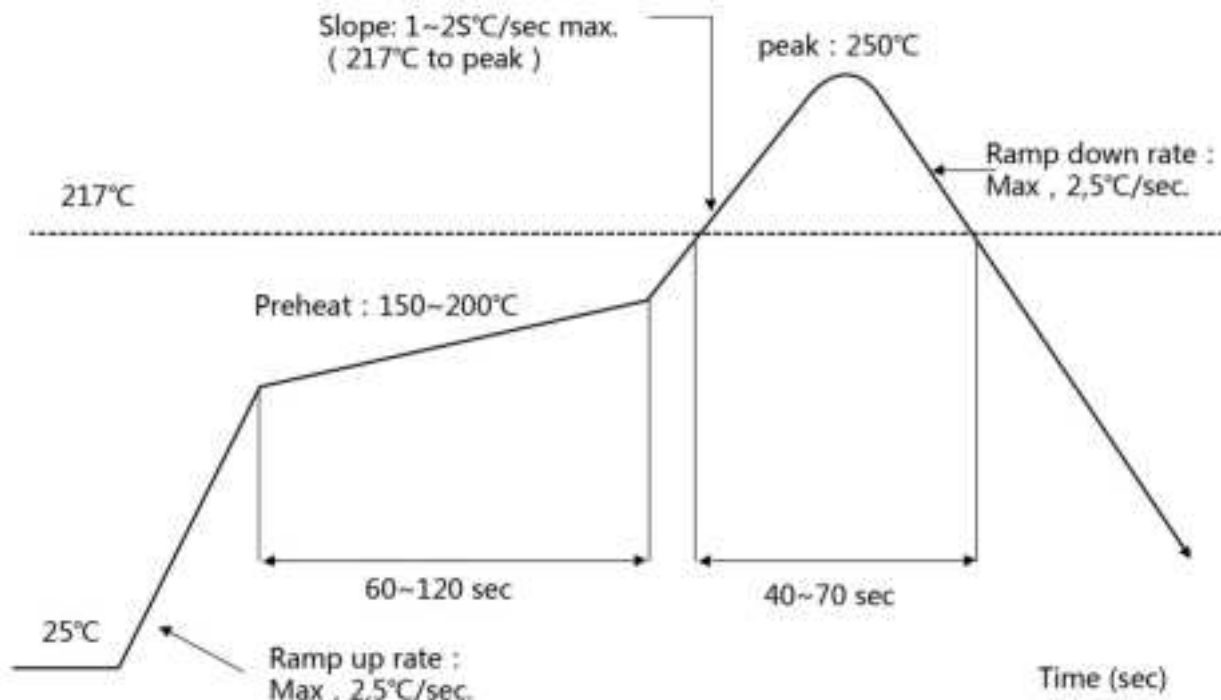
1. GPIO02 is the interrupt signal of SDIO, It also can be configured as dev wake host function.
2. GPIO8 can be setting as SDIO interrupt function.
3. PMU_PWRON is enable pin of the module. Default is pull high.
4. Wake function may not supported with recently applications, for power saving please using POWER EN pin enable or disable the module.

11 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

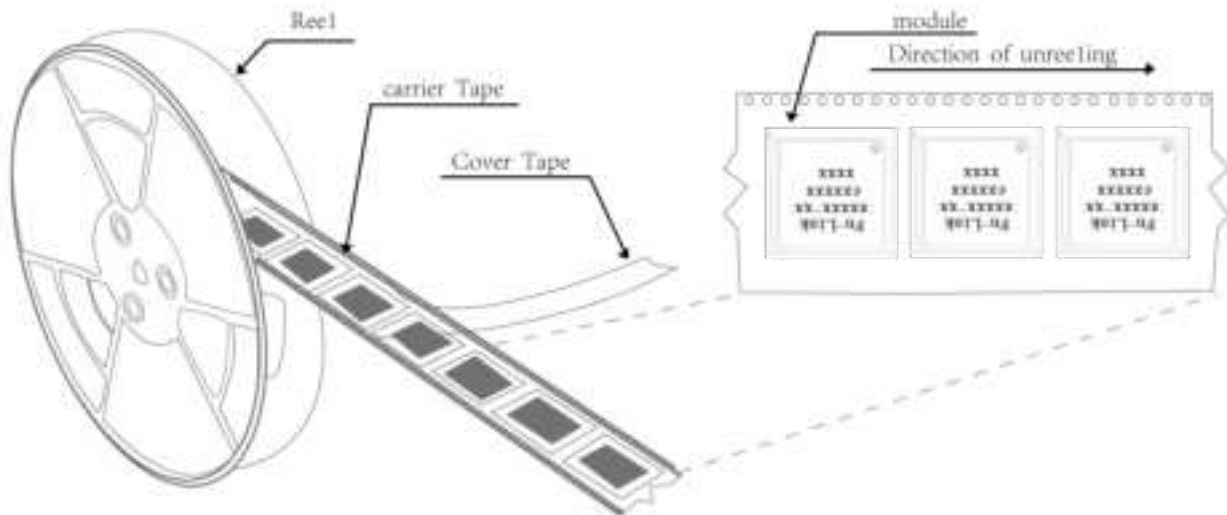
Number of Times : ≤ 2 times



12 Packing Information

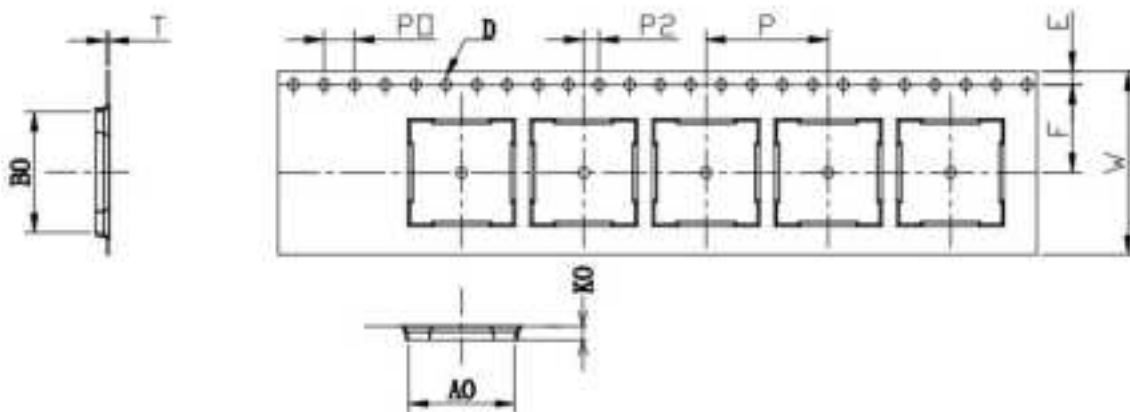
12.1 Reel

A roll of 1500pcs

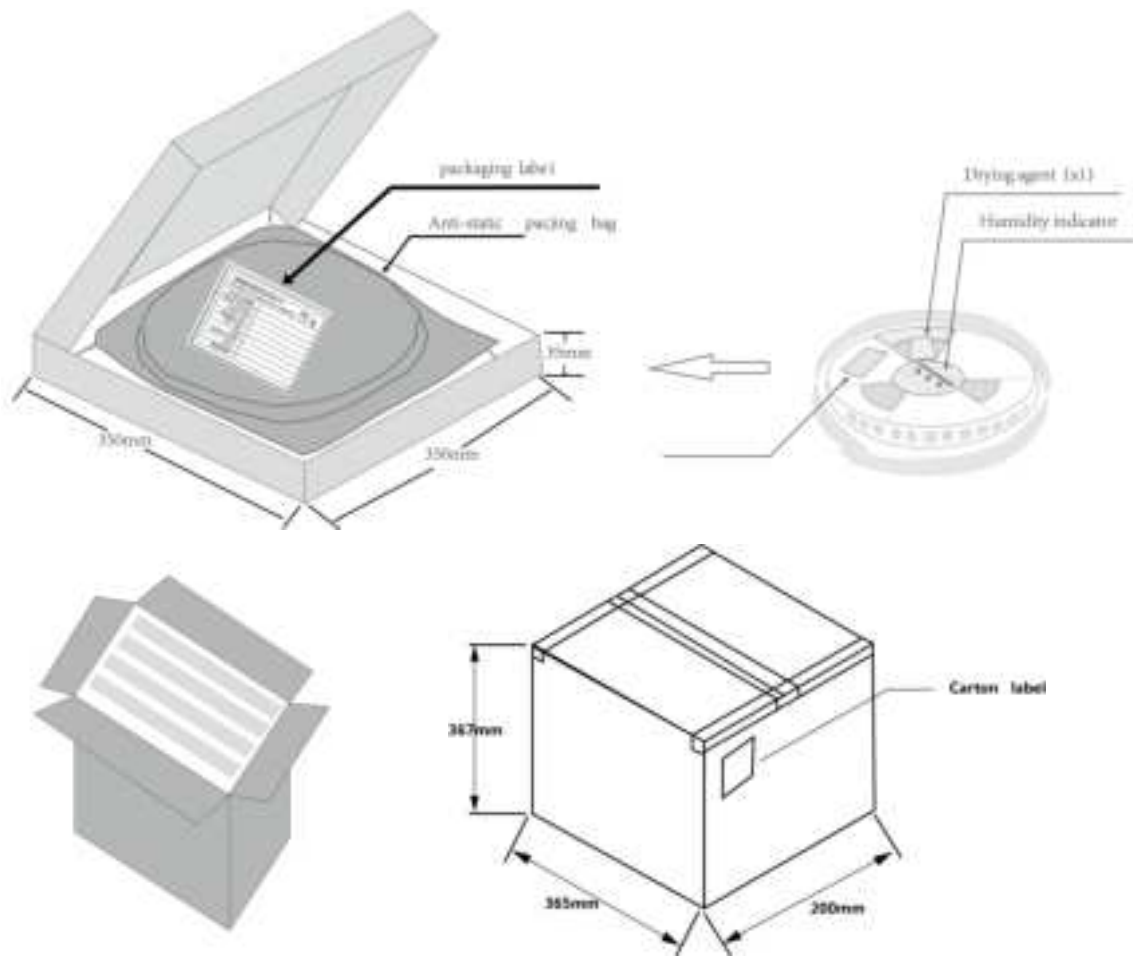


12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	± 0.3 -0.3	± 0.15	± 0.15	± 0.1 -0.1	± 0.1 -0.1	± 0.1	± 0.10	± 0.1	± 0.1	± 0.1	± 0.06



12.3 Packaging Detail



12.4 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH).
- Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
- The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- Baking is required if conditions b) or c) are not respected
- Baking is required if the humidity indicator inside the bag indicates 10% RH or more