Lierda FB82 Series Module Hardware Design Manual

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Document revision history

Document version	Date of change	proposer	auditor	Changes
Rev1.0	23-10-08	TYY	YB	Initial version
Rev1.1	23-10-19	TYY	YB	Modification of charts and refinement of some data

Safety Instructions

It is the user's responsibility to follow the relevant regulations of other countries and the specific environmental regulations for the use of wireless communication modules and equipment. By observing the following safety principles, you can ensure your personal safety and help to protect the product and the working environment from potential damage. We are not liable for damages related to the customer's failure to comply with these regulations.

	Safety on the road comes first! When you are driving, do not use hand-held mobile terminal devices unless they have a hands-free function. Please stop the car before making a call!
	Please turn off your mobile devices before boarding the airplane. The wireless function of mobile devices is prohibited on board to prevent interference with the aircraft's communication system. Ignoring this reminder may lead to flight safety or even violate the law.
	When in a hospital or health care setting, note if there are restrictions on the use of mobile devices.RF interference can cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.
	The mobile device does not guarantee a valid connection in all circumstances, for example if the mobile device is out of credit or the SIM is invalid. When you are in an emergency situation, please remember to use the emergency call and make sure that your device is switched on and in an area with sufficient signal strength.
	Your mobile device receives and transmits RF signals when it is switched on, which can cause RF interference when near a TV, radio computer or other electronic device.
	Keep the mobile terminal unit away from flammable gases. Turn off the mobile device when you are near gas stations, oil depots, chemical plants, or explosive workplaces. It is a safety hazard to operate electronic devices in any place where there is a potential explosion hazard.

Applicable modules Options

serial number	Module Model	Supported Frequency Bands	Dimension(mm)	Module Introduction
1	L-WFIFB82-G5PP4	2.4GHz ISM Band	24.0 x 16.0 x 3.3	PCB Antennas

catalogs

1 introductory

FB82 series module is a general-purpose IoT Wi-Fi4 module supporting 802.11b/g/n @ 2.4 GHz and Bluetooth 5 (LE) features (current default is the on-board antenna version); the built-in chip adopts a RISC-V 32-bit single-core microprocessor, with a main frequency of up to 120MHz; it supports the 1T1R mode, with a data rate of up to 72.2 Mbps; can be widely used in mobile devices, low-power IoT sensor Hubs, PV communication bars, smart homes and other fields.

Figure 1.1 Schematic diagram of FB82 series module

2 Product Overview

2.1 Basic Features

Table 2 1 Module Base Characteristics

characterization	descriptive
package interface	LCC + Stamp Interface
wireless standard	IEEE 802.11 b/g/n + BLE 5.0 (1M and 2M)
Wi-Fi MAC	IEEE802.11 e/i/k/v/w
Module Size	24mm × 16mm × 3.3mm
operating voltage	3.0V ~ 3.6V, 3.3V typical
operating frequency	2400 ~ 2483.5MHz (2.4 GHz ISM Band)
Antenna Gain	TBD
operating temperature	-40 ~ +105°C
Storage temperature	-40 ~ +105°C
peripheral interface	SPI, UART, I2C, LED PWM, general-purpose DMA controllers, ADC and temperature sensors, etc.
Serial Port Configuration	Main serial port UART1 (IO7-TXD1 and IO6-RXD1): ◆ For AT command configuration and data transfer, default baud rate is 115200bps Debugging serial port UART0 (TXD0 and RXD0): ◆ For firmware upgrade, default baud rate is 74880bps, up to 921600bps ◆ Used for serial port command configuration and data transmission during RF testing, default baud rate is 74880bps
Wi-Fi bandwidth	Supports standard 20MHz bandwidth
Storage Characteristics	Supports 2MB SiP FLASH

2.2 Product Advantages

●A complete WiFi subsystem, compliant with IEEE 802.11b/g/n protocols, with Station mode, SoftAP mode, SoftAP +Station mode, and Promiscuous mode (i.e., Promiscuous mode, which is a special mode).

●Low-power Bluetooth subsystem with Bluetooth 5 support for Central and Peripheral roles.

●RISC V 32-bit single-core processor with four-stage pipeline architecture and up to 120MHz main frequency.

●Memory function, built-in 272KB SRAM (of which, 16 KB is dedicated to cache), 576 KB ROM storage space.

●The hardware crypto gas pedal supports ECC, Hash and secure boot, an integrated random number generator, and off-chip memory encryption and decryption functions.

●Abundant communication interfaces and GPIO pins support a wide range of scenarios and complex applications.

2.3 application scenario

●Photovoltaic communication bars/collectors

●consumer electronics product

●industrial automation

●Smart Home, Smart Home Appliances

●Health/medical/caregiving equipment

2.4 functional block diagram

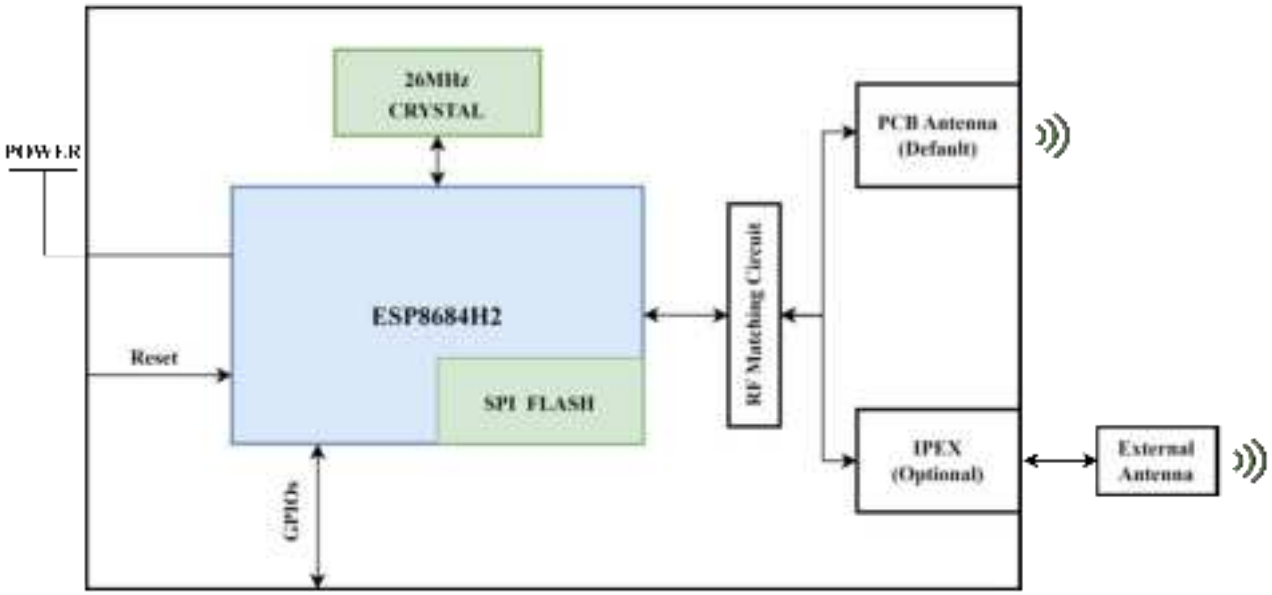

Figure 2.1 Block diagram of FB82 series module structure

2.5 Pinouts

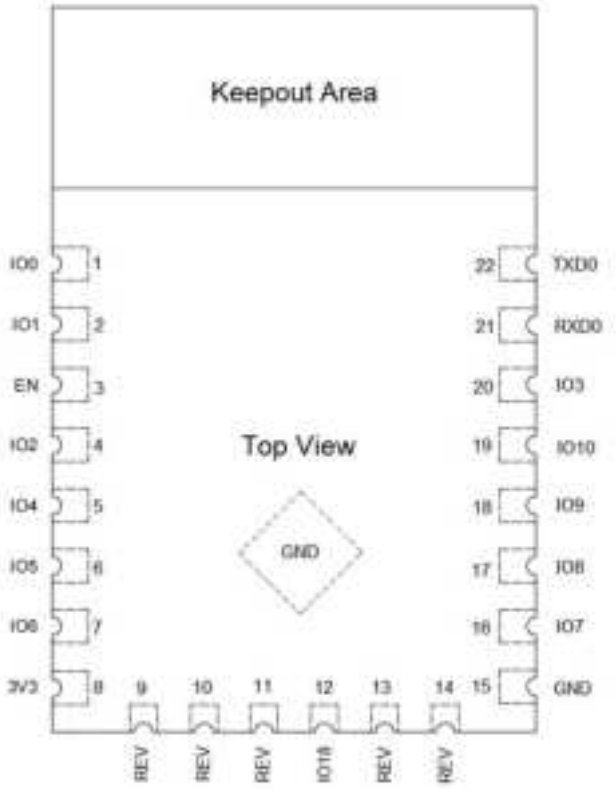

Figure 2.2 Pinout diagram

2.6 Pin Description Table

To facilitate a better understanding of the application, the following table describes the type definitions of the I/O parameters:

Table 2-2 Description of Type Definitions for I/O Parameters

I/O Parameter Type	clarification
IO	input and output
DI	digital input
DO	digital output
P	Power Pins
G	structural particle: used before a verb or adjective, linking it preceding the verb or adjective

Table 2-3 Module Pin Function Description

Pin Number	Name	I/O Type	description	note
1	IO0	I/O	General purpose IO port	GPIO0 of the corresponding IC
2	IO1	I/O	General purpose IO port	GPIO1 of the corresponding IC
3	EN	I	Module Enable	CHIP_EN of the corresponding IC, active high, internal pull-up has been defaulted
4	IO2	I/O	General purpose IO port	GPIO2 of the corresponding IC
5	IO4	I/O	General purpose IO port	MTMS of the corresponding IC (GPIO4)
6	IO5	I/O	General purpose IO port	MTDI of the corresponding IC (GPIO5)
7	IO6	I/O	Main serial port: module receives data	MTCK of the corresponding IC (GPIO6) The default configuration is RXD1
8	3V3	P	Power supply	Supply range 3.0~3.6V, typical 3.3V
9	REV	/	Undefined pins,	/

			dangling handling	
10	REV	/	Undefined pins, dangling handling	/
11	REV	/	Undefined pins, dangling handling	/
12	IO18	I/O	General purpose IO port	GPIO18 of the corresponding IC
13	REV	/	Undefined pins, dangling handling	/
14	REV	/	Undefined pins, dangling handling	/
15	GND	P	structural particle: used before a verb or adjective, linking it preceding the verb or adjective	/
16	IO7	I/O	Main serial port: module sends data	MTDO of the corresponding IC (GPIO7) The default configuration is TXD1
17	IO8	I/O	General purpose IO port	GPIO8 of the corresponding IC Strapping pins, see Table 2-4 for details
18	IO9	I/O	General purpose IO port	GPIO9 of the corresponding IC Strapping pins, see Table 2-4 for details
19	IO10	I/O	General purpose IO port	GPIO10 of the corresponding IC
20	IO3	I/O	General purpose IO port	GPIO3 of the corresponding IC
21	RXD0	DI	Burn test serial port: module receives data	U0RXD of the corresponding IC (GPIO19)
22	TXD0	DO	Burn test serial port: module sends data	U0TXD of the corresponding IC (GPIO20)

2.7 Strapping Pin

FB82 series modules have 2 Strapping pins, IO8 and IO9, which correspond to GPIO8

and GPIO9 of the IC. software can read the *GPIO_STRAPPING field* of the *GPIO_STRAP_REG register* to get the values of GPIO8 and GPIO9.

During the release of the system reset (power-on reset, RTC watchdog reset, undervoltage reset) of the module chip, the Strapping pin samples the level and stores it in the latch, which is latched to "0" or "1" and remains there until the chip is powered down or turned off. and will be held until the chip is powered down or turned off. Each Strapping pin is connected to an internal pull-up/pull-down. If a Strapping pin has no external connection or the connected external line is in a high impedance state, the internal weak pull-up/pull-down will determine the default value of the input level of the Strapping pin. To change the value of Strapping, the user can either apply an external pull-down/pull-up resistor or apply the host MCU's GPIO to control the level of the Strapping pin at the time of the module's power-on reset release. After reset release, the Strapping pin has the same function as the normal pin.

Refer to Table 2-4 for detailed startup modes for configuring the Strapping pin:

Table 2-4 Strapping Pin Descriptions

system boot mode (1)			
Module Pinout	default state	SPI startup mode	burn mode
IO8	pull up	irrelevant item	1
IO9	Internal weak pull-up	1	0

Controls ROM Code printing during system startup		
Module Pinout	default state	functionality
IO,9	pull up	*The EFUSE_UART_PRINT_CONTROL field* of eFuse is At 0 (initial default), power-up prints normally and is not controlled by GPIO8; When 1, if GPIO8 is 0, power-on normal printing; if GPIO8 is 1, power-on no printing;

		When 2, if GPIO8 is 0, power-on does not print; if GPIO8 is 1, power-on prints normally; When 3, power-on does not print, not controlled by GPIO8

(1) GPIO8=0 and GPIO9=0 is not available.

Figure 2.3 gives the build-up time and hold-up time of the module EN (corresponding to the CHIP_EN pin of the IC) before and after powering up the Strapping pin, and the description of each parameter is shown in Table 2-5.

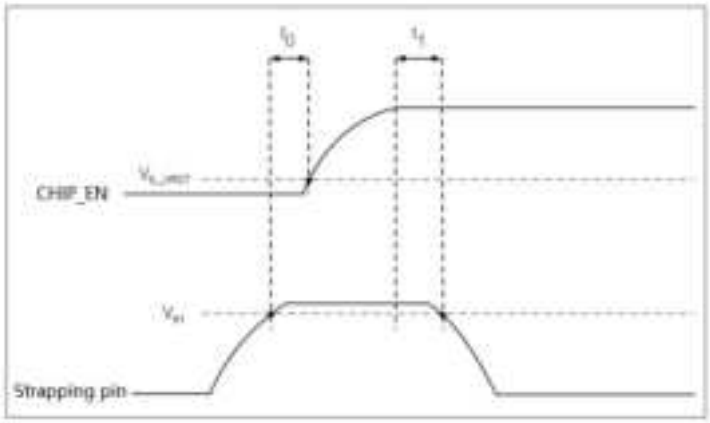

Figure 2.3 Establishment time and hold time of Strapping pins

Table 2-5 Parameter Descriptions for Strapping Pin Establishment Time and Hold Time

parameters	descriptive	minimum value	unit (of measure)
t_0	CHIP_EN Establishment time before power-up	0	ms
t_1	CHIP_EN Hold time after power-up	3	ms

2.8 Evaluation Kits

LILDA can provide complete evaluation and development kits with FB82-GP module development board, welcome to contact us for inquiry.

3 Working Characteristics

3.1 Description of low power consumption

FB82 series modules support 3 low power consumption modes, as shown in the table below, users can choose according to the actual application scenarios.

Table 3-1 FB82 Series Module Low Power Consumption Modes

paradigm	state of affairs	descriptive
Deep sleep	The CPU and most of the peripherals are powered down and only the RTC memory and RTC peripherals are operational	When the set time is up, the module wakes up automatically, calls the Deep-sleep wakeup pile, and then loads the application. For Deep-sleep mode, the only wake-up method is timed wake-up
Light sleep	The CPU is suspended, the RTC memory and peripherals and the ULP coprocessor are running, and any wake-up event (MAC, host, RTC timer, or external interrupt) wakes up the module	The CPU will automatically hibernate and the RF will periodically shut down according to the listening interval set by the AT command.
Modem sleep	CPU can run, clock can be configured. wi-fi baseband, bluetooth baseband and rf off	RF will shut down periodically based on the AP's DTIM (routes generally set DTIM to 1)

3.2 Power and Reset Timing

The following figure shows the FB82 series module power-up and reset timing diagram, and the description of each parameter is shown in Table 3-2.

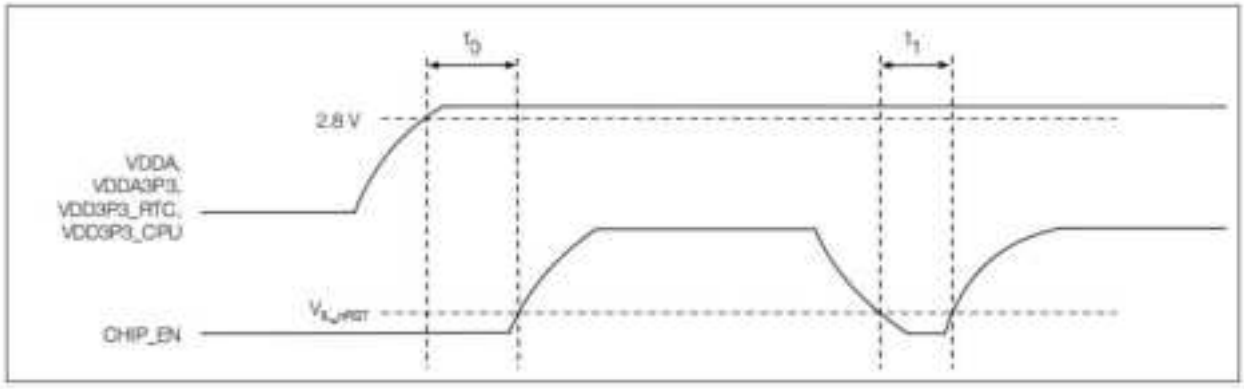

Figure 3.1 Module power-up and reset timing diagram

Table 3-2 FB82 Series Module Power-Up and Reset Timing Diagram Parameter Description

parameters	descriptive	minimum value	unit (of measure)
t_0	Module EN pin (corresponding to chip CHIP_EN) later than system power supply 3.3V power-up delay time	50	μs
t_1	Time that the CHIP_EN level is lower than V_{IL_nRST} (see Table 6-3 in Section 6.3 for its value)	50	μs

note

VDDA, VDDA3P3, VDD3P3_RTC, and VDD3P3_CPU in Figure 3.1 are the main input power supplies to the main chip (system) with a minimum value of 3.0V.

3.3 Power Supply Design

The FB82 series modules have one 3V3 pin for connecting to an external power supply, and the interface is described in the following table:

Table 3-3 Power Pin Definitions

Pin Number	Pin Name	I/O	description	note
8	3V3	PI	Power supply	The power supply must be able to supply up to 500mA of current.
15	GND	G	structural particle: used before a verb or adjective, linking it	

			preceding the verb or adjective	

FB82 series modules must pay attention to the following points when designing the power supply circuit:

●When the module operates in TX mode, the instantaneous current becomes large, so the power supply is required to have a power supply capacity of 500mA or more, and a 22 μF capacitor and a 0.1 μF capacitor are placed close to the pins on the power supply alignment of the module, as shown in Figure 3.2;

●When the module repeatedly turns on and off the power supply, it must ensure that the voltage at the EN pin is ≤0.75V and the duration is ≥50μs for the reset timing requirements. Due to the 3V3 power supply peripheral circuit has a large capacitance, and EN (corresponding to the chip CHIP_EN) is connected to the 3V3 internally, the process of CHIP_PU level to 0 when the power supply power down will be very slow, and it may appear that next time when the power supply is restarted CHIP_PU can not be low enough to lower the level of the phenomenon, which leads to the reset is not sufficient, at this time, we need to have an additional discharging circuit to accelerate the power supply of a large capacitor discharge; and the power supply is not enough for the reset. Discharge;

●Power ripple can greatly affect the RF TX performance, when measuring power ripple, it should be noted that the power ripple must be tested under normal packet sending, and as the power changes in different modes, the power ripple will also change, the higher the packet sending power, resulting in a larger ripple; in general, the peak value of the power ripple peak is less than 90 mV when sending MCS7 @ 11n packets; the peak value of the power ripple peak is less than 120 mV when sending 11M @ 11b packets. When sending 11M @ 11b, the peak power ripple should be less than 120 mV if possible.

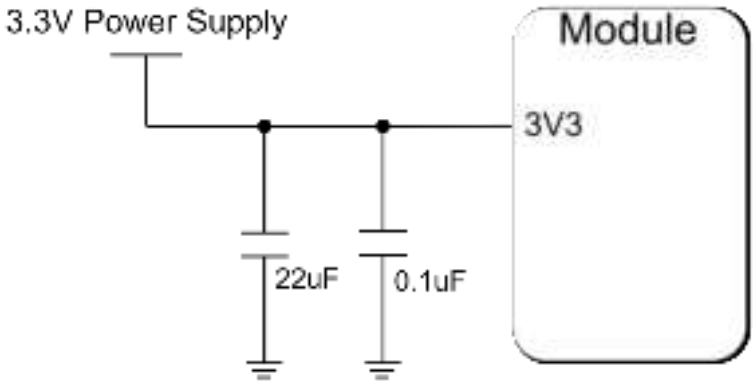

Figure 3.2 Module power supply reference circuit

3.4 Reset design

Pin 3 of the module, EN, is an enable pin, and a low level enables the module to enter the reset state (see section 3.2 for reset timing details). Users can external directly connected to other MCU's IO for control, at this time VIL_nRST is 0.25×VDD(1) ; also can be designed according to the following reference design.

(1)VDD is the power supply for the IO.

3.4.1 Transistor Reset Reference Circuit

The transistor reset circuit is shown in Figure 3.3. Layout should pay attention to the reset alignment should not be too long, pay attention to the packet ground protection, and away from RF, power supply, and strong signal interference sources, transistors as close as possible to the module EN pin, so as to avoid interference from external signals; it is recommended that near the module EN pin to set aside a capacitor 100nF ~ 1μF position, the default is not affixed.

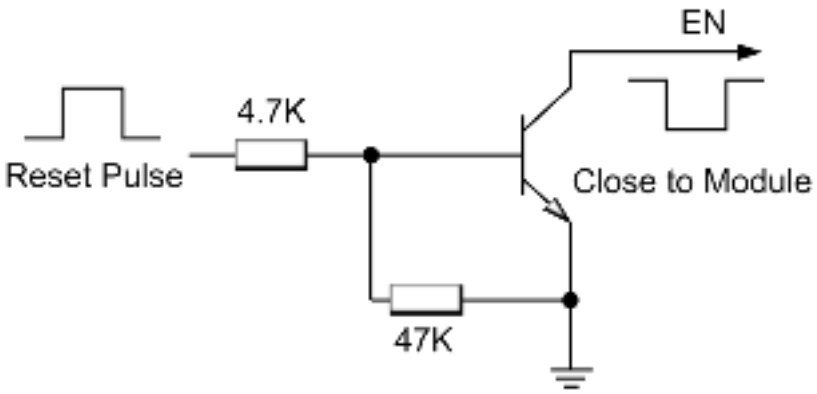

Figure 3.3 Transistor reset reference circuit

3.4.2 Key Reset Reference Circuit

The key reset reference circuit is shown in Figure 3.4. In order to prevent the key from being affected by ESD, it is usually recommended to place a TVS tube close to the key, and a 100nF~1μF capacitor position can be reserved close to the EN pin of the module, which is not affixed by default.

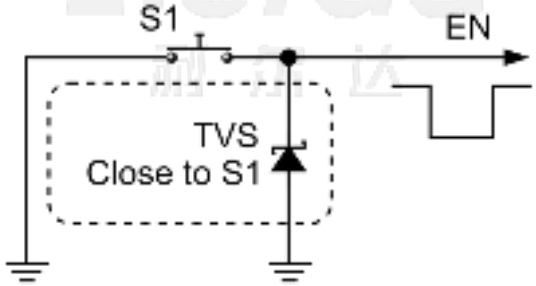

Figure 3.4 Key reset reference circuit

3.4.3 Reset IC Reference Circuit

Customer applications, there are battery-powered scenarios, the battery voltage is too low may lead to the module into an abnormal state and can not start normally, such as low-voltage state may appear FLASH was mistakenly erased leading to the loss of internal information; it is recommended that the module EN pin external power monitoring chip (i.e., reset IC), when the external power supply voltage is lower than a certain threshold, EN will

be pulled down by the reset IC, the module stops working; Only when the power supply voltage returns to the normal stable state, EN will be pulled to high level again, and the module will restart; the reference circuit of reset IC is shown in Figure 3.5.

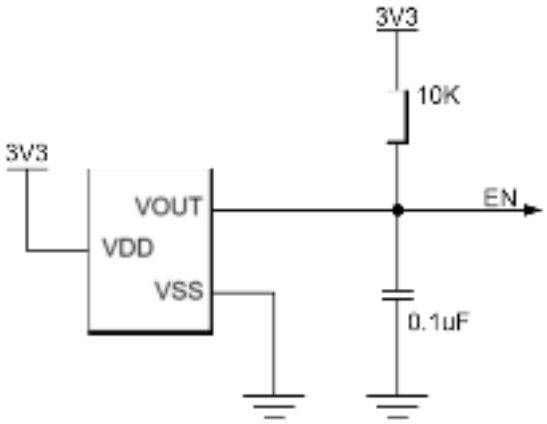

Figure 3.5 Reset circuit

Recommended reset IC for reference:

Brand: SGM Micro Model: SGM809B-RXN3LG/TR Package: SOT-23

4 Application Interface

4.1 UART communication

FB82 series modules provide two UART communication interfaces, the main serial port UART1 and debug serial port UART0.

4.1.1 main serial port

The main serial port UART1 is IO7 (TXD1) and IO6 (RXD1), which is used for AT command configuration and data transmission, the default baud rate is 115200bps, and the serial port connection schematic is as follows:

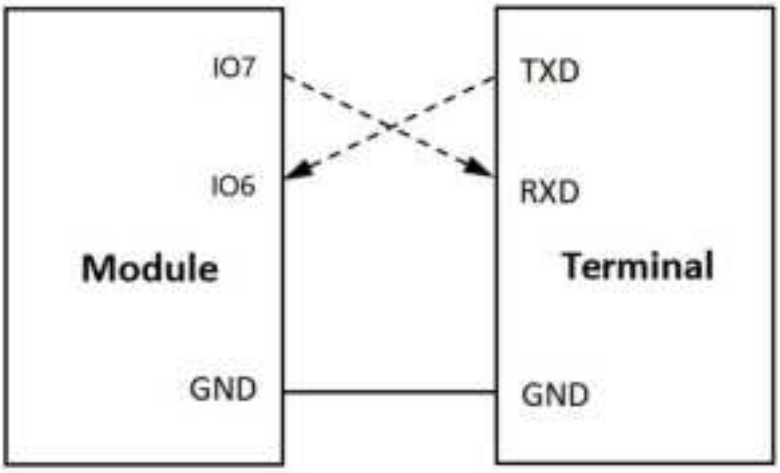

Figure 4.1 Schematic diagram of UART1 serial port connection

4.1.2 Debugging Serial Ports

Debugging serial port UART0 for TXD0 and RXD0, mainly used for firmware upgrades, the default baud rate of 74880bps, up to 921600bps; burning should be noted that the module IO9 pins for burning control feet (module strapping pins, see section 2.7 for details), to enter the burning state must ensure that the module power-up before IO9 is in the state of pulling down, or after IO9 pull down to trigger a hardware reset; through the UART0 serial port burning firmware connection schematic shown in Figure 4.2; through the UART0 serial port burning firmware connection schematic diagram. IO9 is pulled down before the module is powered on, or after IO9 is pulled down, a hardware reset is triggered; the connection schematic for burning the firmware through the UART0 serial port is shown in Figure 4.2:

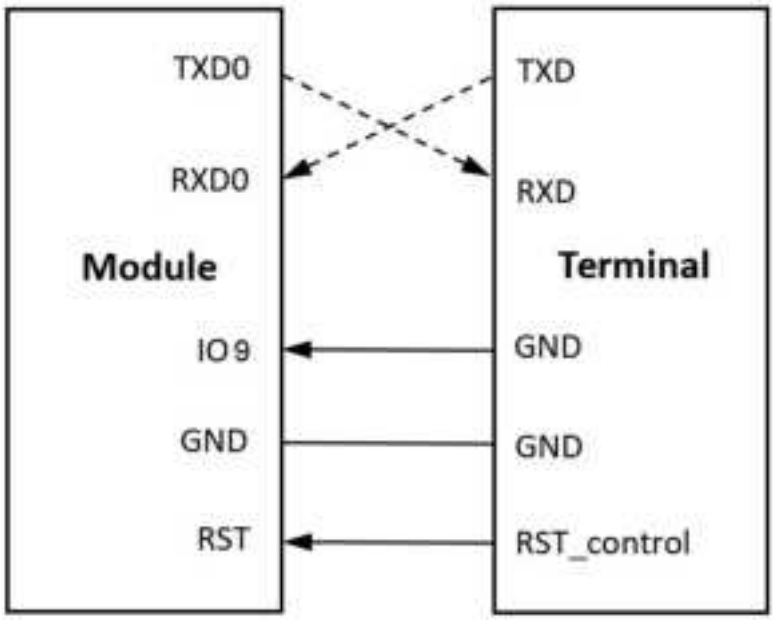

Figure 4.2 Schematic diagram of the UART0 serial port connection during burn-in

UART0 can also be used for serial port command configuration and data transmission during RF test, the baud rate is 74880bps by default, and the wiring is shown in Figure 4.3.

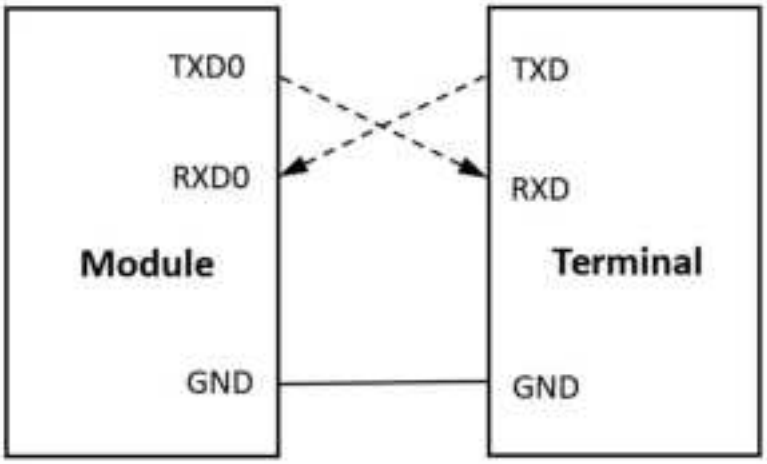

Figure 4.3 Schematic diagram of UART0 serial port connection during debugging

4.2 SPI controller

Serial Peripheral Interface (SPI) is a synchronous serial interface used to communicate with peripheral devices.There are three sets of SPI controllers in the FB82 series modules: SPI0, SPI1, and General Purpose SPI2 (i.e. GP-SPI2).

The SPI0 and SPI1 controllers (MSPI) are primarily for internal use to access Flash or PSRAM, and have been used internally to connect to the SPI interface to SiP Flash.The length of the data transfer in SPI memory mode is measured in bytes, and up to a four-wire STR read/write operation is supported; the clock frequency is configurable, and the maximum clock frequency supported in STR mode is 60MHz.

The SPI2 can be configured in both host and slave modes. Both host and slave modes support two-wire full-duplex and single-wire, two-wire, or four-wire half-duplex communication. the SPI2's host clock frequency is configurable, up to 40 MHz in either host or slave mode, and supports four clock modes for SPI transfers; the length of data transfers is measured in bytes; clock polarity (CPOL) and phase (CPHA) are configurable; and GDMA channels can be connected .

The architecture of the SPI module is illustrated in Figure 4.4.

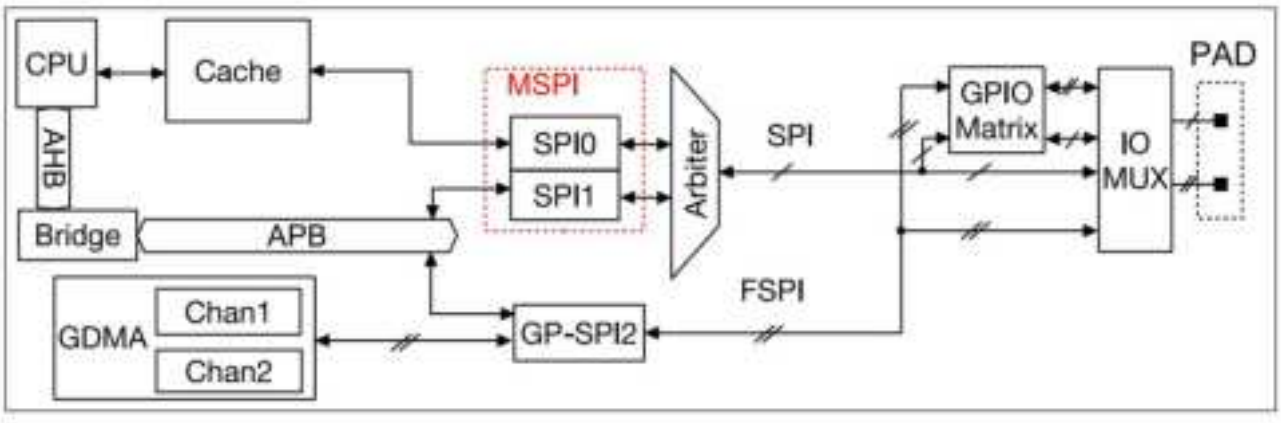

Figure 4.4 SPI module architecture description

The GP-SPI2 exchanges data with SPI devices in the following ways:

- In CPU-controlled transfer mode: CPU ↔ GP-SPI2 ↔ SPI device;
- In CPU-controlled transfer mode: GDMA ↔ GP-SPI2 ↔ SPI device.

The GP-SPI2 input and output signals are prefixed with FSPI, and the FSPI bus signals can be connected to the GPIO pins via the GPIO switching matrix or IO_MUX, as described in Section 4.7.

4.3 I2C Host Controller

FB82 series modules have 1 I2C bus host interface to support:

- Standard mode (100Kbit/s);
- Fast mode (400 Kbit/s);
- Speeds up to 800 Kbit/s are limited by the pull-up strength of SCL and SDA;
- 7-bit addressing mode and 10-bit addressing mode;
- Dual addressing mode;
- 7-bit broadcast address;
- Supports pulling down the SCL clock for continuous data transfer;
- Supports programmable digital noise filtering.

4.4 LED PWM Controller

The LED PWM controller has the following features:

- Six independent PWM generators (i.e. six channels);
- The PWM duty cycle has a maximum precision of 14 bits;
- The phase and duty cycle of the PWM output signal are adjustable;
- PWM duty cycle trimming;
- Duty cycle auto-fade - i.e., the PWM signal duty cycle can be gradually increased or decreased without processor intervention, and an interrupt is generated when the fade is completed;
- PWM signals can be output in low-power mode (Light-sleep mode);
- Three divisible clock sources:
  - PLL_60M_CLK
  - FOSC_CLK
  - XTAL_CLK
- Four independent timers for fractional frequency division.

4.5 Analog/Digital Converter (ADC)

The FB82 series modules contain a successive approximation analog-to-digital converter (SAR ADC).The SAR ADC has the following characteristics:

- The SAR ADC has a dedicated ADC Reader module, Digital_Reader, to obtain the sampling results;
- Supports 12-bit sampling resolution;
- Supports acquisition of analog voltages on up to 5 pins;
- DIG ADC Controller:

  - Equipped with single-sampling and multi-channel scanning control modules, supporting single-sampling mode and multi-channel scanning mode respectively.

  - Supports single-sampling mode and multi-channel scanning mode at the same time

  - In multi-channel scanning mode, support for customizing the order of scanning channels

  - Two filters are provided with configurable filter coefficients.

  - Threshold monitoring is supported, interrupt will be generated if the sampling value is greater than the set high threshold or less than the set low threshold.

The main functional structure of the SAR ADC is shown in Figure 4.5:

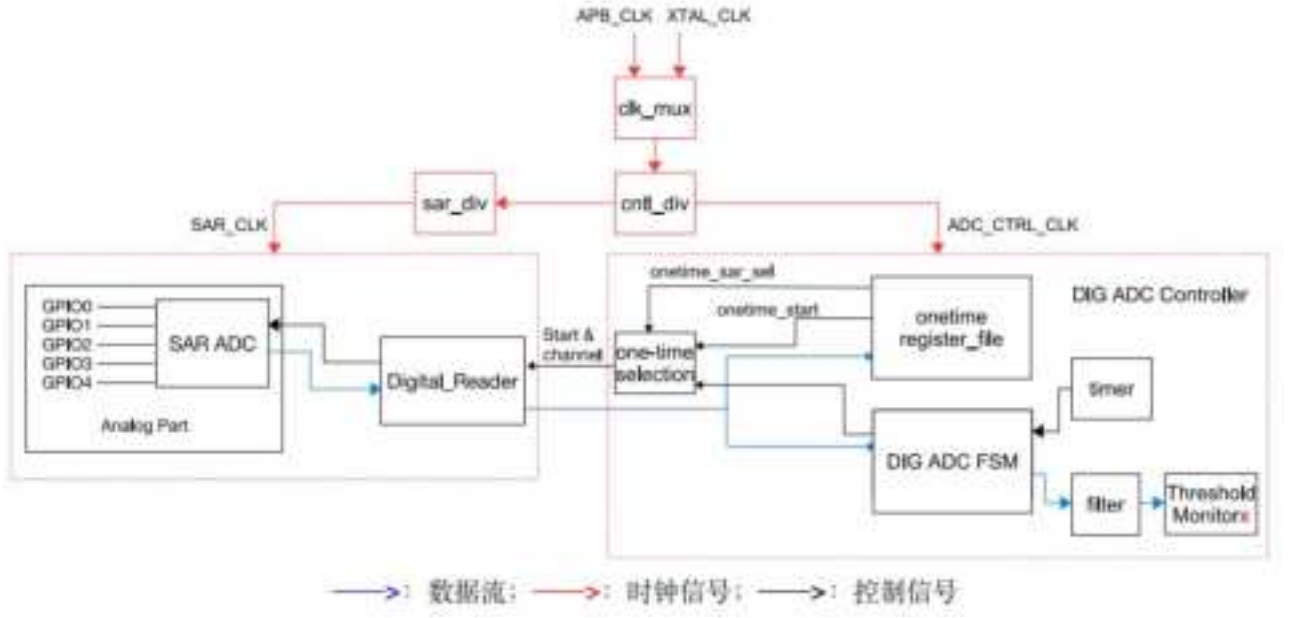

Figure 4.5 Functional overview of the SAR ADC

4.6 temperature sensor

FB82 series modules are equipped with a temperature sensor to monitor the internal temperature of the chip in real time. The temperature sensor generates a voltage that varies with the temperature, and the internal ADC converts the sensor voltage into a digital quantity.

Temperature sensors have a measurement range of -40°C to 125°C and are generally only suitable for monitoring changes in the internal temperature of the chip, a value that varies with the microcontroller clock frequency or IO load. Generally, the internal chip temperature will be higher than the operating ambient temperature.

4.7 I/O_MUX List

Table 4-1 lists the IO_MUX functions for all I/O pins in the main chip.

Table 4-1 I/O_MUX Pin List

module Pin Number	name	GPIO serial number	microchip pinout	Function 0	Function 1	Function 2	driving force	reset	note
1	IO0	0	GPIO0	GPIO0	GPIO0	/	2	0	R
2	IO1	1	GPIO1	GPIO1	GPIO1	/	2	0	R
4	IO2	2	GPIO2	GPIO2	GPIO2	FSPIQ	2	1	R
20	IO3	3	GPIO3	GPIO3	GPIO3	/	2	1	R
5	IO4	4	MTMS	MTMS	GPIO4	FSPIHD	2	1	R
6	IO5	5	MTDI	MTDI	GPIO5	FSPIWP	2	1	R
7	IO6	6	MTCK	MTCK	GPIO6	FSPICLK	2	1(1)	/
16	IO7	7	MTDO	MTDO	GPIO7	FSPID	2	1	/
17	IO8	8	GPIO8	GPIO8	GPIO8	/	2	1	/
18	IO9	9	GPIO9	GPIO9	GPIO9	/	2	3	/
19	IO10	10	GPIO10	GPIO10	GPIO10	FSPICS0	2	1	/

/	/	11	VDD_SPI	GPIO11	GPIO11	/	2	0	S
/	/	12	SPIHD	SPIHD	GPIO12	/	2	3	S
/	/	13	SPIWP	SPIWP	GPIO13	/	2	3	S
/	/	14	SPICS0	SPICS0	GPIO14	/	2	3	S
/	/	15	SPICLK	SPICLK	GPIO15	/	2	3	S
/	/	16	SPID	SPID	GPIO16	/	2	3	S
/	/	17	SPIQ	SPIQ	GPIO17	/	2	3	S
12	IO18	18	GPIO18	GPIO18	GPIO18	/	2	0	/
21	U0RXD	19	U0RXD	U0RXD	GPIO19	/	2	3	/
22	U0TXD	20	U0TXD	U0TXD	GPIO20	/	2	4	/

Drive strength:

In Table 4-1, "Driving Strength" is the default driving strength of each pin after reset.

- 0 - Drive intensity = ~ 5mA
- 1 - Drive intensity = ~ 10mA
- 2 - Drive intensity = ~ 20mA (default)
- 3 - Drive intensity = ~ 40mA

Reset:

In Table 4-1, "Reset" is the default configuration state of each pin after reset.

- 0 - IE = 0 (input off)
- 1 - IE = 1 (input enable)
- 2 - IE = 1, WPD = 1 (input enable, pull-down resistor enable)
- 3 - IE = 1, WPU = 1 (input enable, pull-up resistor enable)
- 4 - OE = 1, WPU = 1 (output enable, pull-up resistor enable)
- 1(1) - If EFUSE_DIS_PAD_JTAG = 1, the MTCK pin floats after reset, i.e., IE = 1;

  If EFUSE_DIS_PAD_JTAG = 0, the MTCK pin is connected to an internal

pull-up resistor, i.e. IE = 1 and WPU = 1.

Description:

(1) The "Remarks" in Table 4-1 are additional descriptions of each IO function.

●R - Represents pins located in the VDD3P3_RTC power domain that partially have analog functionality, see Table 4-2.

●S - For chip versions with built-in SiP Flash, it means that this pin is dedicated to connecting SiP Flash and only function 0 can be used.

(2) For more technical information, such as GPIO switching matrix peripheral signals, please also refer to the module main chip ESP8684 technical manual.

Table 4-2 Analog Functions of the IO MUX Pins

module (computer) Pin Number	module (computer) pinout	GPIO Serial Number	Pin Name	analog function
1	IO0	0	GPIO0	ADC1_CH0
2	IO1	1	GPIO1	ADC1_CH1
4	IO2	2	GPIO2	ADC1_CH2
20	IO3	3	GPIO3	ADC1_CH3
5	IO4	4	MTMS	ADC1_CH4
6	IO5	5	MTDI	ADC2_CH0

5 RF Characterization

5.1 Wi-Fi Performance

Table 5-1 Module Wi-Fi RF parameters

parameters	element	
frequency range	2400MHz ~ 2483.5MHz (2.4GHz ISM Band)	
operating channel	2.4GHz: Ch1 ~ Ch13	
modulation method	802.11b	DQPSK, DBPSK, CCK
	802.11g/n (OFDM)	64-QAM, 16-QAM, QPSK, BPSK
output power	802.11b @ 1Mbps	19.5dBm @ EVM≤ -10.5dB
	802.11b @11Mbps	19.5dBm @ EVM ≤ -15.5dB
	802.11g @ 6Mbps	19.5dBm @ EVM ≤ -5dB
	802.11g @ 54Mbps	18dBm @ EVM ≤ -25dB
	802.11n @ MCS0 (20MHz)	18dBm @ EVM ≤ -5dB
	802.11n @ MCS7 (20MHz)	17dBm @ EVM ≤ -27dB
frequency offset	± 25ppm	
Receive Sensitivity (11b, 20MHz) @ 8% PER	1Mbps	PER @ -97dBm, typical
	11Mbps	PER @ -88dBm, typical
Receive sensitivity (11g, 20MHz) @ 10% PER	6Mbps	PER @ -92dBm, typical
	54Mbps	PER @ -75dBm, typical
Receive sensitivity (11n, 20MHz) @ 10% PER	MCS0	PER @ -91dBm, typical
	MCS7	PER @ -72dBm, typical
Neighbor Channel Suppression	802.11g @ 6Mbps	31dB, typical
	802.11g @ 54Mbps	20dB, typical
	802.11n @ HT20, MCS0	31dB, typical
	802.11n @ HT20, MCS7	16dB, typical

note

The test module is powered by 3.3V and tested in 25° C environment.

5.2 Bluetooth Low Energy (BLE) RF Performance

Table 5-2 Module BLE RF Performance

parameters	element
Bluetooth standard	Bluetooth 5 (LE)
frequency range	2402MHz ~ 2480MHz
operating channel	LE: Ch0 ~ Ch39
modulation method	GFSK
RF transmitter power	20.5dBm, typical
Gain control step	3dB, typical
RF Power Control Range	-24 ~ +21 dBm
Receive sensitivity @ PER=30.8%, LE(1Mbps)	-95dBm, typical
Receive sensitivity @ PER=30.8%, LE(2Mbps)	-94dBm, typical
Maximum Received Signal @ PER=30.8%, LE(1Mbps)	0dBm

note

The test module is powered by 3.3V and tested in 25° C environment.

5.3 Antenna area headroom design points

When designing the FB82 module with on-board antenna on the board, attention should be paid to the layout of the module on the bottom board, and the influence of the bottom board on the performance of the PCB antenna of the module should be minimized. It is recommended to place the module as close as possible to the edge of the baseboard, and if possible, the PCB antenna area should be extended out of the baseboard frame, and make the antenna's feed point the closest to the edge of the half. If there is a bottom plate under the antenna area, make sure to cut it off to minimize the impact of the bottom plate; make sure that the interfering signal alignments (e.g., USB, LCD, camera, power inductors

and crystals, etc.) and apertures are kept away from the antenna by at least 10 mm; if there is a metal casing and a high device height of the components near the antenna area of the module, it should be kept at a distance of more than 10 mm away from the antenna area; and when the whole machine design is involved, the device casing should be kept away from the antenna area by at least 10 mm. When the whole machine is designed, the device shell (especially the material around the antenna) should be made of non-metallic material, and at least 3 mm distance should be kept between the antenna and the shell, and please pay attention to consider the influence of the shell on the antenna. In Fig. 5.1, positions (3) and (4) of the module on the base plate are strongly recommended, positions (1), (2) and (6) are not recommended, and position (5) is prohibited; the base plate will greatly attenuate the antenna's radiating capability if the module antenna area is not cleared.

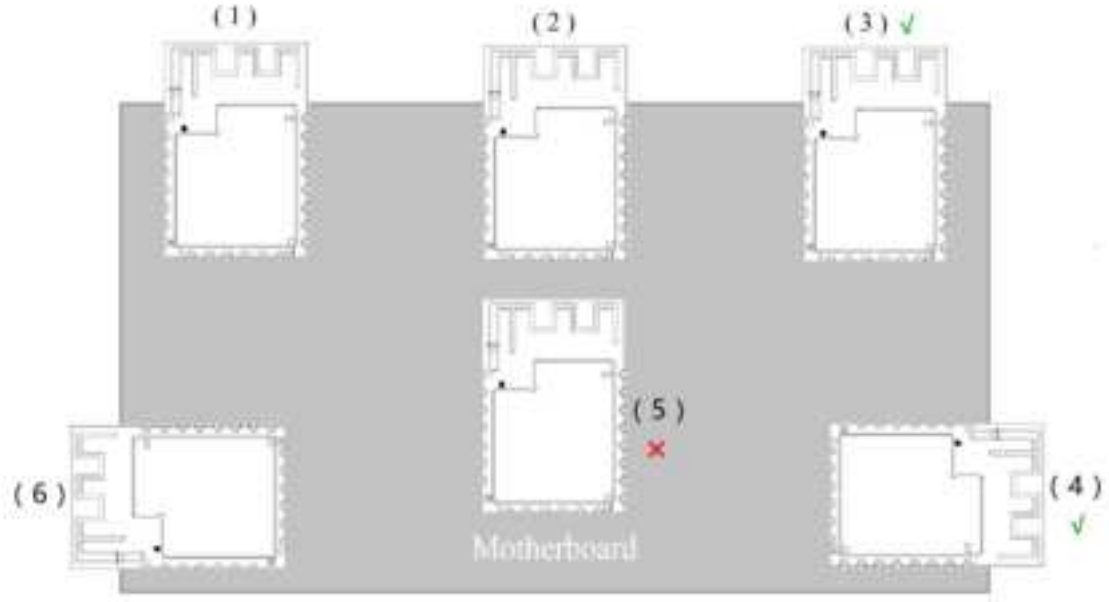

Figure 5.1 Schematic of the position of the FB82 module with on-board antenna on the base plate

If the above method is limited to the ideal situation, please make sure that the module is not wrapped by any metal casing, and the module PCB antenna area and the 15mm outward expansion area must be strictly clear, as shown in Figure 5.2:

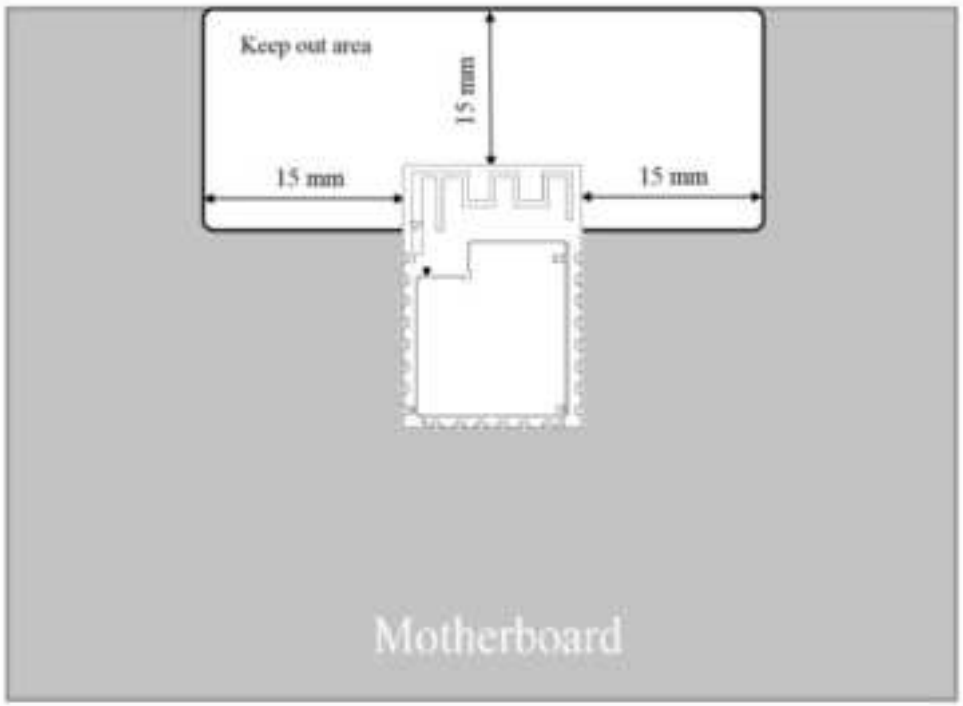

Figure 5.2 Schematic of antenna area clearances

5.4 RF Test Description

Users in the production of RF conduction test prototype, the module on the antenna matching must be disconnected, and the test Cable line soldered to the back of the module on the RF_PAD; due to the existence of the chip platform power self-calibration mechanism, so the test must be connected to the Cable line to the test instrument (to ensure that the RF port end of the 50 Ω characteristics of the impedance load) and then power on the module, otherwise it will be anomalous self-calibration power or Otherwise, the power self-calibration will be abnormal or the EVM will be poor.

RF test requires users to burn special RF test firmware for the module, including signaling and non-signaling test firmware for Wi-Fi & BT, etc. Leerink can provide the corresponding test guide, welcome to contact us for more information.

5.5 Baseboard Layout Considerations

FB82 series module BOTTOM layer no high-speed signals or sensitive signal

alignment, but it is still recommended that the bottom of the TOP layer design alignment to avoid the module, so as not to bring unexpected factors of influence.

There is no excessive hollow out processing requirements in the base plate design, in addition to the antenna area headroom requirements mentioned in section 5.3, the base plate can almost do the whole board to lay copper, but must pay attention to the module BOTTOM layer of the test spot soldering disk due to the open window exposed copper, need to do to avoid the processing of the corresponding position of the base plate can not be placed in the over-hole or exposed copper, and should be added to cover the solder resisting oil, to prevent the short connection. fb82 series module The BOTTOM layer is shown in Figure 5.3:

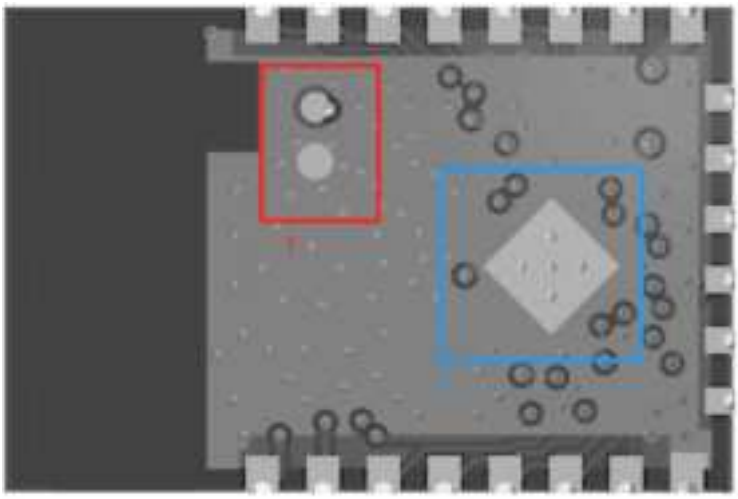

Figure 5.3 Schematic diagram of the copper exposed area in the BOTTOM layer of the FB82 series module with open window

The red box labeled area 1 within the open window exposed copper points for RF test points, mapped to the bottom of the board area of the location must not have any alignment or exposed copper.

Green box labeled area 2 for the module back chip below the heat dissipation pad EXPAD (connected to GND), it is recommended that the corresponding position in the base plate for similar open window exposed copper processing, and as much as possible to play the ground holes, so that the exposed copper area and other layers of the ground plane is

fully connected to enhance the thermal conductivity; and connected to the same layer of the ground plane of the copper laying can not choose the way of the cross-connections (should be Direct), the effect of the cross connection as shown in Figure 5.4. Connect), the effect of the cross connection as shown in Figure 5.4, the heat will accumulate in the middle of the copper block through conduction, resulting in high local temperatures; in addition, it should be noted that the exposed copper area generally can not be tin, but the right amount of tin to optimize the heat conduction effect of the substrate (too much tin may lead to the module solder paste when the floating height of the virtual welding, as well as the leakage of tin through the holes, etc.): If the EXPAD for the whole piece of rectangular If the EXPAD for the whole rectangular window mode, the hole must do half plug hole processing, so as to avoid tin leakage; a more recommended way to optimize the bottom of the board on the EXPAD into a nine-grid way, as shown in Figure 5.5, the gap in the cover ink, and the ground hole in the gap, which can effectively improve the problem of tin leakage.

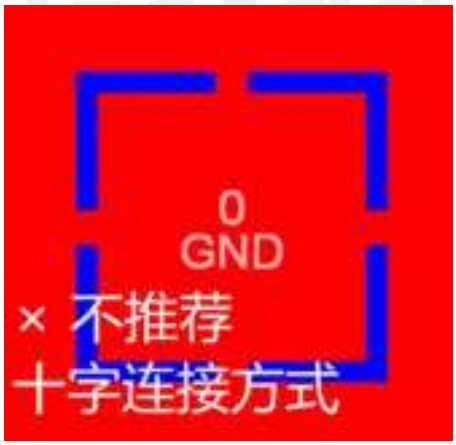

Figure 5.4 Unrecommended Copper Laying Connection

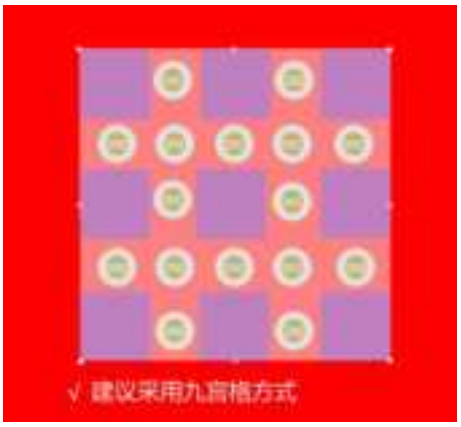

Figure 5.5 Nine-grid approach for the baseboard EXPAD

6 Electrical performance and reliability

6.1 Absolute maximum rating

Exceeding the absolute maximum rating may result in permanent damage to the device.

Table 6-1 Pin Voltage Maximum Ratings

Pin Type	minimum value	maximum values	unit (of measure)	note
V_{DD}	-0.3	3.6	V	Power Supply Pin Voltage
T_{Store}	-40	+105	℃	Storage temperature(1)

(1)This storage temperature range, excluding packaging materials, requires attention to the maximum temperature tolerance of tape and reel packaging.

6.2 Power supply ratings

Table 6-2 Operating Voltage Range

parameters	minimum value	typical value	maximum values	unit (of measure)	note
V_{DD}	+3.0	+3.3	+3.6	V	Supply Voltage(1)
I_{VDD}	0.5	-	-	A	Supply current from external power supply(2)
T_A	-40	+25	+105(3)	℃	Recommended working environment

(1)When the module operates within this voltage range, the relevant performance of the module meets the requirements of the IEEE 802.11 standard.

(2)It is required that the power supply has a through-current capability of 500mA or more, otherwise the values of individual metrics, such as transmit power, EVM rate, and other parameters, may be out of range of the IEEE 802.11 standard.

(3)If the module completes power-on self-calibration in a higher temperature (e.g., 85~105 ° C) environment, the associated performance may exceed the IEEE 802.11 standard requirements.

6.3 DC Gas Characteristics

TABLE 6-3 Module DC Gas Characteristics

notation	descriptive	minimum	typical	maximum	unit (of
V_{IL}	Low Level Input Voltage	-0.3	-	0.25 x VDD	V
V_{IH}	High Level Input Voltage	0.75 x VDD	-	VDD+0.3	V
I_{IL}	Low Level Input Current	-	-	50	nA
I_{IH}	High Level Input Current	-	-	50	nA
V_{OL}	Low Level Input Voltage	-	-	0.1×VDD	V
V_{OH}	High Level Output Voltage	0.8×VDD	-	-	V
R_{PU}	Internal pull-up resistor	-	45	-	KΩ
R_{PD}	Internal pull-down resistor	-	45	-	KΩ
V_{IH_nRST}	Chip Reset Release Voltage	0.75 x VDD	-	VDD+0.3	V
VIL_nRST	EN (corresponding to CHIP_EN of the IC) Turn off the chip's low-level input voltage	-0.3	-	0.25 x VDD	V
T_A	operating temperature	-40	-	+105	℃

6.4 Description of Power Consumption

TABLE 6-4 Description of Module RF Power Consumption

descriptive		TX Current (typical values)	RX Current (typical
Wi-Fi	802.11b, 11 Mbps @ 20dBm, 100% duty cycle	360mA	70mA
	802.11g, 54 Mbps @ 18dBm, 100% duty cycle	290mA	
	802.11n, HT20, MCS7 @ 18dBm, 100% duty cycle	270mA	
BLE	BLE 1M @ MAX power (21dBm)	370mA	

note

(1) Test conditions: VDD: 3.3V, Temp: 25° C, Product: L-WFIFB82-G5PP4.

(2) This power consumption data may vary under different firmware versions, subject to physical testing.

(3) There are more significant fluctuations in the operating current in Wi-Fi TX mode.

TABLE 6-5 Module Low Power Performance

paradigm		typical	unit (of	Module Status
Deep sleep		4.64	μA	deep sleep
Modem sleep	Dtim 1	3.02	mA	Expected sleep time is 100ms
	Dtim 3	1.54		Expected dormancy time is 300
	Dtim 5	1.30		Expected sleep time is 500ms
	Dtim 10	1.19		Expected sleep time is 1000ms
	Dtim 30	1.06		Expected sleep time is 3000ms

note

(1) Test conditions: VDD: 3.3V, Temp: 25° C, Product: L-WFIFB82-G5PP4.

(2) This power consumption data may vary under different firmware versions, subject to physical testing.

6.5 electrostatic protection

In module applications, static electricity generated by human body static electricity, charged friction between microelectronics, etc., discharged to the module through various ways, may cause some damage to the module. Therefore, ESD protection should be emphasized. In the process of research and development, production, assembly and testing, especially in product design, should take ESD protection measures. For example, in the circuit design of the interface and susceptible to electrostatic discharge damage or impact of the point, should increase the anti-static protection; test equipment to ensure good grounding; production should wear anti-static gloves and so on.

Table 6-6 Pin ESD Ratings

Test Port Type	descriptive	contact discharge	unit (of measure)	test standard
Power Pins	Power port and ground	±4	KV	IEC 61000-4-2
RF port	antenna port	±3	KV	

7 Mechanical dimensions

7.1 Mechanical dimensions

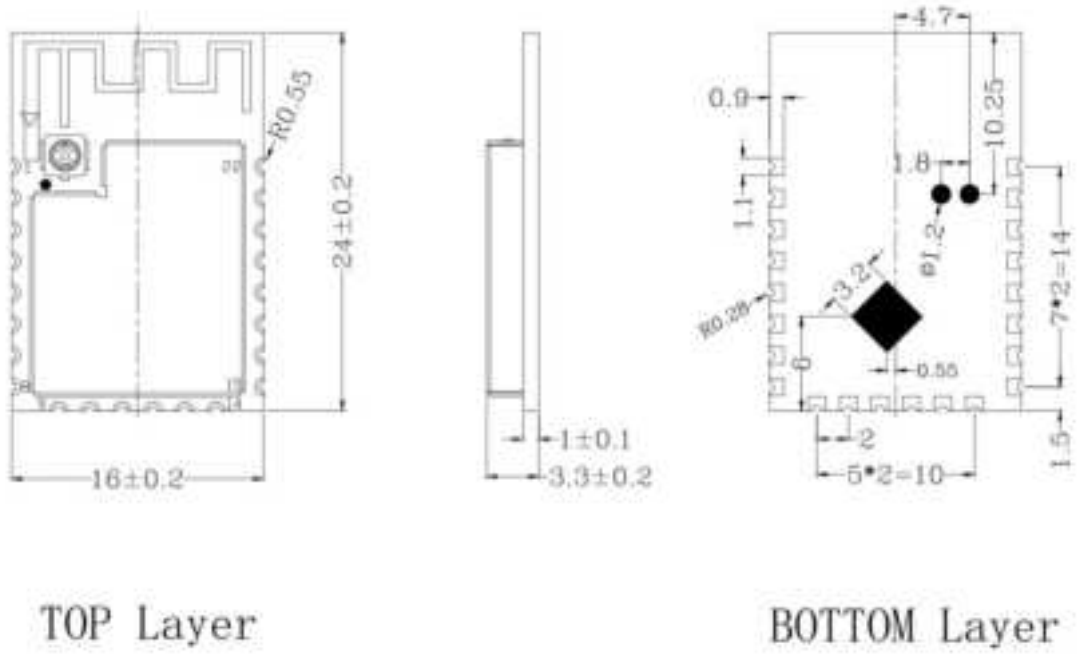

Figure 7.1 Dimensional drawing of the module

7.2 Recommended Packaging

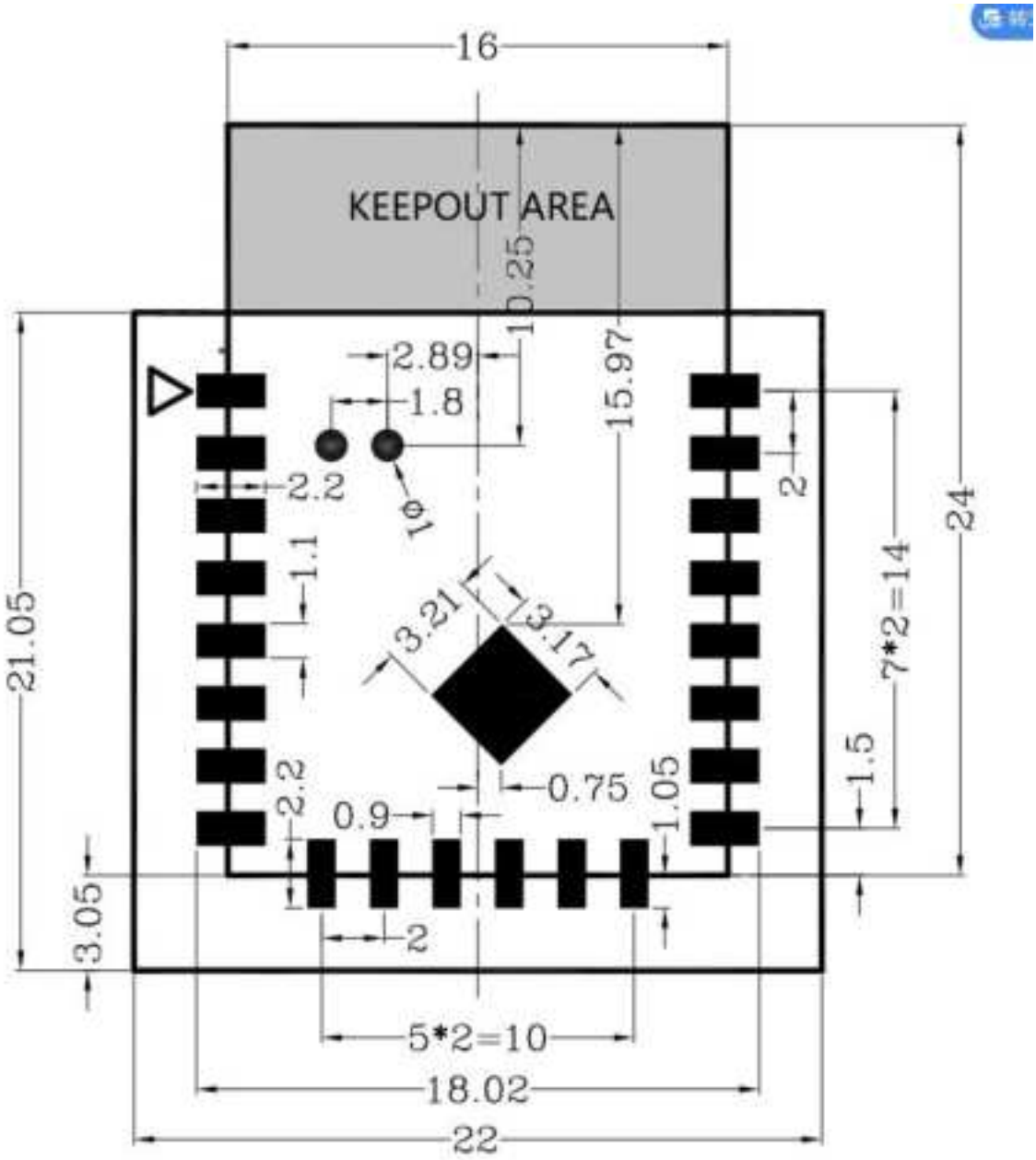

Figure 7.2 PCB Recommended Package

8 Production and Packaging Information

This chapter describes guidance information on packaging, storage, production, and maintenance of modules, and applies to guidance on the assembly process of modules.

8.1 Packaging specification

8.1.1 Packaging

Table 8-1 Module Tape and Reel Packaging Information

model number	Packaging	Full Carton(PCS)	Maximum Package Quantity (PCS)	Number of reels per case
L-WFIFB82-G5PP4	reel	3750	750	5

8.1.2 Belt size and product orientation

Tape and Reel Packaging Module Placement Orientation Schematic: (Reference diagram, label content is subject to actual, note module PIN1 position)

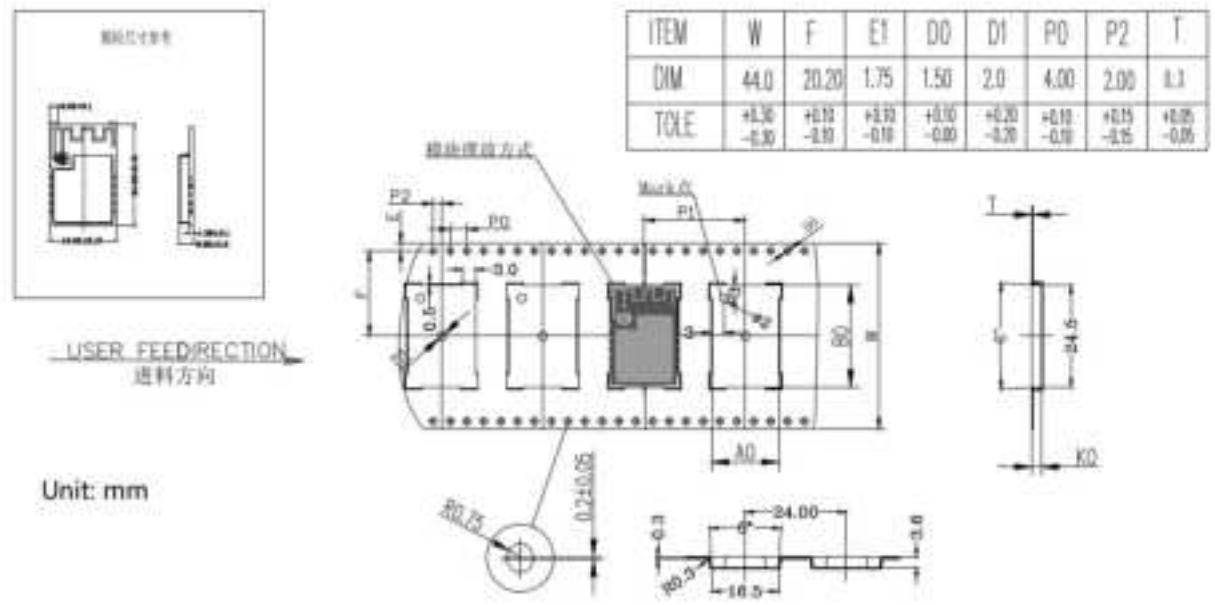

Figure 8.1 Package specifications and dimensions

8.2 storage condition

Modules are shipped in vacuum reel sealed bags with a moisture sensitivity rating of MSL 3.

Storage conditions:

(1) Temperature less than 40°C, humidity less than 90% (RH), and weldability is ensured for 12 months in a well sealed package.

(2) After unpacking, ensure patch assembly within 168 hours at an ambient temperature of less than 30°C and relative humidity of less than 60% (RH).

Baking is required if the above conditions are not met:

(1) Packed in tape and reel, baked at 60℃±5℃ for 24~48 hours.

(2) If accelerated baking is required, the module needs to be removed from the tape and placed on a high-temperature resistant container (e.g., tray) for baking (the removal process needs to pay attention to ESD protection) for 8 hours at 125°C ± 5°C.

(3) The cumulative baking time cannot exceed 96 hours.

Refer to the IPC/JEDECJ-STD-033 specification for more detailed guidance.

8.3 Production Welding

8.3.1 Overfurnace method

If the base plate of the module used by the customer is double-sided, it is recommended that the module be placed on the second patch. The first patch customer's base plate is best in the mesh belt over the furnace, the second patch also try to put on the mesh belt over the furnace, if for special reasons can not be put on the mesh belt over the furnace, but also consider the use of fixtures in the track over the furnace or pad a flat high-temperature straight template to hold the PCBA over the furnace to prevent deformation of the PCB over the furnace, resulting in the module of the virtual soldering.

8.3.2 Module location requirements at the base plate

It is recommended that the base plate module location of the green oil thickness of less than 0.02mm, to avoid excessive thickness, padding module can not effectively contact with the solder paste affects the welding quality. Also need to consider the interface board module location within 2mm around the layout of other devices, in order to protect the maintenance of the module.

8.3.3 Stencil opening design

The thickness of the stencil on the base plate is selected in principle according to the type of packaging of the device on the board to be selected, need to focus on the following requirements:

Module pad locations can be locally thickened to 0.15~0.20mm to avoid void soldering.

8.3.4 Production Precautions

- During the production process, each operator must wear electrostatic gloves;
- Baking should not exceed the specified baking time;
- It is strictly prohibited to add explosive, flammable and corrosive substances during baking;
- During baking, modules should be placed in high temperature trays to maintain air circulation between modules;
- The door of the baking box needs to be closed during baking to ensure that the baking box is closed and to prevent the temperature from leaking out;
- Try not to open the door when the oven is running, if you have to open it, try to shorten the time you can open the door;
- After baking, wait until the module cools down naturally to below 36℃ before taking it out with static gloves to avoid burns;
- When operating, do not allow the bottom surface of the module to get wet or dirty.

8.3.5 Reflow soldering instruction

Note: This work instruction is suitable for lead-free work only and is for reference only.

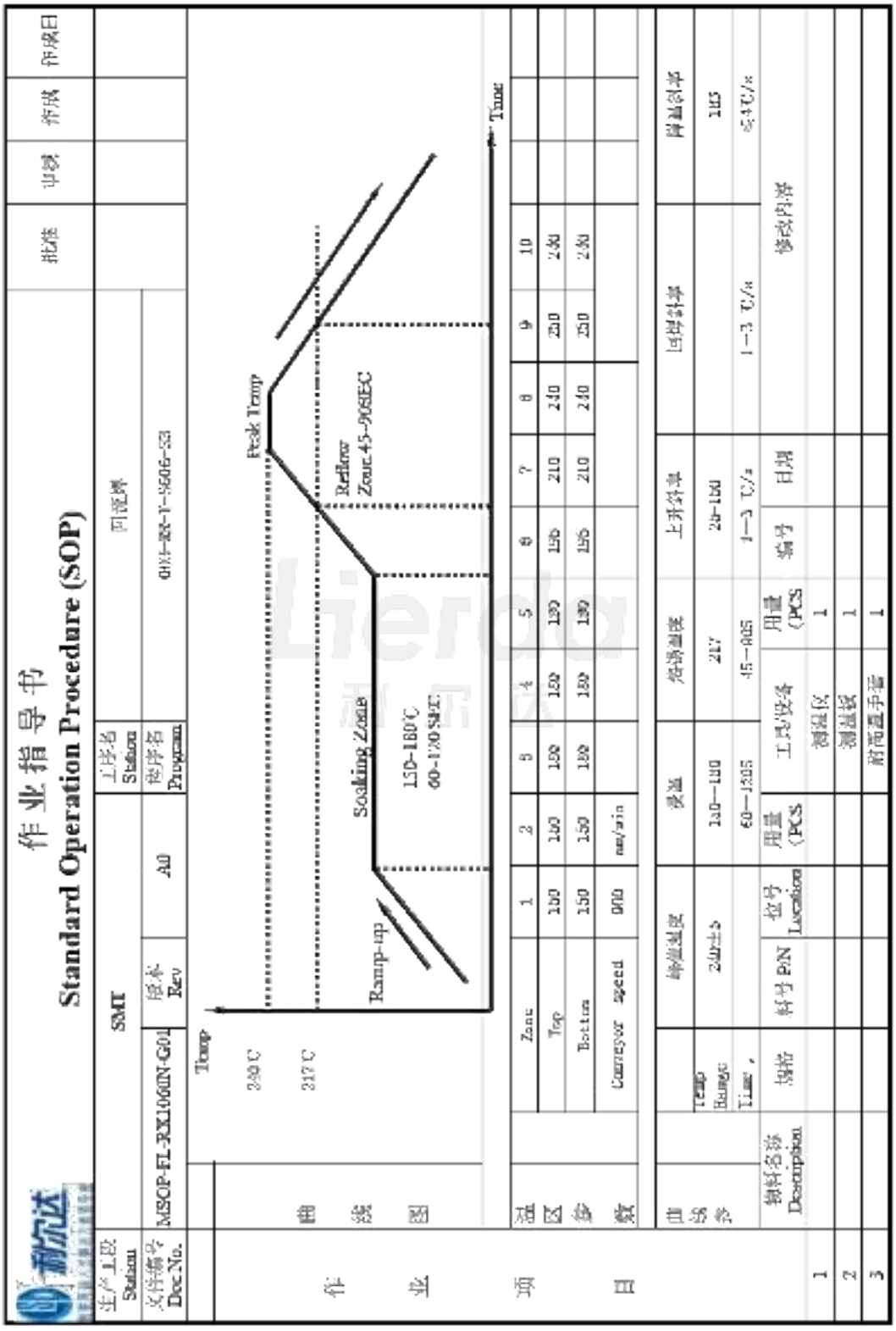

Figure 8.2 Reflow Soldering Operating Instructions

8.3.6 Production process

Do not use any organic solvents (e.g., alcohol, isopropyl alcohol, acetone, trichloroethylene, etc.) to wipe the module shield during production soldering or any other process that may directly contact the module; otherwise, the shield may rust.

If spraying or gluing of the module is required, please make sure that the spraying or gluing material used will not react chemically with the module shield or PCB, and that the spraying or gluing material will not flow into the module.

8.3.7 protect and maintain

If the module needs to be repaired due to defective soldering, shorting, etc., please follow the parameters below:

Lead-free process: soldering iron temperature 380 ± 10 ℃, soldering iron contact time ≤ 5S;

Leaded process: soldering iron temperature 350±10℃, soldering iron contact time ≤5S;

Modules are not recommended to be blown with a hot air gun to avoid affecting module performance.

9 Related Documents and Abbreviations

The following related documents provide the name of the document, please refer to the latest release for the version.

Table 9-1 Related Documents

serial number	document name	marginal notes
[1]	ESP8684_DATASHEET	ESP8684 datasheet
[2]	ESP8684_TECHNICAL_REFERENCE_MANUAL	ESP8684 Technical Manual
[3]	IEC61000-4-2 standard	
[4]	IPC/JEDECJ-STD-033 specification	

Table 9 -Table 9 2 Terminology Abbreviations

abridge	Full name in English	Full name in Chinese
IoT	Internet of Things	Internet of Things (IoT)
IEEE	Institute of Electrical and Electronics Engineers	Institute of Electrical and Electronics Engineers
MAC	Media Access Control	MAC
ISM band	Industrial Scientific Medical Band	Industrial, scientific and medical bands
GPIO	General-purpose input/output	General purpose inputs and outputs
I/O	Input/Output	input-output (interface)
SPI	Serial Peripheral Interface	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter	Universal Asynchronous Transceiver
I2C	Inter-Integrated Circuit	internal integrated circuit
LED PWM	Light Emitting Diode Pulse Width Modulation	Light Emitting Diode Pulse Width Modulation
DMA	Direct Memory Access	direct memory access
SAR ADC	Successive Approximation Register Analog-to-Digital Converter	Successive Approximation Analog-to-Digital Converter
TXD	Transmit external Data	dispatch

RXD	Receive external Data	reception (of transmitted signal)
ECC	Elliptic Curves Cryptography	Elliptic curve encryption algorithm
Hash (SHA-2)	Hash (Secure Hash Algorithm 2)	Secure Hash Algorithm 2
REV	Reserve	reservations
bps	Bits Per Second	unit of speed
MCU	Mirco Controller Unit	microcontroller
CPU	Central Processing Unit	central processing unit (CPU)
RTC	Real Time Clock	real time clock
OFDM	Orthogonal Frequency Division Multiplexing	orthogonal frequency division multiplexing
CCK	Complementary Code Keying	Complementary code keying
PSK	Phase Shift Keying	phase shift keying
QPSK	Quadrature Phase Shift Keying	quadrature phase shift keying
BPSK	Binary Phase Shift Keying	binary phase shift keying
DQPSK	Differential Quadrature (Reference) Phase Shift Keying	Differential Quadrature Phase Shift Keying
DBPSK	Differential Binary (Coherent) Phase Shift Keying	Differential Binary Phase Shift Keying
QAM	Quadrature Amplitude Modulation	orthogonal amplitude modulation
EVM	Error Vector Magnitude	Vector amplitude error
PER	Packets Error Rates	mispacketization rate
GFSK	Gauss Frequency Shift Keying	Gaussian frequency shift keying
PCB	Printed Circuit Board	printed circuit board
RF	Radio Frequency	a radio frequency
ESD	Electro-Static discharge	electrostatic discharge
MSL	Moisture Sentivity levels	moisture sensitive
V_{IL}	Input Low Level Voltage Value	Low Level Input Voltage

V_{IH}	Input High Level Voltage Value	High Level Input Voltage
I_{IL}	Input Low Level Current Value	Low Level Input Current
I_{IH}	Input High Level Current Value	High Level Input Current
V_{OL}	Output Low Level Voltage Value	Low Level Input Voltage
V_{OH}	Output High Level Voltage Value	High Level Input Voltage
R_{PU}	Pull-up resistor value	Pull-up resistor resistance
R_{PD}	Pull-down resistor value	Pull-down resistor resistance

Federal Communication Commission (FCC) Radiation Exposure Statement

When using the product, maintain a distance of 20cm from the body to ensure compliance with RF exposure requirements.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

ORIGINAL EQUIPMENT MANUFACTURER (OEM) NOTES

The OEM must certify the final end product to comply with unintentional radiators (FCC Sections 15.107 and 15.109) before declaring compliance of the final product to Part 15 of the FCC rules and regulations. Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change.

The OEM must comply with the FCC labeling requirements. If the module's label is not visible when installed, then an additional permanent label must be applied on the outside of the finished product which states: "Contains transmitter module FCC ID: 2AOFDL-WFIFB82. Additionally, the following statement should be included on the label and in

the final product's user manual: "This device complies with Part 15 of the FCC Rules. Operation is subject to the following

two conditions: (1) This device may not cause harmful interferences, and

(2) this device must accept any interference received, including interference that may cause undesired operation."

The module is allowed to be installed in mobile and portable applications A module or modules can only be used without additional authorizations if they have been tested and granted under the same intended end - use operational conditions, including simultaneous transmission operations. When they have not been tested and granted in this manner, additional testing and/or FCC application filing may be required. The most straightforward approach to address additional testing conditions is to have the grantee responsible for the certification of at least one of the modules submit a permissive change application. When having a module grantee file a permissive change is not practical or feasible, the following

guidance provides some additional options for host manufacturers. Integrations using modules where additional testing and/or FCCapplication filing(s) may be required are: (A) a module used in devices requiring additional RF exposure compliance information (e.g., MPE evaluation or SAR testing); (B) limited and/or split modules not meeting all of the module requirements; and (C) simultaneous transmissions for independent collocated transmitters not previously granted together.

This Module is full modular approval, it is limited to OEM installation ONLY. Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change. (OEM) Integrator has to assure compliance of the entire end product include the integrated Module. Additional measurements (15B) and/or equipment authorizations(e.g. Verification) may need to be addressed depending on co-location or simultaneous transmission issues if applicable.(OEM) Integrator is reminded to assure that these installation instructions will not be made available to the end user.