Revisions

Date	Rev	Description
June 28, 2005	0.0	Initial Release

P01_COVER_PAGE
P01_COVER_PAGE.sch

P02_POWER
P02_POWER.sch
- VREF
- PWR_RSTn
- DIN

P03_RTL8671_208
P03_RTL8671_208.sch
- RSTn
- EECS
- EEDO
- EEDI
- EESK
- NICLED2
- NICLED3
- MDIO
- MDC
- RXD3
- RXD2
- RXD1
- RXD0
- RXDV
- RXCLK
- TXCLK
- TXEN
- TXD0
- TXD1
- TXD2
- TXD3
- COL
- AD[0..31]
- PCI_CLK
- STOPBn
- INTABn
- PCI_RSTn
- IDSEL0
- GNTB0
- REQB0
- PAR
- DEVSELBn
- TRDYBn
- IRDYBn
- FRAMEBn
- BE3n
- BE2n
- BE1n
- BE0n
- PWR_RSTn
- SDRAM_CLK
- WEn
- CASn
- RASn
- MCS0n
- AA20
- MCS2n
- MCS3n
- DD[0..15]
- AA[0..20]
- PMEB
- TX3_AFE
- TX2_AFE
- TX1_AFE
- TX0_AFE
- CTRLIN_AFE
- CLKM_AFE
- CLWD_AFE
- RX3_AFE
- RX2_AFE
- RX1_AFE
- RX0_AFE
- POWDN_AFE
- VREF

P04_MEMORY&SETTING
P04_MEMORY&SETTING.sch
- MCS0n
- MCS2n
- NICLED3
- TX0_AFE
- NICLED2
- TX2_AFE
- CASn
- CTRLIN_AFE
- DD[0..15]
- SDRAM_CLK
- AA[0..20]
- RASn
- MCS3n
- AA20
- TX3_AFE
- WEn
- POWDN_AFE

P05_RTL8271_64
P05_RTL8271_64.sch
- CLKM_AFE
- RX2_AFE
- CLWD_AFE
- RX3_AFE
- TX3_AFE
- RSTn
- POWDN_AFE
- TX1_AFE
- TX2_AFE
- TX0_AFE
- RX0_AFE
- RX1_AFE
- CTRLIN_AFE
- DIN
- VREF

P06_8305SC
P06_8305SC.sch
- RSTn
- RDIN3
- RDIP3
- TDOP3
- TDON3
- RDIN2
- RDIP2
- TDOP2
- TDON2
- RDIN1
- RDIP1
- TDOP1
- TDON1
- RDIN0
- RDIP0
- TDOP0
- TDON0
- MDC
- MDIO
- TXD0
- TXD1
- TXD2
- TXD3
- TXEN
- TXCLK
- COL
- RXD0
- RXD1
- RXD2
- RXD3
- RXDV
- RXCLK
- ACT3_EN48P1
- ACT0_BCINDROP
- ACT1_GYSPD
- ACT2_P4ANEG

P07_8305SJX
P07_8305SJX.sch
- TDON3
- TDON1
- RDIP1
- RDIP3
- RDIN0
- TDON0
- TDOP2
- RDIP2
- RDIP0
- RDIN2
- TDOP3
- TDOP0
- RDIN1
- TDOP1
- ACT3_EN48P1
- ACT0_BCINDROP
- RDIN3
- TDON2
- ACT1_GYSPD
- ACT2_P4ANEG
- NICLED2
- NICLED3

P08_RTL8185
P08_RTL8185.sch
- DEVSELBn
- TRDYBn
- IRDYBn
- BE3n
- IDSEL0
- REQB0
- AD[0..31]
- STOPBn
- BE1n
- FRAMEBn
- BE0n
- PAR
- PCI_CLK
- PCI_RSTn
- BE2n
- INTABn
- GNTB0
- PMEB
- EEDO
- EESK
- EECS
- EEDI
- TRSW-
- TRSW+
- CALEN
- RIFSCK
- RFLE
- RIFSD
- TXQ+
- TXQ-
- TXI+
- TXI-
- RXI+
- RXI-
- RXQ+
- RXQ-
- RSSI
- TSSI0
- A_PAPE
- 40MHzOSC

P09_RTL8225
P09_RTL8225.sch
- TRSW-
- TRSW+
- A_PAPE
- TSSI0
- CALEN
- RIFSD
- RIFSCK
- RFLE
- 40MHzOSC

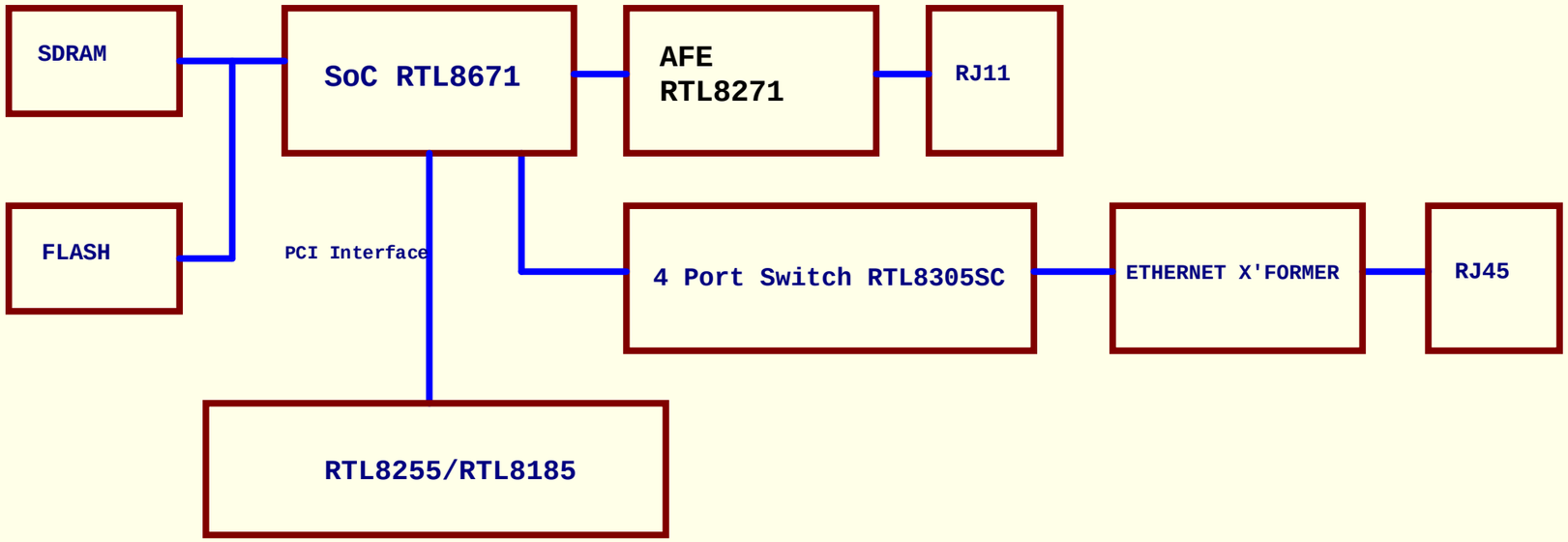
FMA1
FIDUCIAL MARK
FIDUCIAL-MARK

FMB1
FIDUCIAL MARK
FIDUCIAL-MARK

V115
2 — 1
NC/R/0603

Validity Date	FOXCONN	Title	REALTEK ADSL2+ & WIFI SOLUTION
		Doc .NO	T07L028T00
27-Feb-2006	REV: L0 / Rev. Note: / View:	Initial	Gary Yang
	PAGE: 1 of 10	Check	
		Approve	

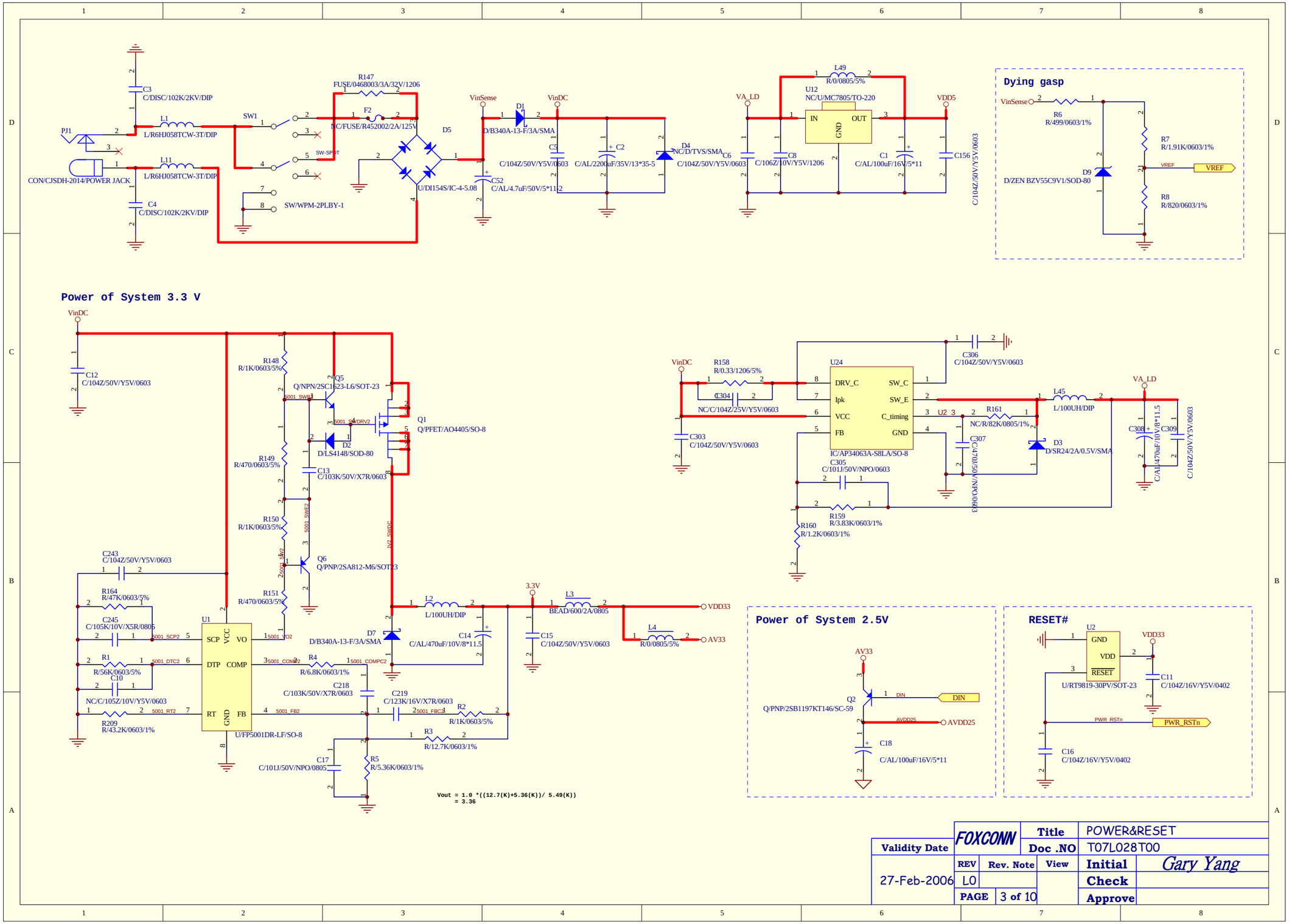
ADSL2+_4 Port Switch_WLAN



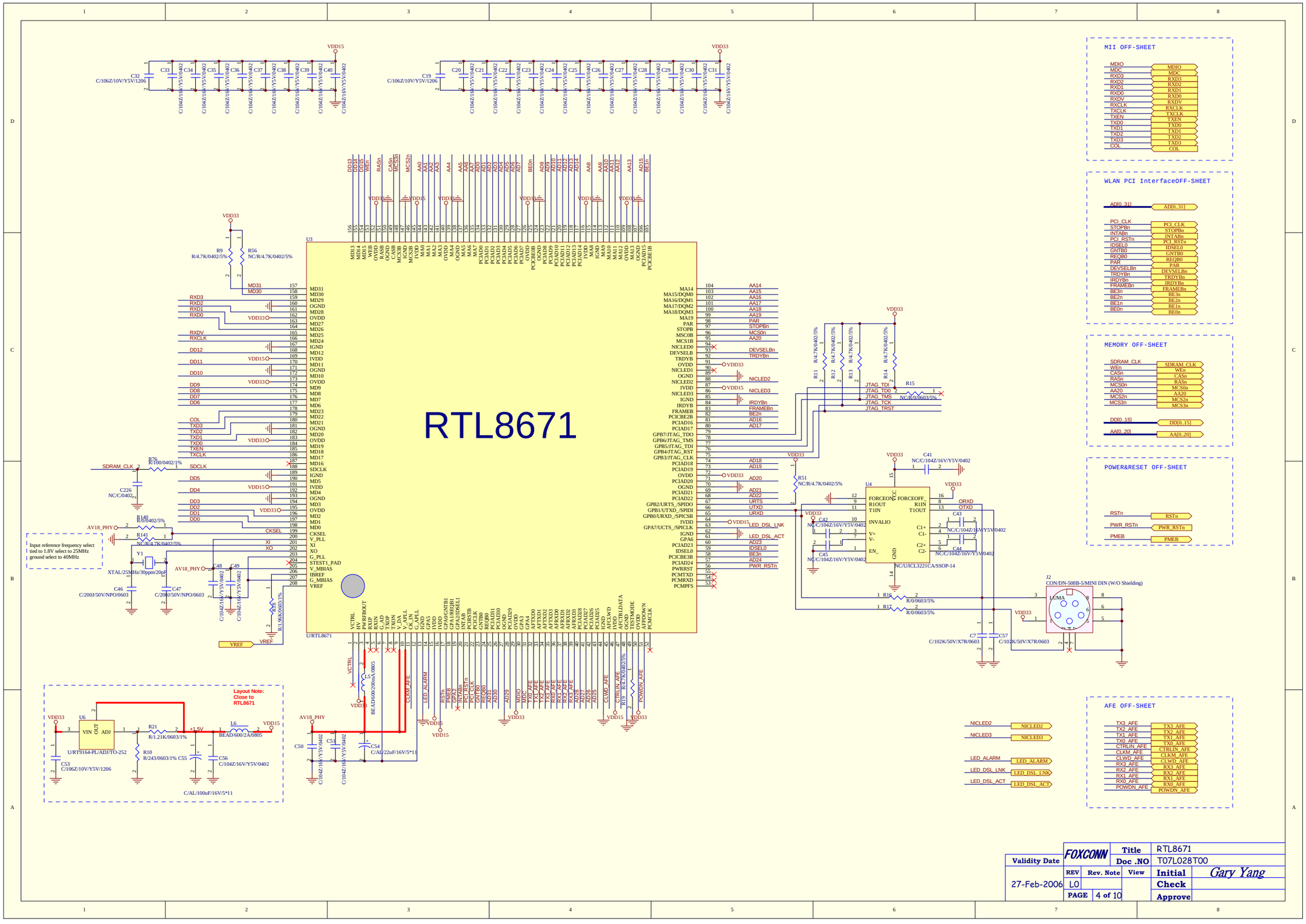
POWER

5V;3.3v;2.5V: for RTL8271
3.3V;1.5V: for RTL8671

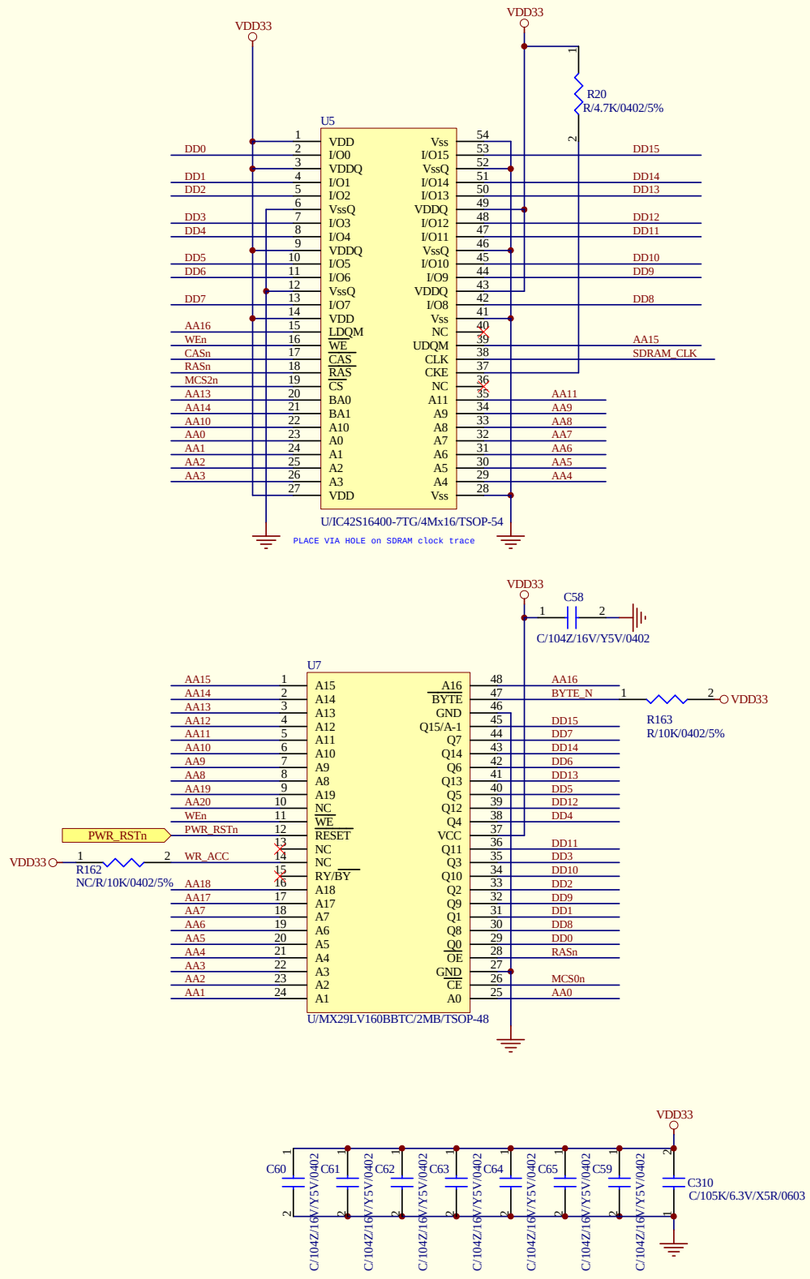
Validity Date	FOXCONN		Title	COVER PAGE	
			Doc .NO	T07L028T00	
27-Feb-2006	REV	Rev. Note	View	Initial	Gary Yang
	L0			Check	
	PAGE	2 of 10		Approve	



Validity Date	FOXCONN	Title	POWER&RESET	
		Doc .NO	T07L028T00	
27-Feb-2006	REV: L0	Rev. Note	View	Initial: Gary Yang
				Check
	PAGE: 3 of 10			Approve



Validity Date	FOXCONN	Title	RTL8671
		Doc .NO	T07L028T00
27-Feb-2006	REV L0	Rev. Note	View
	PAGE 4 of 10		Initial: Gary Yang
			Check
			Approve



SOC Mode

MCS3:0

R22 R/1K/0402/5% — 1 — 2 MCS3n

SDCLK ASYNC Mode

AFTXD0:0

R25 R/1K/0402/5% — 1 — 2 TX0_AFE

PCI as LXBUS in => No

AFPDOWN:0

R26 R/1K/0402/5% — 1 — 2 POWDN_AFE

TEST Mode => NO

AFCTRLDATA:0

R27 R/1K/0402/5% — 1 — 2 CTRLIN_AFE

SDRAM_CLOCK =>125Mhz

SDCLK_SEL[1:0]:00

R28 R/1K/0402/5% — 1 — 2 NICLED3

R29 R/1K/0402/5% — 1 — 2 NICLED2

BUS_CLOCK=>218Mhz

AFTXD[3:2]:11

VDD33 — R30 R/1K/0402/5% — 1 — 2 TX3_AFE

VDD33 — R31 R/1K/0402/5% — 1 — 2 TX2_AFE

Flash bus width
=>16 bits

MCS[1:0]:01

R23 R/1K/0402/5% — 1 — 2 AA20 MCS1#

VDD33 — R24 R/1K/0402/5% — 1 — 2 MCS0n

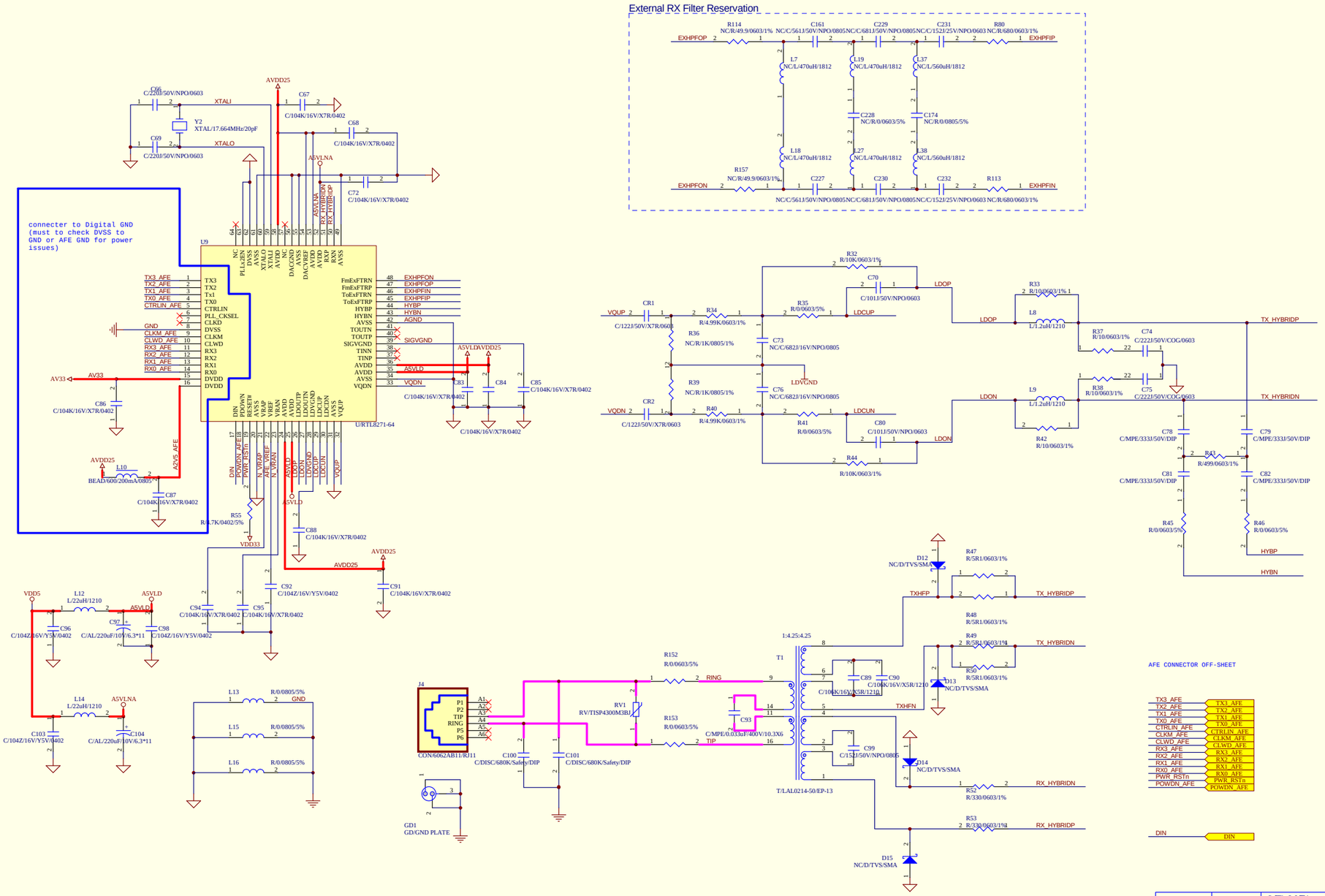
MEMORY OFF-SHEET

SDRAM_CLK	SDRAM_CLK
WEn	WEn
RASn	RASn
CASn	CASn
MCS0n	MCS0n
AA20 MCS1#	AA20
MCS2n	MCS2n
DD[0..15]	DD[0..15]
AA[0..20]	AA[0..20]

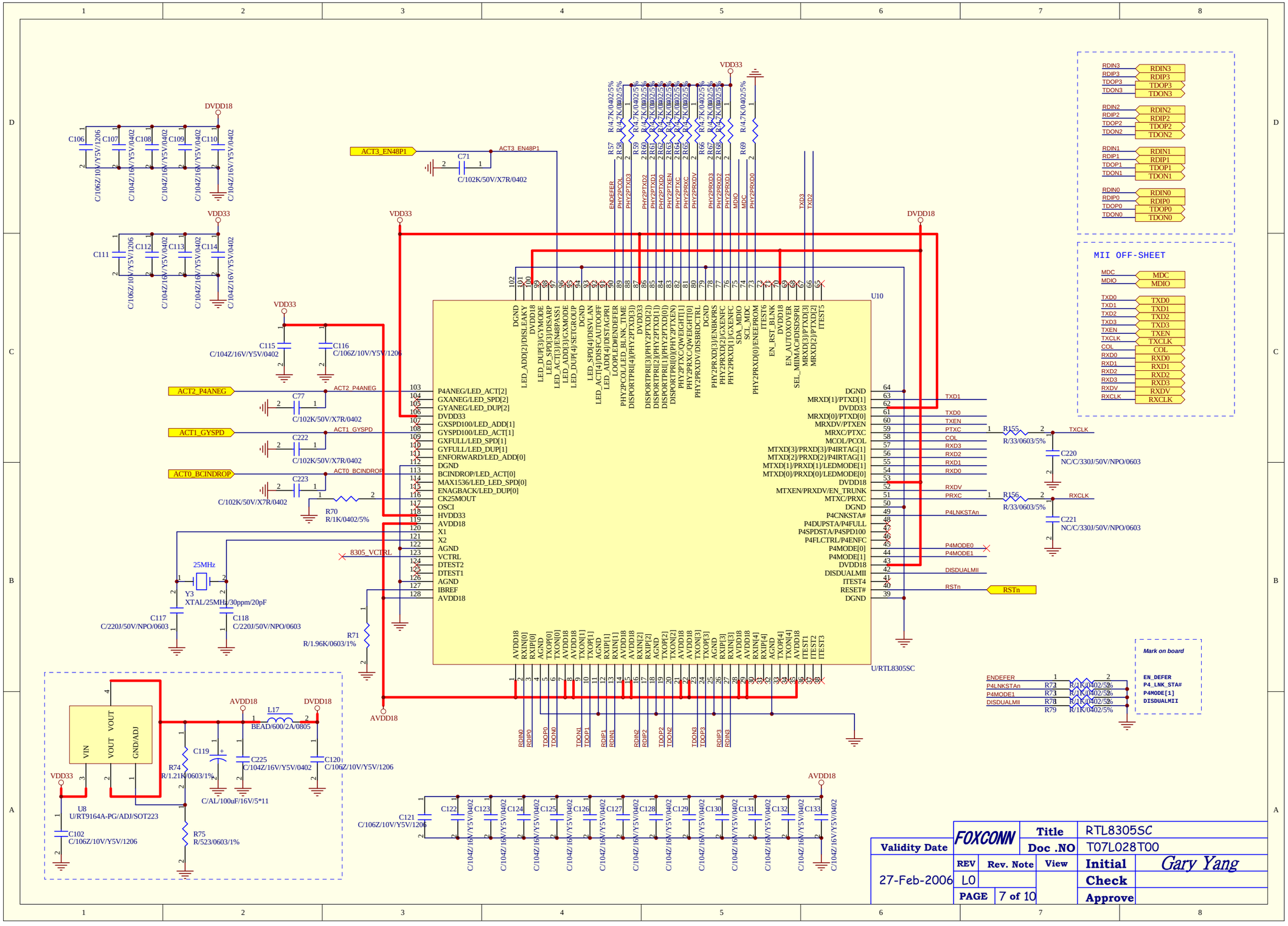
SETTING OFF-SHEET

TX0_AFE	TX0_AFE
TX2_AFE	TX2_AFE
TX3_AFE	TX3_AFE
CTRLIN_AFE	CTRLIN_AFE
POWDN_AFE	POWDN_AFE
MCS3n	MCS3n
NICLED3	NICLED3
NICLED2	NICLED2

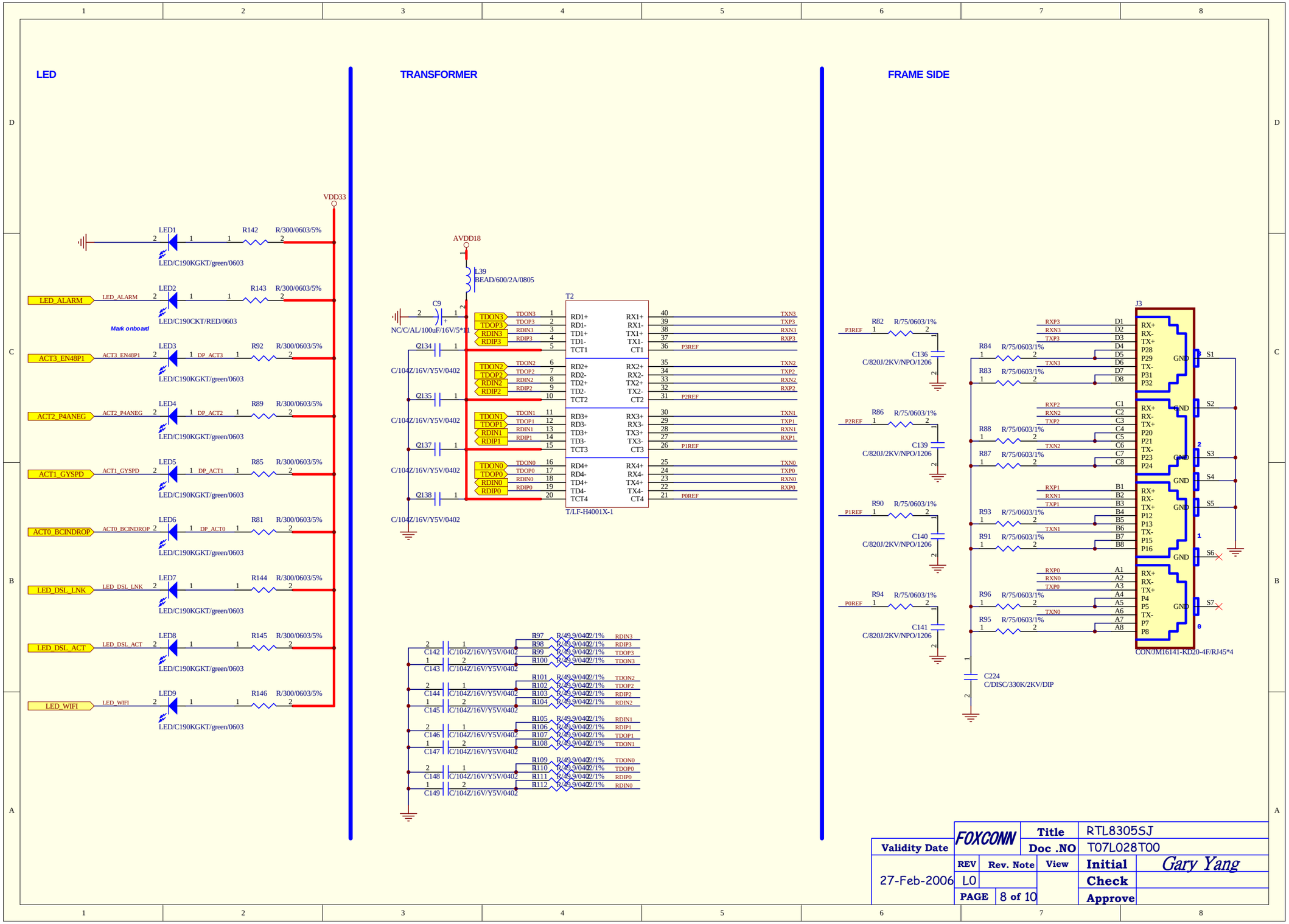
Validity Date	FOXCONN	Title	MEMORY&SETTING
		Doc .NO	T07L028T00
27-Feb-2006	REV L0	Rev. Note	View
	PAGE 5 of 10		Initial: Gary Yang
			Check
			Approve



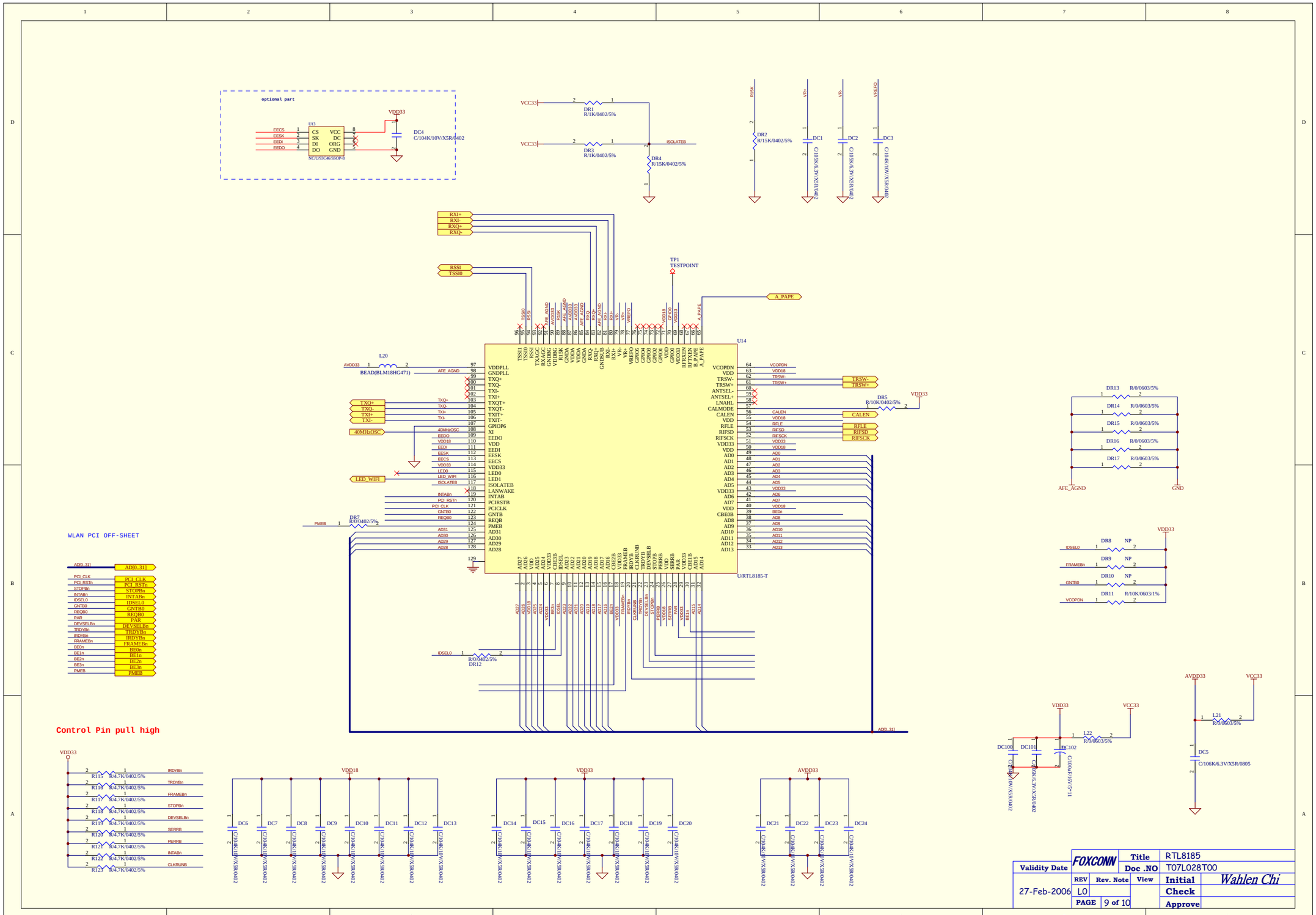
Validity Date	FOXCONN	Title	RTL8271
		Doc .NO	T07L028T00
27-Feb-2006	REV L0 / Rev. Note	View	Initial: Gary Yang
	PAGE 6 of 10		Check
			Approve



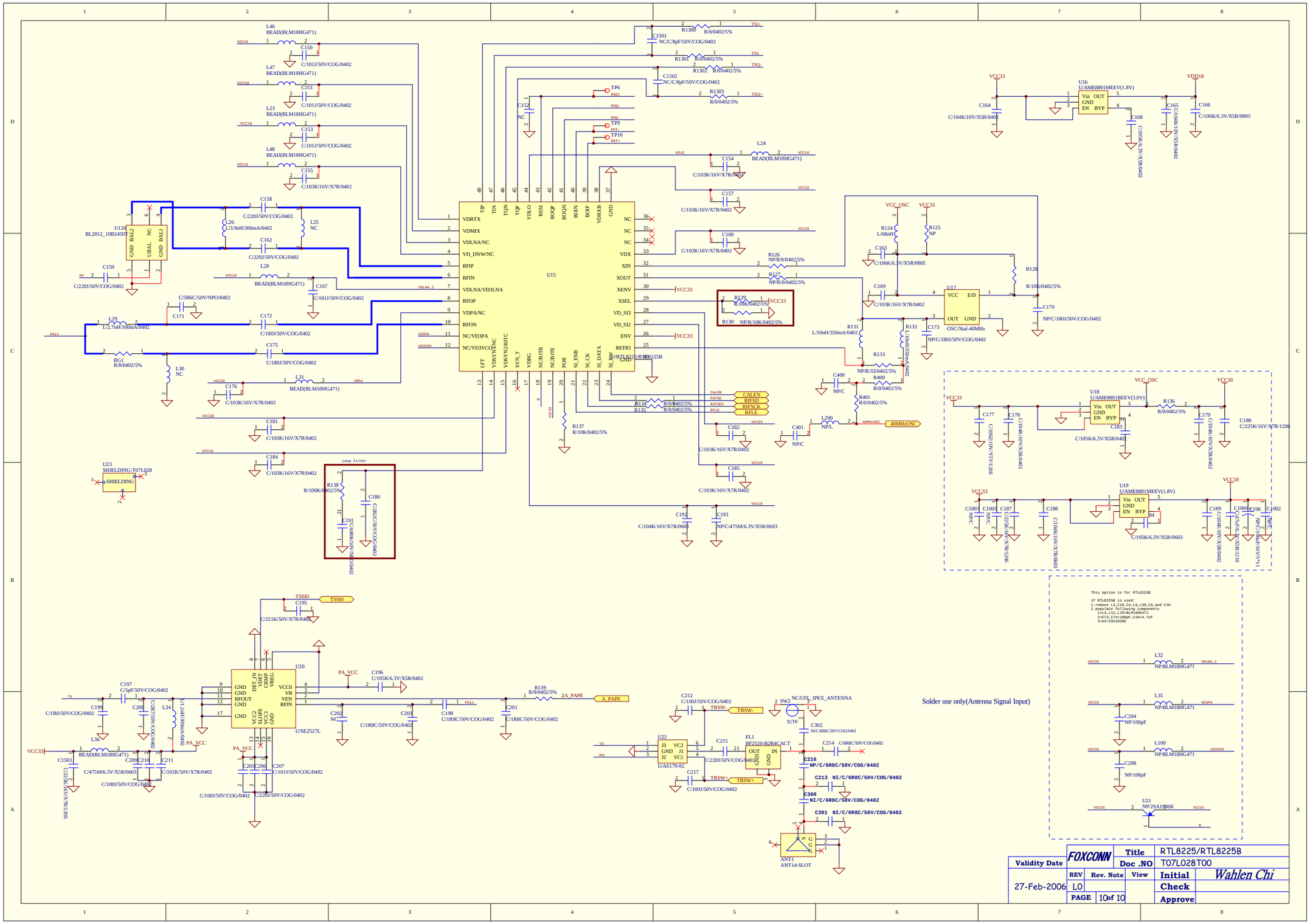
Validity Date	FOXCONN	Title	RTL8305SC
		Doc .NO	T07L028T00
27-Feb-2006	REV: L0	Rev. Note	View
	PAGE: 7 of 10		Initial: Gary Yang
			Check
			Approve



Validity Date	FOXCONN	Title	RTL8305SJ
		Doc .NO	T07L028T00
27-Feb-2006	REV L0 / Rev. Note / View	Initial	Gary Yang
		Check	
	PAGE 8 of 10	Approve	



Validity Date	FOXCONN	Title	RTL8185
		Doc .NO	T07L028T00
27-Feb-2006	REV L0 / Rev. Note	View	Initial: Wahlen Chi
	PAGE 9 of 10		Check
			Approve



Validity Date	FOXCONN	Title	RTL8225/RTL8225B
		Doc .NO	T07L028T00
27-Feb-2006	REV L0	Rev. Note	View
	PAGE 10 of 10		Initial: Wahlen Chi
			Check
			Approve