Processing gain of Direct Sequence Spread Spetrum

Product name: XI300 Wireless LAN PCMCIA card.
Tested by: Zcom, Inc.
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FCC requirements: The processing gain of a direct sequence system shall be at least 10dB. The processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal-to-noise ratio with the system spreading code turned on, as measured at the demodulated output of the receiver.

This document contains theoretical calculation and test setup, procedure, measurement data and report.

Test equipment:

Hp8593 Spectrum analyzer
Hp ESG D3000A signal generator
Hp4418A Power meter
Hp8493A attenuator 1dB steps
Hp8495D attenuator 10dB steps
Hp11636BB power spiltter
Notebook PC X2

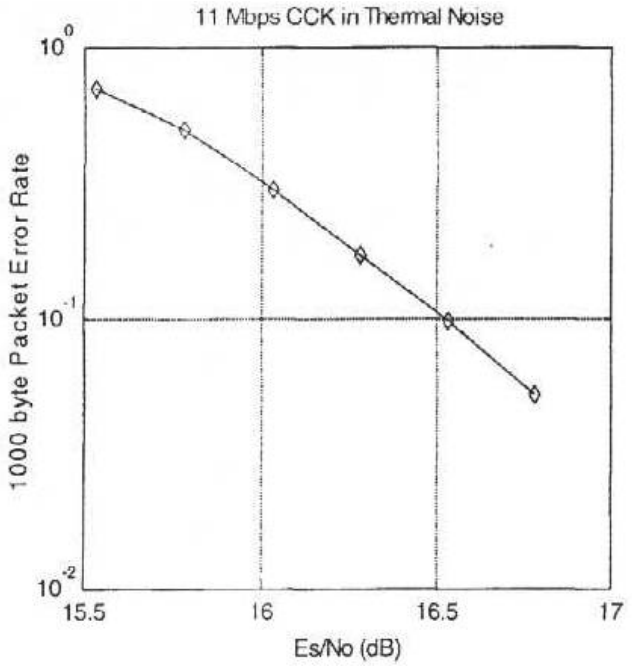
Theoretical calculation: The Processing gain is related to be jamming margin as follows:

$$Gp=(S/N)_{output} + (J/S) + L_{sys}$$

Where $BER_{reference}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin(jamming signal power relative to desired signal power), and L_{sys} is the system losses.

- For 5.5Mbps and 11Mbps case: The HFA 3861A direct sequence spread spectrum baseband processor use CCK modulation which is a form of M-ary Orthogonal Keying. The Probability of error for generalized M-ary orthogonal signaling using coherent demodulation is given by:

$$P_e=1-P_{c1}=1-\frac{1}{\sqrt{2\pi}}\int_{\frac{S_{01}}{N_o}}^{\infty}\left[2\left(1-Q\left\{z+\sqrt{2\frac{E_b}{\eta}}\right\}\right)\right]^{\frac{M}{2}-1} e^{\left\{-\frac{z^2}{2}\right\}}dz$$



So the FER performance curve is given by[1] as left graph:

Therefore:

Gp= (Es/No)o+ (J/S) + Lsys=16.4+2.0+(J/S)

Gp=18.4+(J/S) must >10dB

For the case of the HFA3861A, the bit rates are 1,2, 5.5 and 11Mbps. The corresponding symbol rates are 1, 1, 1.375 and 1.375 MSPS. The chip rate is always 11MCps, so the ratio of chip rate to symbol rate is 11.:1 for the1 and 2Mbps and 8:1 for 5.5 and 11Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain and coding are utilized. This is a reasonable in that they cannot be sperated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.

As can be seen from the curve of figure 1, the Es/No is 16.4dB at the PER of 8%. It is well know that the Eb/No of BPSK is 9.6dB for 1e-5BER, so therefore the coding gain of CCK over BPSK is 2.2dB. We add this to the processing gain of 9B to get 11.2dB overall processing gain for the CW jamming test.

Taking the calculation above, if the (J/S)>-8.4dB then the equipment passes the CW jamming test.

- For 1&2Mbps case: The modulation is either DBPSK or DQPSK for 1and 2Mbps. With differential coding, there is and error extension factor of 2 which from the fact that if one symbol is error, then the next will be demodulated in error too since it's phase is dependant on the change of phase from symbol to symbol. In DBPSK, this result is a simple factor of two in BER. With DQPSK, the picture is a little muddied in that a symbol error may cause one or two bit errors since two bits are carried per symbol. From the book of Fig.7.2, Viterbi, A.J. Principles of Coherent Communications, Page 192 (New York; McGraw-Hill, 1996), the Eb/No of BPSK is 9.6dB. When operating DQPSK at 2Mbps, the Eb/No remains essentially the same, but the Es/No goes up by 3dB. So the (S/N)o is 12.6.

Test procedure:

Obtain the simplex link shown. Perform all independent instrumentation calibration prior to this procedure. Set operating levels using fixed and variable attenuator in system to meet the following objectives:

1. Signal Power at receiver is approximately –60dBm.
2. Signal Power at power meter between –20 and –30dBm.
3. Use spectrum analyzer to monitor test.
4. Ensure that CW jammer generator RF output is disabled and measure the power at the power meter port using Hp4418B power meter. This is relative power, Sr.

5. Disable TX and set CW jammer output frequency equal to the carrier frequency and enable generator output. Set reference CW jammer power level at power meter port 8.4dB below Sr.
6. Disable CW jammer and re-establish Link. FER test should be essentially error free.
7. Enable the CW jammer at the reference power level and verify that FER at the reference power level and verify that FER test indicate less than 8%.
8. Alternatively, adjust the CW jammer level to that which causes 8% FER.
9. Repeat Step 7 for uniform steps in frequency increments of 50KHz across the receiver passband with the CW jammer. In this case, the receiver passband is ±8.5MHz

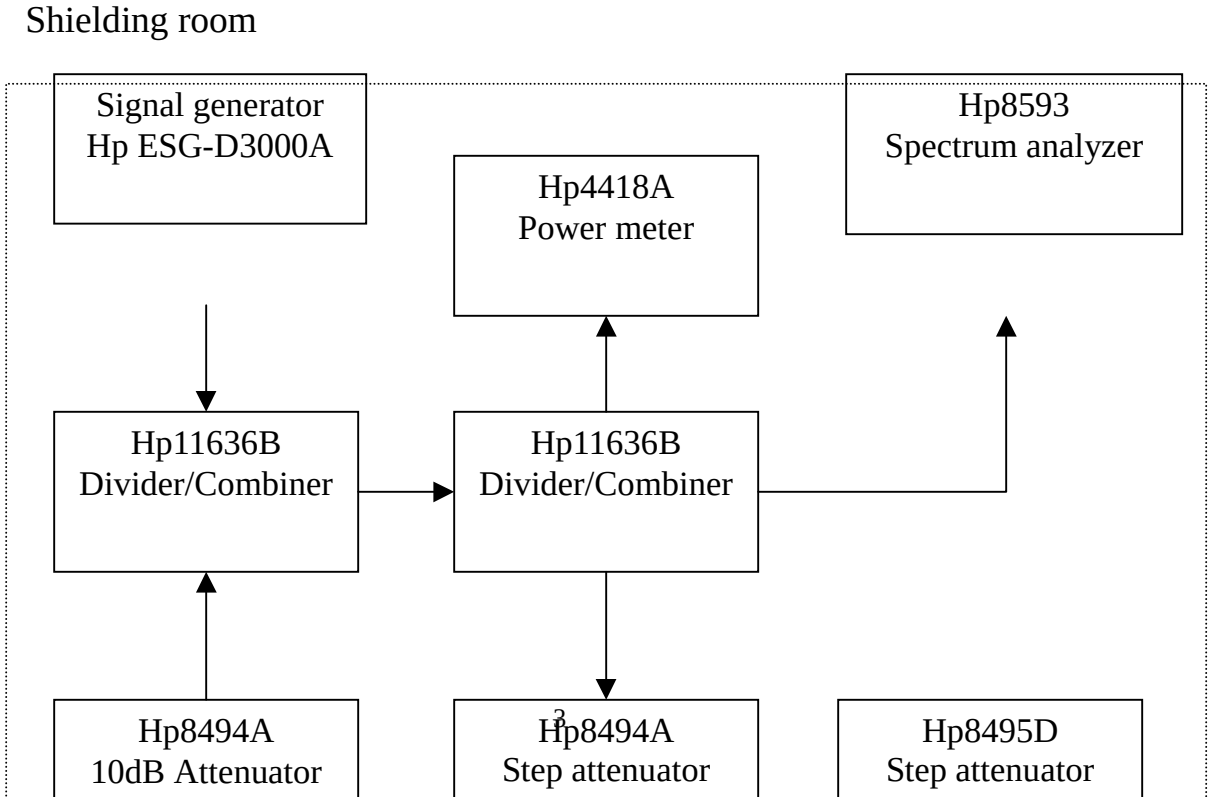
Test setup: as shown at next page

Processing gain test result summary:

Frequency channel	Frequency	Data rate(Mbps)	Gp(dB)
1	2412MHz	11	11.5
6	2437MHz	11	10.6
11	2462MHz	11	11.7
1	2412MHz	2	12
6	2437MHz	2	12.6
11	2462MHz	2	11.9

Reference

[1]. Intersil processing gain test document(Attached file).



Processing gain test setup