Fibocom
PERFECT WIRELESS EXPERIENCE

SC128

Hardware Guide

V1.3

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Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on and ensure that the device is located in an area with sufficient signal strength.

Contents

Applicable Models

No.	Applicable Model	Description
1	SC128-EAU-10	16GB e.MMC+16Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in Europe
2	SC128-EAU-30	32GB e.MMC+24Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in Europe
3	SC128-NA-30	32GB e.MMC+24Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in North America

Change History

V1.3 (2022-12-24)	Update the antenna reference circuit, Corrected AIR mode sleep power consumption
V1.2 (2022-11-24)	Add SC128-NA-30 support.
V1.1 (2022-11-02)	Add SC128-EAU-30 support. Add charging description.
V1.0 (2022-07-12)	Initial version

1 Foreword

1.1 Description

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SC128 series module (hereinafter referred to as module). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

Product Marketing Name：SC128-NA

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time averaging duty factor, antenna gain, and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product:

This device contains FCC ID: ZMOSC128NA

4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain（dBi）
LTE B2	8.00
LTE B4	5.00
LTE B5	9.41
LTE B7	8.00
LTE B12	8.70
LTE B13	9.16
LTE B17	8.74
LTE B25	8.00
LTE B26(814-824)	9.36
LTE B26(824-849)	9.41
LTE B41	8.00
LTE B66	5.00
LTE B71	8.48
BT	NA
WIFI	NA

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For this device, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:

"Contains Transmitter Module FCC ID: ZMOSC128NA" or "Contains FCC ID: ZMOSC128NA" must be used.

The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes, or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to

be compliant with the Part 15B unintentional radiator requirements.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSS. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 21374-SC128NA" or "where: 21374-SC128NA is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 21374-SC128NA " ou "où: 21374-SC128NA est le numéro de certification du module".

i The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, November 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07,2017

2 Product Overview

2.1 General Description

The module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, GSM and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Android operating system and supports various interfaces such as MIPI/USB/UART/SPI/I^2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 1. SC128-EAU supported bands

Mode	Band
GSM	GSM850/EGSM900/DCS1800/PCS1900
WCDMA	Band 1/2/3/5/8
FDD-LTE	Band 1/2/3/4/5/7/8/20/28
TDD-LTE	Band 38/40/41 (2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 2. SC128-NA supported bands

Mode	Band
FDD-LTE	Band 2/4/5/7/12/13/17/25/26/66/71
TDD-LTE	Band 41 (2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz
BT5.0	2402-2480MHz

Mode	Band
GNSS	GPS/GLONASS/BeiDou

2.2 Main Performance

The module is available in LCC + LGA package with 280 pins, including 148 LCC pins and 132 LGA pins. The dimension is 41 (±0.15) mm × 41 (±0.15) mm × 2.85 (max) mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring, multimedia terminals, ECR, and face payment terminals. The following table describes the detailed performance.

Table 2. Performance specifications

Performance	Description
Power Supply	DC: 3.5-4.4 V, typical voltage: 3.8 V
Application processor	ARM® Cortex-A53 Quad-core 64-bit CPU up to 2.0 GHz
Memory	16 Gb LPDDR4X+16 GB eMMC Flash[1)]
	24 Gb LPDDR4X+32 GB eMMC Flash
Power class	Class 4 (33 dBm ± 2 dB) for GSM850/EGSM900 Class 1 (30 dBm ± 2 dB) for DCS1800/PCS1900 Class E2 (27 dBm ± 3 dB) for GSM850/EGSM900 8-PSK Class E2 (26 dBm ± 3 dB) for DCS1800/PCS1900 8-PSK Class 3 (24 dBm + 1/-3 dB) for WCDMA bands Class 3 (23 dBm ± 2 dB) for LTE FDD bands Class 3 (23 dBm ± 2 dB) for LTE TDD bands
GSM/GPRS/EDGE features	R99: CSD transmission rate: 9.6 kbps, 14.4 kbps GPRS:

Performance	Description
	Support GPRS multi-slot class 33 Coding formats: CS-1/CS-2/CS-3 and CS-4 Up to 5 Rx time slots per frame EDGE: Support EDGE multi-slot class 33 Support GMSK and 8-PSK Uplink encoding format: CS 1-4 and MCS 1-9 Downlink encoding format: CS 1-4 and MCS 1-9
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: maximum uplink rate 5.76 Mbps CAT24 HSDPA: maximum downlink rate 42 Mbps
LTE features	Support FDD/TDD R10 Support FDD/TDD CAT4 Support 1.4-20 M RF bandwidth Downlink support 2 × 2 MIMO Maximum uplink rate 50 Mbps, maximum downlink rate 150 Mbps
WLAN features	Support 2.4 G and 5 G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, the maximum rate is up to 433 Mbps
Bluetooth features	BT5.0 (BR/EDR + BLE)
Satellite positioning	GPS/GLONASS/BeiDou
LCD Interface	4-Lane MIPI_DSI interface Support for 1080P maximally

Performance	Description
Camera interface	Two 4-Lane MIPI_CSI interfaces, which can be configured as 4+4 Lanes or 4+2+1 Lanes ISPx2 (13 MP+13 MP or 25 MP)
Audio interface	Input: 3 analog MIC inputs Output: Stereo headphone output Differential receiver output Differential SPKR output, not requires an external audio PA
USB interface	One USB 3.1 interface that is downward compatible with USB 2.0 interface USB 3.1 interface supports the SS (5 Gbps) mode but does not support software download. USB 2.0 interface supports the HS (480 Mbps) mode and software download, and is downward compatible with FS and LS interface, and supports HUB extensible USB OTG.
(U)SIM interface	Two (U)SIM card interfaces, support (U)SIM card: 1.8/3V adaptive Support dual-SIM dual-standby and hot plugging
UART interface	Three UART serial interfaces, with the maximum rate up to 4Mbps One 4-line serial interface, supports hardware flow control One 2-line serial interface One 2-lane debug serial interface
SDIO Interface	Support SD3.0 and 4-bit SDIO; SD card supports hot plugging
I^2C interface	4 sets of I^2C interfaces for TP, camera, sensor, etc.
ADC Interfaces	One general ADC
RTC	Support
Antenna Interface	MAIN antenna, DRX antenna, GNSS antenna, WIFI/BT antenna
Physical characteristics	Dimensions: 41 (±0.15) mm × 41 (±0.15) mm × 2.85 (max) mm

Performance	Description
	Packaging: 148 LCC pins +132 LGA pins Weight: about 9.7 g
Temperature range	Operating temperature[2]: -30°C to 75°C[2] Storage temperature: -40°C to -85°C Extended temperature[3]: -40°C to -85°C[3]
Software update	USB/OTA/SD
RoHS	RoHS compliant

1. The memory can be adjusted and adapted according to different needs.

2. When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

3. Extended temperature: When the module works in this temperature range, the functions of the module are normal and there will be no unrecoverable faults. The related performance of the module may exceed the requirements of the 3GPP standard. When the temperature returns to the normal operating temperature range, the module performance can still meet the 3GPP standard.

2.3 Function Block Diagram

Function block diagram shows the main hardware features of the module, including:

- Baseband
- Wireless transceiver
- Power Management
- Memory

- Peripheral interface
  - Communication expansion interface (USB/UART/I²C/SD)
  - (U)SIM card interface
  - MIPIDSI interface
  - MIPICSI interface
  - Analog audio interface

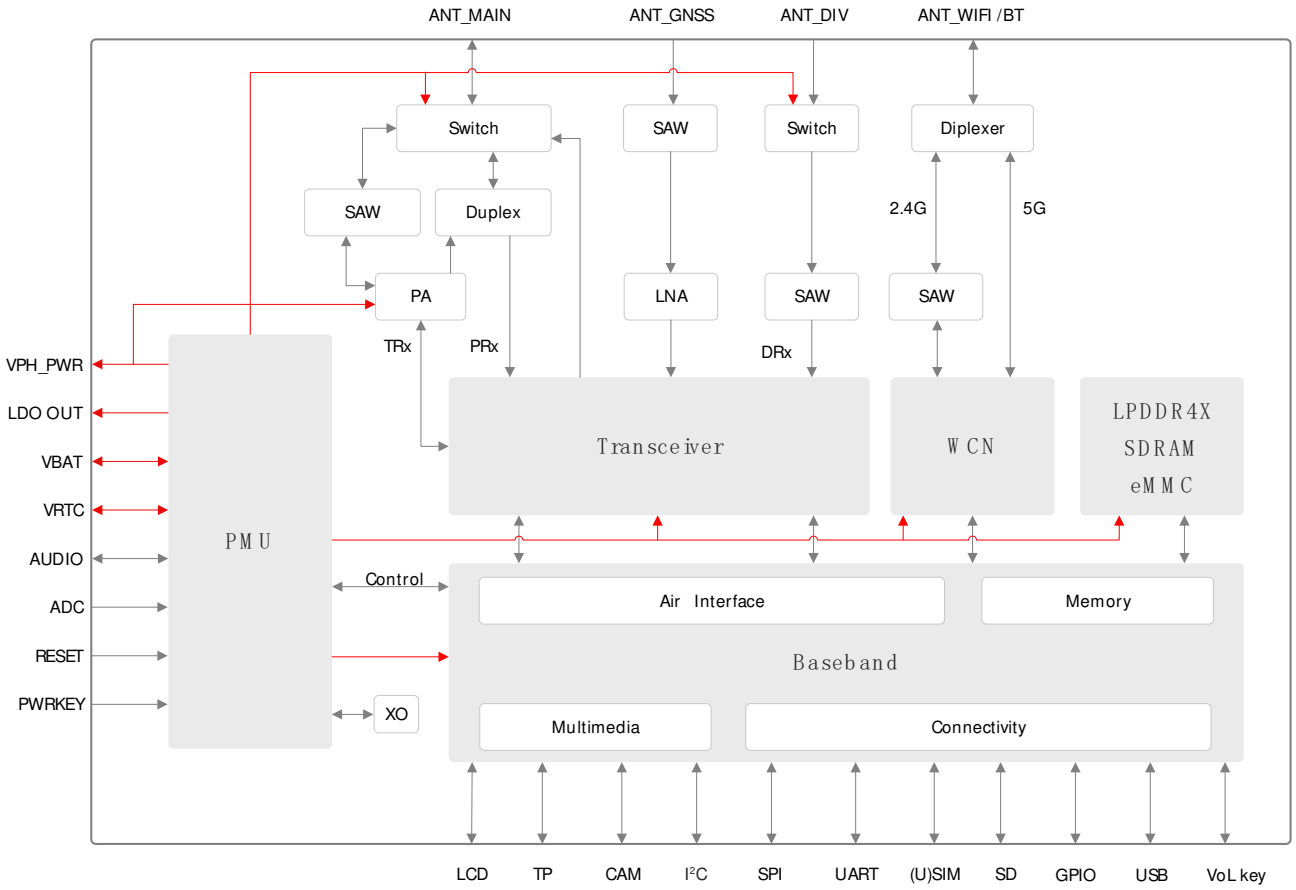

Figure 1. Function block diagram

2.4 Pin Definition

2.4.1 Pin Distribution

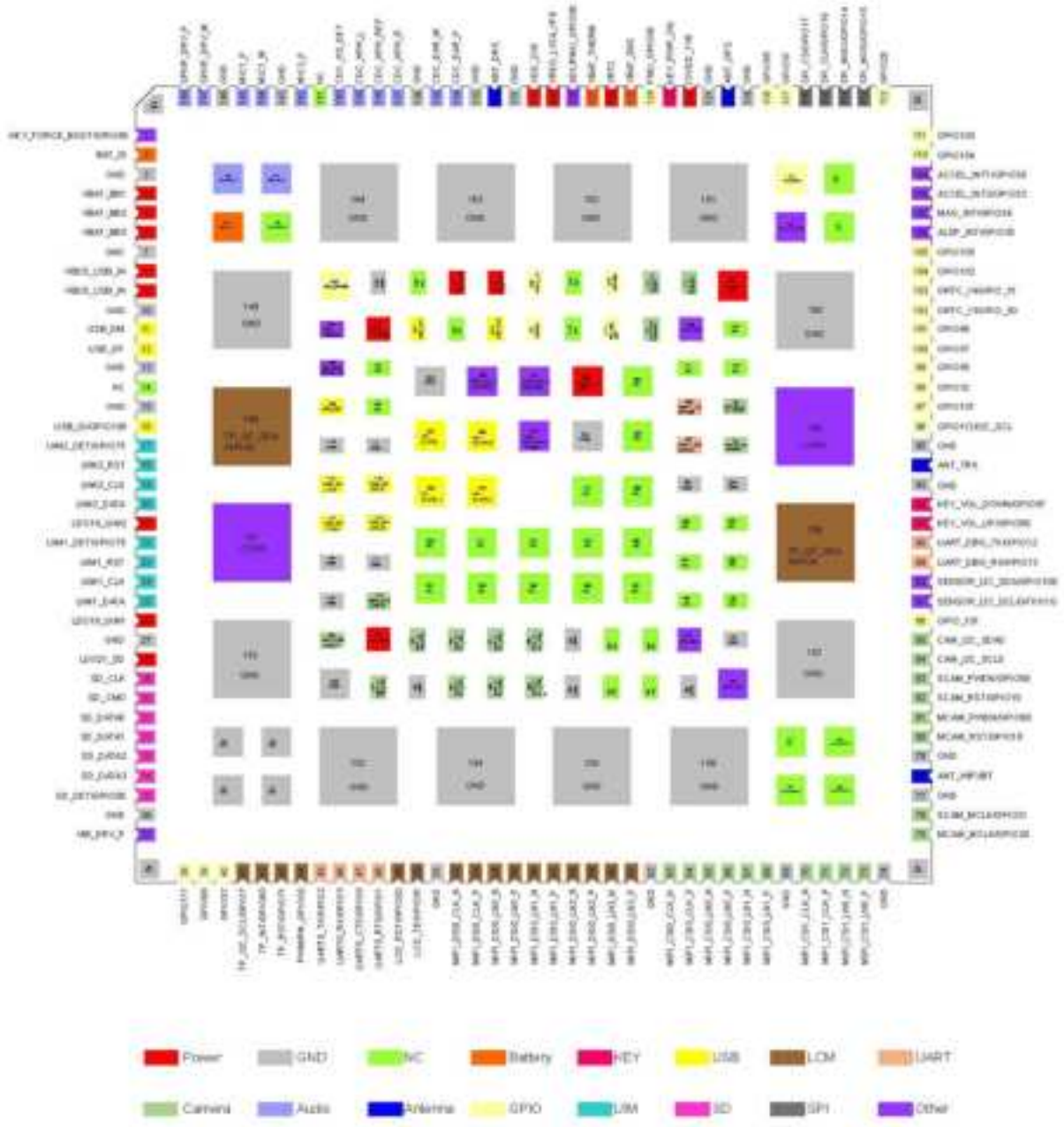

Figure 2. Pin distribution

"NC" indicates No Connect, and the pin for this position is reserved and does not need to be connected.

2.4.2 Pin Description

Table 3. I/O parameters description

Type	Description
I/O	Input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Module pins are described in the following table:

Table 4. Description of module pins

Pin Name	Pin No.	I/O	Pin Description	Remarks
Power interface				
VBAT	4,5,6	PI/PO	Main power supply	--
VRTC	126	PI/PO	RTC power supply	--
VREG_CAM_AVDD_2P8	222	PO	Camera power output	
VREG_CAM_AF_2P8	224	PO	Camera VIB power output	

Pin Name	Pin No.	I/O	Pin Description	Remarks
VDD_2V8	130	PO	2.8V voltage output	--
LDO15_1V8	129	PO	LDO L15 1.8V power output	--
VPH_PWR	278	PO	General-purpose peripheral power output	--
LDO19_UIM2	21	PO	UIM2 card power supply	--
LDO18_UIM1	26	PO	UIM1 card power supply	--
IOVDD_1V8	122	PO	LDO 1.8V power output	--
LDO17A_3V0	266	PO	LDO L17 3.0V power output	--
LDO4_SDIO	277	PO	LDO L4 SD pull-up power output	Use SD pull-up power only
LDO21_SD	38	PO	LDO L21 2.9V SD card power output	Use SD power only
Motor interface				
VIB_DRV_P	37	PO	Motor driver pin	- -
Ground				
GND	3, 7, 10, 13, 15, 27, 36, 51, 62, 69, 74, 77, 79, 93, 95, 119, 121, 131, 133, 136, 143, 146, 149, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 170, 171, 176, 177, 178, 182, 190, 191, 196, 197, 204, 205, 228, 229, 230, 231, 232, 235, 236, 237, 246, 250, 253, 275			58
Battery supply interface				
VBAT_SNS	125	AI	Battery positive detection	Connect the feedback line from the battery end to the module pin separately.

Pin Name	Pin No.	I/O	Pin Description	Remarks
VBAT_M	234	AI	Battery negative detection	Connected to the negative pole of the battery. When battery is unused, connected to GND.
VBAT_THERM	127	AI	Battery temperature detection	Connect the pin to GND with 47 KΩ resistor if the pin is unused
VBAT_ID	2	AI	Battery ID pin	Connect the pin to GND with 100 KΩ resistor if the pin is unused
Button				
KEY_FORCE_BOOT	1	DI	Force download key	Active high
KEY_VOL_UP	91	DI	Volume +	Active low
KEY_VOL_DOWN	92	DI	Volume -	Active low
KEY_PWR_ON	123	DI	Power key	Active low
RESIN_N	166	DI	Reset key	Active low
CBL_PWR_N	165	DI	Auto power-on pin	Active low
(U)SIM card interface				
UIM2_DET	17	DI	UIM2 hot plugging detection	Active high by default
UIM2_RST	18	DO	UIM2 reset signal	--
UIM2_CLK	19	DO	UIM2 clock signal	--
UIM2_DATA	20	DI/DO	UIM2 data signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
UIM1_DET	22	DI	UIM1 hot plugging detection	Active high by default
UIM1_RST	23	DO	UIM1 reset signal	--
UIM1_CLK	24	DO	UIM1 clock signal	--
UIM1_DATA	25	DI/DO	UIM1 data signal	--
SD card interface				
SD_DET	35	DI	SD card detection	Active low by default
SD_DATA3	34	DI/DO	SD card data bit 3	--
SD_DATA2	33	DI/DO	SD card data bit 2	--
SD_DATA1	32	DI/DO	SD card data bit 1	--
SD_DATA0	31	DI/DO	SD card data bit 0	--
SD_CMD	30	DI/DO	SD card command interface	--
SD_CLK	29	DO	SD card clock	--
I^2C interface				
TP_I2C_SCL	41	DO	TP I^2C clock signal	Dedicated for TP
TP_I2C_SDA	150/158	DI/DO	TP I^2C data signal	
CAM_I2C_SCL0	84	DO	CAM0 I^2C clock signal	For camera only
CAM_I2C_SDA0	85	DI/DO	CAM0 I^2C data signal	
CAM_I2C_SCL1	206	DO	CAM1/2 I^2C clock signal	For camera only
CAM_I2C_SDA1	208	DI/DO	CAM1/2 I^2C data signal	
APPS_I2C_SCL	268	DO	APPS_I2C clock signal	For peripheral

Pin Name	Pin No.	I/O	Pin Description	Remarks
APPS_I2C_SDA	267	DI/DO	APPS_I2C data signal	
SENSOR_I2C_SCL	87	DO	Sensor I²C clock	For sensor only
SENSOR_I2C_SDA	88	DI/DO	Sensor I²C data	
USB interface				
USB_VBUS	8, 9	PI	USB 5V power supply	--
USB_DET	168	PI	VBUS 5V Hot Plug Detect	Compatible design, not recommended. Please use pin 8, 9.
USB_ID	16	DI	USB_2.0_ID detec	GPIO106
USB_DM	11	AI/AO	USB 2.0 differential data signal-	--
USB_DP	12	AI/AO	USB 2.0 differential data signal+	--
USB_SS1_RX_M	175	AI	USB 3.1 differential data receiving-	--
USB_SS1_RX_P	173	AI	USB 3.1 differential data receiving+	--
USB_SS1_TX_M	174	AO	USB 3.1 differential data sending-	--
USB_SS1_TX_P	172	AO	USB 3.1 differential data sending+	--
USB_SS2_RX_M	254	AI	USB 3.1 differential data receiving-	--
USB_SS2_RX_P	269	AI	USB 3.1 differential data receiving+	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
USB_SS2_TX_M	255	AO	USB 3.1 differential data sending-	--
USB_SS2_TX_P	270	AO	USB 3.1 differential data sending+	--
USB_CC1	227	AI/AO	USB_CC1	--
USB_CC2	223	AI/AO	USB_CC2	--
UART interface				
UART0_TX	45	DO	UART0 serial interface data sending signal	--
UART0_RX	46	DI	UART0 serial interface data receiving signal	--
UART0_CTS	47	DI	UART0 serial interface CTS signal	--
UART0_RTS	48	DO	UART0 serial interface RTS signal	--
UART_DBG_RX	89	DI	Debugging serial interface UART_RX	--
UART_DBG_TX	90	DO	Debugging serial interface UART_TX	--
UART1_RX	207	DI	Serial interface UART1_RX	--
UART1_TX	209	DO	Serial interface UART1_TX	--
SPI Interface				
SPI_CLK	115	DO	SPI clock	--
SPI_CS	116	DO	SPI chip select	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
SPI_MISO	114	DI	SPI master in slave out	--
SPI_MOSI	113	DO	SPI master output slave input	--
LCD interface				
MIPI_DSI0_CLK_N	52	AO	LCD MIPI-DSI signal	--
MIPI_DSI0_CLK_P	53	AO		--
MIPI_DSI0_LN0_N	54	AO		--
MIPI_DSI0_LN0_P	55	AO		--
MIPI_DSI0_LN1_N	56	AO		--
MIPI_DSI0_LN1_P	57	AO		--
MIPI_DSI0_LN2_N	58	AO		--
MIPI_DSI0_LN2_P	59	AO		--
MIPI_DSI0_LN3_N	60	AO		--
MIPI_DSI0_LN3_P	61	AO		--
PWM	44	DO	LCD backlight brightness PWM control	--
LCD_RST	49	DO	LCD reset signal	--
LCD_TE	50	DI	LCD swipe synchronization signal	--
TP interface				
TP_INT	42	DI	TP interrupt	--
TP_RST	43	DO	TP reset signal	--
Camera interface				
MIPI_CSI0_CLK_P	64	AI	Camera MIPI-CSI0 interface.	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
MIPI_CSI0_CLK_N	63	AI	Keep the unused pins unconnected.	--
MIPI_CSI0_LN0_N	65	AI		--
MIPI_CSI0_LN0_P	66	AI		--
MIPI_CSI0_LN1_N	67	AI		--
MIPI_CSI0_LN1_P	68	AI		--
MIPI_CSI0_LN2_N	183	AI		--
MIPI_CSI0_LN2_P	181	AI		--
MIPI_CSI0_LN3_N	179	AI		--
MIPI_CSI0_LN3_P	180	AI		--
MIPI_CSI1_CLK_N	70	AI	Camera MIPI-CSI1 interface. Keep the unused pins unconnected.	--
MIPI_CSI1_CLK_P	71	AI		--
MIPI_CSI1_LN0_N	72	AI		--
MIPI_CSI1_LN0_P	73	AI		--
MIPI_CSI1_LN1_N	185	AI		--
MIPI_CSI1_LN1_P	184	AI		--
MIPI_CSI1_LN2_N	187	AI		--
MIPI_CSI1_LN2_P	186	AI		--
MIPI_CSI1_LN3_N	189	AI		--
MIPI_CSI1_LN3_P	188	AI		--
MCAM_MCLK	75	DO	Camera 1 clock signal	--
MCAM_RST	80	DO	Camera 1 reset signal	--
MCAM_PWDN	81	DO	Camera 1 shutdown signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
SCAM_MCLK	76	DO	Camera 2 clock signal	--
SCAM_RST	82	DO	Camera 2 reset signal	--
SCAM_PWDN	83	DO	Camera 2 shutdown signal	--
DCAM_PWDN	215	DO	Camera 3 shutdown signal	--
DCAM_RST	214	DO	Camera 3 reset signal	--
DCAM_MCLK	213	DO	Camera 3 clock signal	--
Audio interface				
MIC1_P	145	AI	Main MIC input+	--
MIC1_M	144	AI	Main MIC input-	--
MIC2_P	142	AI	Headphone MIC input+	--
MIC3_P	244	AI	Secondary MIC input+	--
MIC3_M	233	AI	Secondary MIC input-	--
EAR_P	134	AO	Receiver output+	--
EAR_M	135	AO	Receiver output-	--
SPKR_DRV_P	148	AO	Differential lineout output+	It requires an external audio PA.
SPKR_DRV _M	147	AO	Differential lineout output-	
HPH_R	137	AO	Headphone right channel output	--
HPH_GND	138	/	Headphone reference ground	It requires to be grounded.
HPH_L	139	AO	Headphone left channel output	--
HPH_DET	140	AI	Headphone plug detection	--
Antenna interface				

Pin Name	Pin No.	I/O	Pin Description	Remarks
ANT_MAIN	94	AI/AO	Main antenna	--
ANT_DRX	132	AI	Diversity antenna	--
ANT_WIFI/BT	78	AI/AO	WIFI/BT antenna	--
ANT_GNSS	120	AI	GNSS antenna	--
GPIO Interface				
GPIO_28	112	DI/DO	Ordinary GPIO, 1.8V power domain	B-PD: nppukp
GPIO_31	117	DI/DO		B-PD: nppukp
GPIO_32	98	DI/DO		B-PD: nppukp
GPIO_55	118	DI/DO		B-PD: nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_56	100	DI/DO		B-PD: nppukp
GPIO_57	221	DI/DO		B-PD: nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_86	101	DI/DO		B-PD: nppukp
GPIO_98	39	DI/DO		B-PD: nppukp
GPIO_99	216	DI/DO		B-PD: nppukp
GPIO_100	99	DI/DO		B-PD: nppukp
GPIO_101	86	DI/DO		B-PD: nppukp

Pin Name	Pin No.	I/O	Pin Description	Remarks
GPIO_102	104	DI/DO		B-PD: nppukp
GPIO_103	111	DI/DO		B-PD: nppukp
GPIO_104	110	DI/DO		B-PD: nppukp
GPIO_105	105	DI/DO		B-PD: nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_107	97	DI/DO		B-PD: nppukp
GPIO_111	38	DI/DO		B-PD: nppukp
GPIO_112	96	DI/DO		B-PD: nppukp
PM_GPIO_4	249	DI/DO		B-PD: nppukp; PMIC_GPIO
PM_GPIO_3	243	DI/DO		B-PD: nppukp; PMIC_GPIO
PM_GPIO_7	217	DI/DO		B-PD: nppukp; PMIC_GPIO
PM_GPIO_8	124	DI/DO		B-PD: nppukp; PMIC_GPIO
LPI interface				
LPI_GPIO_21	239	DI/DO	LPI GPIO, 1.8V power domain	Reserved. Don't suggest using it as GPIO.
LPI_GPIO_22	238	DI/DO		
LPI_GPIO_25	245	DI/DO		
LPI_GPIO_26	240	DI/DO		

Pin Name	Pin No.	I/O	Pin Description	Remarks
LED interface				
CHG_LED	248	PO	Charge indicator	--
FLASH_LED	252	PO	Flash	--
RG_GRN	280	AO	LED current sink drive	--
RG_RED	279	AO	LED current sink drive	--
INT interface				
ALSP_INT	106	DI	Ambient light sensor interrupt signal	--
ACCEL_INT2	108	DI	G-Sensor interrupt signal 2	--
MAG_INT	110	DI	Magnetic sensor interrupt signal	--
ACCEL_INT1	109	DI	G-Sensor interrupt signal 1	--
Other Interfaces				
ADC	128	AI	ADC input	--
NFC_CLK	256	DO	NFC clock	--
GRFC_13	102	DI/DO	Ordinary GPIO, 1.8V power domain	Dedicated for RF
GRFC_14	103	DI/DO	Ordinary GPIO, 1.8V power domain	Dedicated for RF
GRFC_15	220	DI/DO	Ordinary GPIO, 1.8V power domain	Dedicated for RF
Reserved	14, 141, 167, 169, 192, 193, 194, 195, 198, 199, 200, 201, 202, 203, 210, 211, 212, 218, 219, 225, 226, 241, 242, 247, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 271, 272, 273, 274			--

Table 5. QUP interface description

Pin Name	GPIO	QUP Config		Function 1	Function 2	Function 3	Function 4
47	GPIO_0	QUP SE0	L0	UART_CTS	SPI_MISO	I2C_SDA	I3C_SDA
48	GPIO_1		L1	UART_RTS	SPI_MOSI	I2C_SCL	I3C_SCL
45	GPIO_2		L2	UART_TX	SPI_SCLK	--	--
46	GPIO_3		L3	UART_RX	SPI_CS_0	--	--
267	GPIO_4	QUP SE1	L0	UART_CTS	SPI_MISO	I2C_SDA	--
268	GPIO_5		L1	UART_RTS	SPI_MOSI	I2C_SCL	--
209	GPIO_69		L2	UART_TX	SPI_SCLK	--	--
207	GPIO_70		L3	UART_RX	SPI_CS_0	--	--
150,158	GPIO_6	QUP SE2	L0	UART_CTS	SPI_MISO	I2C_SDA	--
41	GPIO_7		L1	UART_RTS	SPI_MOSI	I2C_SCL	--
43	GPIO_71		L2	UART_TX	SPI_SCLK	--	--
42	GPIO_80		L3	UART_RX	SPI_CS_0	--	--
91	GPIO_96	QUP SE4	L0	UART_CTS	SPI_MISO	I2C_SDA	--
92	GPIO_97		L1	UART_RTS	SPI_MOSI	I2C_SCL	--
90	GPIO_12		L2	UART_TX	SPI_SCLK	--	--
89	GPIO_13		L3	UART_RX	SPI_CS_0	--	--
114	GPIO_14	QUP SE5	L0	UART_CTS	SPI_MISO	I2C_SDA	--
113	GPIO_15		L1	UART_RTS	SPI_MOSI	I2C_SCL	--
115	GPIO_16		L2	UART_TX	SPI_SCLK	--	--
116	GPIO_17		L3	UART_RX	SPI_CS_0	--	--

The QUP interfaces in the same group cannot be configured in different types at the same time, for example, UART and I^2C interfaces.

3 Application Interfaces

3.1 Power Supply

The module provides three VBAT pins for connecting to external power supply source. The input range of power is 3.5 V to 4.4 V and the recommended value is 3.8 V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. The peak current of the module can reach 3 A. If the power supply capacity is insufficient, the power supply transient voltage drops below 3.5 V, which may cause the module power-off or restart. The power supply voltage drop is shown in the following figure:

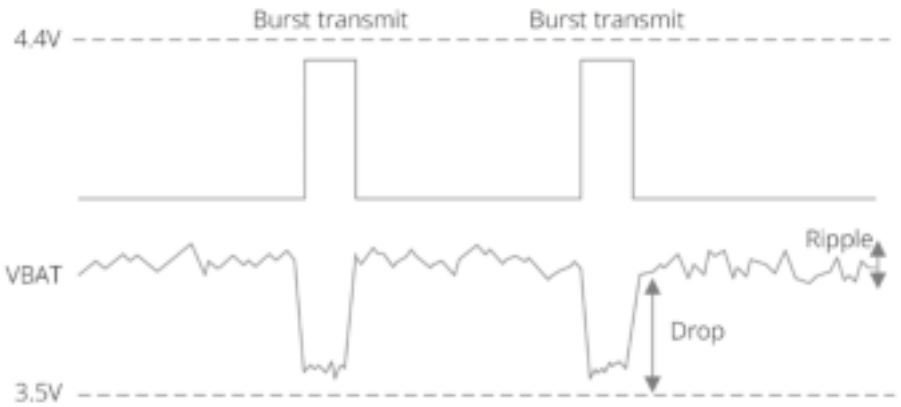

Figure 3. Voltage drop

3.1.1 Power Input

External power source supplies the module by VBAT pins. To ensure the power transient voltage is no less than 3.5 V, it is recommended to connect two 220 µF tantalum capacitors with low ESR and filter capacitors of 1 µF, 100 nF, 39 pF and 33 pF in parallel to the VBAT input of the module. Besides, the PCB route of VBAT should be as short and wide as possible (no less than 3 mm) and the ground plane of the power section should be flat to reduce the equivalent impedance of the VBAT route and avoid significant voltage drop at high currents at maximum transmit power.

Table 6. Power supply

Parameter	Minimum Value	Typical Value	Maximum Value	Unit

VBAT input voltage	3.5	3.8	4.4	V
VBAT operating current	--	--	3	A

The voltage range of VBAT power supply must be between 3.5 V and 4.4 V, including the superimposed value of ripple, drop, instantaneous overshoot and other voltages.

The following figure shows the reference design of power circuit.

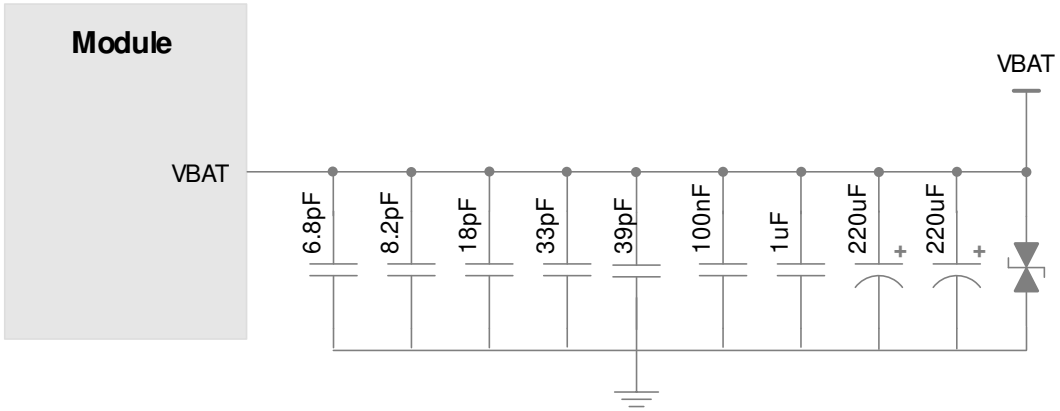

Figure 4. Reference design of power circuit

The following table describes the filter capacitor design of power supply.

Table 7. Filter capacitor design of power supply

Recommended Capacitor	Application	Description
220 µF×2	Regulating capacitor	To reduce power fluctuations during module operation, low ESR capacitors are required. LDO or DCDC power supply requires capacitor with a capacitance of no less than 440 µF. Battery power supply requires capacitors with a capacitance of 100-220 µF.

Recommended Capacitor	Application	Description
1 µF, 100 nF	Low frequency filter capacitors	Filter out interference caused by clock and digital signals.
39 pF, 33 pF, 18 pF, 8.2 pF, 6.8 pF	Decoupling capacitor	Filter high frequency interference.

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When VBAT is disconnected, if the real-time clock needs to be maintained, it needs to be powered by an external power source (such as a coin battery). The VRTC parameters are as follows:

Table 8. VBATBK parameters

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VRTC output voltage	2.45	3.0	3.35	V
VRTC input voltage (clock works well)	2.8	3.0	3.35	V
VRTC input current (clock works well)	9	--	200	uA

The VRTC power supply uses the following reference circuit when powered by an external power source:

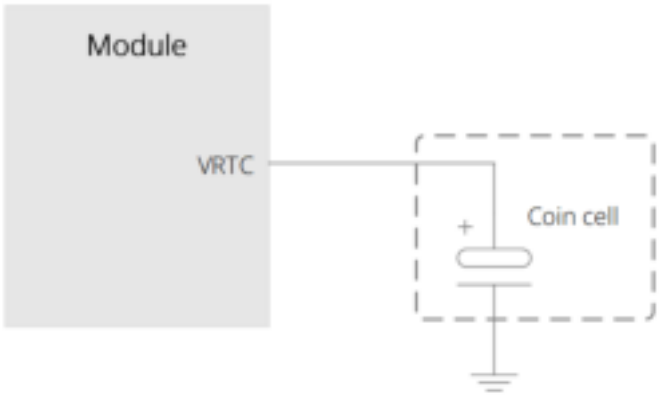

Figure 5. Reference circuit of VRTC power supply

3.1.3 VPH_PWR

The module supports the output of VPH_PWR as the peripheral power supply, the voltage is the same as that of VBAT and the maximum output current is 1A. If the module internal fuel gauge function is used, VPH_PWR needs to be used as the LCD, backlight, camera and other peripheral power supply to obtain higher power calculation accuracy.

3.1.4 Power Output

The module provides multiple power outputs for peripheral circuits. 33 pF and 10 pF capacitors can be connected in parallel to avoid high frequency interference effectively.

Table 9. Power output

Pin Name	Default Voltage (V)	Drive Current (mA)
VDD_2V8	2.8	500
LDO15_1V8	1.8	400
VPH_PWR	=VBAT	1000
LDO19_UIM2	1.8/3.0	100
LDO18_UIM1	1.8/3.0	100
IOVDD_1V8	1.8	300
LDO17A_3V0	3.0	200
LDO4_SDIO	1.8/2.95	20
LDO21_SD	2.95	800

3.2 Control Signal

3.2.1 Power On/Off

The module provides two-way power-on/off control signals to control module's power-on/off, restart and sleep/wakeup.

Table 10. Power-on/off control signal

Pin Name	Pin No.	I/O	Description	Remarks
KEY_PWR_ON	123	DI	Active low, used to power on/off and restart the module, make the module to sleep, and wake up the module	--
CBL_PWR_N	165	DI	Active low, used to power on the module only	--

3.2.1.1 Power-on

After the module's VBAT pin is powered on, pull down KEY_PWR_ON pin for 2s–8s to trigger module to start. The keystroke and OC driver power-on reference circuit are designed as follows:

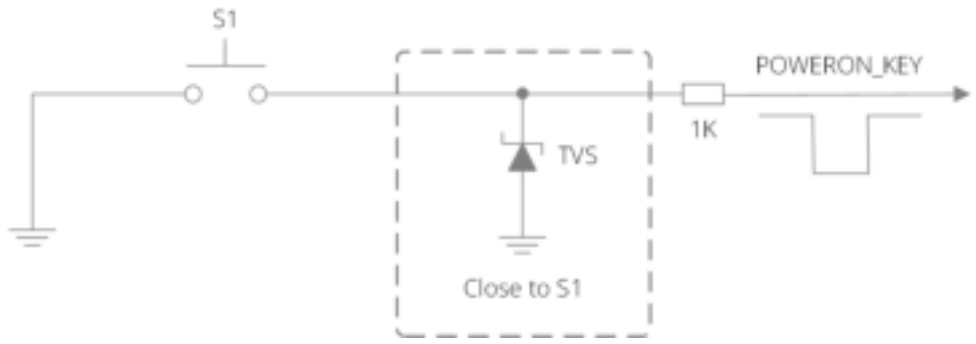

Figure 6. Keystroke power-on reference circuit

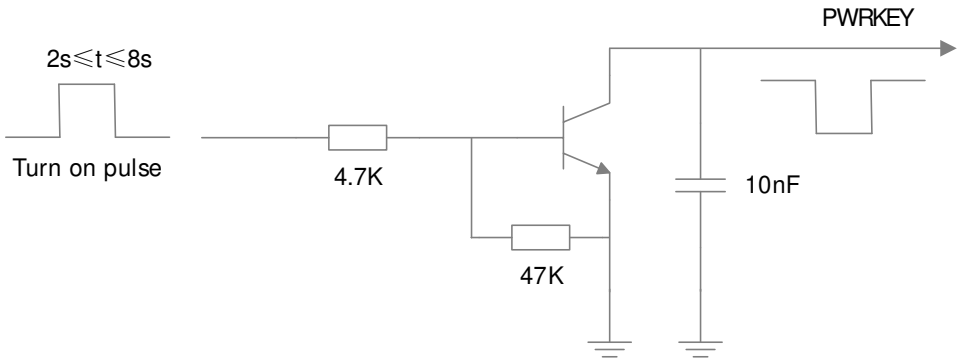

Figure 7. OC driver power-on reference circuit

The CBL_PWR_N pin is connected to the ground through a 1K resistor, and the module can be started up automatically after power-on. The following figure shows the reference circuit for automatic startup upon power-on.

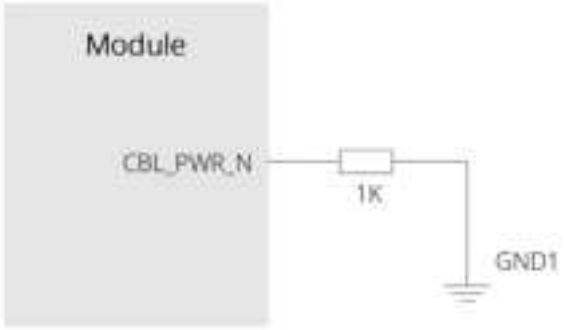

Figure 8. CBL power-on reference circuit

Power on sequence is shown as follows:

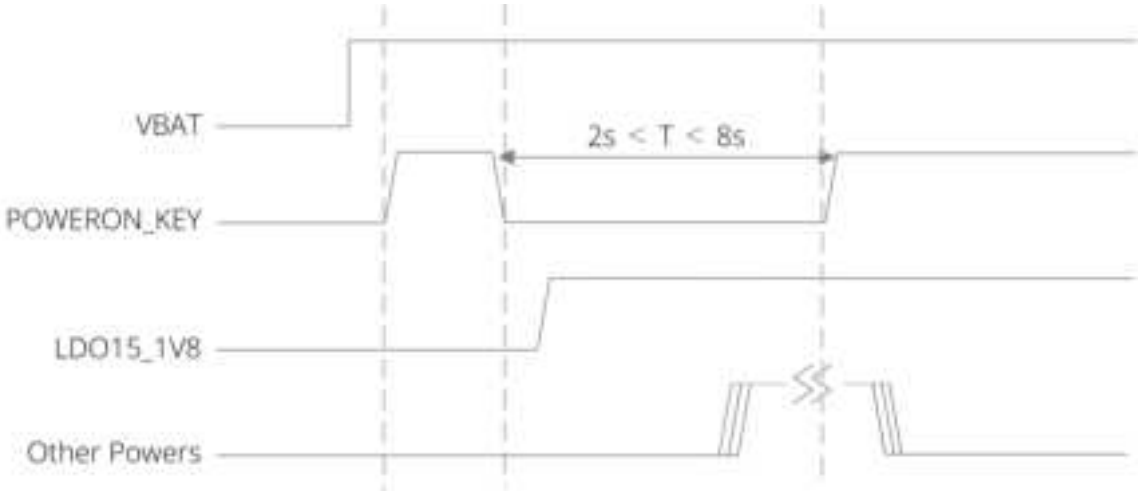

Figure 9. Startup timing sequence

3.2.1.2 Power-off and Reset

Normal power off: When the module is in operating mode, pull down KEY_PWR_ON pin for more than 2s. A dialog box is displayed, prompting you to power off or restart the module.

Forced power off: Pull down KEY_PWR_ON pin for 9s to 15s, and the module will be forcibly powered off. The forced power off timing is as follows:

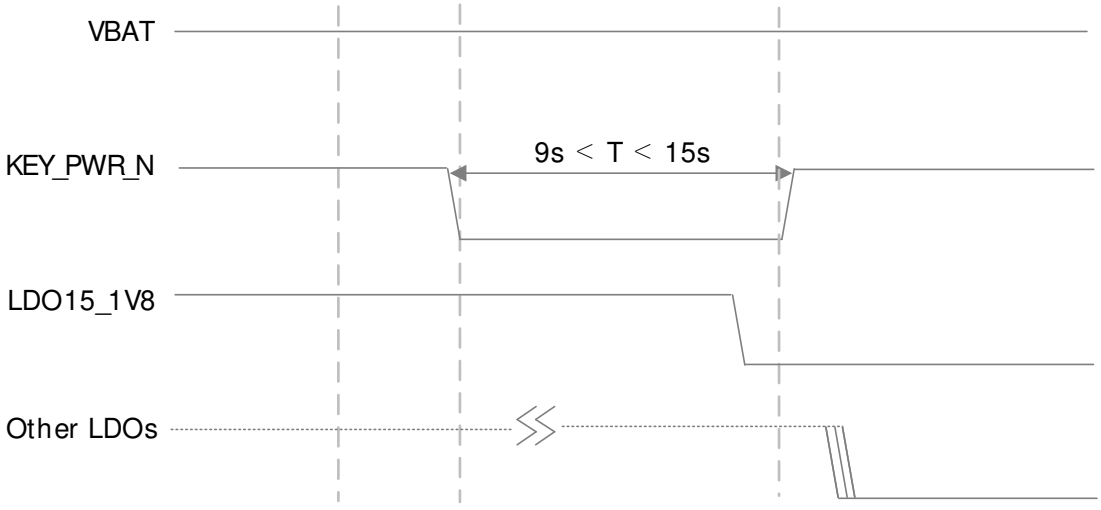

Figure 10. Power-off timing

When the system is abnormal or crashes, you can forcibly reset the module. The normal power-off method is recommended in normal cases, because forced reset may

cause data loss and other anomalies.

Reset: Pull down RESET_N pin for 4s.

3.2.1.3 Sleep/Wakeup

When module is in standby mode, pull down KEY_PWR_ON pin for 0.5s and the module will enter sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

When module is in sleep mode, pull down KEY_PWR_ON pin for 0.5s and the module can be woken up.

3.2.1.4 Volume Control

KEY_VOL_UP and KEY_VOL_DOWN pins are used as the volume down key and volume up key; the volume key circuit design can be referred to the power-on circuit design.

3.3 USB Interface (TYPE-C)

The module supports one USB 3.1 interface that is downward compatible with USB 2.0 interface. USB 3.1 interface supports SS (5 Gbps) mode, but does not support software download.

USB 2.0 interface supports the HS (480 Mbps) mode and software download, and is downward compatible with FS and LS interface.

USB supports OTG function and HUB expansion interface. The pin definition of the USB interface is as follows:

Table 11. USB 3.1 pin definition

Pin Name	Pin No.	I/O	Description	Remarks
USB_SS1_RX_M	175	AI	USB 3.1 differential data receiving-	--

Pin Name	Pin No.	I/O	Description	Remarks
USB_SS1_RX_P	173	AI	USB 3.1 differential data receiving+	--
USB_SS1_TX_M	174	AO	USB 3.1 differential data sending-	--
USB_SS1_TX_P	172	AO	USB 3.1 differential data sending+	--
USB_SS2_RX_M	254	AI	USB 3.1 differential data receiving-	--
USB_SS2_RX_P	269	AI	USB 3.1 differential data receiving+	--
USB_SS2_TX_M	255	AO	USB 3.1 differential data sending-	--
USB_SS2_TX_P	270	AO	USB 3.1 differential data sending+	--
USB_CC1	223	AI/AO	USB_CC1	--
USB_CC2	227	AI/AO	USB_CC2	--

Table 12. USB 2.0 pin definition

Pin Name	Pin No.	I/O	Description	Remarks
USB_VBUS	8,9	PI/PO	USB 5V power supply	--
USB_DM	11	AI/AO	USB 2.0 differential data signal-	--
USB_DP	12	AI/AO	USB 2.0 differential data signal+	--
USB_ID	16	DI	USB 2.0 Device/Host	Reserved

Pin Name	Pin No.	I/O	Description	Remarks
			mode recognition	

The reference circuit design of the USB 3.1 (Type-C) interface is as follows:

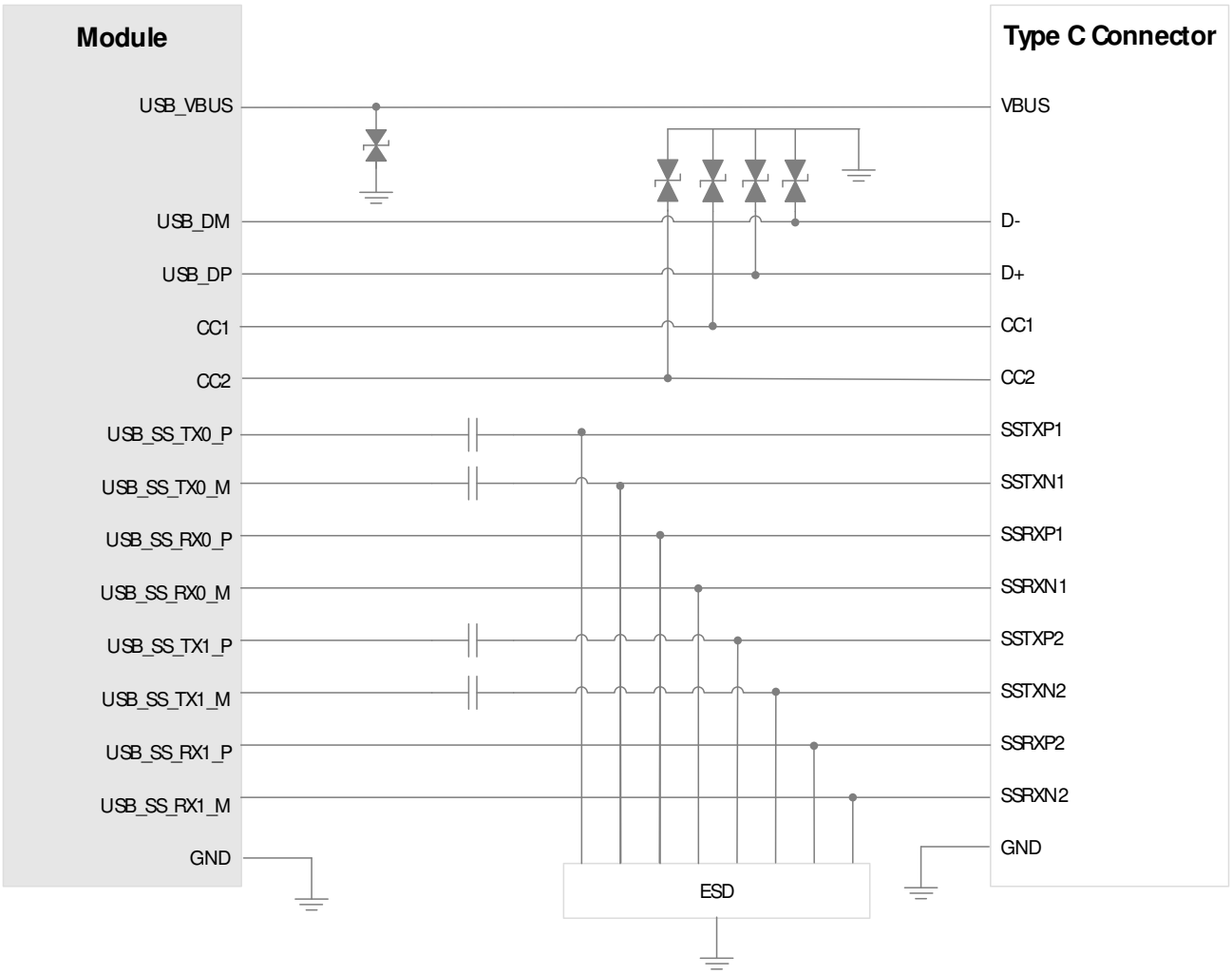

Figure 11. USB 3.1 reference circuit design

Precautions for USB design:

- The junction capacitor for ESD protection device of USB_DP/DM must be less than 2pF.
- USB_DP and USB_DM are high-speed differential signal lines. The highest transmission rate is 480Mbps. Please pay attention to the following requirements during PCB layout:
  - USB_DP and USB_DM signal cables should be parallel and equal in length (differential cable

length differences should be controlled within 2 mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.

- USB2.0 differential signal cables should be fully grounded.

- Support OTG function: The VBUS interface of the module provides 5 V output as OTG power supply.
- The internal charging function of the module depends on CC detection and requires the use of TYPE C connector. Charging will not be supported when using the micro-B.

Precautions for USB 3.1 design:

- USB 3.1 is a high-speed signal cable and needs to be well-shielded (differential cable surrounded by grounding lines should be fully grounded), and follows the principle of high-speed differential cable routing.
- Control the differential impedance, make it 90 Ω ± 10% and ensure that the differential cable length differences are within 0.7 mm.
- The parasitic capacitance of ESD device must be less than 0.5 pF.

3.4 UART

The module defines three sets of UART ports, which are all in 1.8 V voltage domain. The pin definition is as follows:

Table 13. UART pin definition

Pin Name	Pin No.	I/O	Description	Remarks
UART0_TX	45	DO	UART0 serial interface data sending signal	--
UART0_RX	46	DI	UART0 serial interface data receiving signal	--
UART0_CTS	47	DI	UART0 serial interface CTS signal	--
UART0_RTS	48	DO	UART0 serial interface RTS signal	--

Pin Name	Pin No.	I/O	Description	Remarks
UART_DBG_RX	89	DI	Debugging serial interface UART_RX	--
UART_DBG_TX	90	DO	Debugging serial interface UART_TX	--
UART1_RX	207	DI	Serial interface UART1_RX	--
UART1_TX	209	DO	Serial interface UART1_TX	--

The voltage domain of each serial port is 1.8 V; when communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip with the following reference circuit design:

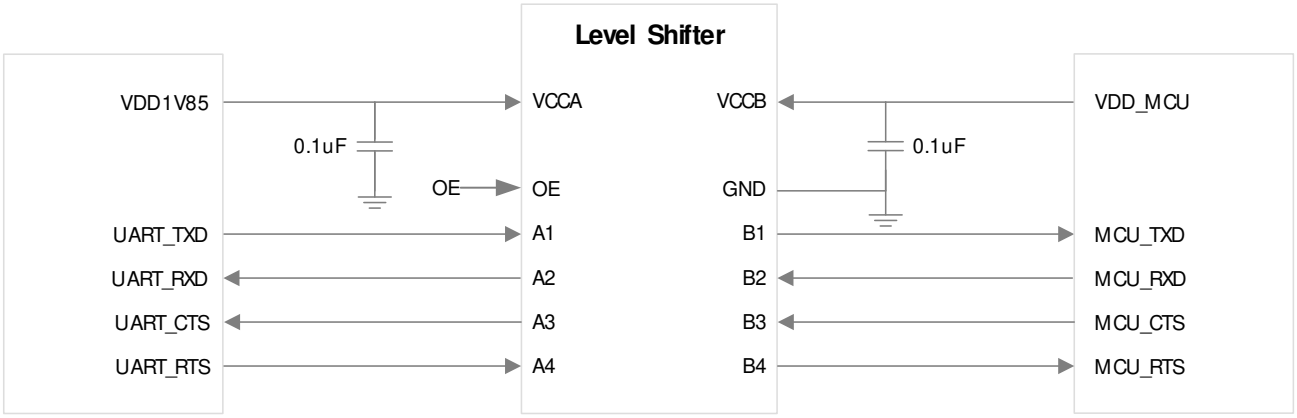

Figure 12. Level conversion reference circuit

3.5 SPI

By default, the module provides one set of SPI interfaces that support primary/secondary mode. The pin definition is as follows:

Table 14. SPI pin definition

Pin Name	Pin No.	I/O	Description	Remarks
SPI_CLK	115	DO	SPI clock	--
SPI_CS	116	DO	SPI chip select	--
SPI_MISO	114	DI	SPI master in slave out	--
SPI_MOSI	113	DO	SPI master output slave input	--

3.6 SD

The module supports one SD interface. The pin definition is as follows:

Table 15. Definition of SD interface pins

Pin No.	Pin Name	I/O	Description	Remarks
SD_DET	35	DI	SD card detection	Active low by default
SD_DATA3	34	DI/DO	SD card data bit 3	--
SD_DATA2	33	DI/DO	SD card data bit 2	--
SD_DATA1	32	DI/DO	SD card data bit 1	--
SD_DATA0	31	DI/DO	SD card data bit 0	--
SD_CMD	30	DI/DO	SD card command interface	--
SD_CLK	29	DO	SD card clock	--
LDO21_SD	28	PO	LDO L21 2.9 V power output	--
LDO4_SDIO	277	PO	LDO L4 SD pull-up power output	--

SD interface reference circuit design is as follows:

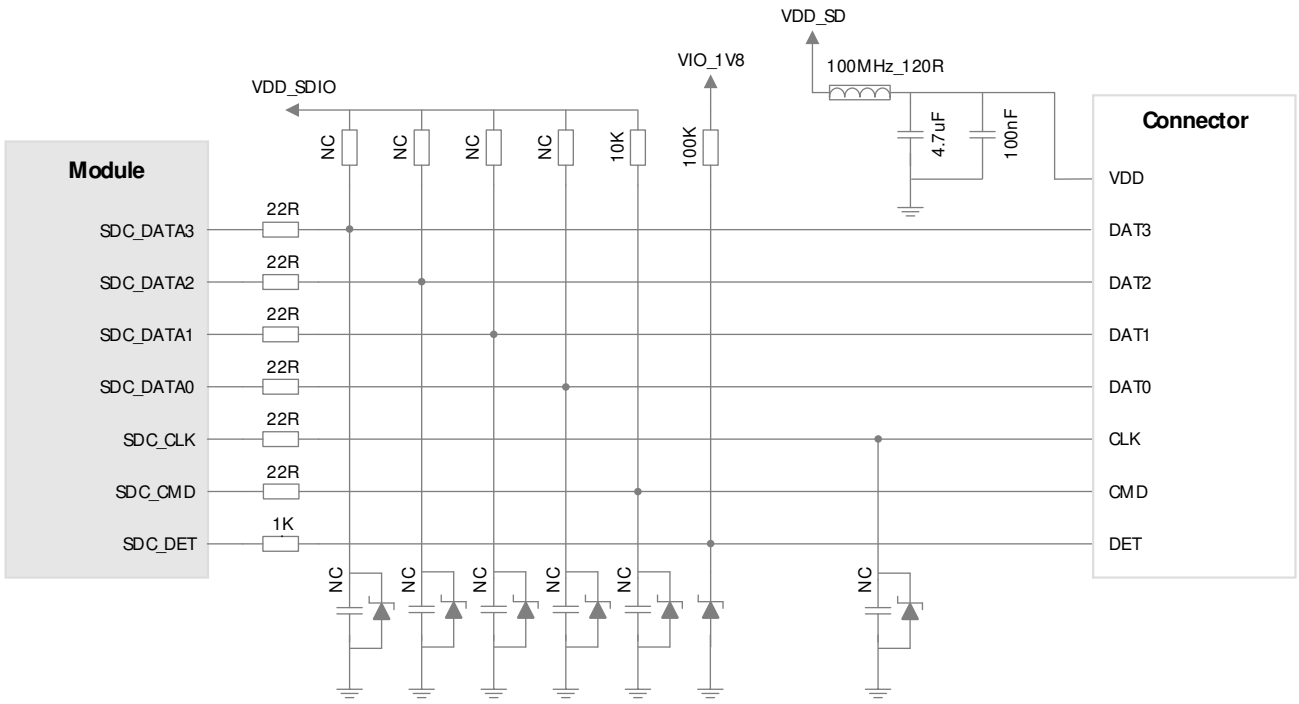

Figure 13. SD reference circuit

- LDO21_SD is the SD card peripheral driving power and can provide about 800 mA current. Pay attention to control the width of cable, which should be larger than 0.8 mm.
- Pull up SD_DET with LDO15_1V8 power supply.
- SD is a high-speed digital signal line and must be shielded. Their length must be equal during layout.
- Note that the length of the SD card clock and signal cables should not exceed 50 mm, and the TVS tube should be a device with a parasitic capacitance less than 0.5 pF.

3.7 SIM

The module provides two (U) SIM card interfaces that support dual card dual standby. The pin definition is as follows:

Table 16. Definition of SIM interface pins

Pin No.	Pin Name	I/O	Description	Remarks
UIM1_DET	22	DI	（U）SIM1 card detection	Active high by default
UIM1_RST	23	DO	（U）SIM1 reset	--
UIM1_CLK	24	DO	（U）SIM1 clock	--
UIM1_DATA	25	DI/DO	（U）SIM1 data	--
UIM2_DET	17	DI	（U）SIM2 card detection	Active high by default
UIM2_RST	18	DO	（U）SIM2 reset	--
UIM2_CLK	19	DO	（U）SIM2 clock	--
UIM2_DATA	20	DI/DO	（U）SIM2 data	--

SIM reference circuit design is as follows:

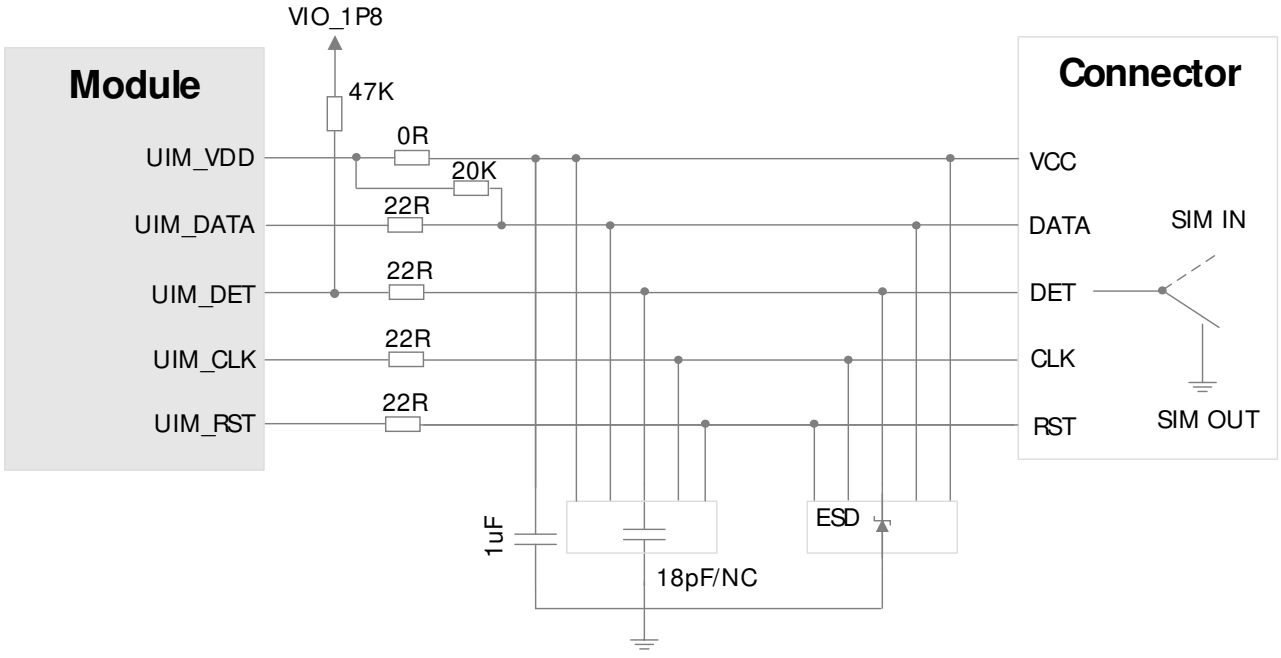

Figure 14. SIM reference circuit

3.8 GPIO

The module has rich GPIO resources and the interface level is 1.8 V. The pin definition is as follows:

Table 17. GPIO list

Pin Name	Pin No.	Reset Status	Interrupt Function
GPIO_28	112	B-PD: nppukp	YES
GPIO_31	117	B-PD: nppukp	YES
GPIO_32	98	B-PD: nppukp	YES
GPIO_55	118	B-PD: nppukp	NO
GPIO_56	100	B-PD: nppukp	NO
GPIO_57	221	B-PD: nppukp	NO
GPIO_86	101	B-PD: nppukp	YES
GPIO_98	39	B-PD: nppukp	NO
GPIO_99	216	B-PD: nppukp	YES
GPIO_100	99	B-PD: nppukp	NO
GPIO_101	86	B-PD: nppukp	YES
GPIO_102	104	B-PD: nppukp	YES
GPIO_103	111	B-PD: nppukp	YES
GPIO_104	110	B-PD: nppukp	YES
GPIO_105	105	B-PD: nppukp	YES
GPIO_107	97	B-PD: nppukp	YES
GPIO_111	38	B-PD: nppukp	NO
GPIO_112	96	B-PD: nppukp	YES
PM_GPIO_4	249	B-PD: nppukp	YES

Pin Name	Pin No.	Reset Status	Interrupt Function
PM_GPIO_3	243	B-PD: nppukp	YES
PM_GPIO_7	217	B-PD: nppukp	YES
PM_GPIO_8	124	B-PD: nppukp	YES

Table 18. Parameter description

Parameter	Description
B	Bidirectional digital with CMOS input
NP	pdpukp: defaulted to no-pull with programmable options following the colon (:).
PD	nppukp: defaulted to pull-down with programmable options following the colon (:).
PU	nppdkp: defaulted to pull-up with programmable options following the colon (:).
KP	nppdpu: defaulted to keeper with programmable options following the colon (:).

3.9 I^2C

The module provides 4 sets of I^2C interfaces for TP, camera, sensor and peripheral. The I^2C pin definition is shown in the following table:

Table 19. I^2C interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
TP_I2C_SCL	41	OD	TP I^2C clock signal	Dedicated for TP
TP_I2C_SDA	150, 158	OD	TP I^2C data signal	
CAM_I2C_SCL0	84	OD	I^2C clock signal of camera 0	For camera only
CAM_I2C_SDA0	85	OD	I^2C data signal of camera 0	
CAM_I2C_SCL1	206	OD	I^2C clock signal of camera 1/2	For camera only

Pin Name	Pin No.	I/O	Description	Remarks
CAM_I2C_SDA1	208	OD	I²C data signal of camera 1/2	
SENSOR_I2C_SCL	87	OD	Sensor I²C clock	For sensor only
SENSOR_I2C_SDA	88	OD	Sensor I²C data	
APPS_I2C_SCL	268	OD	APPS I2C clock	For peripheral
APPS_I2C_SDA	267	OD	APPS I2C data	

When I²C has more than one peripheral, please ensure the uniqueness of every peripheral address. If one of the peripherals has high requirement for timeliness, do not set the peripherals to share one set of I²C interfaces.

3.10 ADC

The module provides one ADC interface and its maximum resolution is 15 bits. The pin definition is as follows:

Table 20. ADC interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
ADC	128	AI	ADC input	Maximum input voltage of 1.8 V

3.11 Battery Supply Interface

Table 21. Battery interface pin definition

Pin Name	Pin Name	I/O	Description	Remarks
VBAT	4,5,6	PI	Main power supply	--
VBAT_SNS	125	AI	Battery positive detection	Connect the feedback line from the battery end to the module pin

Pin Name	Pin Name	I/O	Description	Remarks
				separately. When battery is unused, connected to VBAT.
VBAT_M	234	AI	Battery negative detection	Connected to the negative pole of the battery. When battery is unused, connected to GND.
VBAT_THERM	127	AI	Battery temperature detection	Connect the pin to GND with 10 KΩ resistor if the pin is unused.
BAT_ID	2	AI	Battery ID pin	Connect the pin to GND with 100 KΩ resistor if the pin is unused

3.11.1 Charging Description

The module is integrated with charging function and supports USB-TYPE C interface CC detection specification [1)], but does not support VCONN, USB_PD protocol and custom cable.

The module has integrated Qualcomm battery gauge, and it is a hybrid of voltage and current based state of charge.

Table 22. Charge interface parameters

Parameters	Explain	Minimum Value	Typical Value	Maximum Value	Unit
V_{max}	USB maximum input voltage	--	--	16	V
V_{usb}	USB operating input voltage	3.6	5	6	V
V_{TRKL}	Trickle charge to pre-charge threshold	2	2.1	2.2	V
I_{TRKL}	Trickle charge current	90	100	110	mA

Parameters	Explain	Minimum Value	Typical Value	Maximum Value	Unit
V_{P2F}	Pre-charge to fast-chargevoltage threshold	2.1	--	3.4	V
I_{PRE_CHG}	Pre-charge current range	200	300	350	mA
I_{FC}	Fast charge current range[2)]	0	1.3	2	A
I_{TERM}	Charge termination current range	50	100	750	mA
$I_{BAT-SNS}$	Battery current sensing range	-5	--	5	A
ACC	Average State of Charge accuracy	-2	--	2	%
BAT_THERM	Thermistor supported range	10	10	100	kΩ
BAT_ID	BAT_ID resistor supported range	7.5	100	450	kΩ
I_{OTG_5V}	OTG output current[3)]	--	--	500	mA

1. The internal charging function of the module depends on CC detection and requires the use of TYPE C connector. Charging will not be supported when using the micro-B.
2. The maximum power is 5V2A. The actual charging current may be lower than 2A depending on the protocol type and battery level. The default configuration of the software is I_{FC} =1.3A, and it is recommended that the maximum current should not exceed 1.44A.
3. The module supplies a regulated 5.0V output (sourced by the battery) at the USB_IN pin for powering peripherals compliant with the USB OTG specifications.

3.12 Motor Driver Interface

Table 23. Motor interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
VIB_DRV_P	37	PO	Motor driver pin	Connect to the positive terminal of the motor

3.13 LCD

The screen interface is based on MIPI_DSI standard and supports one set of 4-Lane high-speed differential data transmission. It supports 1080P resolution.

Table 24. LCD pin definition

Pin Name	Pin No.	I/O	Description	Remarks
MIPI_DSI0_CLK_N	52	AO	LCD MIPI-DSI signal	--
MIPI_DSI0_CLK_P	53	AO		--
MIPI_DSI0_LN0_N	54	AO		--
MIPI_DSI0_LN0_P	55	AO		--
MIPI_DSI0_LN1_N	56	AO		--
MIPI_DSI0_LN1_P	57	AO		--
MIPI_DSI0_LN2_N	58	AO		--
MIPI_DSI0_LN2_P	59	AO		--
MIPI_DSI0_LN3_N	60	AO		--
MIPI_DSI0_LN3_P	61	AO		--
PWM	44	DO	LCD backlight brightness PWM	--

Pin Name	Pin No.	I/O	Description	Remarks
			control	
LCD_RST	49	DO	LCD reset signal	--
LCD_TE	50	DI	LCD swipe synchronization signal	--
VDD_2V8	130	PO	2.8V voltage output	--
LDO15_1V8	129	PO	LDO L15 1.8V power output	--

The reference circuit of LCD interface is as follows:

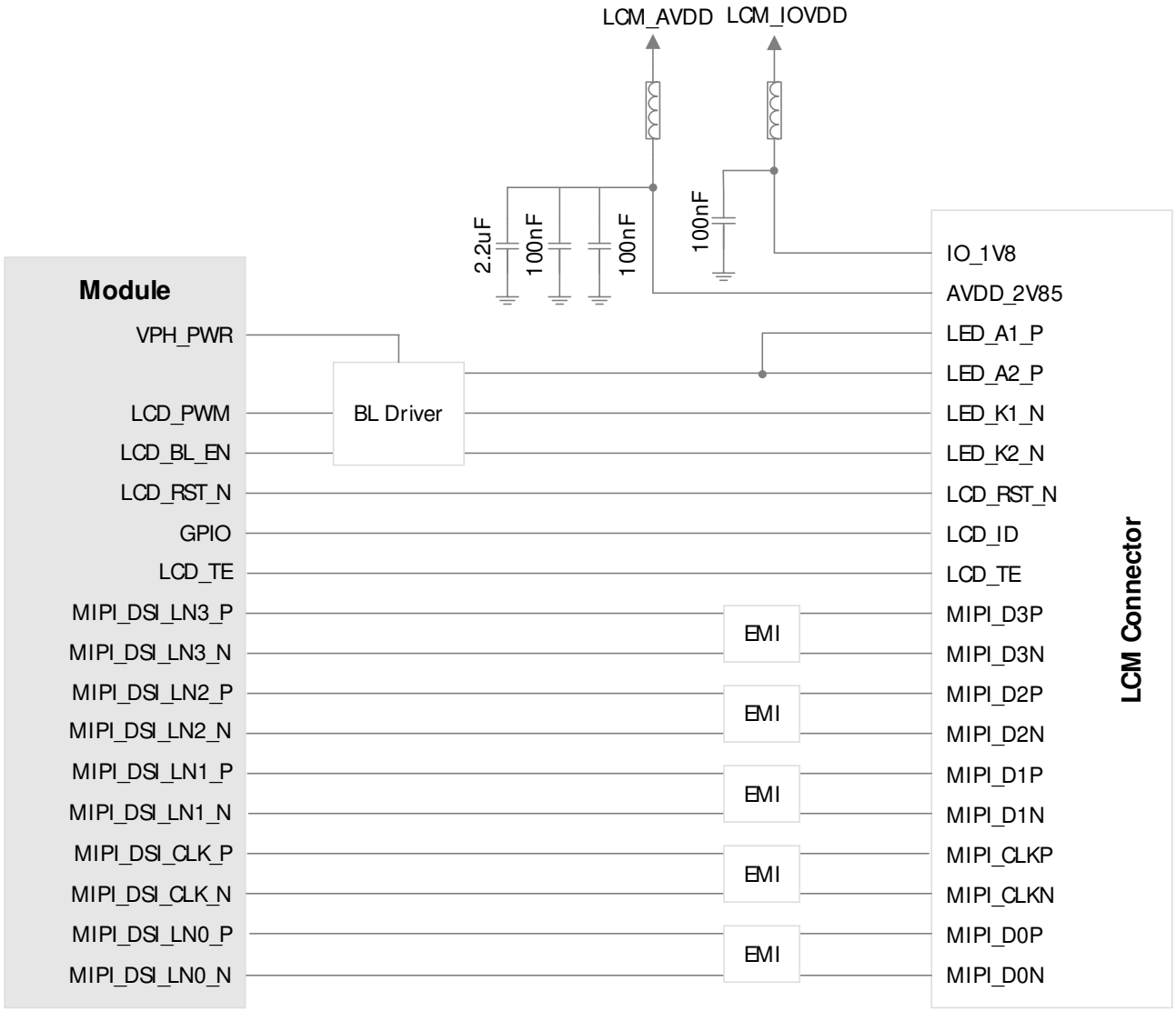

Figure 15. LCD reference circuit

Precautions for LCD design:

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;
- The MIPI signal line needs to be controlled with a 100 Ω differential impedance with tolerance ±10%;
- The total length of the cable shall not exceed 300 mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67 mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3 mm;
- EMI components are optional, and the whole routing stray capacitance should be controlled under 1pF;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

3.14 TP

The module provides one set of I^2C interfaces that can be used to connect to the TP and the module provides power, interrupt, reset pins required for the TP. The pin definition of the module is shown in the following table:

Table 25. TP pin definition

Pin Name	Pin No.	I/O	Description	Remarks
VDD_2V8	130	PO	2.8V voltage output	--
LDO15_1V8	129	PO	LDO L15 1.8V power output	--

Pin Name	Pin No.	I/O	Description	Remarks
TP_INT	42	DI	TP interrupt	--
TP_RST	43	DO	TP reset signal	--
TP_I2C_SCL	41	DO	TP I²C clock signal	--
TP_I2C_SDA	150、158	DI/DO	TP I²C data signal	--

TP reference circuit design is as follows:

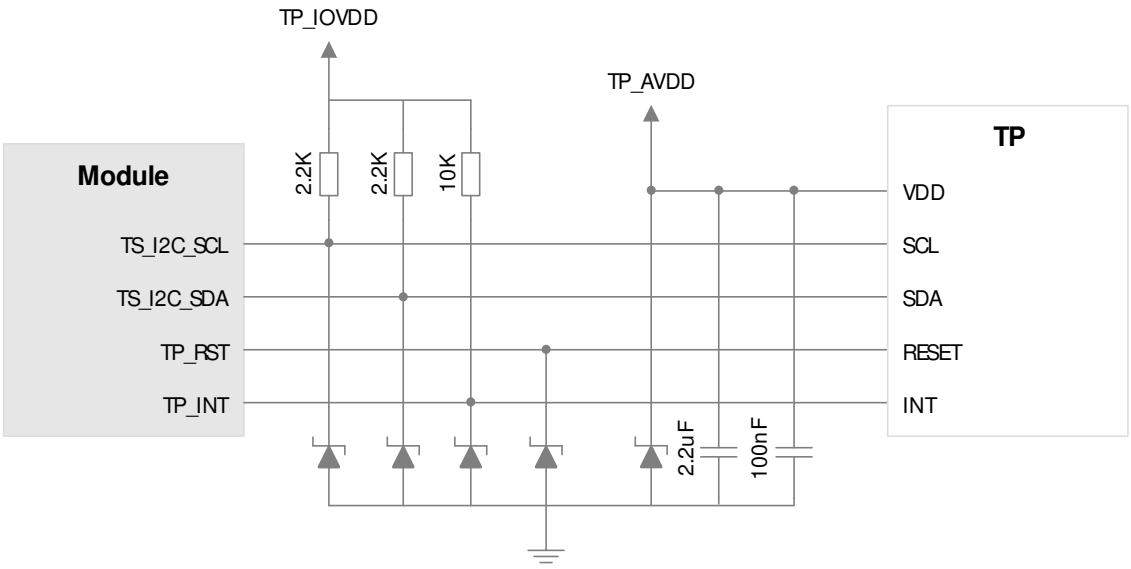

Figure 16. TP reference circuit design

3.15 Camera

The camera interface of module is based on the MIPI_CSI standard, and can support two (4 Lane + 4 Lane) or three (4 Lane + 2 Lane + 1 Lane) cameras. The maximum resolution is 25 MP. The pin definition of camera interface is as follows:

Table 26. Camera interface pin definition

Pin Name	Pin No.	I/O	4-lane + 2-lane + 1-lane
MIPI_CSI0_CLK_P	64	AI	4-lane camera MIPI-CSI0 interface. Keep the unused pins unconnected.
MIPI_CSI0_CLK_N	63	AI	

Pin Name	Pin No.	I/O	4-lane + 2-lane + 1-lane
MIPI_CSI0_LN0_N	65	AI	
MIPI_CSI0_LN0_P	66	AI	
MIPI_CSI0_LN1_N	67	AI	
MIPI_CSI0_LN1_P	68	AI	
MIPI_CSI0_LN2_N	183	AI	
MIPI_CSI0_LN2_P	181	AI	
MIPI_CSI0_LN3_N	179	AI	
MIPI_CSI0_LN3_P	180	AI	
MIPI_CSI1_CLK_N	70	AI	
MIPI_CSI1_CLK_P	71	AI	
MIPI_CSI1_LN0_N	72	AI	2-lane camera CSI1 interface. Keep the unused pins unconnected.
MIPI_CSI1_LN0_P	73	AI	
MIPI_CSI1_LN1_N	185	AI	
MIPI_CSI1_LN1_P	184	AI	
MIPI_CSI1_LN3_N	189	AI	
MIPI_CSI1_LN3_P	188	AI	1-lane camera CSI2 interface (LN3 as MIPI_CLK)
MIPI_CSI1_LN2_N	187	AI	
MIPI_CSI1_LN2_P	186	AI	
MCAM_MCLK	75	DO	Camera 0 clock signal
MCAM_RST	80	DO	Camera 0 reset signal
MCAM_PWDN	81	DO	Camera 0 shutdown signal
SCAM_MCLK	76	DO	Camera 1 clock signal

Pin Name	Pin No.	I/O	4-lane + 2-lane + 1-lane
SCAM_RST	82	DO	Camera 1 reset signal
SCAM_PWDN	83	DO	Camera 1 shutdown signal
DCAM_PWDN	215	DO	Camera 2 shutdown signal
DCAM_RST	214	DO	Camera 2 reset signal
DCAM_MCLK	213	DO	Camera 2 clock signal
CAM_I2C_SCL0	84	DO	I^2C clock signal of camera 0
CAM_I2C_SDA0	85	DI/DO	I^2C data signal of camera 0
CAM_I2C_SCL1	206	DO	I^2C clock signal of camera 1/2
CAM_I2C_SDA1	208	DI/DO	I^2C data signal of camera 1/2
IOVDD_1V8	122	PO	LDO 1.8V power output
VREG_CAM_AVDD_2P8	222	PO	Camera power output
VREG_CAM_AF_2P8	224	PO	Camera VIB power output
External LDO			
VDD_1V2	--	--	The module does not have this power supply, so it needs to be provided by an external high-power noise suppression ratio LDO

3.15.1 Camera 0

The reference circuit design of camera 0 is as follows:

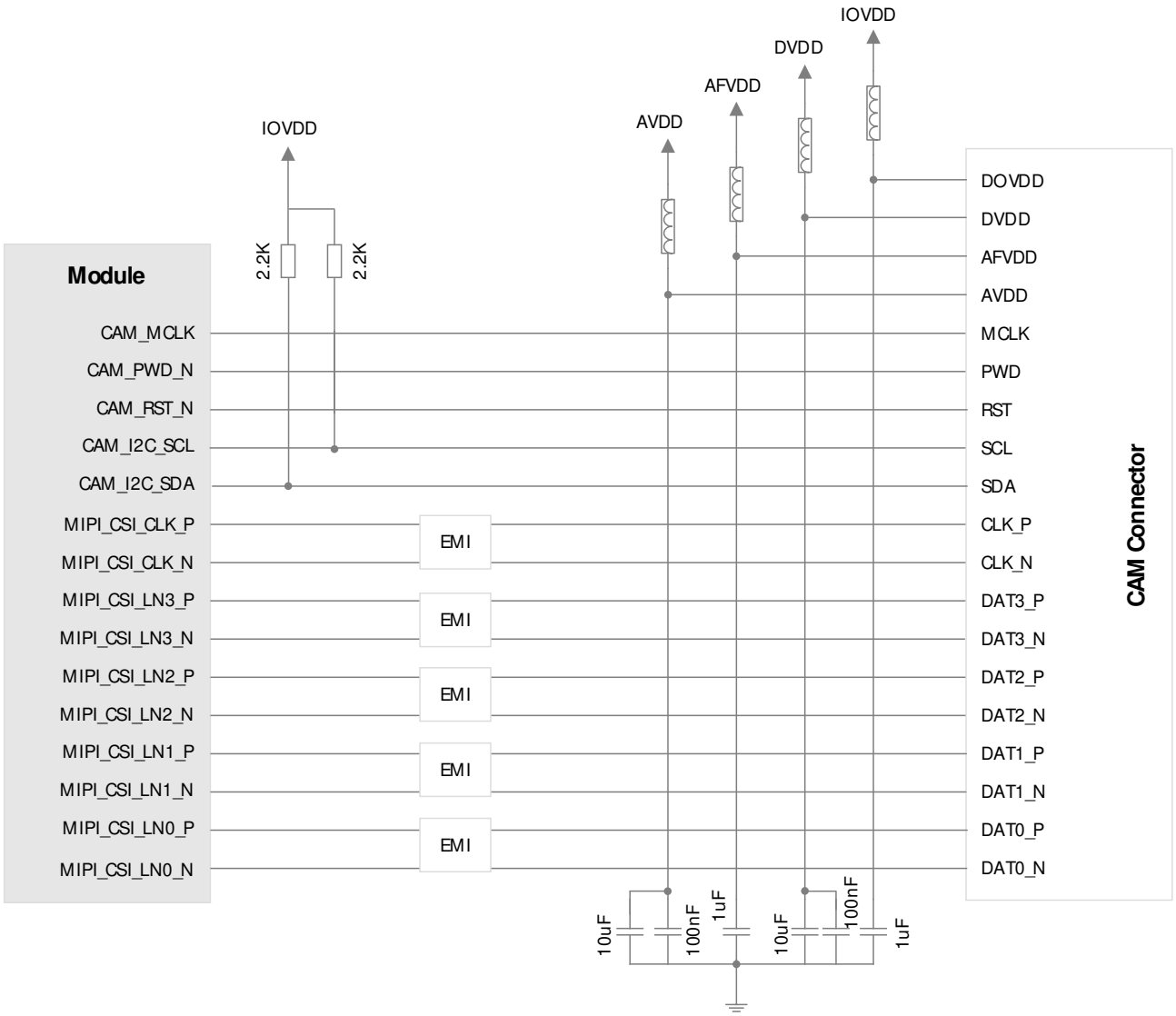

Figure 17. Reference circuit design of camera 0

3.15.2 Camera 1

The reference circuit design of camera 1 is as follows:

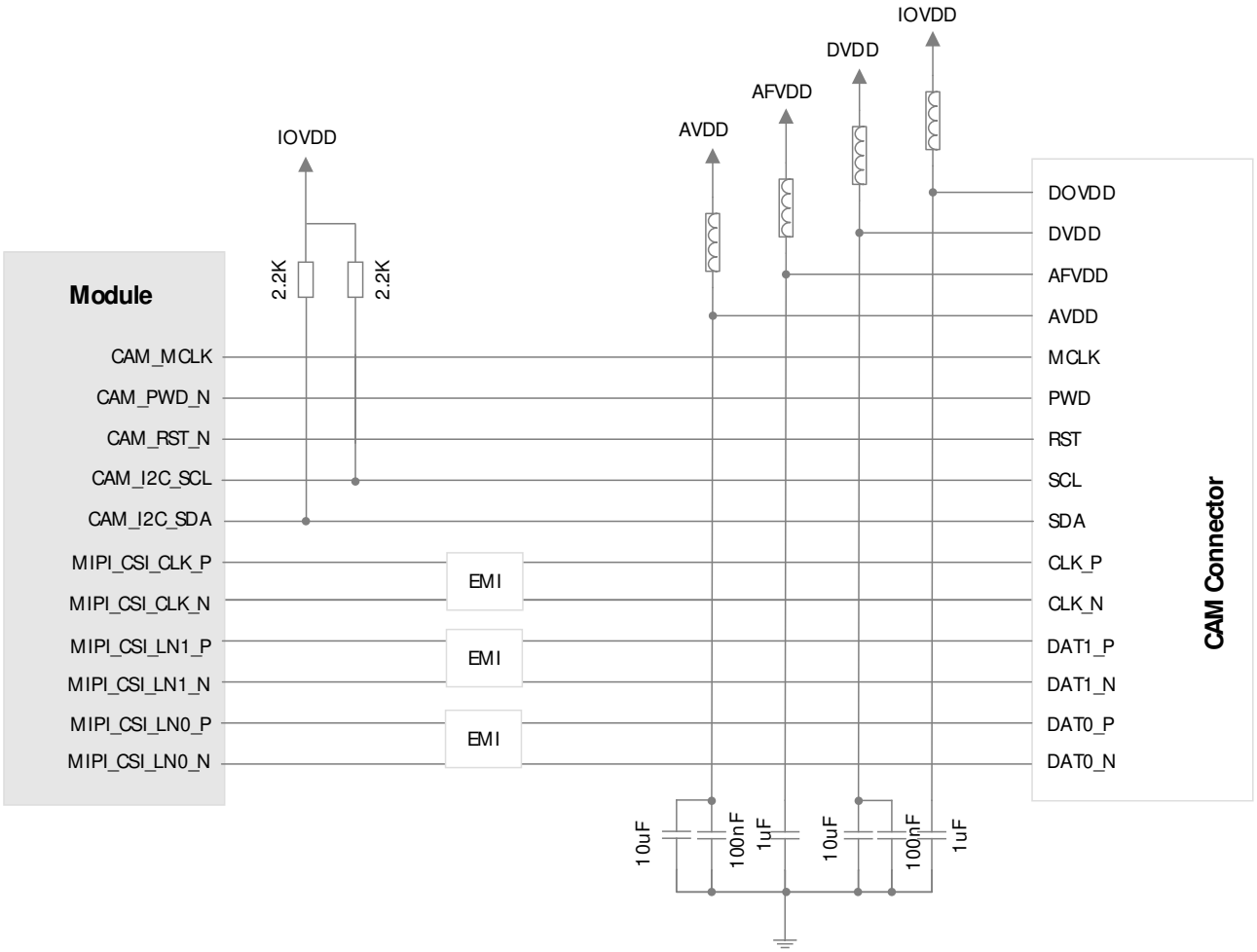

Figure 18. Reference circuit design of camera 1

3.15.3 Camera 2

The reference circuit design of camera 2 is as follows:

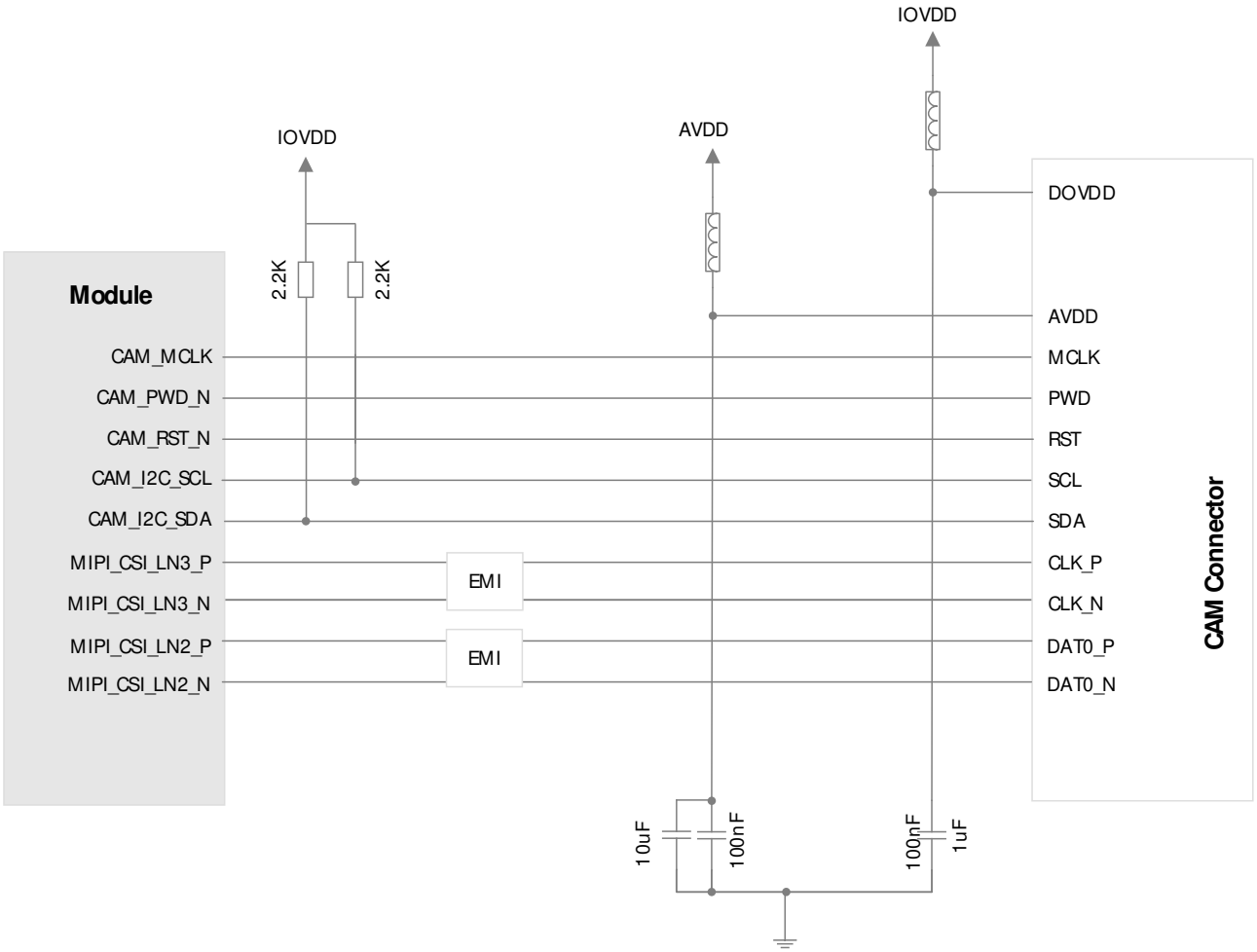

Figure 19. Reference circuit design of camera 3

3.15.4 Design Considerations

MIPI_CSI is a high-speed signal line. Pay attention to the following points during PCB layout.

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the camera connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;
- The MIPI signal line needs to be controlled with a 100 Ω differential impedance with tolerance ±10%;

- The total length of the cable shall not exceed 300 mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67 mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3 mm;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width ;

Design considerations for other signal cable:

- CAM_MCLK is a high-speed clock signal cable and requires fully grounded.
- The camera AVDD power supply routing should be away from interference sources to avoid interference of power noise;
- It is recommended to add LDO with high PSRR ability to the camera AVDD power supply;
- VDD_1V2 should be provided by external high-power noise reduction ratio LDO.
- If you need both two cameras to work at the same time, don't choose to share I2C. If you need to share I^2C, confirm that the I^2C addresses of the two cameras are unique.

3.16 Audio

3.16.1 Definition of Audio Interface

The module supports analog audio interface, and has 3 inputs and 3 outputs. Pin definition is as follows:

Table 27. Audio interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
MIC1_P	145	AI	Main MIC input+	--
MIC1_M	144	AI	Main MIC input-	--

Pin Name	Pin No.	I/O	Description	Remarks
MIC2_P	142	AI	Headphone MIC input+	--
MIC3_P	244	AI	Secondary MIC input+	--
MIC3_M	233	AI	Secondary MIC input-	--
EAR_P	134	AO	Receiver output+	--
EAR_M	135	AO	Receiver output-	--
SPK_PDRV_P	148	AO	Differential speaker output+	It already has PA built in
SPK_PDRV_M	147	AO	Differential speaker output-	
HPH_R	137	AO	Headphone right channel output	--
HPH_GND	138	/	Headphone reference ground	It requires to be grounded.
HPH_L	139	AO	Headphone left channel output	--
HPH_DET	140	AI	Headphone plug detection	--

Audio interface design consideration:

- The MIC_BIAS bias circuit is already set internally, so that you do not need to add it;
- The reference ground of the headphone should be grounded near the connector;
- Differential speaker interface cannot connect to external PA. If necessary, use the headphone interface;
- It is recommended to use receiver with 32 Ω impedance;
- Reduce noise and improve audio quality, the following approaches are recommended:
  - Keep audio PCB routing away from the antenna and high-frequency digital signal;

◦ Reserve LC filter circuit in audio circuit to reduce EMI;

◦ Shield the audio routing.

3.16.2 MIC Circuit Design

It is recommended to use a silicon MIC, and the reference design circuit is as follows:

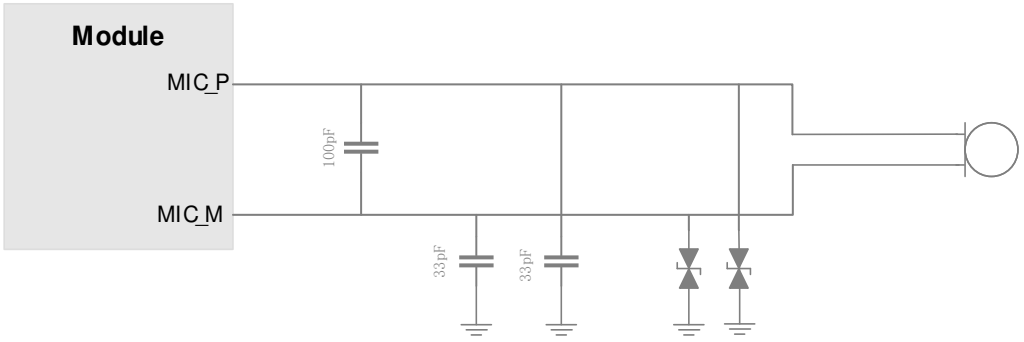

Figure 20. Microphone circuit design

3.16.3 Receiver Circuit Design

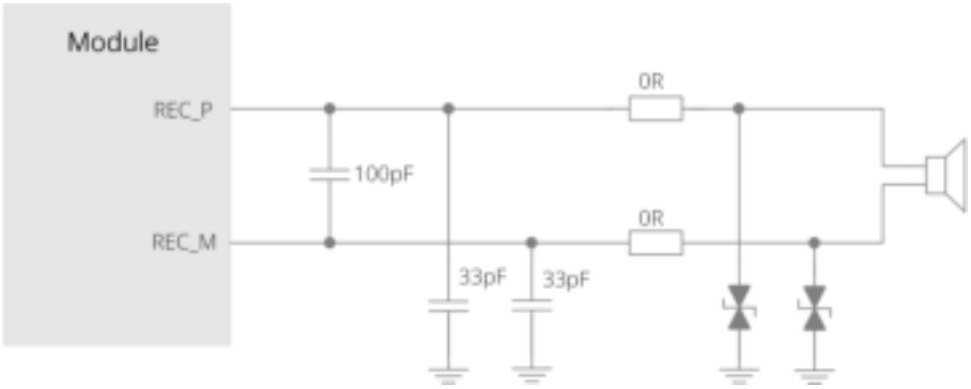

Figure 21. Receiver circuit design

3.16.4 Headphone Interface Circuit Design

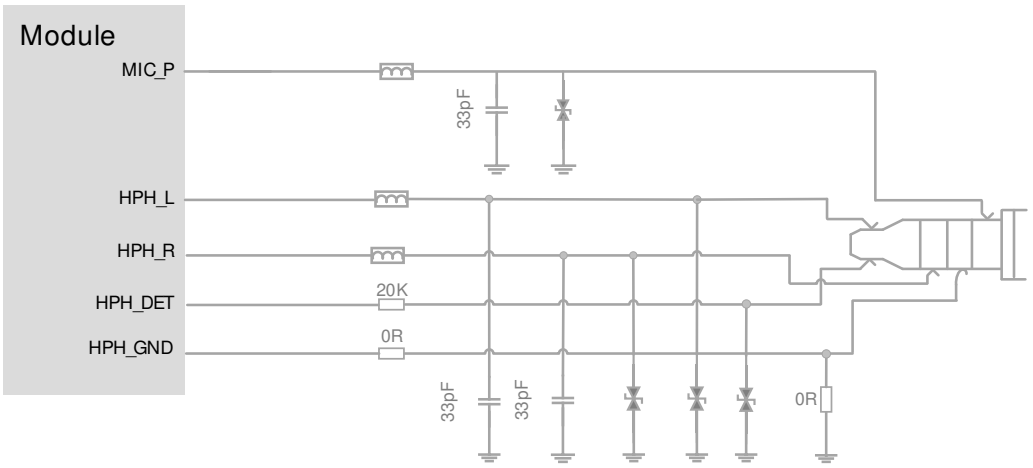

Figure 22. Headphone interface circuit design

Use a bi-directional TVS tube for the ESD protection device of the headphone interface.

3.17 Force Download Interface

The module provides KEY_FORCE_BOOT pin as an emergency download interface. Connect the KEY_FORCE_BOOT pin with LDO15_1V8 pin when powering on, and the module can enter the emergency download mode, which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. The reference circuit is as follows:

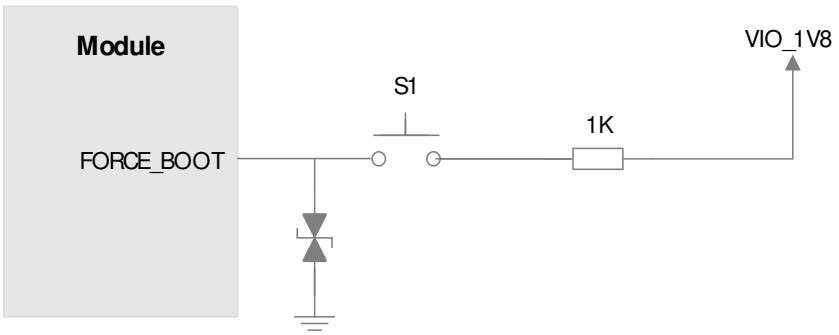

Figure 23. Design of forced download interface

4 Antenna Interface

The module supports 2G/3G/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

The module provides two 2G/3G/4G antenna interfaces. The ANT_MAIN is used to receive and transmit RF signal, and the ANT_DRX is used for diversity reception.

Table 28. MAIN/DRX antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
ANT_MAIN	94	AI/AO	2G/3G/4G main antenna interface	--
ANT_DRX	132	AI	4G diversity antenna interface	--

4.1.1 Operating Bands

Table 29. SC128-EAU operating band

Mode	Band	TX (MHz)	RX (MHz)
GSM	850	824-849	869-894
	900	880-915	925-960
	1800	1710-1785	1805-1880
	1900	850-1910	1930-1990
WCDMA	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 5	824-849	869-894
	Band 8	880-915	925-960

Mode	Band	TX (MHz)	RX (MHz)
LTE FDD	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 8	880-915	925-960
	Band 20	832-862	791-821
	Band 28	703-748	758-803
LTE TDD	Band 38	2570-2620	2570-2620
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690

Table 30. SC128-NA operating band

Mode	Band	TX（MHz）	RX（MHz）
	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 12	699-715.9	729-745.9
	Band 13	777-786.9	746-755.9
	Band 17	704-715.9	734-745.9
	Band 25	1850-1915	1930-1995

Mode	Band	TX（MHz）	RX（MHz）
	Band 26	814-849	859-894
	Band 66	1710-1780	2110-2200
	Band 71	663-698	617-652
LTE TDD	Band 41	2496-2690	2496-2690

4.1.2 Circuit Reference Design

For use of the module, the antenna pin and the RF connector or antenna feed point on the main board should be connected via an RF route. A microstrip is recommended as the RF cable, the insertion loss must be within 0.2 dB, and the impedance must be 50 Ω. A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel devices are directly connected across the RF route without branch pulled out. It is recommended to reserve the TVS device welding position at the antenna interface. The reference circuit is shown below:

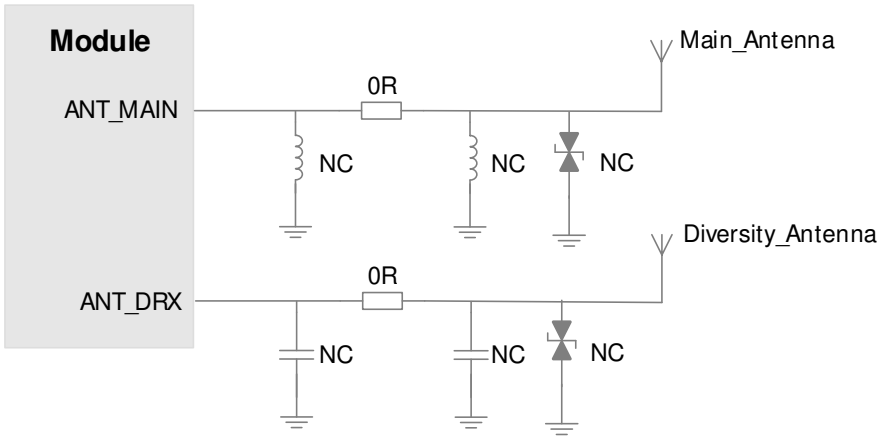

Figure 24. Antenna reference circuit

4.2 WIFI/BT Antenna

Microstrip route is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

Table 31. WIFI/BT antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
WIFI/BT_ ANT	78	AI/AO	WIFI/BT antenna interface	--

4.2.1 Operating Bands

Table 32. Operating band

Mode	Frequency	Unit
WIFI	2402 - 2482	MHz
	5170 - 5835	MHz
BT	2402 - 2480	MHz

4.2.2 Circuit Reference Design

The reference circuit of WIFI/BT antenna is shown as follows:

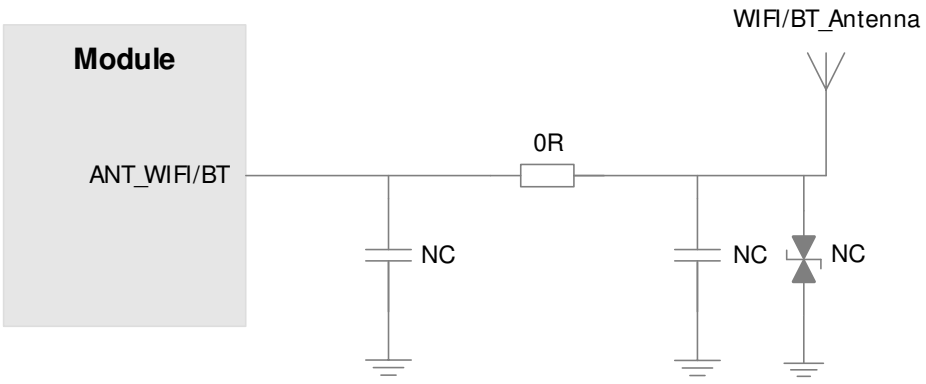

Figure 25. Antenna reference circuit

4.3 GNSS Antenna

GNSS supports GPS, GLONASS, and BeiDou.

Table 33. GNSS antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
GNSS_ANT	120	I	GNSS antenna interface	--

4.3.1 GNSS Operating Frequency

Table 34. GNSS operating frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42 - 1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 Circuit Reference Design

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip route is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50Ω. The GNSS antenna reference design is shown as follows:

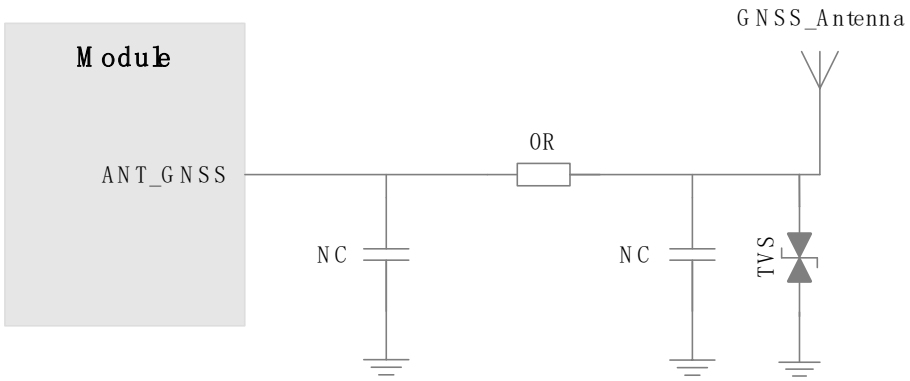

Figure 26. GNSS passive antenna reference circuit

For passive antenna, it is recommended to add a TVS with a junction capacitance of less than 0.5 pF; CJ: 0.5 pF; clamping voltage: 5.0 V. Recommended unit: ESD9D5U.

The active antenna reference circuit is shown in the following figure:

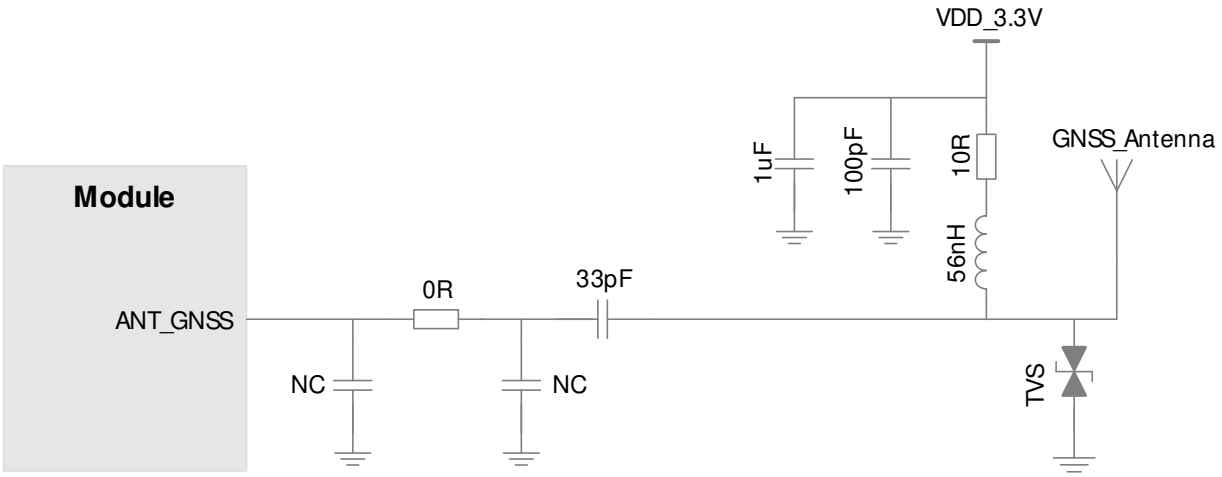

Figure 27. GNSS active antenna connection

The power of the active antenna is fed from the antenna's signal line through a 56 nH inductor. Common active antennas supply power is from 3.3-5.0 V. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-PSRR LDO be used to power the antenna. The gain of the active antenna is required to be <17db. If the gain is >17db, the reserved π-type matching must be used to increase the attenuation network.

4.4 Antenna Requirements

The module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 35. Antenna requirements

Module Antenna Requirement	
Standard	Antenna Requirement
LTE	VSWR: <2 (typical) Gain (dBi): 1 Max input power (W): 5

Module Antenna Requirement	
	Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: <1dB (0.7-1 GHz) Insertion loss: <1.5dB (1.4-2.2 GHz) Insertion loss: <2dB (2.3-2.7 GHz) *[SC128-NA gain]: LTE B2: 4dBi LTE B4: 3dBi LTE B5: 3dBi LTE B7: 4dBi LTE B12: 3dBi LTE B13: 3dBi LTE B17: 3dBi LTE B25: 4dBi LTE B26: 3dBi LTE B41: 4dBi LTE B66: 3dBi LTE B71: 3dBi
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1 dB *[SC128-NA gain]: BT&2.4G WIFI: 1.83dBi 5G WIFI: 5150MHz to 5250MHz: 4.29dBi 5250MHz to 5350MHz: 4.43dBi 5470 to 5725MHz: 3.68dBi 5725MHz to 5850MHz: 1.47dBi
GNSS	Frequency range: 1559 MHz to 1607 MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0 dBi Active antenna NF: < 1.5 dB (typical) Active antenna gain: > -2 dBi
Isolation between GPS and main antenna	> 20 dB
Isolation between WIFI and LTE antenna	> 20 dB

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal routes should be controlled at 50 Ω. In general, the impedance of the RF signal route is determined by the dielectric constant of the material, the route width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually is implemented in two ways: microstrip route and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide when the impedance line is at 50 Ω.

- Microstrip cable complete structure

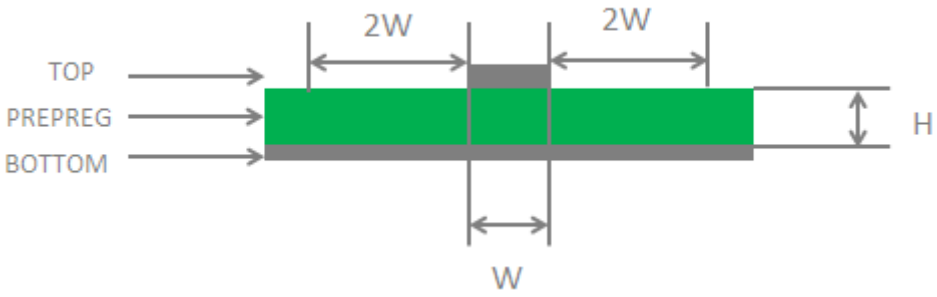

Figure 28. Two-layer PCB microstrip line structure

- Coplanar waveguide complete structure

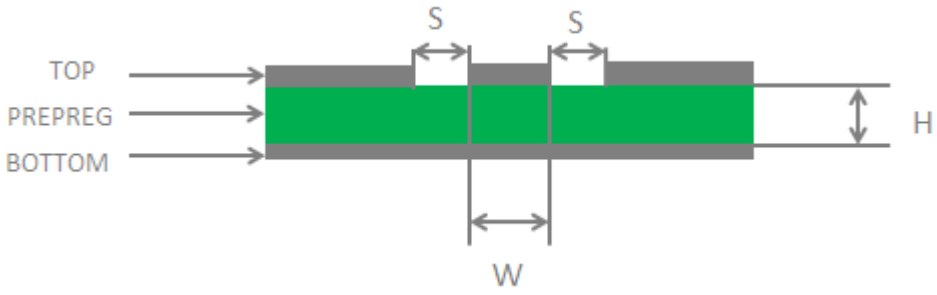

Figure 29. Two-layer PCB coplanar waveguide structure

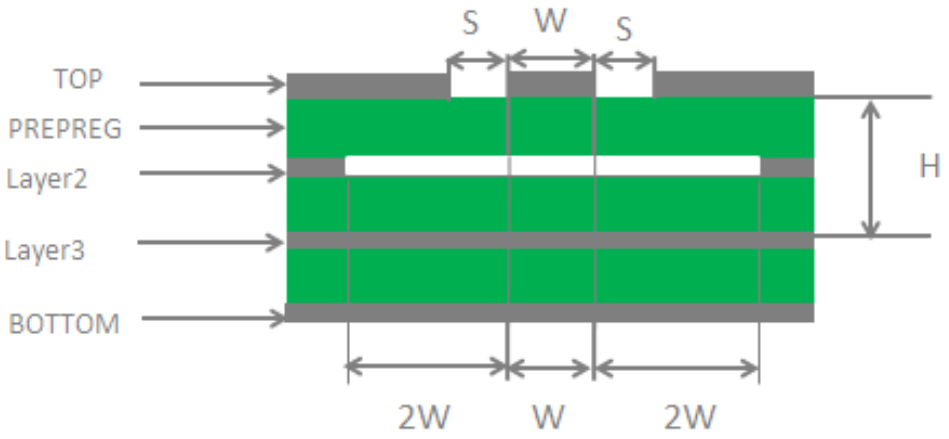

Figure 30 Four-layer PCB coplanar waveguide structure (see ground layer 3)

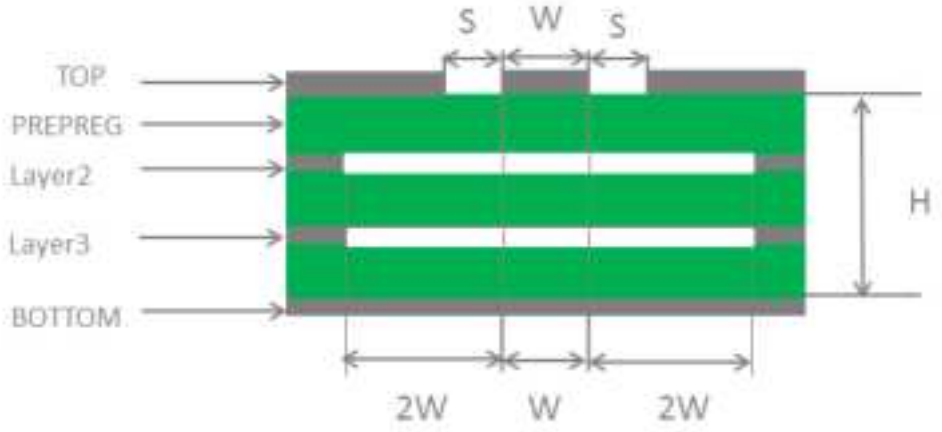

Figure 31. Four-layer PCB coplanar waveguide structure (see ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

Design principles:

- The impedance simulation tool should be used to accurately control the RF signal line at 50 Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degrees.

- When building connector package, keep the signal pin away from the ground.
- The reference ground plane of the RF signal line should be complete; a certain number of ground holes are added around the signal line and the reference ground to help improve the RF performance;
- and the distance between the ground holes and the signal line should be at least 2 times of the line width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4 G and 5 G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum rate up to 433 Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40 (If you need to open 2.4 G WIFI 40 M, you need to configure INI file, but it is not recommended)
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 Bluetooth Overview

The module supports BT5.0 (BR/EDR + BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1 MHz and can accommodate 79 channels. The BLE can accommodate 40 channels. Its main features are as follows:

- BT 5.0 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 36. BT rate and version information

Version	Data Rate	Throughput	Note
BT1.2	1 Mbit/s	> 80 Kbit/s	--
BT2.0 + EDR	3 Mbit/s	> 80 Kbit/s	--
BT3.0 + HS	24 Mbit/s	Refer to 3.0+HS	--
BT4.2 LE	24 Mbit/s	Refer to 4.2 LE	--
BT5.0	24 Mbit/s	Refer to 5.0	--

7 GNSS

7.1 Overview

The module supports multiple positioning systems including GPS, GLONASS and BeiDou. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 GNSS Performance

Test condition: 3.8 V power supply, environment temperature 25°C.

Table 37. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-157	dBm
C/No	-130 dBm	39	dB-Hz
TTFF	Cold Start	44	s
	Warm Start	40	s
	Hot Start	2.5	s
CEP	Static accuracy (95% @-130dbm)	5	m

8 Electricity, Reliability and RF Performance

8.1 Recommended Parameters

Table 38. Recommended parameters

Parameter	Min	Normal	Max	Unit
Battery voltage	3.5	3.8	4.4	V
USB_VBUS	4.75	5	5.25	V
RTC voltage	2.45	3.0	3.35	V
Operating temperature	-30	25	75	°C
Storage temperature	-40	25	85	°C

8.2 Operating Current

Test condition: 3.8 V power supply, environment temperature 25°C.

Table 39. SC128-EAU operating current

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Leakage current before power on	40	uA
	Normal power-off	Power off leakage current	44	
I_{sleep}	Radio Off	AT+CFUN=4 airplane Mode	5.4	mA
	GSM	MFRMS = 5	7	
	WCDMA	DRX = 8	8	
	TDD LTE	DPC (Default Paging Cycle) = #256	8	

Parameter	Description	Condition	Typical Result	Unit
	FDD LTE	DPC (Default Paging Cycle) = #256	8	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850 @ PCL=5	249	mA
		GSM850 @ PCL=19	97	
		EGSM900 @ PCL=5	254	
		EGSM900 @ PCL=19	97	
		DCS1800 @ PCL=0	210	
		DCS1800 @ PCL=15	90	
		PCS1900 @ PCL=0	210	
		PCS1900 @ PCL=15	90	
$I_{GSM-MAX}$	GSM voice Peak current	GSM850 @ PCL=5	2400	mA
		EGSM900 @ PCL=5	2400	
		DCS1800 @ PCL=0	1700	
		DCS1900 @ PCL=0	1700	
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@ Gamma=3 (1UL/4DL)	246	
		GSM850@ Gamma=3 (4UL/1DL)	640	
		EGSM900@ Gamma=3 (1UL/4DL)	245	
		EGSM900@ Gamma=3 (4UL/1DL)	631	
		DCS1800@ Gamma=3 (1UL/4DL)	190	
		DCS1800@ Gamma=3 (4UL/1DL)	500	
		PCS1900@ Gamma=3 (1UL/4DL)	170	
		PCS1900@ Gamma=3 (4UL/1DL)	500	
$I_{EGPRS-RMS}$	EGPRS data	GSM850@ Gamma=6 (1UL/4DL)	180	mA

Parameter	Description	Condition	Typical Result	Unit
	RMS Current	GSM850@ Gamma=6 (4UL/1DL)	446	
		EGSM900@ Gamma=6 (1UL/4DL)	180	
		EGSM900@ Gamma=6 (4UL/1DL)	430	
		DCS1800@ Gamma=5 (1UL/4DL)	170	
		DCS1800@ Gamma=5 (4UL/1DL)	500	
		PCS1900@ Gamma=5 (1UL/4DL)	200	
		PCS1900@ Gamma=5 (4UL/1DL)	510	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power	597	mA
		Band2@ max power	585	
		Band3@ max power	612	
		Band5@ max power	686	
		Band8@ max power	670	
$I_{LTE-RMS}$	FDD data RMS Current	Band1@max power (10MHz, 1RB)	695	mA
		Band2@max power (10MHz, 1RB)	700	
		Band3@max power (10MHz, 1RB)	690	
		Band4@max power (10MHz, 1RB)	725	
		Band5@max power (10MHz, 1RB)	640	
		Band7@max power (10MHz, 1RB)	770	
		Band8@ max power (10MHz,1RB)	729	
		Band20@max power (10MHz, 1RB)	600	
		Band28@max power (10MHz, 1RB)	627	
	TDD data	Band38@ max power (10MHz,1RB)	420	mA

Parameter	Description	Condition	Typical Result	Unit
	RMS Current	Band40@max power (10MHz, 1RB)	380	
		Band41@max power (10MHz, 1RB)	450	

Table 40. SC128-NA operating current

Parameter	Description	Condition	Typical Result	unit
I_{off}	Static leakage current	Leakage current before power on	40	uA
	Normal power-off	Power off leakage current	44	
I_{sleep}	Radio Off	AT+CFUN=4 airplane Mode	5.4	mA
	TDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD data RMS Current	Band2@ max power(10MHz,1RB)	660	
		Band4@ max power(10MHz,1RB)	695	
		Band5@ max power(10MHz,1RB)	680	
		Band7@ max power(10MHz,1RB)	770	
		Band12@ max power(10MHz,1RB)	600	
		Band13@ max power(10MHz,1RB)	650	
		Band17@ max power(10MHz,1RB)	695	
		Band25@ max power(10MHz,1RB)	650	
		Band26@ max	650	

Parameter	Description	Condition		Typical Result	unit
		power(10MHz,1RB)			
		Band66@ power(10MHz,1RB)	max	680	
		Band71@ power(10MHz,1RB)	max	650	
	TDD data RMS Current	Band41@ power(10MHz,1RB)	max	400	mA

8.3 RF Transmit Power

The transmit power of each band of the module is shown in the following table:

Test condition: 3.8 V power supply, environment temperature 25°C, LTE power test performed with 12 MHz bandwidth.

Table 41. RF transmitting power

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	850 (GMSK)	33±2	5±5
	900 (GMSK)	33±2	5±5
	1800 (GMSK)	30±2	0±5
	1900 (GMSK)	30±2	0±5
	850 (8PSK)	27.0±3	5±5
	900 (8PSK)	27.0±3	5±5
	1800 (8PSK)	26.0±3	0±5
	1900 (8PSK)	26.0±3	0±5
	Band 1	24+1/-3	<-49

Mode	Band	Max Power (dBm)	Min Power (dBm)
WCDMA	Band 2	24+1/-3	<-49
	Band 3	24+1/-3	<-49
	Band 5	24+1/-3	<-49
	Band 8	24+1/-3	<-49
LTE FDD	Band 1	23.0±2	<-39
	Band 2	23.0±2	<-39
	Band 3	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39
	Band 8	23.0±2	<-39
	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39
	Band 17	23.0±2	<-39
	Band 20	23.0±2	<-39
	Band 25	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 28	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD	Band 38	23.0±2	<-39
	Band 40	23.0±2	<-39
	Band 41	23.0±2	<-39

8.4 RF Receiver Sensitivity

The sensitivity of each frequency band of the module is shown in the following table:

Test condition: 3.8 V power supply, environment temperature 25°C, LTE power test performed with 10 MHz bandwidth. For RB configuration, see 3GPP standard.

Table 42. SC128-EAU RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
GSM	850	-109	-	-	-102	dBm
	900	-110	-	-	-102	dBm
	1800	-109	-	-	-102	dBm
	1900	-108	-	-	-102	dBm
WCDMA	Band 1	-109.5	-	-	-106.7	dBm
	Band 2	-109.5	-	-	-104.7	dBm
	Band 3	-109.5	-	-	-103.7	dBm
	Band 5	-110	-	-	-104.7	dBm
	Band 8	-110	-	-	-103.7	dBm
LTE FDD	Band 1	-97.3	-98.3	-100.3	-96.3	dBm
	Band 2	-97	-98.5	-100	-94.3	dBm
	Band 3	-97.5	-98	-100	-93.3	dBm
	Band 4	-97	-98	-100	-96.3	dBm
	Band 5	-98	-99	-100.5	-94.3	dBm
	Band 7	-96	-97	-100	-94.3	dBm
	Band 8	-99.3	-99.5	-102.3	-93.3	dBm
	Band 20	-97.5	-98	-100	-93.3	dBm
	Band 28A	-97	-98	-100	-94.8	dBm

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
	Band 28B	-97	-97	-99.5	-94.8	dBm
LTE TDD	Band 38	-96.3	-96.3	-98	-96.3	dBm
	Band 40	-96.3	-96.3	-99	-96.3	dBm
	Band 41	-94.5	-95	-97.5	-94.3	dBm

Table 43. SC128-NA RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	单位
LTE FDD	Band 2	-97	-98.5	-100	-96.3	dBm
	Band 4	-96.5	-98.5	-99.5	-94.3	dBm
	Band 5	-99	-99.5	-102	-93.3	dBm
	Band 7	-96.5	-98	-99.5	-96.3	dBm
	Band 12	-98	-98	-100.5	-94.3	dBm
	Band 13	-98	-98	-100.5	-94.3	dBm
	Band 17	-98	-98	-100.5	-93.3	dBm
	Band 25	-97.2	-99	-100	-93.3	dBm
	Band 26	-98.5	-99.5	-100.5	-94.8	dBm
	Band 66	-96.5	-98.5	-99	-94.8	dBm
	Band 71	-98.5	-97.5	-100	-94.8	dBm
LTE TDD	Band 41	-95	-97	-98	-94.3	dBm

8.5 Electrostatic Protection

In the application of the module, static electricity generated by human body and static electricity

generated by friction between micro-electronics are discharged to the module through various channels and may cause damage to the module. Therefore, ESD protection should be taken seriously. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should be added at the designed circuit interfaces and at the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

The following table lists ESD performance parameters (Temperature: 25°C, Humidity: 45%–65%):

Table 44. ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
Antenna Interface	±5	±10	KV
Other interfaces	±0.5	±1	KV

9 Structure Specifications

9.1 Product Appearance

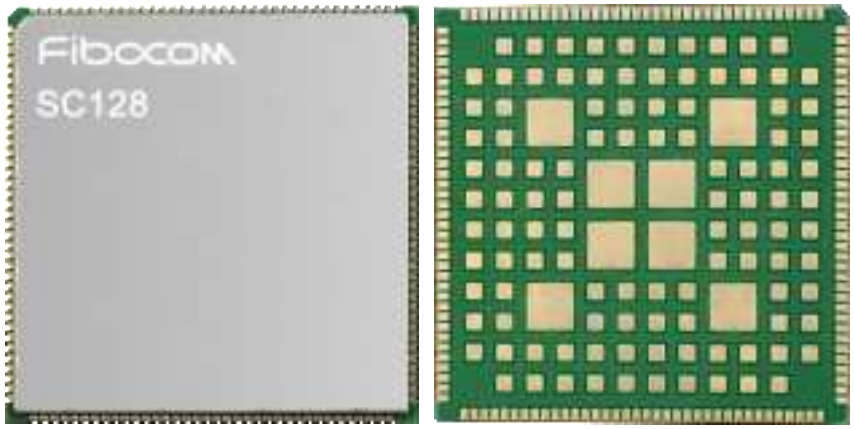

Figure 32. Product appearance

9.2 Structural Dimensions

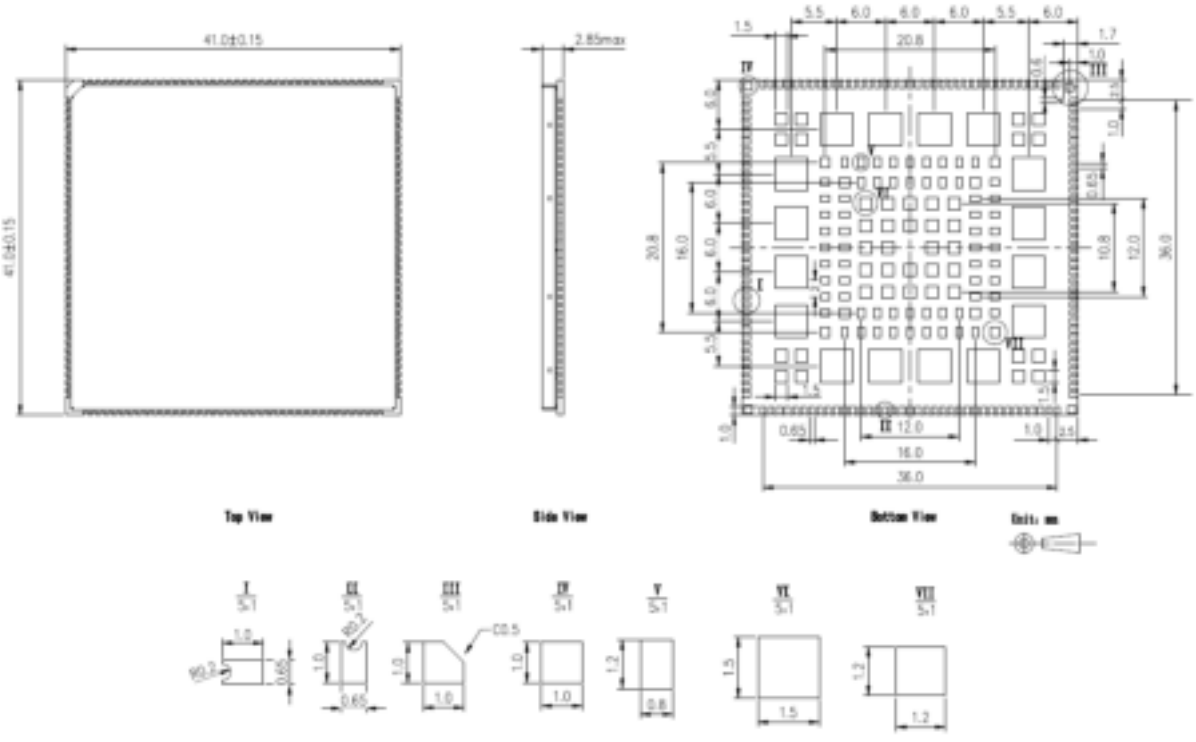

Figure 33. Structural dimensions

9.3 Recommended PCB Soldering Pad Design

For PCB soldering pad and stencil design, please refer to *Fibocom_SC128_SMT Design Guide*.

9.4 Recommended Thermal Design

For recommended module and peripheral thermal design, see *Fibocom_SC128_Thermal Design Guide*.

10 Production and Storage

10.1 SMT

See *Fibocom_SC128_SMT Design Guide*.

10.2 Packaging and Storage

See *Fibocom_SC128_SMT Design Guide*.

Appendix A Acronyms and Abbreviations

Table 45. Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

Abbreviation	Description
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value

Abbreviation	Description
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Appendix B GPRS Encoding Scheme

Table 46. GPRS encoding scheme

Encoding Method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

Appendix C GPRS Multi-timeslot

In the GPRS standard, 29 types of GPRS multi-timeslot modes are defined for mobile stations. The multi-timeslot class defines the maximum uplink and downlink rates, represented by 3+1 or 2+2. The first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications at the same time.

Table 47. Multislot allocation of different classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Appendix D EDGE Modulation and Encoding Method

Table 48. EDGE modulation and encoding method

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbit/s	18.1kbit/s	36.2kbit/s
CS-2	GMSK	/	13.4kbit/s	26.8kbit/s	53.6kbit/s
CS-3	GMSK	/	15.6kbit/s	31.2kbit/s	62.4kbit/s
CS-4	GMSK	/	21.4kbit/s	42.8kbit/s	85.6kbit/s
MCS-1	GMSK	C	8.80kbit/s	17.6kbit/s	35.2kbit/s
MCS-2	GMSK	B	11.2kbit/s	22.4kbit/s	44.8kbit/s
MCS-3	GMSK	A	14.8kbit/s	29.6kbit/s	59.2kbit/s
MCS-4	GMSK	C	17.6kbit/s	35.2kbit/s	70.4kbit/s
MCS-5	8-PSK	B	22.4kbit/s	44.8kbit/s	89.6kbit/s
MCS-6	8-PSK	A	29.6kbit/s	59.2kbit/s	118.4kbit/s
MCS-7	8-PSK	B	44.8kbit/s	89.6kbit/s	179.2kbit/s
MCS-8	8-PSK	A	54.4kbit/s	108.8kbit/s	217.6kbit/s
MCS-9	8-PSK	A	59.2kbit/s	118.4kbit/s	236.8kbit/s