BLOCK DIAGRAMS

A general description of the overall circuit is covered in the instruction manual. This section provides the description of circuits required by subpart 2.983 of the Commissions' rules. Circuits not described in the manual are covered in this exhibit.

This exhibit contains descriptions of the frequency generation, modulation and transmitter circuits in accordance with FCC Rules Part 2.983(d).

The following descriptions are included:

EXHIBIT 5A - Means for Frequency Stabilization, 2.983 (d) 10

EXHIBIT 5B - Means for Limiting Modulation and Attenuation of Higher Audio Frequencies, 2.983 (d) 11

EXHIBIT 5C - Means for Attenuation of Spurious Emissions, 2.983 (d) 11

EXHIBIT 5D - Means for Limiting Power Output, 2.983 (d) 11

EXHIBIT 5E - Modulation Techniques, 2.983 (d) 12

MEANS FOR FREQUENCY STABILIZATION

Circuit Description:

A 16.8 MHz Temperature Controlled Crystal Oscillator (TCXO), U5700 (a “Pendulum” oscillator), maintains frequency stability of the transmitted carrier. The TCXO features low current drain and a ±1.5-ppm frequency versus temperature capability. In addition, this TCXO offers digital tuning and a temperature referenced 5 bit Digital to Analog Converter (DAC). Frequency tuning has 128 steps of resolution.

The 16.8 MHz output frequency of the TCXO is divided into one of three reference frequencies in the fractional-N frequency synthesizer IC, U5702. These reference frequencies are compared to the divided outputs of the VCOs in a phase detector. The output of the phase detector provides a DC correction voltage back to the VCOs.

The carrier frequency for conventional operation, in the range of 896 to 902 MHz, is generated using a Bipolar Transistor, Q5706, configured as a voltage controlled oscillator (VCO). The Q5706 VCO also supplies the injection power for the first mixer of the receiver. The carrier frequency for talk-around operation, in the range of 937 to 943 MHz, is generated using a Bipolar Transistor, Q5704, configured as a voltage controlled oscillator (VCO). Only one VCO is operating during transmissions.

The output of one or the other of the VCOs is applied to the input of fractional-N, frequency synthesizer integrated circuit, U5702. U5702 consists of a phase-locked loop circuit with the output of the VCOs fed to a programmable divider chain. The divide ratios are determined from information stored in the Electrically Erasable Programmable Read Only Memory (EEPROM) in the microcomputer, U0101, and bussed to the synthesizer. The microcomputer extracts the data for the division ratios as determined by the mode (channel) of operation selected. Using a time averaged algorithm a combination of divide ratios is used so that the reference frequency can be a much higher value than the value of the frequency resolution. Modulation occurs by a combination of directly coupling the modulation signal to the low pass filter in the loop and by processing the modulation signal to alter the divider values.

A block diagram of the VCO/Synthesizer system is shown in Figure 5.1.

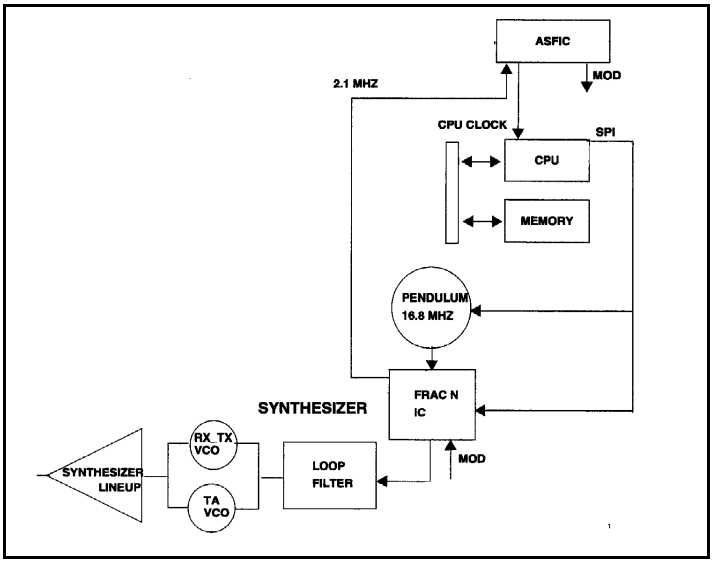

Figure 5.1 – Carrier Frequency Generation and Stabilization

MEANS FOR LIMITING MODULATION AND ATTENUATION OF HIGHER AUDIO FREQUENCIES

Circuit Description:

Modulation limiting is accomplished within the custom audio processor IC, U0201 ("ASFIC"). The limiting action itself occurs at the rails (i.e., 5V and ground). Using an operational amplifier with feedback, very hard limiting is obtained.

The limited modulation signal output of the limiter is applied to a low-pass filter in U0201. The filter is a fifth-order, Butterworth switched capacitor filter with the 3-dB roll-off corner frequency located at 3250 Hz.

The output of the low-pass filter is applied to the input of the electronic attenuator. The electronic attenuator is controlled by the microcomputer of the transceiver. To keep the deviation constant over the RF frequency range, the microcomputer adds the proper correction factor to the attenuator.

A block diagram of the limiting and low pass filtering is shown in figure 5.2.

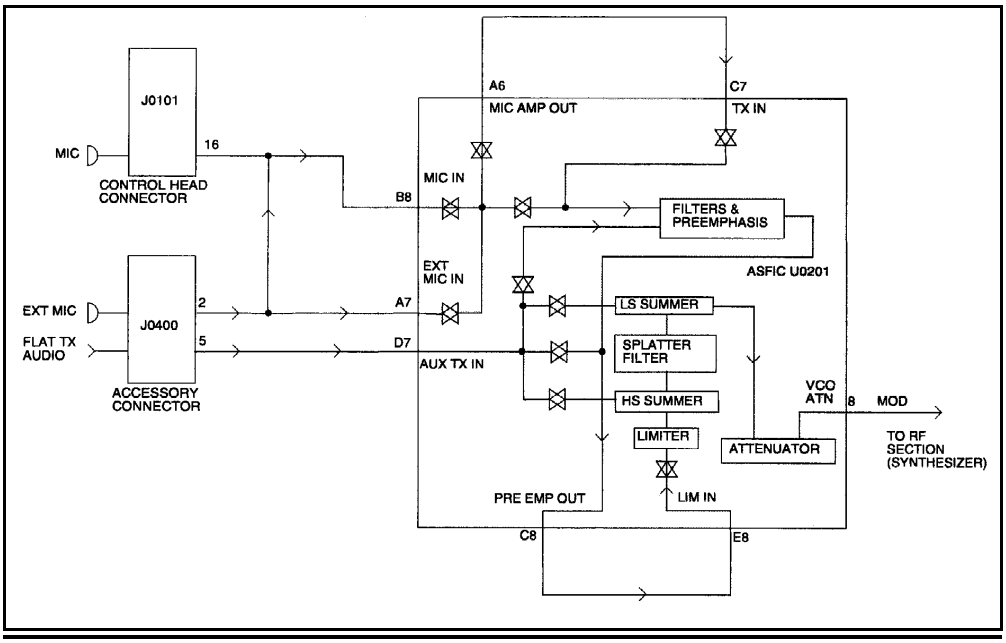

Figure 5.2 – Transmitter Modulation Limiting and Lowpass Filtering

MEANS FOR ATTENUATION OF SPURIOUS EMISSIONS

Circuit Description:

The final stage of the RF power amplifier circuit feeds a low-pass filter in order to attenuate harmonics of the output frequency as well as spurious outputs. The filter is a seventh-order, 0.1 dB Chebychev design using LC reactive elements.

Shielding of the transmitter RF power amplifier circuit also attenuates spurious emissions.

The circuit diagram may be found in Figure 5.3.

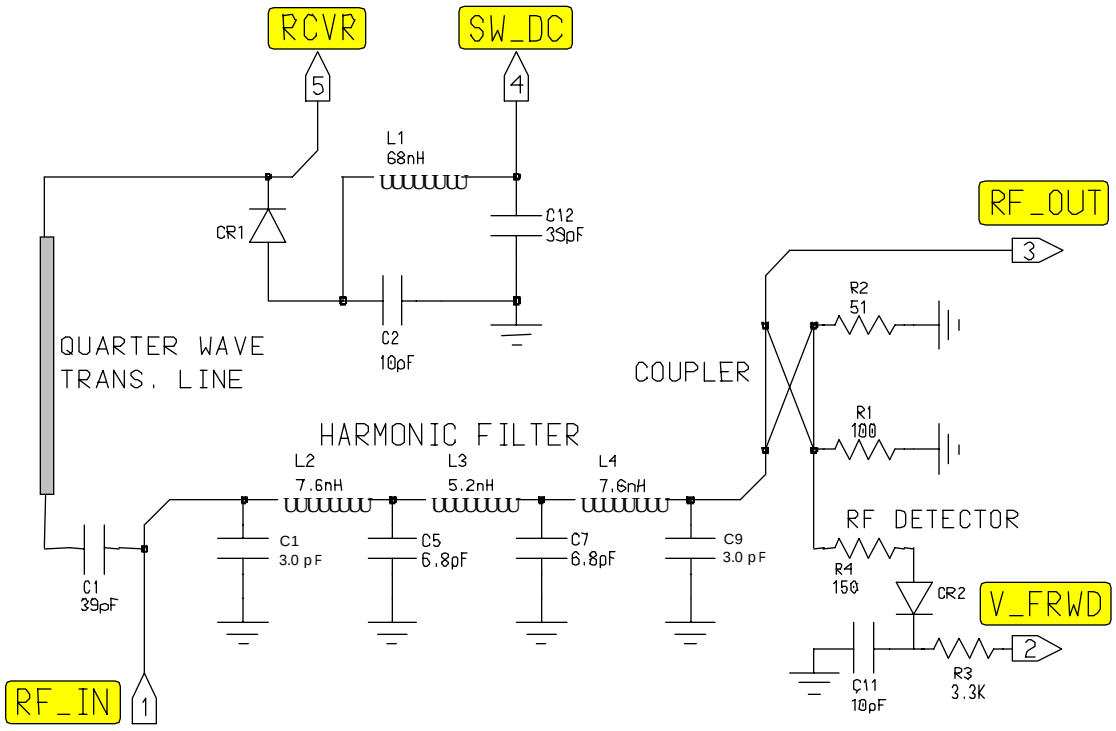

Figure 5.3 – Transmitter Lowpass Filter

MEANS FOR LIMITING POWER OUTPUT

Circuit Description

A forward power detecting, current sensing ALC loop regulates the output power of the transmitter.

The forward power detector is placed after the harmonic filter and before the antenna connector. The forward power detector is a microstrip printed circuit, directional coupler. A sample of the forward energy is rectified by CR6506 to produce a dc voltage proportional to the output power of the transmitter. That voltage is applied to the Power Control IC, U1503, and is compared to a preprogrammed voltage reference. Any difference between the two inputs generates an error voltage. The error voltage is amplified and the resulting output from the power control is used as a bias control voltage for the first transmitter stage, Q6501. The bias control voltage changes the gain of Q6501 to maintain constant dc voltage from the power detector and, therefore, transmitter output power.

The voltage drop across current sensing resistor R6520 is proportional to the collector current of the final power amplifier transistor, Q6505. The voltage drop is applied to the Power Control IC, U1503. That voltage is compared to a preprogrammed current limit reference. If the limit value is exceeded, an error voltage is generated. The error voltage is amplified and the resulting output from the power control is used as a bias control voltage for the first transmitter stage, Q6501. The bias control voltage changes the gain of Q6501 to limit the maximum current drain of the final power amplifier device and protects the device from over dissipation.

The circuit diagram of the power limiting circuit may be found in Figure 5.4.

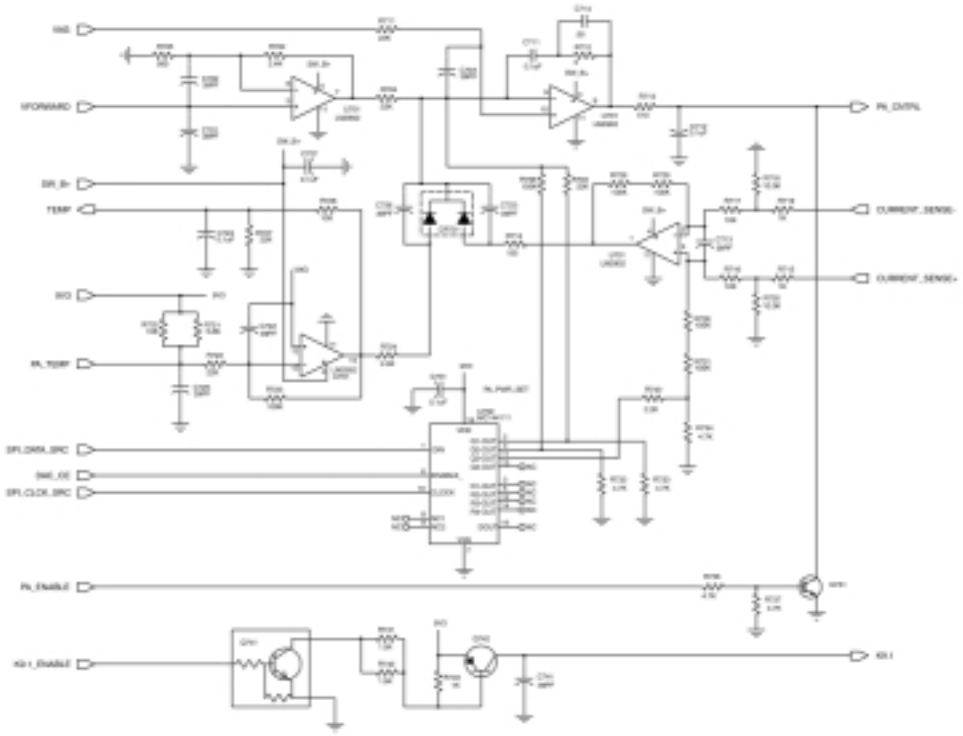

Figure 5.4 - Transmitter Power Limiting Circuit Diagram

Modulation Techniques

The transmitter is capable of the following types of modulation:

1) Modulation of TPL (Tone Private Line) - Direct FM tone modulation of 67 Hz to 250.3 Hz at 15% of full system deviation.

2) Modulation of DPL (Digital Private Line) - Direct FM modulation at 134 bits per second (BPS) at 15% of full system deviation.

3) Modulation of LTR® Lowspeed Trunking Data - Direct FM modulation at 300 BPS at up to 35% of full system deviation.

The signal that will directly frequency modulate the transmitter carrier for TPL, DPL and LTR lowspeed trunking data is generated by a 6-bit Digital to Analog Converter contained within the Audio and Signal Filtering IC (ASFIC), U201. The frequency determining clock signal, at 2.1 MHz is obtained from the Fractional-N synthesizer, U5702. A five pole, switched capacitor filter limits the bandwidth of the modulation signal. The output of the filter is applied to an electronic attenuator within U5702.

The microcomputer adjusts the attenuator in U5702 to compensate for modulation sensitivity variations of the synthesizer over the frequency range of the transmitter. This ensures the nominal 15% of full system deviation for TPL and DPL and up to 35% of full system deviation for LTR trunking lowspeed data is maintained regardless of the transmit frequency.

4) Modulation of Highspeed Trunking Data - Direct FM modulation at 3600 BPS at 70% of full system deviation.

Highspeed data refers to the 3600 bauds data that forms the Inbound Service Word (ISW) used in trunking systems. The ISW communicates with the Central Controller of the trunking system. The data signal that will directly frequency modulate the transmitter carrier for the highspeed trunking data is generated in the ASFIC, U201.

The microcomputer, U101, and the ASFIC, U201 generate the highspeed data. U101 programs the filter and gain settings of U201. U101 then strobes the “TRKCLKIN” input of U201 with a pulse whenever the polarity of the data is to change. The input to U201 is routed to an internal 5-3-2 State Encoder. For the highspeed trunking data, the Encoder is operating in the 2-state mode. The splatter filter in U201 limits the bandwidth of the output signal from the Encoder.

5) Modulation of DTMF tones at nominally 60% of full system deviation.

The microcomputer and the ASFIC are capable of generating seven, standard DTMF frequencies. These are divided into two groups, the low group for 697, 770 852, and 941 Hz, and the high group for 1209, 1336 and 1477 Hz.

The high group is generated by the microcomputer strobing the ASFIC input U201- G1 at six (6) times the tone frequency for the 1209 and 1336 Hz tones and at 2880 Hz for the 1440 Hz tone.

The low group tone is generated by the microcomputer strobing the ASFIC input U201-G2 at six (6) times the tone frequency.

The tones from the low group and the high group are summed in the ASFIC. Before summing, the amplitude of the tone from the high group is increased approximately 2-dB. The output of the tone summing stage is passed through the pre-emphasis network, the transmit audio summing stage and the splatter filter before modulating the RF carrier.