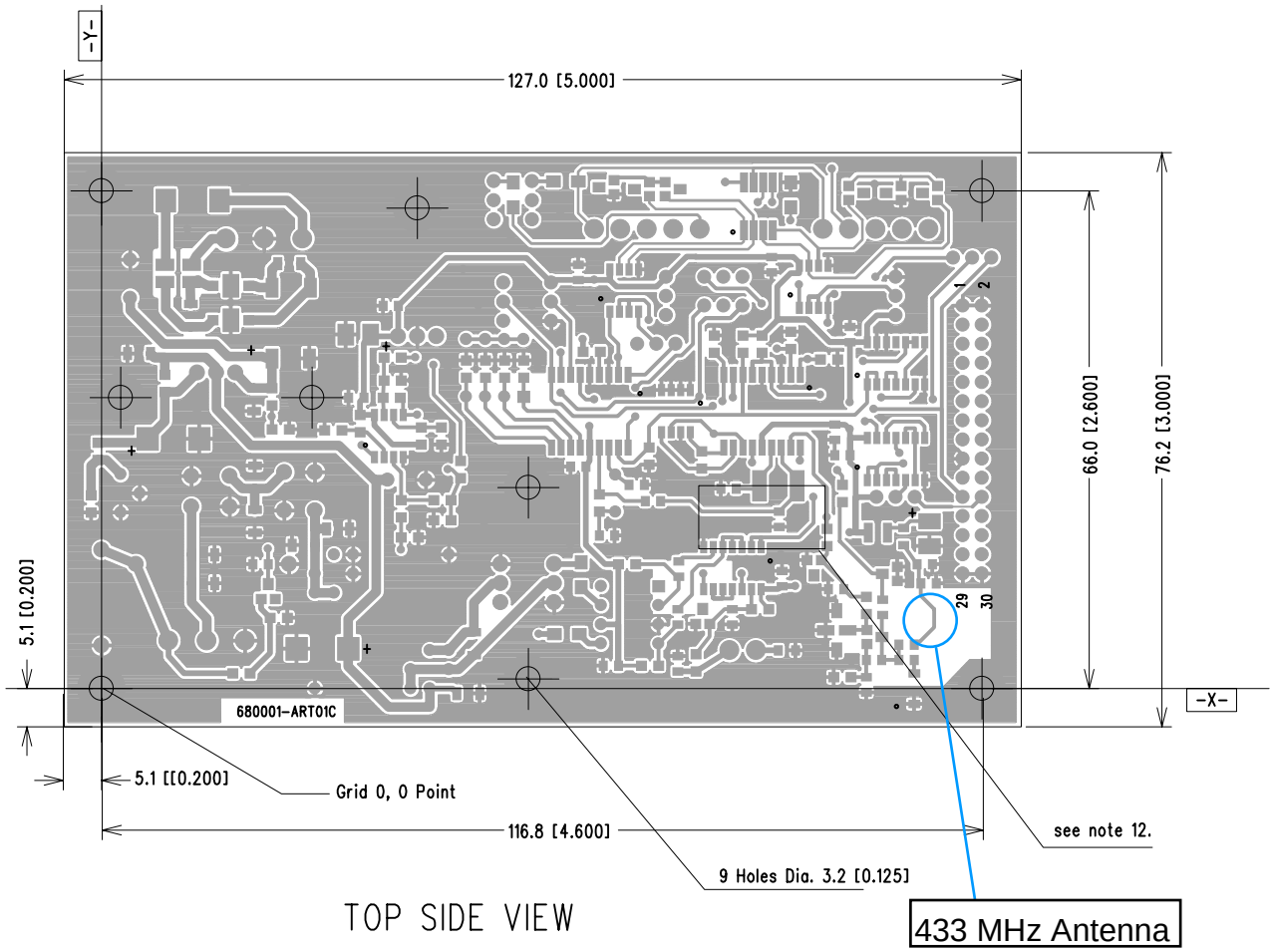

TOP SIDE VIEW

NOTE, unless otherwise stated:

1. PCB material : – Epoxy glass laminate FR4; permitivity @ 1 MHz; 4.2 – 4.9.
   – Core thickness 1.5 +/– 0.2 mm [0.059 +/– 0.008 in]
   – Cooper cladding 1 oz per sq. ft.
2. Minimum cooper plating in plated holes and on conductors to be 0.02[0.0008]
   All holes are plated–through.
3. Drill board using drill data provided. Holes locations may vary within
   0.004 in (Radial error) about true position. Minimum anular ring 0.005 in.
4. Solder mask on both side over bare coper. Thickness 0.0007 in min/0.002 in max.
   Material to be light green in color and highly transparent.
   Misregistration shall not exceed +/– 0.004 in.
   No overlap permitted on SMD rectangular lands.
5. PCB documentation include :
   – Master layout file 350882cm.pcb, dated 13/Jun/01
   – Artwork top side files art01.pho and art01.rep; layer 680001–ART01C
   – Artwork bottom side files art02.pho and art02.rep; layer 680001–ART02C
   – Solder mask top files sm0125.pho and sm0125.rep; layer 680001–SMT25C
   – Solder mask bottom files smo228.pho and sm0228.rep; layer 680001–SMB28C
   – Silk screen top side files sst0126.pho and sst0126.rep; layer 680001–SST26C
   – Silk screen bottom side files 350882cm–ssb0229.pho and 350882cm–ssb29.rep
   – Solder paste mask top files smd0122.pho and 0122.rep; layer 680001–SPT22C
   – Drill files drl00.drl, drl00.rep and drl00.lst; layer 680001–DRL24C
   All holes are platted. Drilling format Excellon, digits 2 integer
   3 decimal, leading zero suppresion, type absolute, units inches.
6. All exposed cooper surfaces shall be tin–lead coated.
   Minimum plating thickness on surface mount lands: 0.001 in
7. Silk–screen on top side of board using white epoxi base ink.
8. Finished conductor and space width tolerance is +/– 0.001 in.
9. Dimensions after etching and plating
   All dimensions and tolerances are expressed in mm {inch].
   Dimensions tolerance +/– 0.1 [0.0025].
10. Bow and rwist shall not exceed 1 % in accordance with
    IPC–TM–650, method 2.4.22.
11. Grid system used to locate componentsand holes is 0.005 in.
12. Board manufacturer shall apply date code and fabricator's
    I.D. on the silk–screen bottom side where indicated.
13. Overall PCB thickness: 1.6 [0.063].

REV	ECO NO	BY	CHK	DATE
C	019, 025	MPAU	MHUZ	08Jan97
B	003, 012	IMP	MH	27Jun96

KASTEN CHASE
Applied Research

BY	MPAU	10Feb97
CHK	MHUZ	10Feb97
APRV	DFER	10Feb97

NAME PCB EXT95
Raw Card

PART NO	DWG NO	REV
350882	900260	C

SCALE	SIZE	SHEET
– –	A	1 of 1