

APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

All 40 channels of transmitting, and receiving, frequencies are provided by PLL (Phase Locked Loop) (IC1) circuitry.

The purpose of the PLL is to provide a multiple number of frequencies from a VCO (Voltage Controlled Oscillator) with quartz crystal accuracy and stability locked to crystal oscillator reference frequency.

The reference crystal oscillator frequency is 4.5 MHz.

CIRCUITS AND DEVICES TO
STABILIZE FREQUENCY
FCC ID: MMA77235ESP

APPENDIX 7

ATTN = MR. WILLIAM WONG
C.C. = MR. SIT.

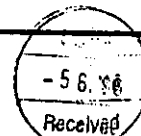
CMOS LSI

LC72322

SANYO

No. 4797A

Single-Chip Microcontroller with PLL and LCD Driver



Overview

The LC72322 is a single-chip microcontroller for use in electronic tuning applications. It includes on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. It features a large-capacity ROM, a highly efficient instruction set, and powerful hardware.

Functions

- Stack: Eight levels
- Fast programmable divider
- General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
- LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
- Program memory (ROM): 4 k words by 16 bits
- Data memory (RAM): 256 4-bit digits
- All instructions are single-word instructions
- Cycle time: 2.67 μ s, 13.33 μ s, or 40.00 μ s (option)
- Unlock FF: 0.55 μ s detection, 1.1 μ s detection
- Timer FF: 1 ms, 5ms, 25ms, 125ms
- Input ports*: One dedicated key input port and one high-breakdown voltage port
- Output ports*: Two dedicated key output ports, one high-breakdown voltage open-drain port
Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)
Seven CMOS output ports (mask option switchable to use as LCD ports)
- I/O ports*: One switchable between input and output in four-bit units and one switchable between input and output in one-bit units

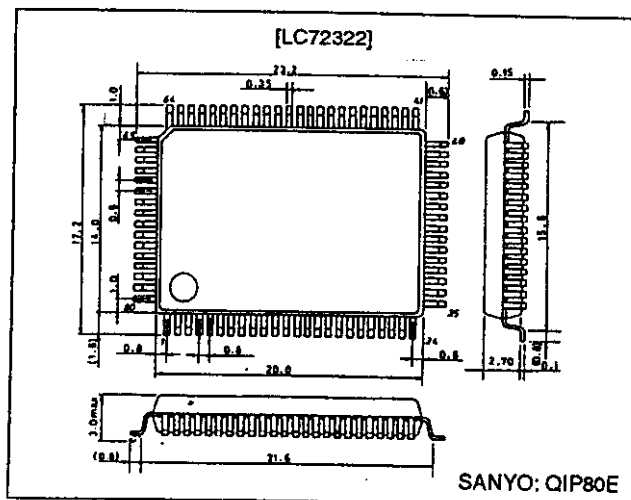
Note: * Each port consists of four bits.

- Program runaway can be detected and a special address set (Programmable watchdog timer).
- Voltage detection type reset circuit
- One 6-bit A/D converter
- Two 8-bit D/A converters (PWM)
- One external interrupt
- Hold mode for RAM backup
- Sense FF for hot/cold startup determination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V

Package Dimensions

unit: mm

3174-QFP80E



This LSI can easily use CCB that is SANYO's original bus format.

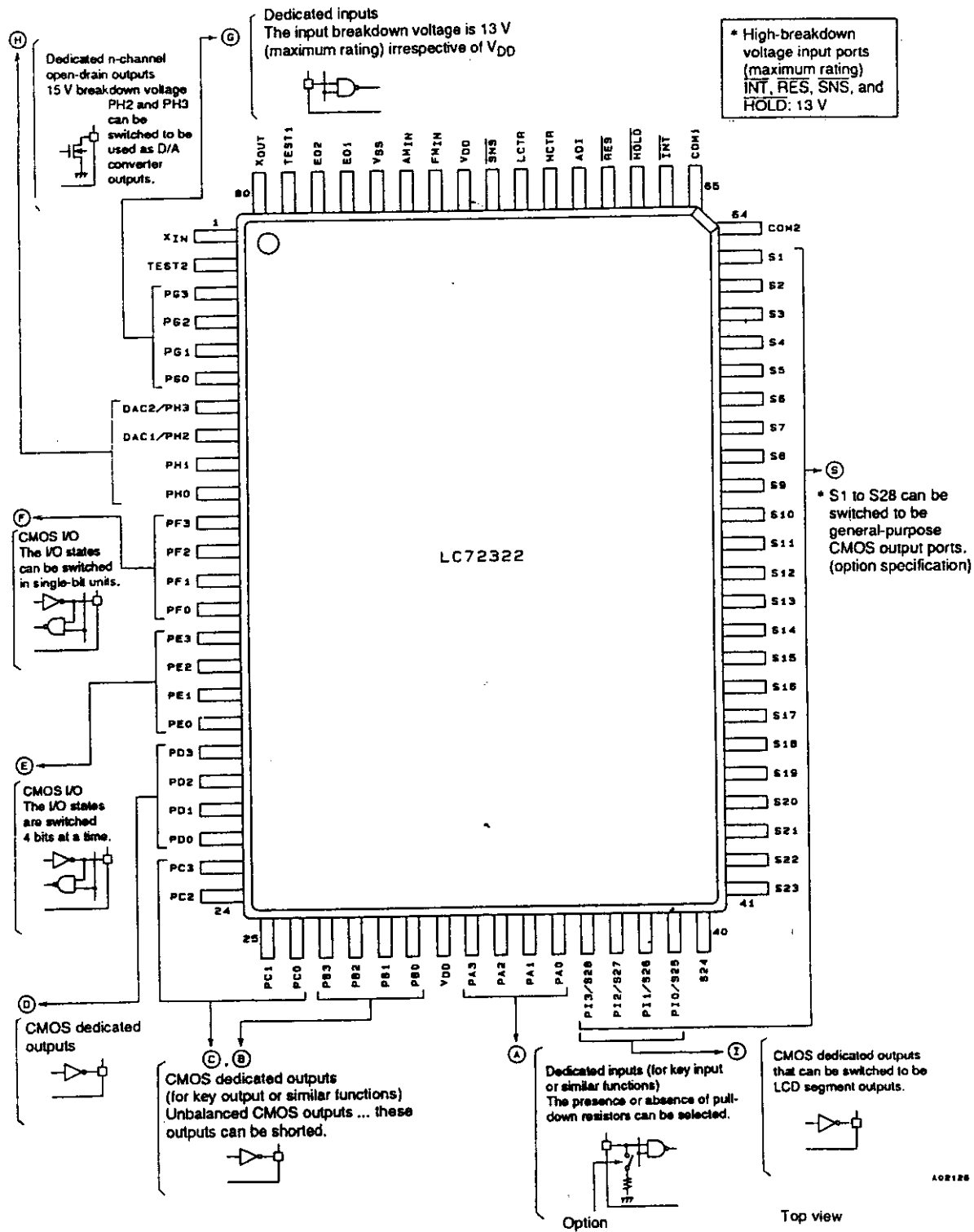


- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Hongo, Teito-ku, TOKYO 110 JAPAN

Pin Assignment



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	V_{IN1}	HOLD, INT, RES, ADI, SNS, and the G port	-0.3 to +13	V
	V_{IN2}	Inputs other than V_{IN1}	-0.3 to $V_{DD} + 0.3$	V
Output voltage	V_{OUT1}	H port	-0.3 to $V_{DD} + 0.3$	V
	V_{OUT2}	Outputs other than V_{OUT1}	-0.3 to $V_{DD} + 0.3$	V
Output current	I_{OUT1}	All D and H port pins	0 to 5	mA
	I_{OUT2}	All E and F port pins	0 to 3	mA
	I_{OUT3}	All B and C port pins	0 to 1	mA
	I_{OUT4}	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a = -40\text{ to }+85^\circ\text{C}$	300	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-45 to +125	$^\circ\text{C}$

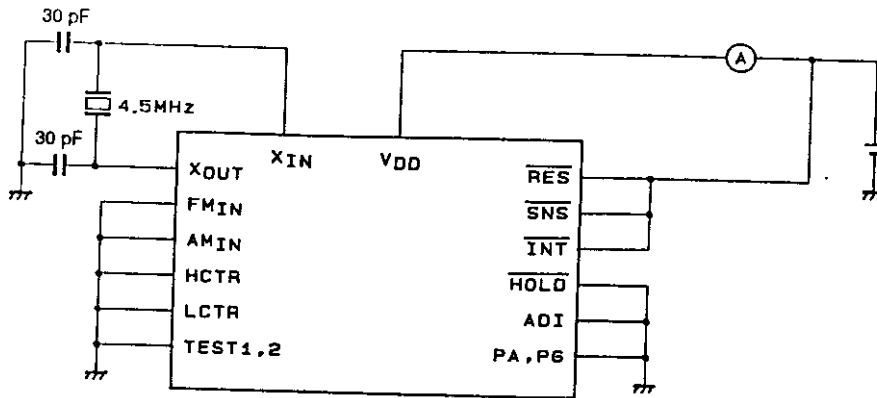
Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = 3.5\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	CPU and PLL operating	4.5		5.5	V
	V_{DD2}	CPU operating	3.5		5.5	V
	V_{DD3}	Memory retention voltage	1.3		5.5	V
Input high level voltage	V_{IH1}	G port	$0.7 V_{DD}$		8.0	V
	V_{IH2}	RES, INT, HOLD	$0.8 V_{DD}$		8.0	V
	V_{IH3}	SNS	2.5		8.0	V
	V_{IH4}	A port	$0.6 V_{DD}$		V_{DD}	V
	V_{IH5}	E, F port	$0.7 V_{DD}$		V_{DD}	V
	V_{IH6}	LCTR (period measurement), V_{DD1} , PE1, PE3	$0.8 V_{DD}$		V_{DD}	V
Input low level voltage	V_{IL1}	G port	0		$0.3 V_{DD}$	V
	V_{IL2}	RES, INT, PE1, PE3	0		$0.2 V_{DD}$	V
	V_{IL3}	SNS	0		1.3	V
	V_{IL4}	A port	0		$0.2 V_{DD}$	V
	V_{IL5}	PE0, PE2, F port	0		$0.3 V_{DD}$	V
	V_{IL6}	LCTR (period measurement), V_{DD1}	0		$0.2 V_{DD}$	V
	V_{IL7}	HOLD	0		$0.4 V_{DD}$	V
Input frequency	f_{IN1}	XIN	4.0	4.5	5.0	MHz
	f_{IN2}	FMIN, V_{IN2} , V_{DD1}	10		130	MHz
	f_{IN3}	FMIN, V_{IN3} , V_{DD1}	10		150	MHz
	f_{IN4}	AMIN (L), V_{IN4} , V_{DD1}	0.5		10	MHz
	f_{IN5}	AMIN (H), V_{IN5} , V_{DD1}	2.0		40	MHz
	f_{IN6}	HCTR, V_{IN6} , V_{DD1}	0.4		12	MHz
	f_{IN7}	LCTR (frequency), V_{IN7} , V_{DD1}	100		500	kHz
	f_{IN8}	LCTR (frequency), V_{IN6} , V_{IL6} , V_{DD1}	1		20×10^3	Hz
Input amplitude	V_{IN1}	XIN	0.50		1.5	Vrms
	V_{IN2}	FMIN	0.10		1.5	Vrms
	V_{IN3}	FMIN	0.15		1.5	Vrms
	$V_{IN4, 5}$	AMIN	0.10		1.5	Vrms
	$V_{IN6, 7}$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	V_{IN8}	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	LCTR (period), RES, INT, PE1, PE3	$0.1 V_{DD}$			V
Rejected pulse width	P_{REJ}	SNS			50	μs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Input high level current	I_{IH1}	INT, HOLD, RES, ADI, SNS, and the G port: $V_I = 5.5 V$			3.0	μA
	I_{IH2}	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD} . $V_I = V_{DD}$			3.0	μA
	I_{IH3}	XIN: $V_I = V_{DD} = 5.0 V$	2.0	5.0	15	μA
	I_{IH4}	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0 V$	4.0	10	30	μA
	I_{IH5}	A port: With an R_{PD} . $V_I = V_{DD} = 5.0 V$		50		μA
Input low level current	I_{IL1}	INT, HOLD, RES, ADI, SNS, and the G port: $V_I = V_{SS}$			3.0	μA
	I_{IL2}	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD} . $V_I = V_{SS}$			3.0	μA
	I_{IL3}	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	μA
	I_{IL4}	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	μA
Input floating voltage	V_{IF}	A port: With an R_{PD}			$0.05 V_{DD}$	V
Pull-down resistance	R_{PD}	A port: With an R_{PD} . $V_{DD} = 5.0 V$	75	100	200	k Ω
Output high level off leakage current	I_{OFFH1}	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	I_{OFFH2}	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	μA
	I_{OFFH3}	H port: $V_O = 13 V$			5.0	μA
Output low level off leakage current	I_{OFFL1}	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	I_{OFFL2}	B, C, D, E, F, and I ports: $V_O = V_{SS}$			3.0	μA
Output high level voltage	V_{OH1}	B and C ports: $I_O = 1 mA$	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
	V_{OH2}	E and F ports: $I_O = 1 mA$	$V_{DD} - 1.0$			V
	V_{OH3}	EO1, EO2: $I_O = 500 \mu A$	$V_{DD} - 1.0$			V
	V_{OH4}	XOUT: $I_O = 200 \mu A$	$V_{DD} - 1.0$			V
	V_{OH5}	S1 to S28 and the I port: $I_O = -0.1 mA$	$V_{DD} - 1.0$			V
	V_{OH6}	D port: $I_O = 5 mA$	$V_{DD} - 1.0$			V
	V_{OH7}	COM1, COM2: $I_O = 25 \mu A$	$V_{DD} - 0.75$	$V_{DD} - 0.5$	$V_{DD} - 0.3$	V
Output low level voltage	V_{OL1}	B and C ports: $I_O = 50 \mu A$	0.5	1.0	2.0	V
	V_{OL2}	E and F ports: $I_O = 1 mA$			1.0	V
	V_{OL3}	EO1, EO2: $I_O = 500 \mu A$			1.0	V
	V_{OL4}	XOUT: $I_O = 200 \mu A$			1.0	V
	V_{OL5}	S1 to S28 and the I port: $I_O = 0.1 mA$			1.0	V
	V_{OL6}	D port: $I_O = 5 mA$			1.0	V
	V_{OL7}	COM1, COM2: $I_O = 25 \mu A$	0.3	0.5	0.75	V
	V_{OL8}	H port: $I_O = 5 mA$, V_{DD1}	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_{M1}	COM1, COM2: $V_{DD} = 5.0 V$, $I_O = 25 \mu A$	2.0	2.5	3.0	V
A/D conversion error		ADI: V_{DD1}	-1/2		1/2	LSB
Current drain	I_{DD1}	V_{DD1} , $f_{IN2} = 130 MHz$		15	20	mA
	I_{DD2}	V_{DD1} , PLL stopped, CT = 2.67 μs (HOLD mode, Figure 1)		1.5		mA
	I_{DD3}	V_{DD1} , PLL stopped, CT = 13.33 μs (HOLD mode, Figure 1)		1.0		mA
	I_{DD4}	V_{DD1} , PLL stopped, CT = 40.00 μs (HOLD mode, Figure 1)		0.7		mA
	I_{DD5}	$V_{DD} = 5.5 V$, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			5	μA
		$V_{DD} = 2.5 V$, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			1	μA

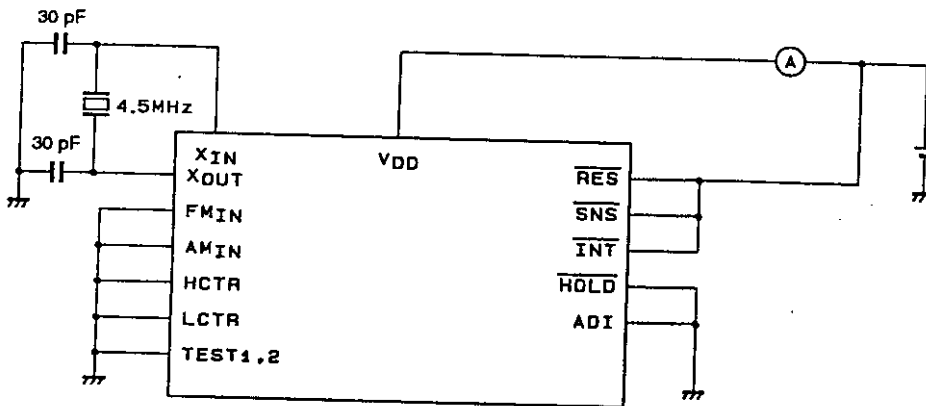
Test Circuits



Note: PB to PF, PH, and PI are all open. However, PE and PF are output selected.

A02105

Figure 1 I_{DD2} to I_{DD4} in HOLD Mode

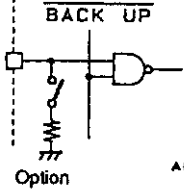
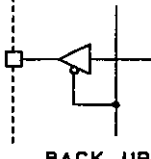
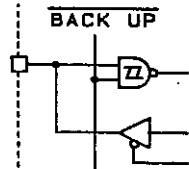
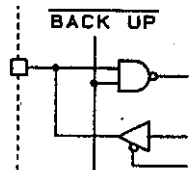
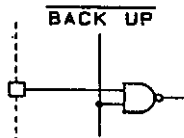


Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

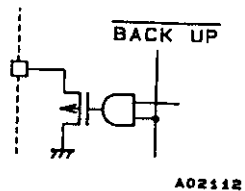
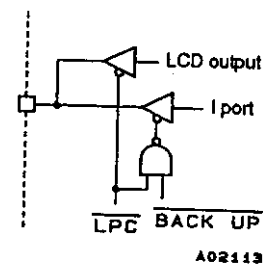
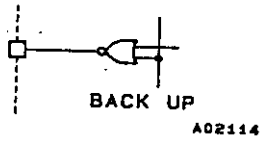
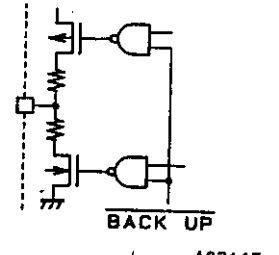
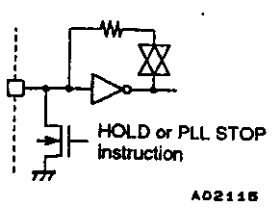
A02105

Figure 2 I_{DD5} in BACK UP Mode

Pin Functions

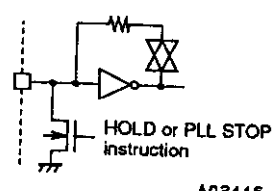
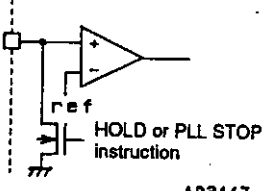
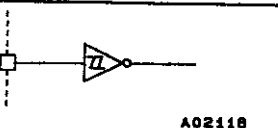
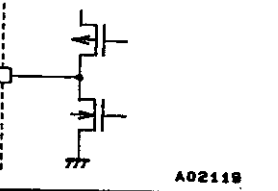
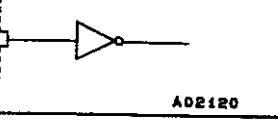
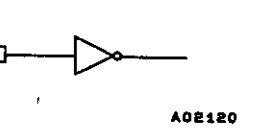
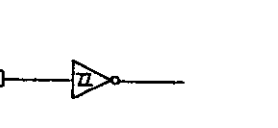
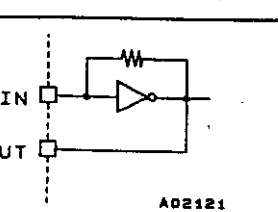
Pin	Pin No.	Functions	I/O	I/O circuit type
PA0 PA1 PA2 PA3	35 34 33 32	Low-threshold type dedicated input port These pins can be used, for example, for key data acquisition. Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins. Input through these pins is disabled in BACK UP mode.	Input	 A02107
PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	30 29 28 27 26 25 24 23	Dedicated output ports Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high-impedance state in BACK UP mode. These pins go to the low level during a reset, i.e., when the RES pin is low.	Output	 A02108
PD0 PD1 PD2 PD3	22 21 20 19	Dedicated output ports These are normal CMOS outputs. These pins go to the output high-impedance state in BACK UP mode. These pins go to the low level during a reset, i.e., when the RES pin is low.		
PE0 PE1 PE2 PE3	18 17 16 15	I/O port These pins are switched between input and output as follows: Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode. These pins go to the input mode during a reset, i.e., when the RES pin is low. In BACK UP mode these pins go to the input mode with input disabled.	I/O	PE1, PE3  A02109 Others  A02110
PF0 PF1 PF2 PF3	14 13 12 11	I/O port These pins are switched between input and output by the FPC instruction. The I/O states of this port can be specified for individual pins. These pins go to the input mode during a reset, i.e., when the RES pin is low. In BACK UP mode these pins go to the input mode with input disabled.		
PG0 PG1 PG2 PG3	6 5 4 3	Dedicated input port Input through these pins is disabled in BACK UP mode.	Input	 A02111

Continued from preceding page.

Pin	Pin No.	Functions	I/O	I/O circuit type
PH0 PH1 PH2/DAC1 PH3/DAC2	10 9 8 7	Dedicated output port Since these pins are high-breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching. Note that PH2 and PH3 also function as the DAC1 and DAC2 outputs. These ports go to the high impedance state during a reset, i.e., when the $\overline{\text{RES}}$ pin is low, and in BACK UP mode.	Output	 A02112
PI0/S25 PI1/S26 PI2/S27 PI3/S28	39 38 37 36	Dedicated output port While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually. The LCD driver function is selected and a segment-off signal is output when power is first applied or when $\overline{\text{RES}}$ is low. These pins are held at the low level in BACK UP mode. Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.	Output	 A02113
S1 to S24	63 to 40	LCD driver segment outputs A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used. A segment-off signal is output when power is first applied or when $\overline{\text{RES}}$ is low. These pins are held at the low level in BACK UP mode. The use of these pins as general-purpose output ports can be specified as an option.	Output	 A02114
COM1 COM2	65 64	LCD driver common outputs A 1/2 duty, 1/2 bias drive type is used. The output when power is first applied or when $\overline{\text{RES}}$ is low is identical to the normal operating mode output. These pins are held at the low level in BACK UP mode.	Output	 A02115
FMIN	74	FM VCO (local oscillator) input The input must be capacitor coupled. The input frequency range is from 10 to 130 MHz.	Input	 A02116
AMIN	75	AM VCO (local oscillator) input The band supported by this pin can be selected using the PLL instruction. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW		

Continued on next page.

Continued from preceding page.

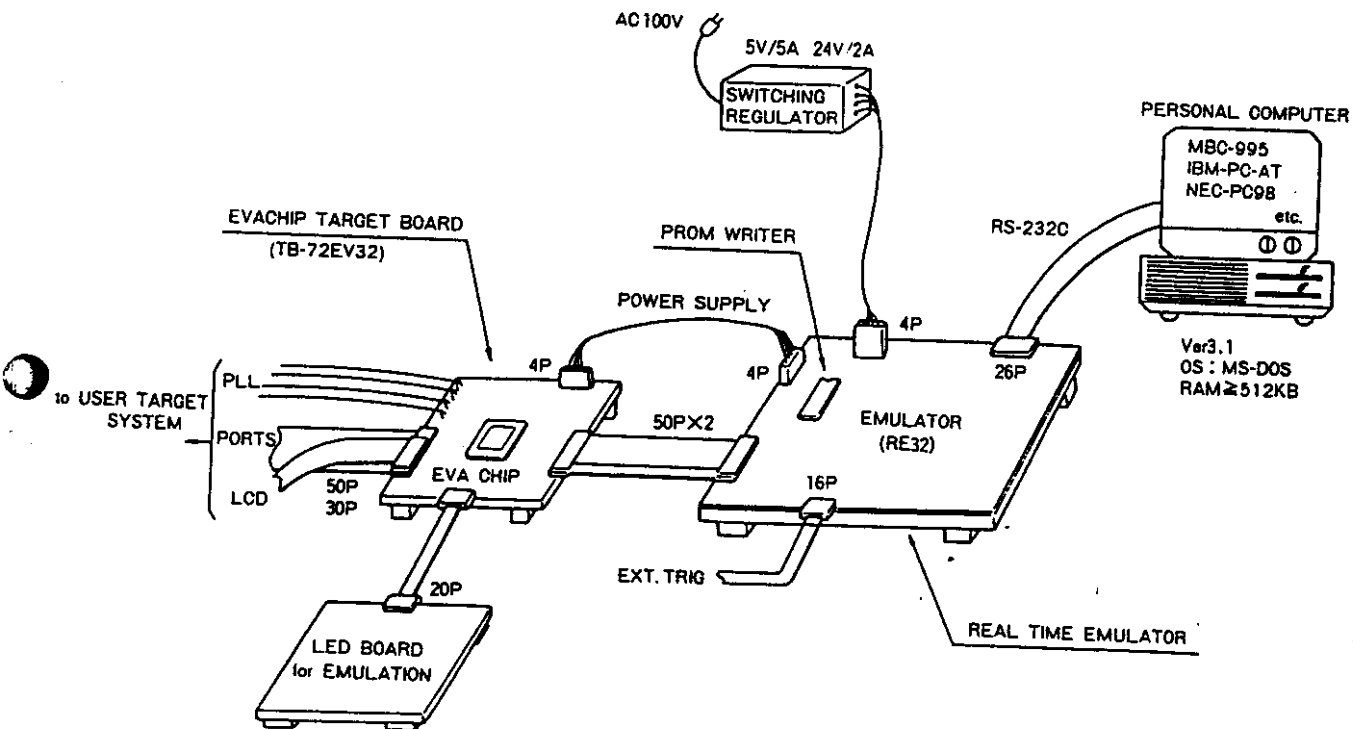
Pin	Pin No.	Functions	I/O	I/O circuit type
HCTR	70	Universal counter input The input should be capacitor coupled. The input frequency range is from 0.4 to 12 MHz. This input can be effectively used for FM IF or AM IF counting.	Input	 A02116
LCTR	71	Universal counter input The input should be capacitor coupled for input frequencies in the range 100 to 150 kHz. Capacitor coupling is not required for input frequencies from 1 to 20 Hz. This input can be effectively used for AM IF counting. This pin can also be used as a normal input port.		
ADI	69	A/D converter input A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is $((63/96) \cdot V_{DD})$ for a data value of 3FH.	Input	 A02117
INT	66	External interrupt request input An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input. This pin can also be used as a normal input port.	Input	 A02118
EO1 EO2	77 78	Reference frequency and programmable divider phase comparison error outputs Charge pump circuits are built in. EO1 and EO2 are the same.	Output	 A02119
SNS	72	Input pin used to determine if a power outage has occurred in BACK UP mode This pin can also be used as a normal input port.	Input	 A02120
HOLD	67	Input pin used to force the LC72322 to HOLD mode The LC72322 goes to HOLD mode when the HOLDEN flag is set (by an SS instruction) and the HOLD input goes low. A high-breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch.	Input	 A02120
RES	68	System reset input This signal should be held low for 75 ms after power is first applied to effect a power-up reset. The reset starts when a low level has been input for at least six reference clock cycles.	Input	 A02118
XIN XOUT	1 80	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output	 A02121
TEST1 TEST2	2 79	LSI test pins. These pins must be connected to V _{SS} .	—	—
V _{DD} V _{SS}	31, 73 76	Power supply	—	—

Mask Options

No.	Description	Selections
1	WDT (watchdog timer) inclusion selection	WDT included No WDT
2	Port A pull-down resistor inclusion selection	Pull-down resistors included No pull-down resistors
3	Cycle time selection	2.67 μ s 13.33 μ s 40.00 μ s
4	LCD port/general-purpose port selection	LCD ports General-purpose output ports

Development Environment

- The LC72P321 is used for OTP.
- The LC72EV321 is used as the evaluation chip.
- A total debugging system is available in which the TB-72EV32 evaluation chip board and the RE32 multi-function emulator are controlled by a personal computer.



LC72321 Instruction Table

Abbreviations:

ADDR: Program memory address [12 bits]

b: Borrow

B: Bank number [2 bits]

C: Carry

DH: Data memory address high (row address) [2 bits]

DL: Data memory address low (column address) [4 bits]

I: Immediate data [4 bits]

M: Data memory address

N: Bit position [4 bits]

Pn: Port number [4 bits]

r: General register (one of the locations 00 to 0FH in bank 0)

(): Contents of register or memory

()N: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15 14 13 12				11 10 9 8			7 6 5 4				3 2 1 0				
						D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	DH		DL				Rn			
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0	1	0	0	0	1	DH		DL			Rn				
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	DH		DL			Rn				
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	1	0	0	DH		DL			Rn				
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	DH		DL			I				
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0	1	0	1	0	1	DH		DL			I				
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	DH		DL			I				
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0	1	0	1	1	1	DH		DL			I				
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	DH		DL			Rn				
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if borrow	0	1	1	0	0	1	DH		DL			Rn				
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	DH		DL			Rn				
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0	1	1	0	1	0	DH		DL			Rn				
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	DH		DL			I				
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0	1	1	1	0	1	DH		DL			I				
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	DH		DL			I				
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0	1	1	1	1	1	DH		DL			I				
Comparison instructions	SEQ	r	M	Skip if r equals M	$r - M$ skip if zero	0	0	0	0	0	1	DH		DL			Rn				
	SGE	r	M	Skip if r is greater than or equal to M	$r - M$ skip if not borrow ($r \geq M$)	0	0	0	0	1	1	DH		DL			Rn				
	SEQI	M	I	Skip if M equal to I	$M - I$ skip if zero	0	0	1	1	0	1	DH		DL			I				
	SGEI	M	I	Skip if M is greater than or equal to I	$M - I$ skip if not borrow ($M \geq I$)	0	0	1	1	1	1	DH		DL			I				

Continued on next page.

APPENDIX 10
FINAL RF AMPLIFIER DATA SHEETS

THREE (3) PAGES FOR 2SC2078 FOLLOW THIS SHEET

FINAL RF AMP DATA SHEET
FCC ID: MMA77235ESP

APPENDIX 10

ws\mid77235.ta

E

2010A

NPN Epitaxial Planar Silicon Transistor

27MHz High Frequency Power Amp Applications

452D

Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$

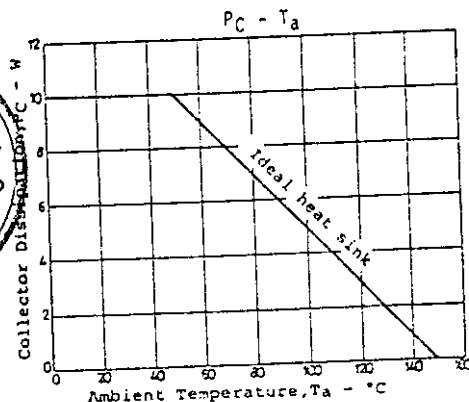
Collector to Base Voltage	V _{CBO}	80	V
Collector to Emitter Voltage	V _{CER}	75	V
Emitter to Base Voltage	V _{EBO}	5	V
Collector Current	I _C	3	A
Peak Collector Current	i _{cp}	5	A
Collector Dissipation	P _C	1.2	W
	T _C =50°C	10	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

Electrical Characteristics Characteristics at $T_a=25^{\circ}\text{C}$

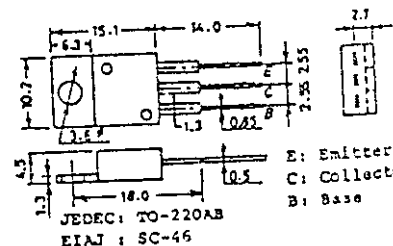
Electrical Characteristics		Characteristics	Typical	Min	Max
Collector Cutoff Current	I_{CBO}	$V_{CB}=40V, I_E=0$	10		
Emitter Cutoff Current	I_{EBO}	$V_{EB}=4V, I_C=0$	10		
DC Current Gain	h_{FE}	$V_{CE}=5V, I_C=0.5A$	25*		200*
Gain Bandwidth Product	f_T	$V_{CE}=10V, I_C=0.1A$	100	150	
Output Capacitance	c_{ob}	$V_{CB}=10V, f=1MHz$		45	60
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=1A, I_B=0.1A$		0.15	0.6
B-E Saturation Voltage	$V_{BE(sat)}$	$I_C=1A, I_B=0.1A$		0.9	1.2
C-B Saturation Voltage	$V_{(BR)CBO}$	$I_C=100\mu A, I_B=0$	80		
C-E Saturation Voltage	$V_{(BR)CER}$	$I_C=1mA, R_{\theta\theta}=150ohm$	75		
E-B Saturation Voltage	$V_{(BR)EBO}$	$I_E=100\mu A, I_C=0$	5		
[At specified test circuit]					
Output Power	P_o	$V_{CC}=12V, f=27MHz, P_i=0.2W$	4.0		
Power Efficiency	η		60		

*:The 2SC2078 is classified by 0.5A h_{FE} as follows:

25	B	50	40	C	80	60	D	120	100	E	200
----	---	----	----	---	----	----	---	-----	-----	---	-----

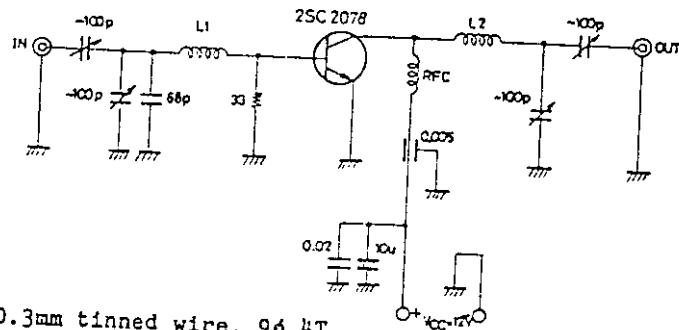


Case Outline 2010A
(unit:mm)

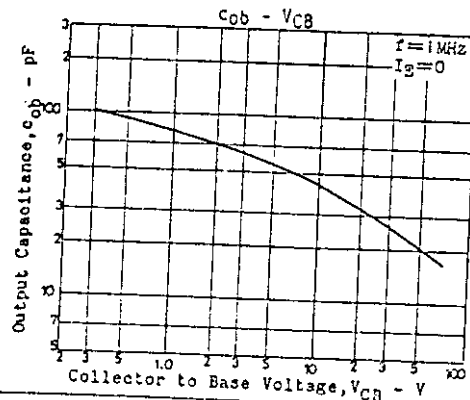
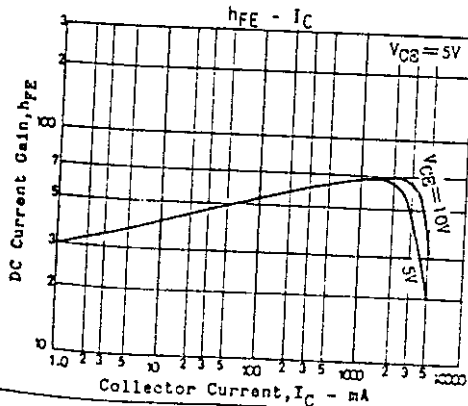
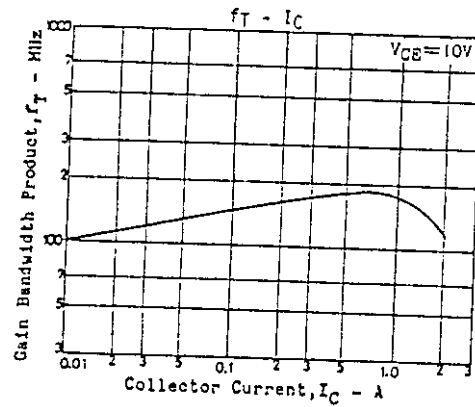
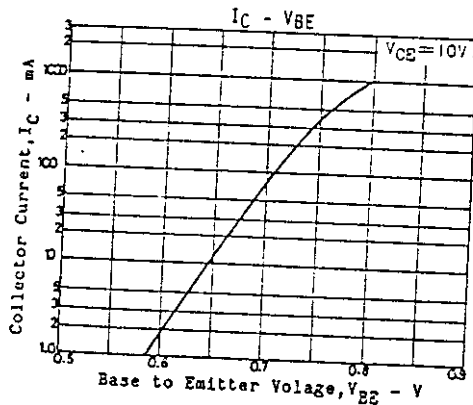
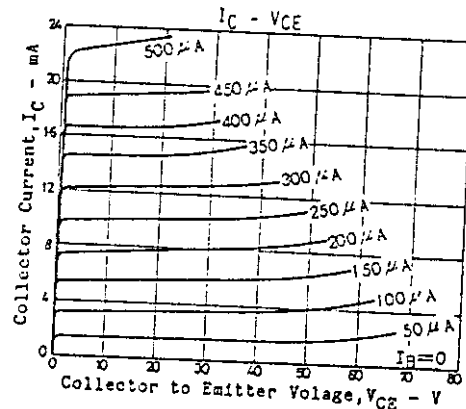
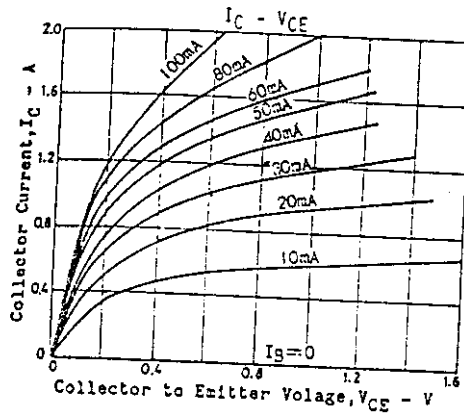


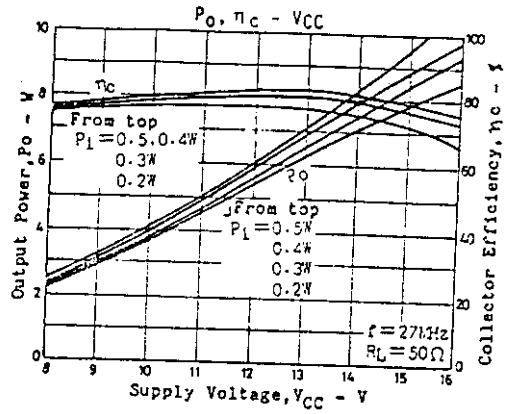
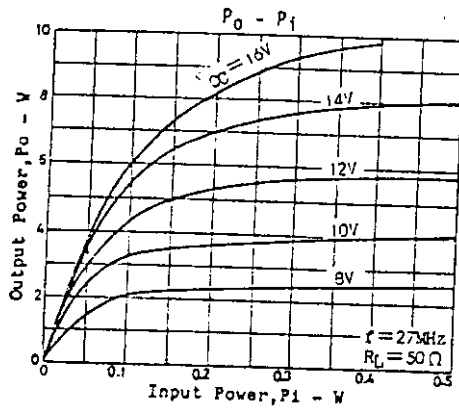
4147KI/3145KI/2274ki No. 468

2SC2078 27MHz Output Power Test Circuit



Coil data L1: 0.3mm tinned wire, 9 ϕ 4T
L2: 0.6mm tinned wire, 9 ϕ 4T
RFC 2.2uH





APPENDIX 3
FUNCTION OF DEVICES

<u>Reference</u>	<u>Type</u>	<u>Function</u>
Q22	2SC5343MY	VCO Amp.
Q23	2SC5343MY	Buffer
Q24	2SC5343MY	Doubler
Q25	2SC5343MY	Pre-Driver
Q26	2SC2314E	Driver
Q27	KTC2078	Final RF Amplifier
IC1	LC72322	CPU/PLL
IC2	4558	Mike Amp/Limiter
IC3	TDA2003V	Modulator

FUNCTION OF DEVICES
FCC ID: MMA77235ESP

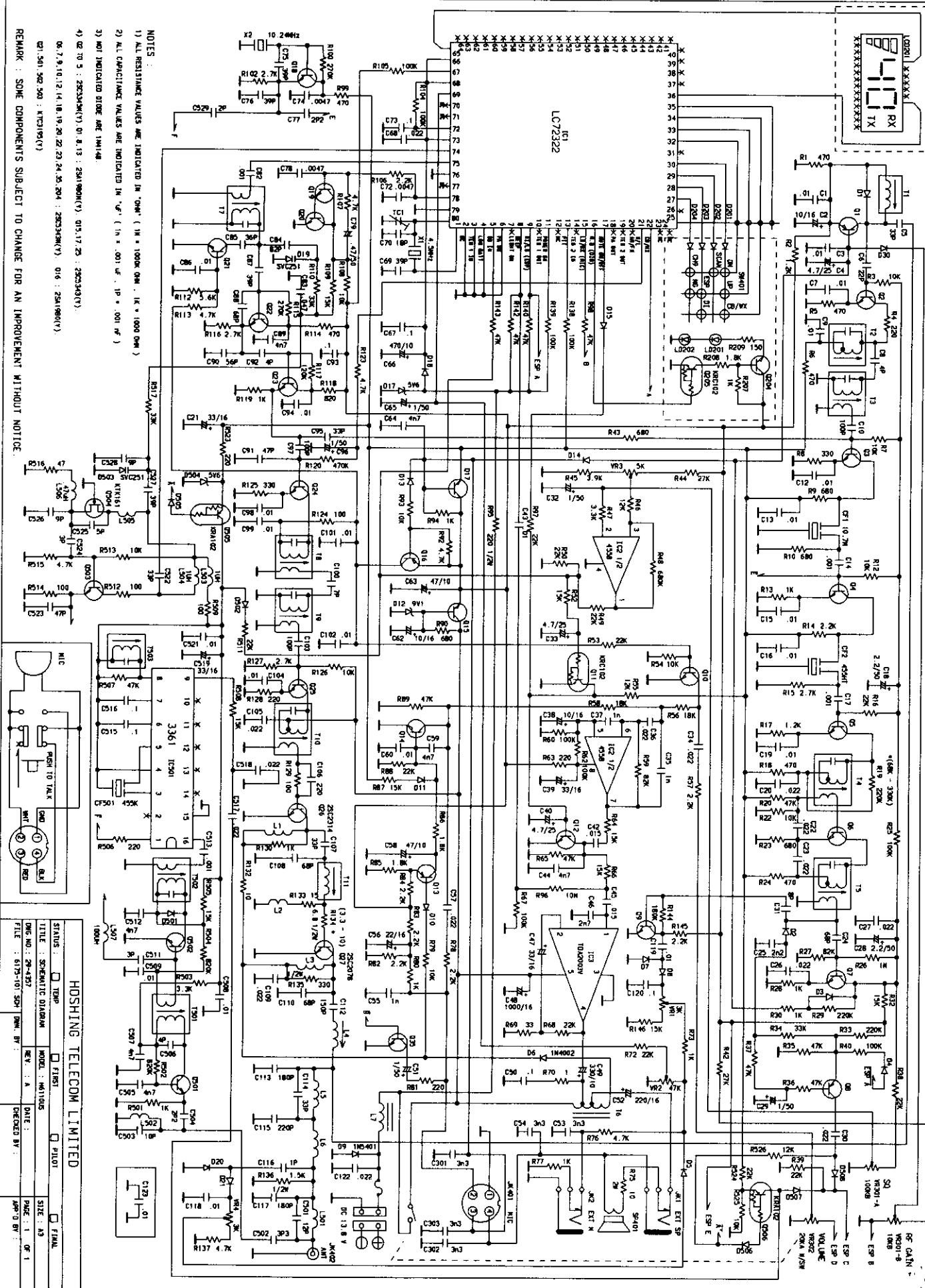
APPENDIX 3

APPENDIX 4
SCHEMATIC DIAGRAMS

TWO (2) SCHEMATIC DIAGRAMS FOLLOW THIS SHEET

SCHEMATIC DIAGRAMS
FCC ID: MMA77235ESP

APPENDIX 4



FCC ID: MMA77235ESP

HOSHING TELECOM LIMITED			
STATUS :	☐ TEMP	☐ FIRST	☐ PILOT
TITLE :	SCHEMATIC DIAGRAM		MODEL : H6175 ESP
DWG. NO. :	29-4358	REV. :	A
DATE :		CHECKED BY :	
FILE :	6175A101 SCH	DNW. BY :	
APP'D BY :		SIZE :	A3
		PAGE :	2 OF 2

