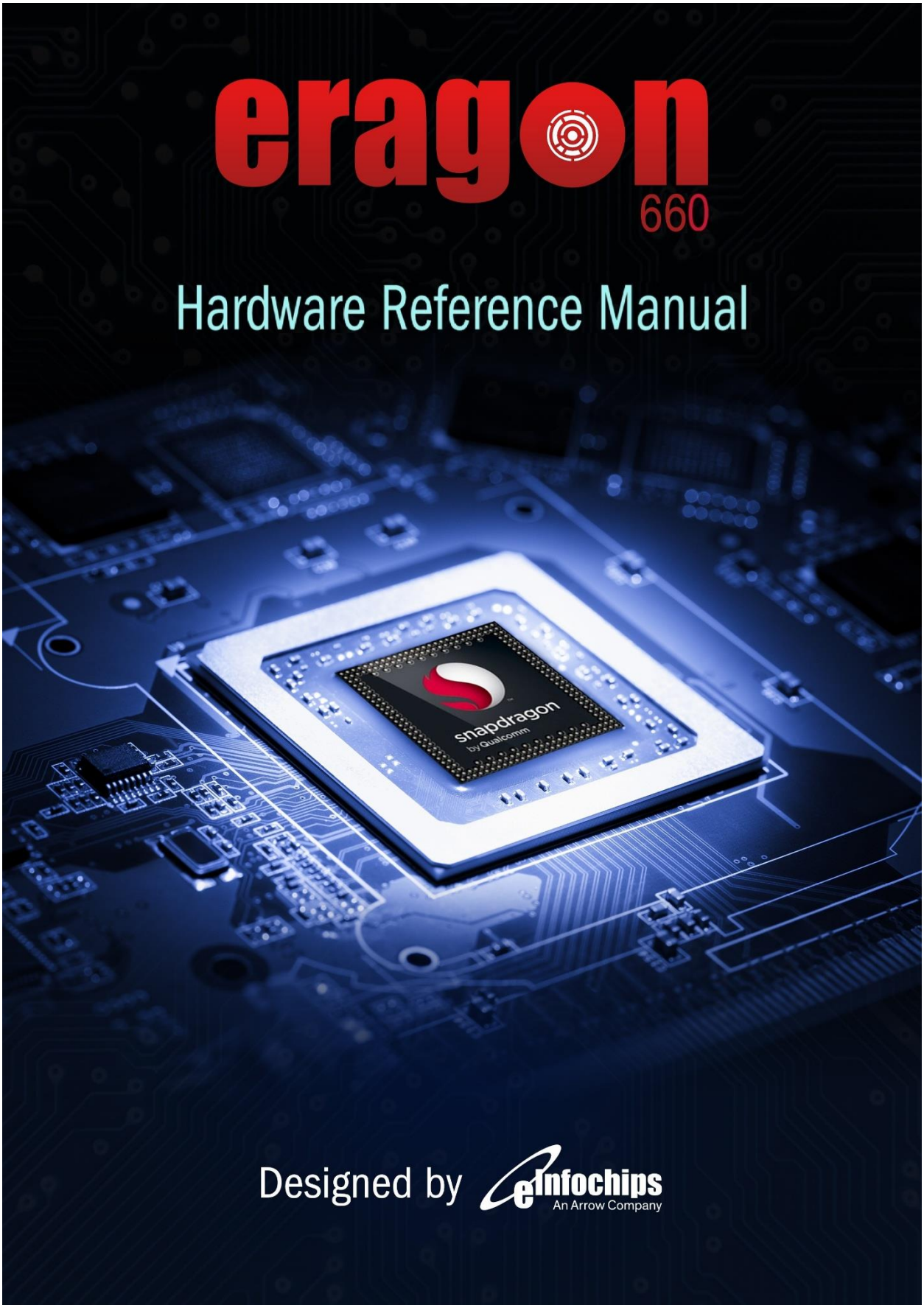
eragon 660

Hardware Reference Manual



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1 Document Details

1.1 Document History

Version	Author		Description Of Changes
	Name	Date	
1.0	*eInfochips*	*23-oct-2018*	*Initial release*

Table 1: Document History

1.2 Definition, Acronyms and Abbreviations

Definition/Acronym/Abbreviation	Description
BLE	Bluetooth Low Energy
BT	Bluetooth
CPU	Central Processing Unit
CSI	Camera Serial Interf BLE e
DC	Direct Current
DDR	Double Data Rate
DSI	Display Serial Interface
eI	eInfochips
GB	Giga Byte
GPIO	General Purpose Interface
GPS	Global Positioning System
HD	High Definition
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit

IC	Integrated Circuit
Inc.	Incorporated
JTAG	Joint Test Application Group
LAN	Local Area Network
LPDDR	Lower Power DDR
MIPI	Mobile protocol working Alliance (not an Acronym)
MMC	Multi Media Card
MOSI	Master Out Slave In
MP	Mega Pixel
OTG	On The Go
PMIC	Power Management IC
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
Rx	Receive
SBC	Single Board Computer
SPI	Serial peripheral Interface
Tx	Transmit
UART	Universal Asynchronous Interface
USB	Universal Serial Bus
ADB	Android Debug Bridge
WLAN	Wireless LAN

Table 2 : Definition, Acronyms and Abbreviations

1.3 References

No.	Document	Version	Remarks
1	ERAGON660 SBC Schematic File	1.1	
2.	ERAGON660 IO Card Schematic File	1.1	

Table 3 : References

2 License Agreement

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3 Preface

This document provides an overview of the ERAGON660 SBC and development kit based on the Qualcomm Snapdragon™ 660. It provides step-by-step information about hardware components and associated software release Android 8.1.0 (Oreo).

3.1 Intended Audience

This document is intended to be used by for technically qualified personnel. It is not intended for general audiences.

3.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. It comes with Android software packages. This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

4 Overview

The ERAGON660 SBC provides an ideal building block for simple integration with a wide range of products in target markets requiring rich multimedia functionality, powerful graphics processing and video capabilities, as well as high-processing power, in a compact, RoHS compliant, fan less, cost effective SBC with low power consumption.

The ERAGON660 SBC leverages cutting edge mobile computing for embedded and industrial product designs, based on the Qualcomm Snapdragon™ 660 2.2 GHz octa core CPU, high performance Adreno™ 512 GPU and a dedicated DSP for advanced A/V processing.

The SBC is equipped with full range of interfaces available in the Qualcomm Snapdragon SDA660 SoC, which are routed on the 300 pins of three (100 pins each) board-to-board connectors.

The SDA660 SBC supports Android Oreo operating system (Version :- TBD)

The ERAGON660 Development kit is based on ERAGON660 SBC for the developers to quick start their application development and is ideal for rapid prototyping of product. With support for almost all the peripherals, it reduces the design time of innovative applications and helps to achieve early time to market. With variety of peripherals, this kit is targeted for wide range of applications supporting bulk storage, faster connectivity, higher through put and performance at lower power.

4.1 Key Features

CPU • Qualcomm Snapdragon 660 • 8x Qualcomm® Kryo™ 260 CPU at up to 2.2 GHz per core • 64-Bit processor • Qualcomm Adreno 512 GPU. • Up to 4K UltraHD capture @ 30 fps Video Encode • Up to 4K UltraHD playback @30fps,H.264(AVC),H.265(HEVC),VP9 Video Decode • 2x Image Sensor Processor (ISP) • Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (dual-HVX512) 787 MHz	**Audio** **PM660l(On SBC)** :- Two single-ended and one differential (microphone) inputs Four outputs: EAR, HPHL + HPHR, and class-D speaker driver Supports 8, 16, 32, 44.1, 48, and 192 kHz sample rates **WCD9335(On IO Card)** :- IO Card has Audio codec WCD9335 along with two Audio Amplifiers WSA8810 • 3.5mm ANC Audio Jack • 2x 16 pin Audio header which supports. Input: 3xAnalog Mic, 3xDigital Mic Output: o 2x Stereo Amplified Output o 2x External Headphone Output o 1x Earphone Output
Memory • **RAM:** Up to 6GB LPDDR4X Up to 1866MHz • **Storage:** Up to 64 GB eMMC or UFS(Optional)	**Connectivity** • IEEE 802.11 a/b/g/n/ac • Bluetooth 5
Camera • Dual camera support (up to 16 MP) • 3x MIPI CSI- 4 lane (2x CSI simultaneous support)	**Display** • 2x DSI 4-lane each • 2560 x 1600 at 60fps • 1080p at 30fps Miracast or 4k at 30fps. • DisplayPort and USB Type-C support
Operating System • Android 8.1.0	**Multimedia** • Audio and Video as mention above
USB • USB HUB for 2x USB 2.0 Host • 1x USB 3.1 (Type-C) for high speed data transfer	**Miscellaneous** 1x UART,2x I2C, 2x SPI, Sensors 3-Axis Accelerometer , 3- Axis Gyroscope, Ambient Light , Proximity ,1x JTAG ,1x microSD card, Integrated Qualcomm GPS (Supports GPS, GLONASS, BeiDou, Gallileo)
Power Input & Consumption Voltage In: (1) +12V@3A through DC jack (2) Battery through Battery connector	**Physical & Operating Characteristics** • **Dimension:** ○ SBC: 85mm x 55mm ○ IO Card: 160mm x 114mm • **Storage Temperature Range:** ○ -20 to 70° C • **Operating Temperature Range:** ○ 0 to 50° C

4.2 Applications

The ERAGON606 Kit is used in a wide range of products across many different target markets. Eragon660 of the typical applications are:

- Consumer Electronics
- Internet of Things
- Marine
- Automotive
- Domestic Robot
- Digital signage
- Security & Surveillance
- Biometric Access Control Systems
- Home and Health Hub
- Human-machine interface
- Home energy management systems
- In-flight entertainment
- Intelligent industrial control systems
- Portable medical

5 Getting Started

5.1 Prerequisites

Before user power up the ERAGON660 board for the first time, will need following things:

Sr No.	Details	MFG Part/EI Part	Qty :-
1	ERAGON660 (only SBC or SBC with IO card) board	17_00515_01/17_00617_01	1
2	Eragon Display board	17_00453_02	1
3	Power adapter (12V@3A)	PTDA402D-120300	1
4	FFC Cable for connecting LCD display to the ERAGON660 SBC Board	687640152002	1

Table 4 : Prerequisite table

5.2 Starting the board for the first time

To start the board, follow these simple steps:

Step 1. First, connect the ERAGON660 SBC Board to the Display board through FFC cable (DSI cable)

Step 2. Connect the Type C-USB cable to connector J13 of SBC

Step 3. Ensure that the boot switches SW3 are set to '0000', all in off position.

Step 4. Connect the complaint power supply to power connector J9.

Step 5. On the switch SW2.

Now board is in the booting process.

Please note that the first boot takes several minutes due to Androids initialization. Subsequent boot times should be faster.

6.1 ERAGON660

6.1.1 ERAGON660 SBC (Single Board Computer) Image

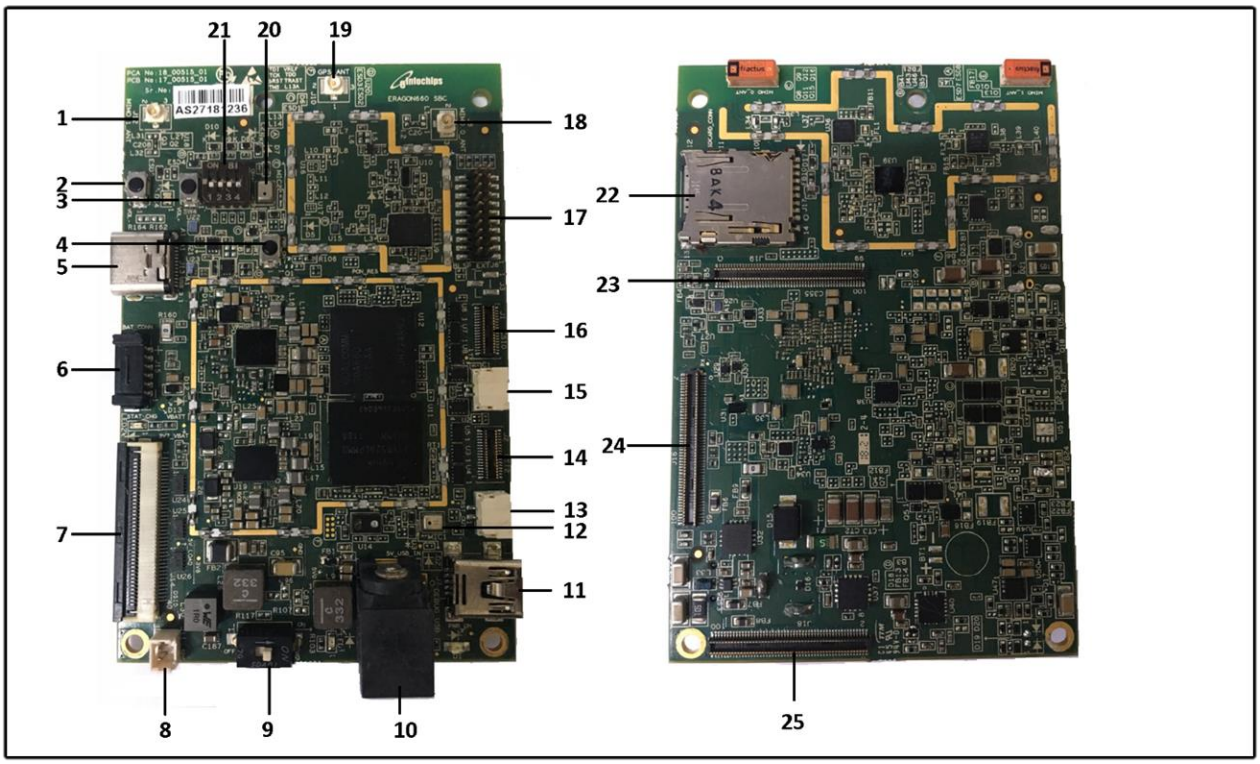

Figure 3 – ERAGON660 Single Board Computer (SBC) Image

The ERAGON660 SBC offers a wide range of interfaces and peripherals, including several high-speed signals through its edge connectors. The major parts of ERAGON660 SBC are marked with labels in above figures and the name of it is, are listed in the below table.

No.	Interface Name	No.	Interface Name
1	U.FL connector for WIFI+BT External ANTENNA 1	**14**	Camera Connector (J2)
2	Volume Down Switch	**15**	Flash LED Connector
3	Volume Up Switch	**16**	Camera Connector (J1)
4	Power on Switch	**17**	BLSP Connectors
5	USB 3.1 Type-C Connector	**18**	U.FL connector for WIFI+BT External ANTENNA 0
6	Battery Connector	**19**	U.FL connector for GPS ANTENNA
7	Display Connector	**20**	MIC 2 (microphone -2)
8	Speaker Connector	**21**	Boot Mode Configuration Switch
9	Input Supply ON/OFF Switch	**22**	Micro SD Card Connector
10	Input Supply Connector	**23**	Board to Board Connector (Left Connector)
11	Debug USB Connector	**24**	Board to Board Connector (Right Connector)
12	MIC 1 (microphone -1)	**25**	Board to Board Connector (Top Connector)
13	Flash LED Connector		

Table 5 : ERAGON660 SBC (Single Board Computer) Components

6.1.2 ERAGON660 IO Card Image

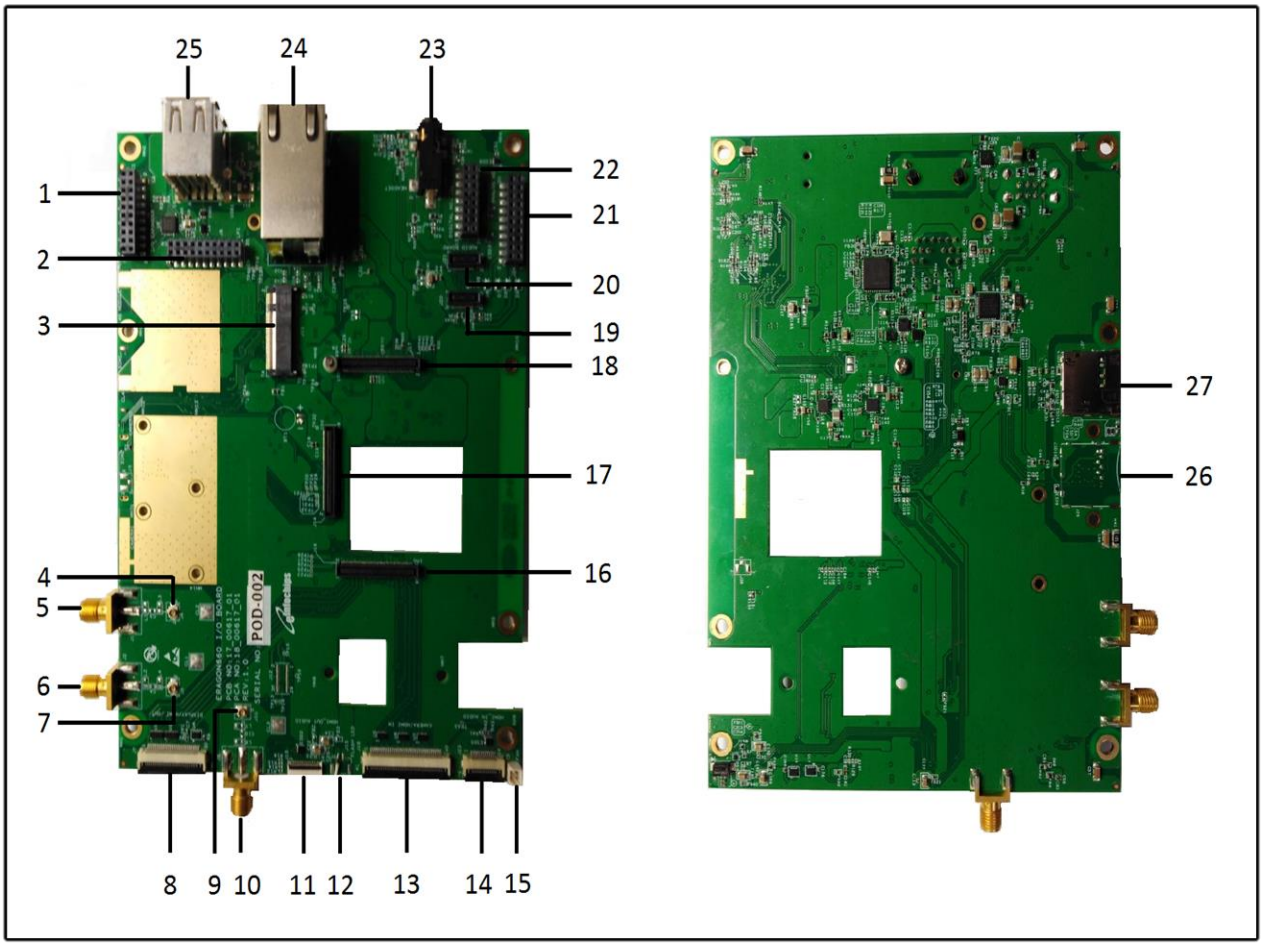

Figure 4 – ERAGON660 IO Card Image

The ERAGON660 IO Card offers a wide range of interfaces and peripherals, including several high-speed signals through its edge connectors. The major parts of ERAGON660 IO Card are marked with labels in above figures and the name of it is, are listed in the below table.

No.	Interface Name	No.	Interface Name
1	EXPANSION Connector (J4)	**15**	FAN Connector (J25)
2	LPI EXPANSION Connector (J8)	**16**	Board to Board Connector (J16)
3	4G LTE MODEM Connector (J11)	**17**	Board to Board Connector (J14)
4	U.FL connector for GPS ANTENNA (J6)	**18**	Board to Board Connector (J17)
5	SMA connector for GPS ANTENNA (J1)	**19**	Audio Board B TO B Connector (J20)
6	SMA connector for WIFI ANTENNA (J2)	**20**	Audio Board B TO B Connector (J21)
7	U.FL connector for WIFI ANTENNA (J5)	**21**	Analog Mic Connector (J24)
8	CSI1 Camera Connector (J7)	**22**	Digital Mic Connector (J22)
9	U.FL connector for WIFI ANTENNA (J10)	**23**	HEADSET (J19)
10	SMA connector for WIFI ANTENNA (J9)	**24**	Ethernet Connector (E1)
11	Audio Connector for HDMI_IN (J13)	**25**	USB Type A Dual Connector (USB1)
12	Flash LED Connector (J15)	**26**	SIM Card Connector (J26)
13	DSI1 Display Connection (J18)	**27**	SIM Card Connector (J27)
14	AUDIO FOR HDMI_OUT (J23)		

Table 6 : ERAGON660 IO Card Components

The Eragon660 SBC and IO Card are interfaced through three Hirose DF40C-100DP-0.4V (51) Connectors. The pin outs for these three connectors is described below,

SBC Pin No.	I/O Card Pin No.	Signal Name	Default Pin Function	Voltage Level
J16.1	J14.1	GND	Ground	-
J16.2	J14.2	GND	Ground	-
J16.3	J14.3	LPI_GPIO29_EXTR4	LPI_GPIO_29	1.8V
J16.4	J14.4	LPI_I2C_3_SDA	LPI_I2C_3_SDA	1.8V
J16.5	J14.5	LPI_GPIO26_EXTR1	LPI_GPIO26	1.8V
J16.6	J14.6	LPI_I2C_3_SCL	LPI_I2C_3_SCL	1.8V
J16.7	J14.7	LPI_GPIO27_EXTR2	LPI_GPIO27	1.8V
J16.8	J14.8	GND	Ground	-
J16.9	J14.9	GND	Ground	-
J16.10	J14.10	LPI_UART_2_TX	LPI_GPIO_14	1.8V
J16.11	J14.11	BLSP_I2C_SCL_6	BLSP 6 - I2C CLOCK	1.8V
J16.12	J14.12	LPI_UART_2_RX	LPI_GPIO_15	1.8V
J16.13	J14.13	BLSP_I2C_SDA_6	BLSP 6 - I2C DATA	1.8V
J16.14	J14.14	GND	Ground	-
J16.15	J14.15	GND	Ground	-
J16.16	J14.16	LPI_GPIO28_EXTR3	LPI_GPIO28	1.8V
J16.17	J14.17	HDMI_MI2S_3_SCK	MI2S Clock signal	1.8V
J16.18	J14.18	GND	Ground	-
J16.19	J14.19	HDMI_MI2S_3_D1	MI2S Data1 signal	1.8V
J16.20	J14.20	GND	Ground	-
J16.21	J14.21	HDMI_MI2S_3_WS	MI2S Word Select signal	1.8V

J16.22	J14.22	VREG_L3A	PM660 Linear regulator L3 output	1.0V
J16.23	J14.23	HDMI_MI2S_3_D0	MI2S Data0 signal	1.8V
J16.24	J14.24	BLSP_I2C_SDA_2	BLSP 2 - I2C DATA	1.8V
J16.25	J14.25	HDMI_RST_N	HDMI RESET	1.8V
J16.26	J14.26	BLSP_I2C_SCL_2	BLSP 2 - I2C CLOCK	1.8V
J16.27	J14.27	HDMI_INT_GPIO	HDMI INTERRUPT	1.8V
J16.28	J14.28	VREG_L1A	PM660 Linear regulator L1 output	1.232V
J16.29	J14.29	VCC_1V8	1.8V Switching Regulator input	1.8V
J16.30	J14.30	VREG_L1A	PM660 Linear regulator L1 output	1.232V
J16.31	J14.31	VCC_1V8	1.8V Switching Regulator input	1.8V
J16.32	J14.32	GND	Ground	-
J16.33	J14.33	VCC_1V8	1.8V Switching Regulator input	1.8V
J16.34	J14.34	RESOUT_N	Reset out from CPU.	1.8V
J16.35	J14.35	GND	Ground	-
J16.36	J14.36	GND	Ground	-
J16.37	J14.37	GND	Ground	-
J16.38	J14.38	LTE_MODEM_DCD	LTE Modem Disable signal from CPU/GPIO_88	1.8V
J16.39	J14.39	VREG_L19A	PM660 Linear regulator L19 output	3.3V
J16.40	J14.40	LTE_WIRELESS_POWER	GPIO_89/LTE Modem Antenna control(no. 0)	1.8V
J16.41	J14.41	VREG_L19A	PM660 Linear regulator L19 output	3.3V
J16.42	J14.42	LTE_MODEM_DSR	LTE Modem Reset/ GPIO_85	1.8V
J16.43	J14.43	VREG_L19A	PM660 Linear regulator L19 output	3.3V
J16.44	J14.44	GND	Ground	-

J16.45	J14.45	GND	Ground	-
J16.46	J14.46	LTE_MODEM_VBUS_EN	LTE Modem Disable(#2) signal/ GPIO87	1.8V
J16.47	J14.47	GND	Ground	-
J16.48	J14.48	GPIO_112	GPIO_112/LTE Modem Antenna control(no. 0)	1.8V
J16.49	J14.49	BLSP_UART_RX(1)	BLSP1 UART Receive/GPIO29	1.8V
J16.50	J14.50	LTE_MODEM_POWER	Modem Turn ON/OFF signal	1.8V
J16.51	J14.51	BLSP_UART_TX(1)	BLSP1 UART Transmit/GPIO28	1.8V
J16.52	J14.52	GPIO_110	GPIO 110	1.8V
J16.53	J14.53	BLSP_UART_CTS_N(1)	BLSP1 UART CTS/GPIO30	1.8V
J16.54	J14.54	GND	Ground	-
J16.55	J14.55	BLSP_UART_RFR_N(1)	BLSP1 UART TRTS/ GPIO31	1.8V
J16.56	J14.56	LTE_MODEM_RING	Modem Dynamic power control	1.8V
J16.57	J14.57	GND	Ground	-
J16.58	J14.58	MODEM_POWER_EN	Can be used as GPIO_107.	1.8V
J16.59	J14.59	MI2S2_LTE_CLK	MI2S(2) Clock signal	1.8V
J16.60	J14.60	GPIO_108	GPIO 108	1.8V
J16.61	J14.61	MI2S2_LTE_DIN	MI2S (2) Data1 signal	1.8V
J16.62	J14.62	LTE_MODEM_DTR	For LED driver of Modem	1.8V
J16.63	J14.63	MI2S2_LTE_SYNC	MI2S word select	1.8V
J16.64	J14.64	GND	Ground	-
J16.65	J14.65	MI2S2_LTE_DOUT	MI2S (2) Data out	1.8V
J16.66	J14.66	GND	Ground	-
J16.67	J14.67	GND	Ground	-

J16.68	J14.68	GND	Ground	-
J16.69	J14.69	NC	No Connection	-
J16.70	J14.70	GND	Ground	-
J16.71	J14.71	NC	No Connection	-
J16.72	J14.72	GND	Ground	-
J16.73	J14.73	GND	Ground	-
J16.74	J14.74	GND	Ground	-
J16.75	J14.75	GND	Ground	-
J16.76	J14.76	GND	Ground	-
J16.77	J14.77	GND	Ground	-
J16.78	J14.78	GND	Ground	-
J16.79	J14.79	GND	Ground	-
J16.80	J14.80	GND	Ground	-
J16.81	J14.81	GND	Ground	-
J16.82	J14.82	GND	Ground	-
J16.83	J14.83	GND	Ground	-
J16.84	J14.84	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.85	J14.85	GND	Ground	-
J16.86	J14.86	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.87	J14.87	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.88	J14.88	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V

J16.89	J14.89	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.90	J14.90	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.91	J14.91	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.92	J14.92	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.93	J14.93	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.94	J14.94	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.95	J14.95	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.96	J14.96	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.97	J14.97	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.98	J14.98	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.99	J14.99	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J16.100	J14.100	VPH_PWR_CON	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V

Table 7 : Connector J16 pin details

SBC Pin No.	I/O Card Pin No.	Signal Name	Default Pin Function	Voltage Level
J18.1	J17.1	GND	Ground	-
J18.2	J17.2	VREG_L13A	PM660 Linear regulator L13 output	1.8V
J18.3	J17.3	CDC_HS_DET_PMIC_CONN	Headset detection	-
J18.4	J17.4	GND	Ground	-
J18.5	J17.5	CDC_HPH_L_PMIC_CONN	Headphone output, left channel	-
J18.6	J17.6	GND	Ground	-
J18.7	J17.7	CDC_HPH_R_PMIC_CONN	Headphone output, right channel	-
J18.8	J17.8	CDC_IN3_P_PMIC	Earpiece output, plus (+)	-
J18.9	J17.9	GND	Ground	-
J18.10	J17.10	CDC_EAR_M_PMIC	Earpiece output, minus (-)	-
J18.11	J17.11	CDC_MIC2_P_PMIC_CONN	Microphone input 2	-
J18.12	J17.12	GND	Ground	-
J18.13	J17.13	CDC_HPH_REF_PMIC_CONN	Headphone ground reference	-
J18.14	J17.14	WCD_SDM_MCLK	Audio codec PDM clock signal and codec master clock/ LPI bit 18	1.8V
J18.15	J17.15	GND	Ground	-
J18.16	J17.16	GND	Ground	-
J18.17	J17.17	GRFC_0	Generic RF controller bit 0 Configurable I/O	1.8V
J18.18	J17.18	WSA_SPKR_SD_N_1	GPIO 105 /WSA8815 control pin	1.8V
J18.19	J17.19	HAP_LINE_OUT3	PWM input for haptic control	1.8V
J18.20	J17.20	WSA_SPKR_SD_N_2	GPIO 106 /WSA8815 control pin	1.8V

J18.21	J17.21	LPI_AUD_CDC_RSTN	Audio codec PDM receive 1 (DRE)/ LPI bit 24	1.8V
J18.22	J17.22	LPI_AUD_CDC_INT1	Audio codec PDM receive 0 (DRE)/LPI bit 22	1.8V
J18.23	J17.23	GND	Ground	-
J18.24	J17.24	LPI_AUD_CDC_INT2	Audio codec PDM receive 1 /LPI bit 23	1.8V
J18.25	J17.25	WCD_MCLK	19.2MHz clock for external audio codec.	1.8V
J18.26	J17.26	GND	Ground	-
J18.27	J17.27	GND	Ground	-
J18.28	J17.28	LPI_AUD_SB_DATA0	Audio codec PDM transmit data channel/ LPI bit 20	1.8V
J18.29	J17.29	LTE_WAKE_HOST#	GPIO 75/ Modem wake up signal to Host.	1.8V
J18.30	J17.30	LPI_AUD_SB_DATA1	Audio codec PDM receive data channel 0/LPI bit 21	1.8V
J18.31	J17.31	LTE_COEX	GPIO 86/ Modem Antenna coexistence	1.8V
J18.32	J17.32	GND	Ground	-
J18.33	J17.33	GND	Ground	-
J18.34	J17.34	LPI_AUD_SB_CLK	Audio codec PDM synchronization signal/ LPI bit 19	1.8V
J18.35	J17.35	FLASH_LED2	Flash LED 2	-
J18.36	J17.36	GND	Ground	-
J18.37	J17.37	FLASH_LED2	Flash LED 2	-
J18.38	J17.38	5V_LOAD	5V Supply from SBC	5V
J18.39	J17.39	FLASH_LED2	Flash LED supply for CSI1.	

J18.40	J17.40	5V_LOAD	5V Supply from SBC	5V
J18.41	J17.41	VCOIN	Coin-cell battery/capacitor or backup battery charger supply and input	3V
J18.42	J17.42	5V_LOAD	5V Supply from SBC	5V
J18.43	J17.43	VCOIN	Coin-cell battery/capacitor or backup battery charger supply and input	3V
J18.44	J17.44	5V_LOAD	5V Supply from SBC	5V
J18.45	J17.45	GND	Ground	-
J18.46	J17.46	5V_LOAD	5V Supply from SBC	5V
J18.47	J17.47	GND	Ground	-
J18.48	J17.48	5V_LOAD	5V Supply from SBC	5V
J18.49	J17.49	GND	Ground	-
J18.50	J17.50	5V_LOAD	5V Supply from SBC	5V
J18.51	J17.51	GND	Ground	-
J18.52	J17.52	5V_LOAD	5V Supply from SBC	5V
J18.53	J17.53	GND	Ground	-
J18.54	J17.54	GND	Ground	-
J18.55	J17.55	VREG_WLED	Regulated supply for White LED of LCD.	
J18.56	J17.56	GND	Ground	-
J18.57	J17.57	VREG_WLED	Regulated supply for White LED of LCD.	
J18.58	J17.58	GND	Ground	-
J18.59	J17.59	GND	Ground	-
J18.60	J17.60	GND	Ground	-

J18.61	J17.61	GND	Ground	-
J18.62	J17.62	GND	Ground	-
J18.63	J17.63	GND	Ground	-
J18.64	J17.64	GND	Ground	-
J18.65	J17.65	LCD1_VDISP_M_OUT	Display bias minus: negative LCD regulated output	+5V
J18.66	J17.66	GND	Ground	-
J18.67	J17.67	LCD1_VDISP_P_OUT	Display bias plus: boost SMPS regulated output	-5V
J18.68	J17.68	GND	Ground	-
J18.69	J17.69	GND	Ground	-
J18.70	J17.70	GND	Ground	-
J18.71	J17.71	GND	Ground	-
J18.72	J17.72	GND	Ground	-
J18.73	J17.73	GPIO_13_NFC_EN	GPIO13 /NFC Enable.	1.8V
J18.74	J17.74	BLSP_I2C_SDA_6	BLSP6 I2C data	1.8V
J18.75	J17.75	GPIO_40_NFC_DWL_REQ	GPIO40/ Request for NFC IC.	1.8V
J18.76	J17.76	BLSP_I2C_SCL_6	BLSP6 I2C Clock	1.8V
J18.77	J17.77	GPIO_90_NFC_ESE_PWR_REQ	GPIO 90	1.8V
J18.78	J17.78	GND	Ground	-
J18.79	J17.79	VDD_NFC_OUT_2	NC	
J18.80	J17.80	BLSP1_SPI_MOSI_NFC	BLSP1- SPI Master out slave in signal	1.8V
J18.81	J17.81	GND	Ground	-
J18.82	J17.82	BLSP1_SPI_MISO_NFC	BLSP1- SPI Master in slave out signal	1.8V

J18.83	J17.83	GND	Ground	-
J18.84	J17.84	BLSP1_SPI_CS_N_NFC	BLSP1 - SPI chip select signal	1.8V
J18.85	J17.85	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.86	J17.86	BLSP1_SPI_CLK_NFC	BLSP1- SPI clock signal	1.8V
J18.87	J17.87	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.88	J17.88	GND	Ground	-
J18.89	J17.89	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.90	J17.90	LNBBCLK3	19.2Mhz clock output	-
J18.91	J17.91	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.92	J17.92	GND	Ground	-
J18.93	J17.93	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.94	J17.94	GPIO_12_NFC_IRQ	GPIO 12/ NFC Interrupt	1.8V
J18.95	J17.95	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.96	J17.96	NFC_CLK_REQ	PM660L-GPIO 04/NFC clock request from NFC IC.	1.8V
J18.97	J17.97	3.7V_LOAD_REG	3.7V Supply from SBC (Battery/Input Power Supply)	3.5V-4.2V
J18.98	J17.98	VDD_NFC_OUT_1	NC	-
J18.99	J17.99	GND	Ground	-
J18.100	J17.100	GND	Ground	-

Table 8 : Connector J18 pin details

SBC Pin No.	I/O Card Pin No.	Signal Name	Default Pin Function	Voltage Level
J19.1	J16.1	GND	Ground	-
J19.2	J16.2	GND	Ground	-
J19.3	J16.3	MIPI_CSI1_CLK_P	MIPI CSI 1, differential clock – plus	
J19.4	J16.4	VREG_DVDD_1P2	1.2V from LDO for Digital section of camera sensor	1.2V
J19.5	J16.5	MIPI_CSI1_CLK_N	MIPI CSI 1, differential clock – minus	
J19.6	J16.6	VREG_DVDD_1P2	1.2V from LDO for Digital section of camera sensor	1.2V
J19.7	J16.7	GND	Ground	-
J19.8	J16.8	GND	Ground	-
J19.9	J16.9	MIPI_CSI1_DATA1_P	MIPI CSI 1, differential lane 1 – plus	
J19.10	J16.10	CAM_AVDD_2P8	2.8V from LDO for Analog section of camera sensor	2.8V
J19.11	J16.11	MIPI_CSI1_DATA1_N	MIPI CSI 1, differential lane 1 – minus	
J19.12	J16.12	GND	Ground	-
J19.13	J16.13	GND	Ground	-
J19.14	J16.14	VCM_MCAM2_2P8	2.8V from LDO for Actuator of camera sensor	2.8V
J19.15	J16.15	MIPI_CSI1_DATA2_P	MIPI CSI 1, differential lane 2 – plus	
J19.16	J16.16	GND	Ground	-
J19.17	J16.17	MIPI_CSI1_DATA2_N	MIPI CSI 1, differential lane 2 – minus	

J19.18	J16.18	VREG_BOB	Regulated power supply from PMIC	3.3 V - 3.55V
J19.19	J16.19	GND	Ground	-
J19.20	J16.20	VREG_BOB	Regulated power supply from PMIC	3.3 V - 3.55V
J19.21	J16.21	MIPI_CSI1_DATA3_N	MIPI CSI 1, differential lane 3 – minus	
J19.22	J16.22	VREG_BOB	Regulated BOB output of PMIC660L	3.3 V - 3.55V
J19.23	J16.23	MIPI_CSI1_DATA3_P	MIPI CSI 1, differential lane 3 – plus	
J19.24	J16.24	GND	Ground	-
J19.25	J16.25	GND	Ground	-
J19.26	J16.26	GND	Ground	-
J19.27	J16.27	MIPI_CSI1_DATA0_N	MIPI CSI 1, differential lane 0 – minus	
J19.28	J16.28	VREG_L11A	PM660 Linear regulator L11 output	1.8V
J19.29	J16.29	MIPI_CSI1_DATA0_P	MIPI CSI 1, differential lane 0 – plus	
J19.30	J16.30	GND	Ground	-
J19.31	J16.31	GND	Ground	-
J19.32	J16.32	CAM_MCLK2	MCLK2 for camera Sensor	1.8V
J19.33	J16.33	CAM_MCLK3	MCLK3 for camera Sensor	1.8V
J19.34	J16.34	GND	Ground	-
J19.35	J16.35	GND	Ground	-
J19.36	J16.36	CSI1_CAM_STROBE	Strobe signal for camera Sensor	1.8V
J19.37	J16.37	CCI_I2C_SDA1	Camera I2C Data	1.8V

J19.38	J16.38	CAM2_STANDBY_N	Power down signal for camera sensor	1.8V
J19.39	J16.39	CCI_I2C_SCL1	Camera I2C Clock	1.8V
J19.40	J16.40	CAM2_RST_N	Reset signal for Camera	1.8V
J19.41	J16.41	GND	Ground	-
J19.42	J16.42	GND	Ground	-
J19.43	J16.43	USB2_HS_DP	USB high-speed 2 data – plus	
J19.44	J16.44	GPIO103_ETHERNET_RESET	GPIO103/ Reset signal for Ethernet	1.8V
J19.45	J16.45	USB2_HS_DM	USB high-speed 2 data – minus	
J19.46	J16.46	USB_HUB_EN	GPIO 76/ Enable signal for USB HUB IC.	1.8V
J19.47	J16.47	GND	Ground	-
J19.48	J16.48	GPIO74_USB_HUB_RESET	GPIO 74/ Reset signal for USB HUB IC.	1.8V
J19.49	J16.49	LCD1_MIPI_DSI0_RST	Reset signal for optional LCD	1.8V
J19.50	J16.50	GND	Ground	-
J19.51	J16.51	LCD1_DSI0_TOUCH_INT	Interrupt signal (of Touch screen) for optional LCD.	1.8V
J19.52	J16.52	LCD1_DSI0_BL_EN	Enable signal for optional LCD.	1.8V
J19.53	J16.53	LCD1_DSI0_TOUCH_RESET	Reset signal (of touch screen) for optional LCD.	1.8V
J19.54	J16.54	LCD1_WLED_SINK1	WLED low-side current sink input, string 1	-
J19.55	J16.55	LCD1_DSI0_TOUCH_GPIO	GPIO 73	1.8V
J19.56	J16.56	LCD1_WLED_SINK2	WLED low-side current sink input, string 2	-
J19.57	J16.57	GND	Ground	-

J19.58	J16.58	GND	Ground	-
J19.59	J16.59	NC	No Connection	-
J19.60	J16.60	NC	No Connection	-
J19.61	J16.61	NC	No Connection	-
J19.62	J16.62	NC	No Connection	-
J19.63	J16.63	GND	Ground	-
J19.64	J16.64	GND	Ground	-
J19.65	J16.65	LCD1_BLSP_I2C_SCL_4	BLSP4- I2C Clock , Used for LCD	1.8V
J19.66	J16.66	GND	Ground	-
J19.67	J16.67	LCD1_BLSP_I2C_SDA_4	BLSP4- I2C DATA , Used for LCD	1.8V
J19.68	J16.68	GND	Ground	-
J19.69	J16.69	LCD1_WLED_SINK3	WLED low-side current sink input, string 3	-
J19.70	J16.70	VREG_L5B	PM660L Linear regulator L5 output	2.96V
J19.71	J16.71	LCD1_DSI0_BACKLIGHT_PWM	PWM signal for back light of optional LCD.	1.8V
J19.72	J16.72	VREG_L5B	PM660L Linear regulator L5 output	2.96V
J19.73	J16.73	LCD1_BACKLIGHT_0	External dimming control pin PWM input, controls LED brightness	-
J19.74	J16.74	GND	Ground	-
J19.75	J16.75	GND	Ground	-
J19.76	J16.76	GND	Ground	-
J19.77	J16.77	MIPI_DSI1_LANE2_P	MIPI display serial interface 1 lane 2– positive	

J19.78	J16.78	GND	Ground	-
J19.79	J16.79	MIPI_DSI1_LANE2_N	MIPI display serial interface 1 lane 2– negative	
J19.80	J16.80	GND	Ground	-
J19.81	J16.81	GND	Ground	-
J19.82	J16.82	GND	Ground	-
J19.83	J16.83	MIPI_DSI1_LANE1_P	MIPI display serial interface 1 lane 1– positive	-
J19.84	J16.84	VREG_L17A	PM660 Linear regulator L17 output	1.8V
J19.85	J16.85	MIPI_DSI1_LANE1_N	MIPI display serial interface 1 lane 1– negative	-
J19.86	J16.86	GND	Ground	-
J19.87	J16.87	GND	Ground	-
J19.88	J16.88	VREG_L15A	PM660 Linear regulator L15 output	1.8V
J19.89	J16.89	MIPI_DSI1_CLK_P	MIPI display serial interface 1 clock – positive	-
J19.90	J16.90	GND	Ground	-
J19.91	J16.91	MIPI_DSI1_CLK_N	MIPI display serial interface 1 clock – negative	-
J19.92	J16.92	GND	Ground	-
J19.93	J16.93	GND	Ground	-
J19.94	J16.94	GND	Ground	-
J19.95	J16.95	MIPI_DSI1_LANE0_P	MIPI display serial interface 1 lane 0– positive	-
J19.96	J16.96	MIPI_DSI1_LANE3_P	MIPI display serial interface 1 lane 3 – positive	-

J19.97	J16.97	MIPI_DSI1_LANE0_N	MIPI display serial interface 1 lane 0– negative	-
J19.98	J16.98	MIPI_DSI1_LANE3_N	MIPI display serial interface 1 lane 3– negative	
J19.99	J16.99	GND	Ground	-
J19.100	J16.100	GND	Ground	-

Table 9 : Connector J19 pin details

6.2 Major Interfaces of ERAGON660 SBC

6.2.1 Processor SDA660 - Features and interfaces

- The Qualcomm SDA660 includes a customized 64-bit ARM v8-compliant applications processor (Kryo 260)
- Quad high-performance Kryo cores targeting 2.2 GHz – Gold cluster with 1 MB L2 & Quad low-power Kryo cores targeting 1.843 GHz – Silver cluster with 1 MB L2
- It embraces Qualcomm Hexagon DSP with Hexagon Vector eXtensions (dual-HVX512) 787 MHz.
- Low power island with Hexagon DSP consists of Snapdragon sensor core and low power audio subsystem

Memory Support Features

- Dual-channel non-PoP high-speed memory – LPDDR4 /LPDR4x SDRAM designed for a 1866 MHz clock.
- Support up to 64GB external eMMC v5.1 memory via SDC1 interface.
- UFS 2.1 gear 3 (one-lane) and SD 3.0

Multimedia features

- Three 4-lane CSIs (4/4/4 or 4/4/2/1) D-PHY 1.2 at 2.1 Gbps per lane or three 3-lane C-PHY 1.0 at 17 Gbps (2.5 G symbols per trio per second)
- Dual 14-bit image signal processing (ISP): 16 +16 MP, 540 MHz each; 24MP30 ZSL with dual ISP; 16 MP 30 ZSL with a single ISP
- Video support: 3840 × 2160 at 30 Hz, HEVC Main 10, VP9, H264, and other popular video formats Two MI2S Ports for Audio interface.
- Processor supports one port SLIM bus interfaces to WCD9335 codec.
- Processor also support CDC PDM port to interface with PM660l for audio applications.

Web technologies

- V8 JavaScript Engine optimizations
- Web kit browser JPEG hardware decode acceleration
- Networking Stack IP and HTTP tuning
- Flash 10.x and video processor decode optimization.

Connectivity

- 8, 4-bits each BLSP Ports which can be configured as UART, I2C and SPI.
- One USB 3.1/2.0 Port.
- Gigabit Ethernet connectivity on IO Card.

Wireless Connectivity

- With WCN3990, it supports 802.11 b/g/n/ac mode for 2.4GHz band and with MIMO configuration; it supports 802.11 a/n/ac mode for 5GHz band with MIMO configuration.
- WCN3990 also supports Bluetooth 5.0.
- With SDR660 receiver, SDA660 supports GPS location suite.

Power Management

- Combination of PM660 and PM660L interfaced through two 2-line SPMI.
- Dedicated clock and reset lines; plus other GPIOs as needed.

6.2.2 Memory Interface

In ERAGON660 SBC integrates with single Embedded Multi Chip Package (eMCP) has dual function of LPDDR4X RAM and eMMC v5.1 flash. SBC supports up to 4GB of LPDDR4X RAM at max 1833 MHz clock and 64GB of eMMC flash.

- The LPDDR4X has 32-bit wide bus width interfaced with SDA660 through EBI.
- The eMMC v5.1 has 8-bit wide bus width interfacing with SDA660 through SDC1 interface.

6.2.3 Wi-Fi + BT Interface

The ERAGON660 board deployed Qualcomm's RF chip WCN3990B solution that integrates two different wireless connectivity technologies into a single device, the interfaces are:

- Dual-band 2.4GHz and 5GHz WLAN compliant with IEEE 802.11 a/b/g/n/ac specifications and supports external PA for both bands
- Bluetooth compliant with the BT specifications version 5.0 (BR/EDR + BLE).

All above RF signal is routed through a dual antenna (MIMO). To connect external antenna on ERAGON660 SBC board U.FL connector is provided. In addition, support for chip antenna is given on ERAGON660 SBC. In default the RF path is connected with chip antenna.

6.2.4 GPS Interface

The ERAGON660 board supports GPS interface, for which SDA660 is interfaced with Qualcomm's GNSS receiver chip SRD660G. U.FL connector is provided on SBC for GPS external antenna.

6.2.5 PMIC Interface

ERAGON660 SBC module has combination of PM660 and PM660L for Power management. Both the PMICs are interfaced to SDA660 through two-line SPMI bus.

6.2.6 System LEDs

There are four notification LEDs provided on SBC module as described below,

- LED1 (Processor reset out LED): its glow indicates that processor came out of reset
- LED2 (Charging LED): Indicates battery charging status.
- D1: Indicates that 12V DC supply present.
- D14(RGB LED) : Multipurpose led

6.3 Major Blocks of ERAGON660

6.3.1 Power Supply

ERAGON660 kit can be powered through 12V@3A DC adapter or 3.8V Li battery. Switching between these supplies can be done through switch (SW2). Both power modes are described below,

6.3.1.1 DC mode

In DC mode, 12VDC adapter need to plug into connector J9 of SBC with below settings,

- Pull switch (SW2) direction towards DC Jack (ON).

From this 12V supply, remaining power supplies generated for other peripherals.

Figure 5 – SBC DC Jack (J9)

Figure 6 – SBC Switch (SW2)

6.3.1.2 Battery mode

In Battery mode, battery need to connected on connector J15 of SBC with below settings,

- Pull switch (SW2) direction opposite of DC jack (Off).

Figure 7 – SBC Battery Connector (J15)

6.3.2 Boot Configuration

The ERAGON660 can be configured to function in different modes by selecting the switch SW3 provided on SBC. Below table mentions different boot configurations options,

CONFIG_3 (Position-3)	CONFIG_2 (Position-2)	CONFIG_1 (Position-1)	FORCE_USB_BOOT (Position-4)	Function
0	0	0	0	eMMC --> SD --> USB
0	0	1	0	SD --> eMMC
0	1	0	0	SD
0	1	1	0	USB
1	0	0	0	UFS HS-G1
1	0	1	0	SD --> UFS

Table 10: ERAGON660 BOOT Configuration options

CONFIG switch in ON position indicates level 1. To boot through eMMC --> SD --> USB make sure SW3 is 0000.

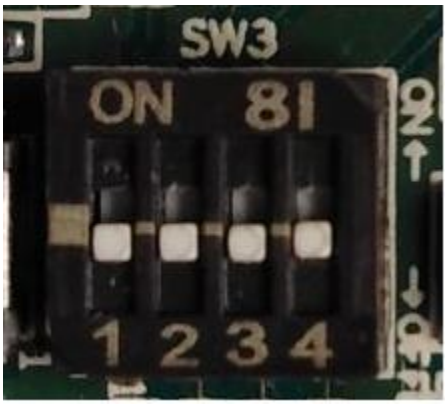

Figure 8 – SBC Boot Configuration Switch (SW1)

6.3.3 General Purpose Keys

There are three general-purpose keys provided on SBC. Their applications are as below,

- SW1 (Power ON/Sleep mode switch): If board goes in the sleep mode, then by pressing SW1 we can get Board out of sleep mode. After power ON the board with battery, this key need to be press to boot up.
- SW4 (Volume up): This key is pressed to up the volume of media.
- SW5 (Fast boot switch or Volume down): This switch is pressed to get processor into Fast boot mode or to reduce the volume of media.

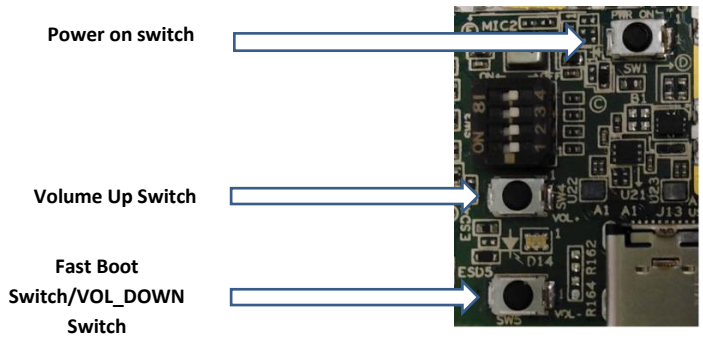

Figure 9 – SBC General Purpose Keys (SW1,SW4 & SW5)

6.3.4 MIPI CSI Interface

ERAGON660 kit supports three 4 Lane MIPI CSI ports; however only two can work concurrently. Below are its features,

- Three 4 Lane CSI Ports at 2.1 Gbps per lane data rate.
- Dual 14-bit image signal processing (ISP): 16 +16 MP, 540 MHz each; 24MP30 ZSL with dual ISP; 16 MP 30 ZSL with a single ISP
- There are two dedicated I2C (CCI0 & CCI1) signals along with reset and power down signals for camera interface.
- CSI0 and CSI2 connector is on SBC and CSI2 connector on IO Card.

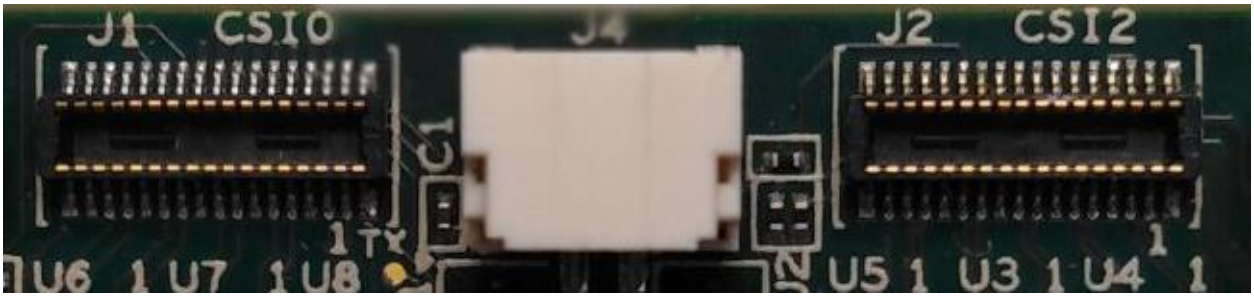

Figure 10 – SBC MIPI CSI connectors (CSI0, CSI2)

Pin description for CSI interface is as below, Camera board direct connect with SBC and connect the Camera board to IO card through FPC cable.

Pin Number	Net Name	Pin Function
J1.1	MIPI_CSI0_DATA2_P_CONN	MIPI CSI0 Data 2 Positive
J1.2	VREG_DVDD_1P2	1.2V supply
J1.3	MIPI_CSI0_DATA2_N_CONN	MIPI CSI1 Data 2 Negative
J1.4	VREG_DVDD_1P05V	1.5V supply
J1.5	GND	Ground
J1.6	VREG_DVDD_1P05V	1.5V supply
J1.7	MIPI_CSI0_DATA3_P_CONN	MIPI CSI0 Data 3 Positive
J1.8	GND	Ground
J1.9	MIPI_CSI0_DATA3_N_CONN	MIPI CSI0 Data 3 Negative
J1.10	GND	Ground
J1.11	GND	Ground
J1.12	CAM_AVDD_2P8	2.8V supply
J1.13	MIPI_CSI0_DATA1_P_CONN	MIPI CSI0 Data 1 Positive
J1.14	VREG_L11A	1.8V supply
J1.15	MIPI_CSI0_DATA1_N_CONN	MIPI CSI0 Data 1 Negative
J1.16	VCM_MCAM2_2P8	2.8V supply
J1.17	GND	Ground
J1.18	GND	Ground
J1.19	MIPI_CSI0_CLK_P_CONN	MIPI CSI0 Clock Positive
J1.20	CAM_MCLK0	Master Clock0 for camera
J1.21	MIPI_CSI0_CLK_N_CONN	MIPI CSI0 Clock Negative
J1.22	CSI0_CAM_STROBE	Camera Strobe Signal
J1.23	GND	Ground
J1.24	CAM0_RST_N	Camera Reset Signal
J1.25	MIPI_CSI0_DATA0_P_CONN	MIPI CSI0 Data 1 Positive
J1.26	CAM0_STANDBY_N	Camera Standby Signal
J1.27	MIPI_CSI0_DATA0_N_CONN	MIPI CSI0 Data 1 Negative
J1.28	CCI_I2C_SCL0	I2C-0 System Clock
J1.29	GND	Ground
J1.30	CCI_I2C_SDA0	I2C-0 System Data

Table 11: SBC MIPI CSI0 Pin Description (J1)

Pin Number	Net Name	Pin Function
J2.1	MIPI_CSI2_DATA2_P_CONN	MIPI CSI2 Data 2 Positive
J2.2	VREG_DVDD_1P2	1.2V supply
J2.3	MIPI_CSI2_DATA2_N_CONN	MIPI CSI2 Data 2 Negative
J2.4	VREG_DVDD_1P05V	1.5V supply
J2.5	GND	Ground
J2.6	VREG_DVDD_1P05V	1.5V supply
J2.7	MIPI_CSI2_DATA3_P_CONN	MIPI CSI2 Data 3 Positive
J2.8	GND	Ground
J2.9	MIPI_CSI2_DATA3_N_CONN	MIPI CSI2 Data 3 Negative
J2.10	GND	Ground
J2.11	GND	Ground
J2.12	CAM_AVDD_2P8	2.8V supply
J2.13	MIPI_CSI2_DATA1_P_CONN	MIPI CSI2 Data 1 Positive
J2.14	VREG_L11A	1.1V supply
J2.15	MIPI_CSI2_DATA1_N_CONN	MIPI CSI2 Data 1 Negative
J2.16	VCM_MCAM2_2P8	2.8V supply
J2.17	GND	Ground
J2.18	GND	Ground
J2.19	MIPI_CSI2_CLK_P_CONN	MIPI CSI2 Clock Positive
J2.20	CAM_MCLK1	Master Clock0 for camera
J2.21	MIPI_CSI2_CLK_N_CONN	MIPI CSI2 Clock Negative
J2.22	CSI2_CAM_STROBE	Camera Strobe Signal
J2.23	GND	Ground
J2.24	CAM1_RST_N	Camera Reset Signal
J2.25	MIPI_CSI2_DATA0_P_CONN	MIPI CSI2 Data 1 Positive
J2.26	CAM1_STANDBY_N	Camera Standby Signal
J2.27	MIPI_CSI2_DATA0_N_CONN	MIPI CSI2 Data 1 Negative
J2.28	CCI_I2C_SCL1	I2C-1 System Clock
J2.29	GND	Ground
J2.30	CCI_I2C_SDA1	I2C-1 System Data

Table 12: SBC MIPI CSI2 Pin Description (J2)

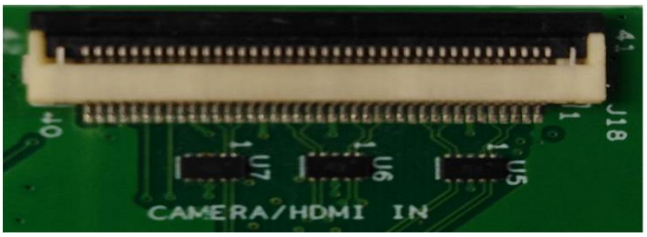

Figure 11 – IO Card MIPI CSI1 connectors (J18)

Pin Number	Net Name	
J18.1	GND	Ground
J18.2	MIPI_CSI1_CLK_P	MIPI CSI1 Clock Positive
J18.3	MIPI_CSI1_CLK_N	MIPI CSI1 Clock Negative
J18.4	GND	Ground
J18.5	MIPI_CSI1_DATA2_N	MIPI CSI1 Data 2 Negative
J18.6	MIPI_CSI1_DATA2_P	MIPI CSI1 Data 2 Positive
J18.7	GND	Ground
J18.8	MIPI_CSI1_DATA1_P	MIPI CSI1 Data 1 Positive
J18.9	MIPI_CSI1_DATA1_N	MIPI CSI1 Data 1 Negative
J18.10	GND	Ground
J18.11	MIPI_CSI1_DATA0_P	MIPI CSI1 Data 0 Positive
J18.12	MIPI_CSI1_DATA0_N	MIPI CSI1 Data 0 Negative
J18.13	GND	Ground
J18.14	MIPI_CSI1_DATA3_N	MIPI CSI1 Data 3 Negative
J18.15	MIPI_CSI1_DATA3_P	MIPI CSI1 Data 3 Positive
J18.16	GND	Ground
J18.17	5V_LOAD_CSI	5V Supply
J18.18	5V_LOAD_CSI	5V Supply
J18.19	5V_LOAD_CSI	5V Supply
J18.20	CAM2_STANDBY_N	Camera -2 Standby Signal
J18.21	CAM_MCLK2	Master Clock2 for camera
J18.22	CAM2_RST_N	Camera – 2 Reset Signal
J18.23	GND	Ground
J18.24	CCI_I2C_SDA1	I2C-1 System Data
J18.25	CCI_I2C_SCL1	I2C-1 System Clock
J18.26	GND	Ground
J18.27	CAM_MCLK3	Master Clock3 for camera
J18.28	CSI1_CAM_STROBE	Camera Strobe Signal
J18.29	NC	Not Connected
J18.30	GND	Ground
J18.M1	GND	Mechanical pin Grounded
J18.M2	GND	Mechanical pin Grounded

Table 13 : IO Card MIPI CSI1 Pin Description (J18)

6.3.5 MIPI DSI Interface

ERAGON660 kit supports Dual 4 Lane MIPI DSI ports, DSI0 and DSI1. SBC has DSI0 and IO card has DSI1. Display support up to 2560 × 1600, 10 bit at 60 Hz.

- On DSI0 Port connect LCD display with backlight bridge board and on DSI1, we can connect DSI to HDMI Bridge board to display the data on HDMI supported display screen.
- Connect these bridge boards to IO Card through FPC cable.

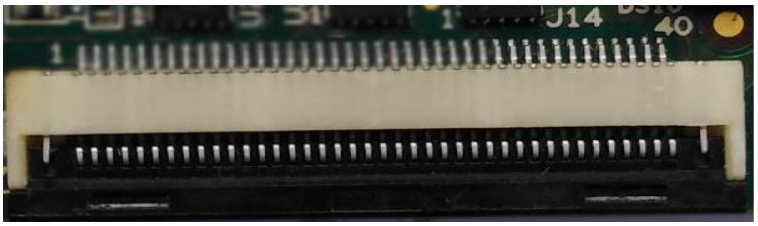

Figure 12 – SBC MIPI DSI0 connectors (J14)

There Pin specification is described in below tables,

Pin Number	Net Name	Pin Function
J14.1	GND	Ground
J14.2	LCD0_REG_WLED	Display backlight LED anode
J14.3	MIPI_DSI0_CLK_P_CONN	MIPI DSI0 Clock Positive
J14.4	LCD0_VDISP_M_OUT	Display Bias supply Negative
J14.5	MIPI_DSI0_CLK_M_CONN	MIPI DSI0 Clock Negative
J14.6	LCD0_VDISP_P_OUT	Display Bias supply Positive
J14.7	GND	Ground
J14.8	5V_LOAD_DISPLAY	5V Supply
J14.9	MIPI_DSI0_D0_P_CONN	MIPI DSI0 Data 0 Positive
J14.10	5V_LOAD_DISPLAY	5V Supply
J14.11	MIPI_DSI0_D0_M	MIPI DSI0 Data 0 Negative
J14.12	GND	Ground
J14.13	GND	Ground
J14.14	LCD0_MDP_VSYNC_P	
J14.15	MIPI_DSI0_D1_P_CONN	MIPI DSI0 Data 1 Positive
J14.16	LCD0_MIPI_DSI0_RST	MIPI DSI0 Reset
J14.17	MIPI_DSI0_D1_M_CONN	MIPI DSI0 Data 1 Negative
J14.18	NC	Not Connected
J14.19	GND	Ground
J14.20	LCD0_DSI0_BACKLIGHT_PWM	Display Backlight
J14.21	MIPI_DSI0_D2_P_CONN	MIPI DSI0 Data 2 Positive
J14.22	GND	Ground
J14.23	MIPI_DSI0_D2_M_CONN	MIPI DSI0 Data 2 Negative
J14.24	LCD0_DSI0_BL_EN	PMI White LED Enable
J14.25	GND	Ground
J14.26	LCD0_WLED_SINK1	Display backlight LED cathode 1

J14.27	MIPI_DSI0_D3_P_CONN	MIPI DSI0 Data 3 Positive
J14.28	LCD0_WLED_SINK2	Display backlight LED cathode 2
J14.29	MIPI_DSI0_D3_M_CONN	MIPI DSI0 Data 3 Negative
J14.30	LCD0_BACKLIGHT_0	PMI Backlight control signal
J14.31	GND	Ground
J14.32	GND	Ground
J14.33	LCD0_BLSP_I2C_SCL_4	MIPI DSI0 I2C Clock
J14.34	LCD0_DSI0_TOUCH_INT	Display Touch Interrupt
J14.35	LCD0_BLSP_I2C_SDA_4	MIPI DSI0 I2C2 Data
J14.36	LCD0_DSI0_TOUCH_RESET	Display Touch Reset
J14.37	GND	Ground
J14.38	LCD0_DSI0_TOUCH_GPIO	MIPI DSI0 Touch GPIO
J14.39	GND	Ground
J14.40	LCD0_WLED_SINK3	Display backlight LED cathode 3
J14.41	GND	Ground
J14.42	GND	Ground

Table 14: SBC MIPI DSI0 Pin Description (J14)

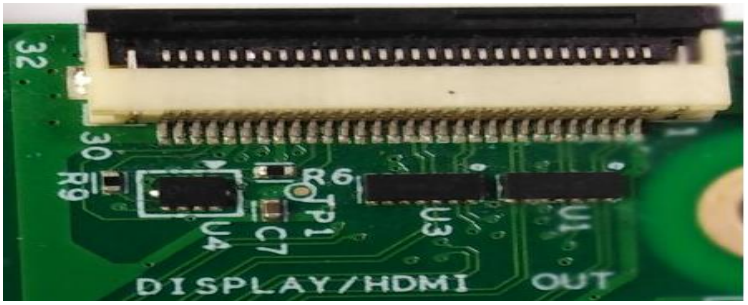

Figure 13 – IO Card MIPI DSI1 connectors (J18)

Pin Number	Net Name	Pin Function
J18.1	GND	Ground
J18.2	LCD1_REG_WLED	Display backlight LED anode
J18.3	MIPI_DSI1_CLK_P_CONN	MIPI DSI1 Clock Positive
J18.4	LCD1_VDISP_M_OUT	Display Bias supply Negative
J18.5	MIPI_DSI1_CLK_M_CONN	MIPI DSI1 Clock Negative
J18.6	LCD1_VDISP_P_OUT	Display Bias supply Positive
J18.7	GND	Ground
J18.8	5V_LOAD_DISPLAY	5V Supply
J18.9	MIPI_DSI1_D0_P_CONN	MIPI DSI1 Data 0 Positive
J18.10	5V_LOAD_DISPLAY	5V Supply

J18.11	MIPI_DSI1_D0_M_CONN	MIPI DSI1 Data 0 Negative
J18.12	GND	Ground
J18.13	GND	Ground
J18.14	NC	Not Connected
J18.15	MIPI_DSI1_D1_P_CONN	MIPI DSI1 Data 1 Positive
J18.16	LCD1_MIPI_DSI0_RST	MIPI DSI0 Reset
J18.17	MIPI_DSI1_D1_M_CONN	MIPI DSI1 Data 1 Negative
J18.18	NC	Not Connected
J18.19	GND	Ground
J18.20	LCD1_DSI0_BACKLIGHT_PWM	Display Backlight
J18.21	MIPI_DSI1_D2_P_CONN	MIPI DSI1 Data 2 Positive
J18.22	GND	Ground
J18.23	MIPI_DSI1_D2_M_CONN	MIPI DSI1 Data 2 Negative
J18.24	LCD1_DSI0_BL_EN	PMI White LED Enable
J18.25	GND	Ground
J18.26	LCD1_WLED_SINK1	Display backlight LED cathode 1
J18.27	MIPI_DSI1_D3_P_CONN	MIPI DSI0 Data 3 Positive
J18.28	LCD1_WLED_SINK2	Display backlight LED cathode 2
J18.29	MIPI_DSI1_D3_M_CONN	MIPI DSI0 Data 3 Negative
J18.30	LCD1_BACKLIGHT_0	PMI Backlight control signal
J18.31	GND	Ground
J18.32	GND	Ground
J18.33	LCD1_BLSP_I2C_SCL_4	MIPI DSI0 I2C Clock
J18.34	LCD1_DSI0_TOUCH_INT	Display Touch Interrupt
J18.35	LCD1_BLSP_I2C_SDA_4	MIPI DSI0 I2C2 Data
J18.36	LCD1_DSI0_TOUCH_RESET	Display Touch Reset
J18.37	GND	Ground
J18.38	LCD1_DSI0_TOUCH_GPIO	MIPI DSI0 Touch GPIO
J18.39	GND	Ground
J18.40	LCD1_WLED_SINK3	Display backlight LED cathode 3
J18.41	GND	Ground
J18.42	GND	Ground

Table 15: IO Card MIPI DSI1 Pin Description (J18)s

For more information about IO Card Display port (DSI1) selection and Related change in SBC (Single Board Computer), Kindly refer **the Eragon660_SBC_Display_Port_Selection_Guideline_Rev1.0**.

6.3.6 USB Interface

SDA660 supports one USB2.0 high speed and one USB3.1 (type C) Super speed Port with display port and USB2.0 out of them one USB2.0 comes to IO card through B2B connector. USB3.1 (Type C) use as ADB port and data port during OTG pen drive connection.

Figure 14 – SBC USB 3.1 Connector (J13)

Pinout Specification for the J13 are below,

Pin Number	Net Name	Pin Function
J13.A1	GND	Ground
J13.A2	USB3_SS_TX0_CONN_P	USB Super Speed Transmit Signal Positive
J13.A3	USB3_SS_TX0_CONN_M	USB Super Speed Receive Signal Negative
J13.A4	USB_VBUS_CONN	USB 5V Supply
J13.A5	USB3_CC1_CONN	USB CC1 (Configuration channel)
J13.A6	USB3_HS_CONN_DP	USB High Speed Signal Positive
J13.A7	USB3_HS_CONN_DM	USB High Speed Signal Negative
J13.A8	USB3_SBU1	Sideband use (SBU)
J13.A9	USB_VBUS_CONN	USB 5V Supply
J13.A10	USB3_SS_RX1_CONN_M	USB Super Speed Receive Signal Negative
J13.A11	USB3_SS_RX1_CONN_P	USB Super Speed Receive Signal Positive
J13.A12	GND	Ground
J13.B1	GND	Ground
J13.B2	USB3_SS_TX0_CONN_P	USB Super Speed Transmit Signal Positive
J13.B3	USB3_SS_TX0_CONN_M	USB Super Speed Receive Signal Negative
J13.B4	USB_VBUS_CONN	USB 5V Supply
J13.B5	USB3_CC2_CONN	USB CC2 (Configuration channel)
J13.B6	USB3_HS_CONN_DP	USB High Speed Signal Positive
J13.B7	USB3_HS_CONN_DM	USB High Speed Signal Negative
J13.B8	USB3_SBU2	Sideband use (SBU)
J13.B9	USB_VBUS_CONN	USB 5V Supply
J13.B10	USB3_SS_RX1_CONN_M	USB Super Speed Receive Signal Negative
J13.B11	USB3_SS_RX1_CONN_P	USB Super Speed Receive Signal Positive

J13.B12	GND	Ground
11	GND_EARTH_USB	EARTH
12	GND_EARTH_USB	EARTH
13	GND_EARTH_USB	EARTH
14	GND_EARTH_USB	EARTH
15	GND_EARTH_USB	EARTH
16	GND_EARTH_USB	EARTH
17	GND_EARTH_USB	EARTH
18	GND_EARTH_USB	EARTH

Table 16: SBC USB3.1 connector (J13) Pinout

IO card has USB 2.0 hub and Hub has 4 downstream port as mentioned below.

- Port 1: Downstream Port 1 is directly connected to M.2 (4G LTE) connector..
- Port 2: Downstream Port 2 is directly connected to Ethernet MAC.(USB to Ethernet)
- Port 3 and Port 4: These both Ports comes on USB1 (Dual row stack connector). Any USB 2.0 device can be connected to these hosts.

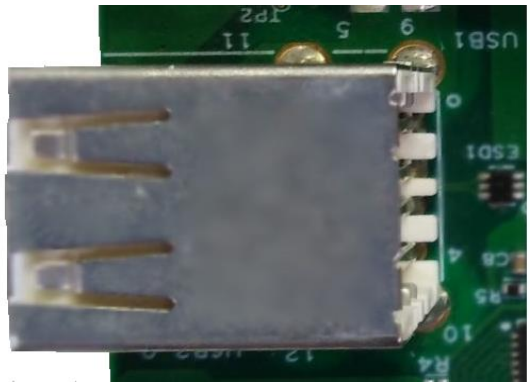

Figure 15 – IO Card USB Host1 and Host2 connections to USB Stack (USB1)

Pinout Specification for the J33 are below,

Pin Number	Net Name	Pin Function
USB1.A1	VCC_USB_HOST1	USB Host_1 5V Supply
USB1.A2	USB_DM_HOST4_CONN	USB Host_4 High Speed Signal Negative
USB1.A3	USB_DP_HOST4_CONN	USB Host_4 High Speed Signal Positive
USB1.A4	GND	Ground
USB1.B1	VCC_USB_HOST2	USB Host_2 5V Supply
USB1.B2	USB_DM_HOST3_CONN	USB Host_3 High Speed Signal Negative
USB1.B3	USB_DP_HOST3_CONN	USB Host_3 High Speed Signal Positive
USB1.B4	GND	Ground

USB1.S1	USB_SHEILD_GND	Shield Ground
USB1.S2	USB_SHEILD_GND	Shield Ground
USB1.S3	USB_SHEILD_GND	Shield Ground
USB1.S4	USB_SHEILD_GND	Shield Ground

Table 17: USB2.0 Host connector (J33) Pinout

6.3.7 Gigabit Ethernet

Gigabit Ethernet connectivity on ERAGON660 IO card is provided in below flow,
USB2.0 ->USB 2.0 HUB ->USB2.0 to Ethernet (MAC+PHY) to RJ45 connector
Second downstream port of USB Hub is connected with the Ethernet MAC controller. Then MAC controller is interfaced with Ethernet PHY which supports 10,100 and 1000Mbps speed and at the end Ethernet signals come to the RJ45 connector (E1) on IO card.

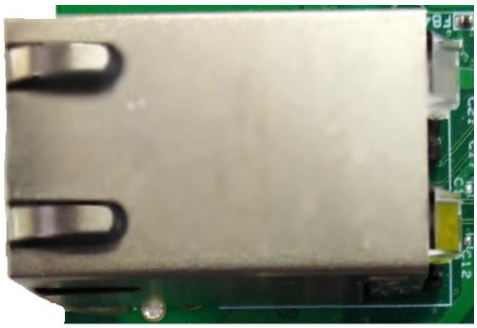

Figure 16 – IO Card Ethernet connector (E1)

Pinout of E1 are as below,

Pin Number	Net Name	Pin Function
E1.1	VDD_2V5_ETHERNET	2.5V Supply
E1.2	TR2N	TXRXC Negative
E1.3	TR2P	TXRX2 Positive
E1.4	TR1P	TXRX1 Positive
E1.5	TR1N	TXRX1 Negative
E1.6	VDD_2V5_ETHERNET	2.5V Supply
E1.7	VDD_2V5_ETHERNET	2.5V Supply
E1.8	TR3P	TXRX3 Positive
E1.9	TR3N	TXRX3 Negative
E1.10	TR0N	TXRX0 Negative
E1.11	TR0P	TXRX0 Positive

E1.12	VDD_2V5_ETHERNET	2.5V Supply
E1.13	GPIO4/LED4	GPIO -4 Pin
E1.14	VDD_2V5	2.5V Supply(Yellow Led anode)
E1.15	GPIO0/LED0	GPIO -0 Pin
E1.16	VDD_2V5	2.5V Supply(Orange Led anode)
E1.17	ETH_SHEILD_GND	Shield Ground
E1.18	ETH_SHEILD_GND	Shield Ground
E1.19	ETH_SHEILD_GND	Shield Ground
E1.20	ETH_SHEILD_GND	Shield Ground

Table 18: IO Card Ethernet (E1) Pinout

6.3.8 Audio Interface

ERAGON660 kit can support two audio codecs; WCD9335 is externally connected to IO Card as a daughter board and second is PMIC's internal codec. By default SBC will have connect with internal PMIC audio codec. SBC have two on board DMIC and connect the speaker on connector (J11). Connect Speaker Positive terminal of Speaker to J11.1 pin and Speaker Negative to J11.2 pin.

Figure 17 – SBC Speaker connector (J11)

To use the WCD9335 SBCe register DNP on SBC and WCD9335 daughter board connected to the IO Card card at connectors J20 and J21. This daughter board also has WSA8810 audio amplifier interfaced with codec.

ERAGON660 IO card supports 5 analog MICs,1 headset MIC, 3 Digital MICs, 2 stereo speaker outputs, 1 headset output, 1 Earpiece output, 2 Line outputs and all these peripherals excluding can be connected on headset connector J19, Female headers J24 & J22.

For more information about Audio Codec Selection and Related change in SBC (Single Board Computer), see **the Eragon660_SBC_Audio_Codec_Selection_Guideline_Rev1.0.**

Figure 18 – IO Card WCD9335 Audio Code Daughter Board

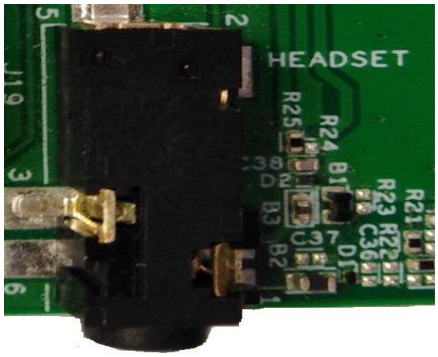

Figure 19 – IO Card Audio Headset Jack (J19)

Below is the Pinout Specification of Headset Jack,

Pin Number	Net Name	Pin Function
J19.1	AUDIO_JACK_SLEVE_MIC	MIC2 Input Positive
J19.2	AUDIO_JACK_TIP_LEFT	Headphone Left Channel
J19.3	AUDIO_JACK_RING1_RIGHT	Headphone Right Channel
J19.4	CDC_HPH_REF	Headphone Reference Signal (Ground)
J19.5	AUDIO_JACK_TIP_DET	Headset Detect Signal
J19.6	NC	Connected to Ground

Table 19: IO Card Headset (J19) Pinout

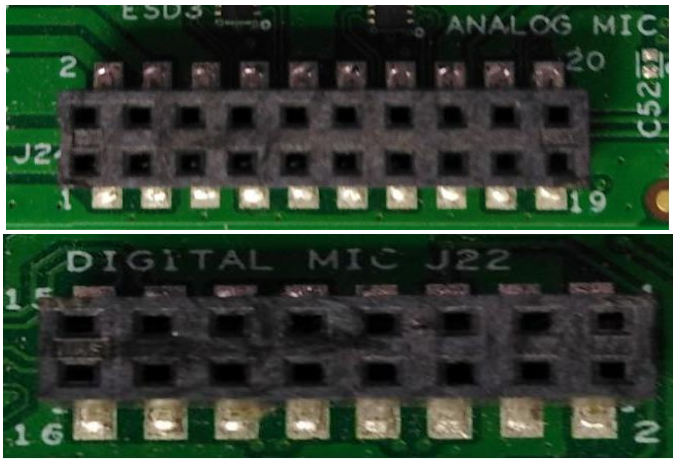

Figure 20 – IO Card Analog and Digital Codec Headers (J24 & J22)

Below is the Pinout Specification of J24,

Pin Number	Net Name	Pin Function
J24.1	CDC_SPEAKER1_OUT_M	Speaker1 Output Negative
J24.2	CDC_SPEAKER2_OUT_M	Speaker2 Output Negative
J24.3	CDC_SPEAKER1_OUT_P	Speaker1 Output Positive
J24.4	CDC_SPEAKER2_OUT_P	Speaker2 Output Positive
J24.5	GND	Ground
J24.6	GND	Ground
J24.7	CDC_IN3_M_CONN	MIC3 Input Negative
J24.8	CDC_IN4_M_CONN	MIC4 Input Negative
J24.9	CONN_CDC_MIC3_P	MIC3 Input Positive
J24.10	CONN_CDC_MIC4_P	MIC4 Input Positive
J24.11	CDC_IN1_M_CONN	MIC1 Input Negative
J24.12	CONN_CDC_MIC5_P	MIC5 Input Positive
J24.13	CONN_CDC_MIC1_P	MIC1 Input Positive
J24.14	CDC_IN5_M_CONN	MIC5 Input Negative
J24.15	GND	Ground
J24.16	GND	Ground
J24.17	CDC_EAR_P	Earpiece Output Positive
J24.18	CDC_IN6_M_CONN	MIC6 Input Negative
J24.19	CDC_EAR_M	Earpiece Output Negative
J24.20	CONN_CDC_MIC6_P	MIC6 Input Positive

Table 20: IO Card Audio Header (J24) Pinout

Below is the Pinout Specification of J22,

Pin Number	Net Name	Pin Function
J22.1	CDC_MIC_BIAS3	MIC Bias_3 Voltage
J22.2	CDC_MIC_BIAS4	MIC Bias_4 Voltage
J22.3	GND	Ground
J22.4	GND	Ground
J22.5	CDC_MIC_BIAS1	MIC Bias_1 Voltage
J22.6	CDC_DMIC_CLK1	Digital MIC_1 Clock
J22.7	GND	Ground
J22.8	CDC_DMIC_DATA1	Digital MIC_1 Data
J22.9	CDC_DMIC_CLK0	Digital MIC_0 Clock
J22.10	CDC_DMIC_CLK2	Digital MIC_2 Clock
J22.11	CDC_DMIC_DATA0	Digital MIC_0 Data
J22.12	CDC_DMIC_DATA2	Digital MIC_2 Data
J22.13	CDC_LINE_OUT1_M	Line Output_2 Positive
J22.14	CDC_LINE_OUT2_P	Line Output_1 Positive

J22.15	CDC_LINE_OUT1_P	Line Output_2 Negative
J22.16	CDC_LINE_OUT2_M	Line Output_1 Negative

Table 21: IO Card Audio Header (J22) Pinout

6.3.9 Sensors

ERAGON660 supports multiple sensors as below,

- Magnetometer, Accelerometer& Gyrometer, Pressure sensor and ALSP (Ambient Light and Proximity) sensor interfaced to SDA660 through LPI I2C and SPI.

6.3.10 Micro SD Card

The ERAGON660 SBC has push-push type Micro SD card slot for external storage device (SD card). SD card is interfaced with SDA660 (on SBC) through 4-bit SDC2 data signals along with SDC2 clock and SDC2 command signals. GPIO_54 of SDA660 is used to detect SD card insertion and removal.

Figure 21 – SBC Micro SD card connector

6.3.11 DSI to HDMI

The Qualcomm SDA660 Processor does not include a built-in HDMI interface. The ERAGON660 has the built-in MIPI-DSI 4 lanes interface, which is used, as a source for the HDMI output. A DSI to HDMI Bridge Board performs this task and it supports a resolution from 480p to 720p at 30Hz.

While the ADV7533 on the DSI to HDMI Bridge board supports automatic input video format timing detection (CEA-861E) and an I2C channel from the SDA660 allows the user to configure the operation of this Bridge Board. The BLSP4_I2C interface is used from the SoC that connects to the Bridge board.

This Bridge Board supports audio as well. The ERAGON660 uses a single bit MI2S_1 interface from the SNAPDRAGON 660 chip which is mentioned in the below block. The ERAGON660 contains the 14 pin HDMI Audio Connector (J23) on the board. A 3-wire (audio out only) I2S channel is routed directly from the SNAPDRAGON 660 SoC I2S interface pins to the DSI-HDMI bridge Board through HDMI Audio connector.

Figure 22 – IO Card HDMI to CSI Audio Connector (J23)

Pin specifications for J23 is mentioned below,

Pin Number	Net Name	
J23.1	VCC_3V3_C_HDMI	3.3V Supply
J23.2	NC	Not Connected
J23.3	VCC_5V_C_HDMI	5V Supply
J23.4	NC	Not Connected
J23.5	HDMI_1.8V_DSI	1.8V Supply
J23.6	NC	Not Connected
J23.7	GND	Ground
J23.8	GND	Ground
J23.9	LNBBCLK3_HDMI	CLK-3
J23.10	HDMI_MI2S_3_SCK	HDMI I2S 3 I2S Clock
J23.11	HDMI_HPD_N	HDMI Hot plug detection
J23.12	HDMI_MI2S_3_WS	HDMI I2S 3 Word Sync Clock
J23.13	GPIO_110_HDMI_INT_GPIO	HDMI Interrupt
J23.14	HDMI_MI2S_3_D0	HDMI I2S 3 Data 0 Signal
J23.M1	GND	Ground
J23.M2	GND	Ground

Table 22: IO Card HDMI Audio Connector (J23) Pinout

6.3.12 HDMI to CSI Audio interface

The Qualcomm SDA660 Processor does not include a built-in HDMI interface. The ERAGON660 has the built-in MIPI-CSI 4 lanes interface, which is used, as HDMI input. A HDMI to CSI bridge chip TC358840 converts HDMI signals to MIPI CSI Signals. These CSI signals interfaced with SNAPDRAGON 660 through MIPI CSI connectors mentioned in CSI section.

This Bridge Board supports audio as well. The ERAGON660 uses a MI2S_1 interface from the SNAPDRAGON 660 chip which is mentioned in the below block. The ERAGON660 contains the 16 pin HDMI Audio Connector (J13) on the board. A 6-wire (audio input) I2S channel is routed directly from the SNAPDRAGON 660 SoC I2S interface pins to the HDMI to CSI Bridge Board through HDMI Audio connector.

Figure 23 – IO Card DSI to HDMI Audio Connector (J13)

Pin specifications for J26 is mentioned below,

Pin Number	Net Name	
J13.1	GND	Ground
J13.2	GND	Ground
J13.3	GPIO_110_HDMI_INT_GPIO	HDMI Interrupt
J13.4	GPIO_29_HDMI_RST_N	HDMI Reset
J13.5	HDMI_MI2S_3_D0	HDMI I2S 3 Data 0 Signal
J13.6	HDMI_MI2S_3_D1	HDMI I2S 3 Data 1 Signal
J13.7	HDMI_MI2S_3_D2	HDMI I2S 3 Data 2 Signal
J13.8	HDMI_MI2S_3_D3	HDMI I2S 3 Data 3 Signal
J13.9	HDMI_MI2S_3_WS	HDMI I2S 3 Word Sync Clock
J13.10	HDMI_MI2S_3_SCK	HDMI I2S 3 I2S Clock
J13.11	BLSP_I2C_SCL_2	I2C 2 Clock
J13.12	BLSP_I2C_SDA_2	I2C 2 Data
J13.13	HDMI_1.8V	1.8V Supply
J13.14	HDMI_1.2V	1.2V Supply
J13.15	HDMI_3.3V	3.3V Supply
J13.16	HDMI_3.3V	3.3V Supply
J13.M1	GND	Ground
J13.M2	GND	Ground

Table 23: IO Card HDMI Audio Connector (J26) Pinout

6.3.13 WiFi + BT chip antenna

As mentioned in ERAGON660 SBC blocks, Default Wi-Fi + BT RF signal routed to Fractus chip antenna FR05-S1-NO-1-004 (ref ANTENNA1) to radiate. To use the external antenna mount/demount resistor and connect the external antenna on J8 and J12.

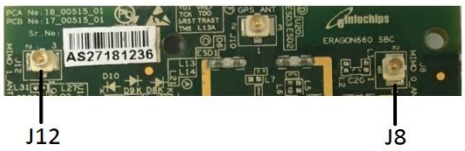

Figure 24 – SBC Routing of UFL cable from SBC to IO Card (J8 & J12)

6.3.14 GPS chip antenna

Connect the GPS external antenna on connector (J10)

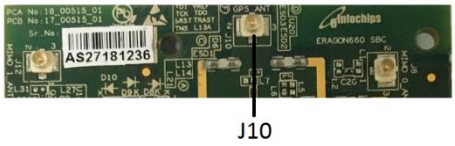

Figure 25 – SBC Routing of UFL cable from SBC to IO Card (10)

6.3.15 M.2 (4G LTE) connector

ERAGON660 kit supports 75-pin M.2 connector (J11) to plug 4G LTE modem on IO card. This 4G module is interfaced with first downstream port of USB Hub which it is connected to SDA660 processor, MI2S_2 interface, and few other GPIOs of SDA660 and Dual SIM card connectors (SIM1-J27, SIM2-J26).

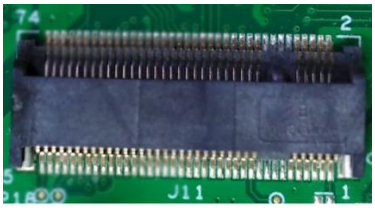

Figure 26 – IO Card M.2 connector (J11)

Figure 27 – IO Card SIM card connectors (J26 & J27)

Pinout specifications of J11 are below,

Pin Number	Net Name	
J11.1	NC	Not Connected
J11.2	3.7V_LOAD_REG	3.7V Supply For LTE Modem
J11.3	GND	Ground
J11.4	3.7V_LOAD_REG	3.7V Supply For LTE Modem
J11.5	GND	Ground
J11.6	LTE_MODEM_POWER	LTE Modem Power Control Signal
J11.7	USB_HS_D_P_HOST1	USB High Speed Data Positive Signal
J11.8	LTE_MODEM_W_DISABLE#1	LTE RF Radio Disable control GPIO

J11.9	USB_HS_D_M_HOST1	USB High Speed Data Negative Signal
J11.10	LTE_MODEM_LED#1	LED Driver Control GPIO
J11.11	GND	Ground
J11.12	NC	Not Connected
J11.13	NC	Not Connected
J11.14	NC	Not Connected
J11.15	NC	Not Connected
J11.16	NC	Not Connected
J11.17	NC	Not Connected
J11.18	NC	Not Connected
J11.19	NC	Not Connected
J11.20	MI2S2_LTE_CLK	I2S_2 Bit Clock
J11.21	TP17	Test Point 17
J11.22	MI2S2_LTE_DOUT	I2S_2 Data 0
J11.23	LTE_WAKE_HOST#_4G	Wake Host Signal
J11.24	MI2S2_LTE_DIN	I2S_2 Data 1
J11.25	LTE_MODEM_DPR	Dynamic Power Control
J11.26	LTE_MODEM_W_DISABLE#2	LTE GNSS Radio Disable control GPIO
J11.27	GND	Ground
J11.28	MI2S2_LTE_SYNC	I2S_2 Word Sync Clock
J11.29	NC	Not Connected
J11.30	SIM1_RST	SIM Card _1 Reset Signal
J11.31	NC	Not Connected
J11.32	SIM1_CLK	SIM Card _1 Clock
J11.33	GND	Ground
J11.34	SIM1_DATA	SIM Card _1 Data Signal
J11.35	NC	Not Connected
J11.36	SIM1_PWR	SIM Card _1 Power Supply
J11.37	NC	Not Connected
J11.38	NC	Not Connected
J11.39	GND	Ground
J11.40	SIM2_DETECT	SIM Card _2 Detect Signal
J11.41	NC	Not Connected
J11.42	SIM2_DATA	SIM Card _2 Data Signal
J11.43	NC	Not Connected
J11.44	SIM2_CLK	SIM Card _2 Clock
J11.45	GND	Ground
J11.46	SIM2_RST	SIM Card _2 Reset Signal
J11.47	NC	Not Connected
J11.48	SIM2_PWR	SIM Card _2 Power Supply
J11.49	NC	Not Connected
J11.50	NC	Not Connected

J11.51	GND	Ground
J11.52	NC	Not Connected
J11.53	NC	Not Connected
J11.54	NC	Not Connected
J11.55	NC	Not Connected
J11.56	NC	Not Connected
J11.57	GND	Ground
J11.58	NC	Not Connected
J11.59	GPIO_112_ANTCTL0	GPIO -112 Pin
J11.60	GPIO28_COEX3	GPIO for Coexistence
J11.61	GPIO_108/ANTCTL1	GPIO -108 Pin
J11.62	GPIO31_COEX2	Coexistence UART Transmit
J11.63	ANTCTL3	
J11.64	GPIO30_COEX1	Coexistence UART Receive
J11.65	GPIO_89/ANTCTL4	GPIO -89 Pin
J11.66	SIM1_DETECT	SIM Card _1 Detect Signal
J11.67	LTE_MODEM_RST	Modem Reset Signal
J11.68	NC	Not Connected
J11.69	TP19	Test Point 19
J11.70	3.7V_LOAD_REG	3.7V LTE RF Power Supply
J11.71	GND	Ground
J11.72	3.7V_LOAD_REG	3.7V LTE RF Power Supply
J11.73	GND	Ground
J11.74	3.7V_LOAD_REG	3.7V LTE RF Power Supply
J11.75	TP18	Test Point 18

Table 24: IO Card M.2 connector (J11) Pinout

SIM Card_1 Connector Pin specifications are as follows,

Pin Number	Net Name	Pin Function
J27.1	CONN_SIM1_PWR	SIM1 Power Supply
J27.2	SIM1_RST	SIM1 Reset Signal
J27.3	SIM1_CLK	SIM1 Clock
J27.4	GND	Ground
J27.5	NC	Not Connected
J27.6	SIM1_DATA	SIM1 Data
J27.7	SIM1_DETECT	SIM1 Card Detect
J27.8 to J27.17	SHEILD_GND	Shield Ground

Table 25: IO Card SIM CARD_1 connector (J27) Pinout

SIM Card_2 Connector Pin specifications are as follows,

Pin Number	Net Name	Pin Function
J26.1	CONN_SIM2_PWR	SIM2 Power Supply
J26.2	SIM2_RST	SIM2 Reset Signal
J26.3	SIM2_CLK	SIM2 Clock
J26.4	GND	Ground
J26.5	NC	Not Connected
J26.6	SIM2_DATA	SIM2 Data
J26.7	SIM2_DETECT	SIM2 Card Detect
J26.8 to J26.17	SHEILD_GND	Shield Ground

Table 26: IO Card SIM CARD_2 connector (J26) Pinout

6.3.16 Battery

ERAGON660 has a support to connect external rechargeable battery on connector J15 at SBC. Connect +Ve terminal of battery to J15.5 & J15.6 pin and GND to J15.1 & J15.2 pin.

Figure 28 – SBC Battery Connector (J15)

Battery Connector Pin specifications are as follows,

Pin Number	Net Name	Pin Function
J15.1	GND / VBATT_SNS_M	Ground and Battery Sense Negative
J15.2	GND / VBATT_SNS_M	Ground and Battery Sense Negative
J15.3	BATT_THERM	Battery therm
J15.4	BATT_ID	Battery ID
J15.5	VBATT_CONN / VBATT_SNS_P	Battery Supply Positive and Battery Sense Positive
J15.6	VBATT_CONN / VBATT_SNS_P	Battery Supply Positive and Battery Sense Positive

Table 27: SBC Battery Connector (J15) Pinout

6.3.17 FAN

ERAGON660 IO card also have support to connect 5VDC Fan at connector J5.
Connect +Ve terminal of Fan to J5.1 pin and GND to J5.2 pin.

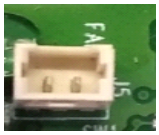

Figure 29 – IO Card FAN connector (J5)

6.3.18 Debug Port

ERAGON660 support a debug Port to capture the system logs. SBC has on board UART to USB converter chip FT230XQ-R (U32). It converts BLSP2 UART signals from SDA660 to USB high-speed signals. Therefore, to capture the logs, user only need to connect Micro USB cable to connector J7 on SBC.

Figure 30 – SBC Debug Port connection (J7)

Pinout specification of J7 mentioned below,

Pin Number	Net Name	Pin Function
J7.1	VBUS_5V_DEB	USB 5V Supply
J7.2	USB_DM_DEBUG_CONN	USB Data Negative
J7.3	USB_DP_DEBUG_CONN	USB Data Positive
J7.4	NC	Not Connected
J7.5	GND	Ground
J7.6 to J7.9	GND_EARTH_USB1	SHEILD_GND

Table 28: SBC Debug Port Connector (J7) Pinout

6.3.19 Low Speed Expansion Connector

Multiple BLSP signals brought from SDA660 to 20 pin male header (J6). User can use this signals to connect more peripherals.

J6 Pin Specification are given in below table.

Figure 31 – SBC Low Speed Expansion Header (J6)

Pin Specification of J6 mentioned below,

Pin Number	Net Name	
J6.1	VCC_1V8	1.8V Supply
J6.2	5V_USB_IN	5V Supply
J6.3	GND	GND
J6.4	GND	GND
J6.5	BLSP_SPI_CLK_3	BLSP_SPI_Clock
J6.6	BLSP_SPI_CS_N_3	BLSP_SPI_CS_3
J6.7	BLSP_SPI_MOSI_3	BLSP_SPI_MOSI
J6.8	BLSP_SPI_MISO_3	BLSP_SPI_MISO
J6.9	BLSP_I2C_SCL_6	BLSP_I2C_SCL_6
J6.10	BLSP1_SPI_CS_N_EXP	BLSP1_SPI_CS_N_EXP
J6.11	BLSP_I2C_SDA_6	BLSP_I2C_SDA_6
J6.12	BLSP1_SPI_MISO_EXP	BLSP1_SPI_MISO_EXP
J6.13	BLSP1_SPI_CLK_EXP	BLSP1_SPI_CLK_EXP
J6.14	BLSP_UART_TX_5	BLSP_UART_TX_5
J6.15	BLSP1_SPI_MOSI_EXP	BLSP1_SPI_MOSI_EXP
J6.16	BLSP_UART_RX_5	BLSP_UART_RX_5
J6.17	LNBBCLK3	LNBBCLK3
J6.18	BLSP_UART_CTS_N_5	BLSP_UART_CTS_N_5
J6.19	GND	GND
J6.20	BLSP_UART_RFR_N_5	BLSP_UART_RFR_N_5

Table 29: SBC Low Speed Expansion Header (20) Pinout

Note: SBCe of above interfaces are multiplexed with other peripherals also.

6.3.20 Expansion Connector

Different signals from SBC module are brought to IO card on 20 pin Female Headers (J4, J8).
IO Card has I2C base GPIO expander chip and its signal came on connector J4.
User can interface other I2S based peripherals to SBC module through connector J8.

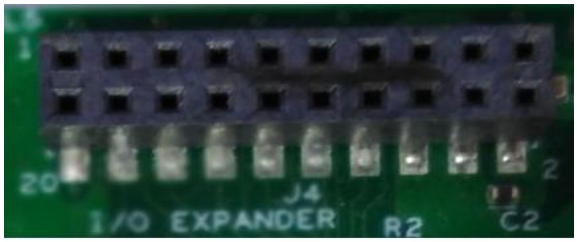

Figure 32 – IO Card Expansion Header (J4)

Pinout specification of J4 is given below,

Pin Number	Net Name	Pin Function
J4.1	VCC_1V8	1.8V Supply
J4.2	VCC_3V3	3.3V Supply
J4.3	GND	Ground
J4.4	GND	Ground
J4.5	GND	Ground
J4.6	GND	Ground
J4.7	IOE_GPIO_1	GPIO -1 Pin
J4.8	IOE_GPIO_2	GPIO -2 Pin
J4.9	IOE_GPIO_3	GPIO -3 Pin
J4.10	IOE_GPIO_4	GPIO -4 Pin
J4.11	IOE_GPIO_5	GPIO -5 Pin
J4.12	IOE_GPIO_6	GPIO -6 Pin
J4.13	IOE_GPIO_7	GPIO -7 Pin
J4.14	IOE_GPIO_9	GPIO -9 Pin
J4.15	IOE_GPIO_11	GPIO -11 Pin
J4.16	IOE_GPIO_10	GPIO -10 Pin
J4.17	GPIO_28_1	GPIO -28 Pin
J4.18	IOE_GPIO_12	GPIO -12 Pin
J4.19	LPI_GPIO_16	GPIO -16 Pin
J4.20	LPI_GPIO_17	GPIO -17 Pin

Table 30: IO Card Expansion Header (20) Pinout

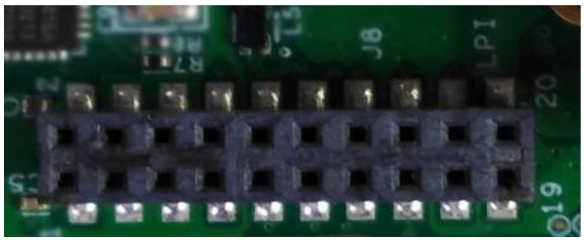

Figure 33 – IO Card Expansion Header (J8)

Pinout specification of J8 is given below,

Pin Number	Net Name	Pin Function
J8.1	VCC_1V8	1.8V Supply
J8.2	VCC_3V3	3.3V Supply
J8.3	GND	Ground
J8.4	GND	Ground
J8.5	GND	Ground
J8.6	GND	Ground
J8.7	I2C_SCL	I2C Clock
J8.8	I2C_SDA	I2C Data
J8.9	LPI_I2C_3_SDA	I2C – 3 Data
J8.10	LPI_UART_2_RX	UART-2 receive
J8.11	LPI_I2C_3_SCL	I2C – 3 Clock
J8.12	LPI_GPIO26_EXTR1	GPIO -26 Pin
J8.13	LPI_UART_2_TX	UART-2 transmit
J8.14	HDMI_MI2S_3_SCK	I2C – 3 Clock
J8.15	HDMI_MI2S_3_WS	HDMI I2S 3 Word Sync Clock
J8.16	LPI_GPIO27_EXTR2	GPIO -27 Pin
J8.17	LPI_GPIO29_EXTR4	GPIO -29 Pin
J8.18	LPI_GPIO28_EXTR3	GPIO -28 Pin
J8.19	HDMI_MI2S_3_D1	HDMI I2S 3 Data 1 Signal
J8.20	HDMI_MI2S_3_D0	HDMI I2S 3 Data 0 Signal

Table 31: IO Card Expansion Header (20) Pinout

7 Electrical Specification

7.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
VBATT+	Main Battery Input Supply Voltage	-0.5	6.0	V
VDC	12VDC Input Supply Voltage	-0.5	16	V
VCOIN	RTC Input Supply Voltage	-0.5	3.5	V
USB_VBUS	USB VBUS Input Supply Voltage	-0.3	16	V

Table 32 : Absolute Maximum Ratings

7.2 Operating Conditions s

Parameter		Min	Typ	Max	Unit
VBATT+	Main Battery Input Supply Voltage	2.8	3.8	4.75	V
VDC	12VDC Input Supply Voltage	11.5	12	12.5	V
VCOIN	RTC Input Supply Voltage	2.1	3.0	3.25	V
USB_VBUS	USB VBUS Input Supply Voltage	3.6	5.0	10	V

Table 33 : Operating Conditions

8 Mechanical Specification

8.1 SBC Board Dimensions

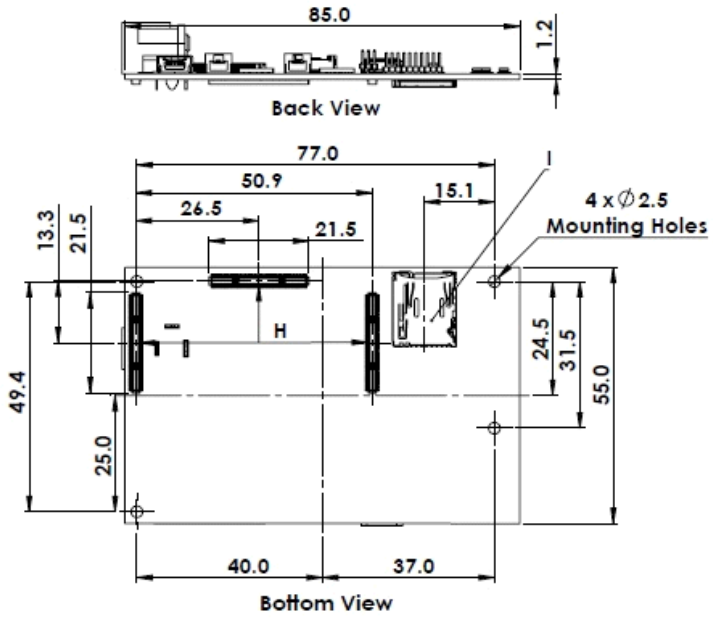

Figure 34 – SBC Module Dimension

For more information about SBC mechanical dimension , kindly refer **the Eragon660 SBC .dxf** file.

8.2 IO Card Dimension

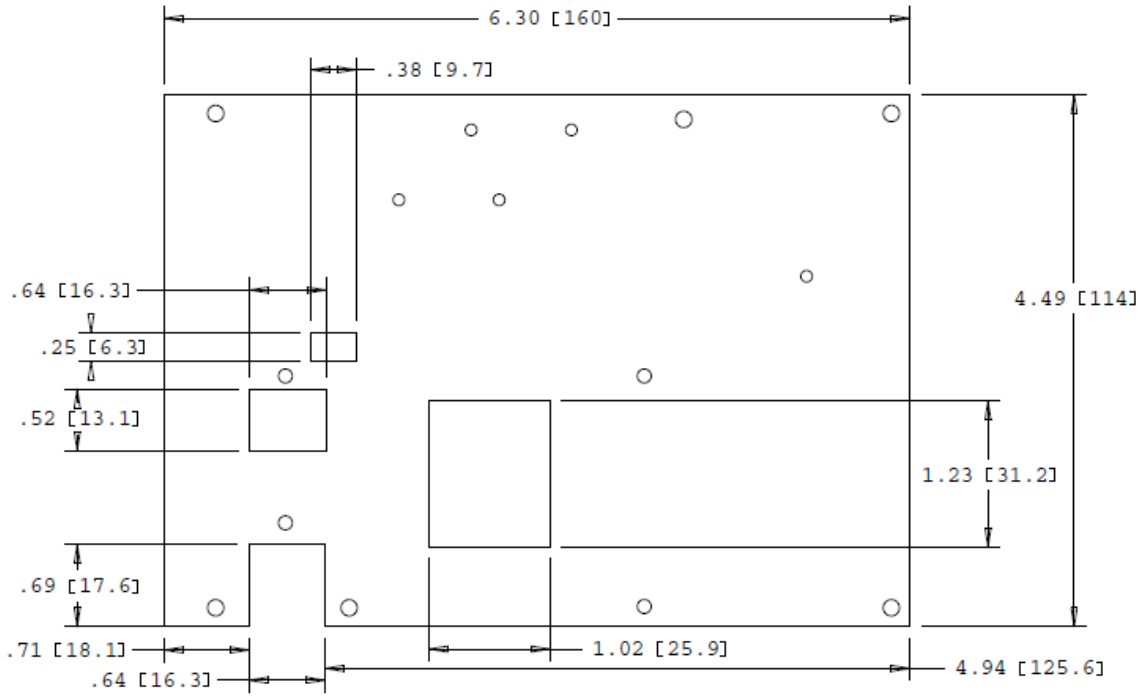

Figure 35 – IO Card Dimension

9 Special Care when using ERAGON660 Board

9.1 Development Device Notice

This device contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is intended for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

9.2 Anti-Static Handling Procedure

This device has exposed PCB and chips. Accordingly, proper anti-static precautions should be employed when handling the kit, including:

- Use a grounded anti-static mat
- Use a grounded wrist or foot strap

10 About eInfochips

eInfochips is a partner of choice for Fortune 500 companies for product innovation and hi-tech engineering consulting. Since 1994, eInfochips has provided solutions to key verticals like Aerospace & Defense, Consumer Electronics, Energy & Utilities, Healthcare, Home, Office, and Industrial Automation, Media & Broadcast, Medical Devices, Retail & e-Commerce, Security & Surveillance, Semiconductor, Software/ISV and Storage & Compute.

Covering every aspect of the product lifecycle, eInfochips draws from an experience of building 500+ products that have over 10 Million units deployed – to provide solutions on Product Design and Development, QA and Certifications, Reengineering, Sustenance and Volume Production. Being an innovation driven company, 5% of our revenues are earmarked for building reusable IPs that will accelerate product design cycles and reduce product risks.

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Today, more than 1400 chip mates operate from over 10 Design Centers and dozen Sales Offices spread across Asia, Europe and US.

Our clients have recognized our teams for commitment, teamwork and initiatives that we have brought forward, adding immense value to client processes and products. Chip mates have a strong growth path defined for them, with specific soft-skills training modules – Lagaan, Pegasus and Altius – to groom leaders for the future.

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Technical Assistance:	eInfochips Qualcomm portal (www.supportcenter.einfochips.com)
Technical Support:	QCSupport@einfochips.com
Sales/Marketing Support:	marketing@einfochips.com

The host product shall be properly labelled to identify the modules within the host product.
The ISED certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labelled to display the ISED certification number for the module, preceded by the word "contains" or similar wording expressing the same meaning, as follows:
Contains IC: XXXXXX-YYYYYYYYYY
In this case, XXXXXX-YYYYYYYYYY is the module's certification number.

Le produit hôte devra être correctement étiqueté, de façon à permettre l'identification des modules qui s'y trouvent.
L'étiquette d'homologation d'un module d'ISDE devra être apposée sur le produit hôte à un endroit bien en vue, en tout temps. En l'absence d'étiquette, le produit hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module d'ISDE, précédé du mot « contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit :
Contient IC : XXXXXX-YYYYYYYYYY
Dans ce cas, XXXXXX-YYYYYYYYYY est le numéro d'homologation du module.

RF exposure Information

This device has been designed and manufactured to comply with the limits for exposure to RF energy set by the Federal Communications Commission (FCC) of the United States, Industry Canada (IC) and the European Union and other countries.

This product is of a fixed type, and the distance from the human body during normal use is >20CM, FCC RF exposure limit is 1 mW/cm^2 , IC RF exposure limit is 2.68W. The highest reported RF exposure value to FCC 0.01762 mW/cm2 ,The highest reported RF exposure value to IC 88.57mW.

Regulation Information

[FCC Information]

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Warning&Caution:

Any changes or modifications to the equipment not expressly approved by the party responsible for compliance could void user's authority to operate the equipment. Antenna shall be mounted in such a manner to minimize the potential for human contact during normal operation. The antenna should not be contacted during operation to avoid the possibility of exceeding the FCC radio frequency exposure limit.

A minimum separation distance of 20 cm must be maintained between the antenna and the person for this appliance to satisfy the RF exposure requirement.

Regulation Information
[IC Information]
This device complies with Industry Canada license-exempt RSS standard(s). Operation in subject to The following two conditions:
(1) this device may not cause interference, and
(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme avec Industrie Canada RSS standard exempts de licence(s), Son utilisation est soumise à Les deux conditions suivantes: (1) cet appareil ne peut pas provoquer d'interférences et (2) cet appareil doit accepter Toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement du dispositif.

※ This device is going to be operated in 5 150 MHz ~ 5 250 MHz frequency range, it is restricted in indoor environment only.

Information for OEM Integrator

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

[End product labelling]

The label for end product must include “Contains FCC ID: 2ATUP-Q660500, Contains IC: 25301-Q660500”.

[CAUTION: Exposure to Radio Frequency Radiation]

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. “This equipment should be installed and operated with minimum distance of 20cm between the radiator and your body. This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users.”