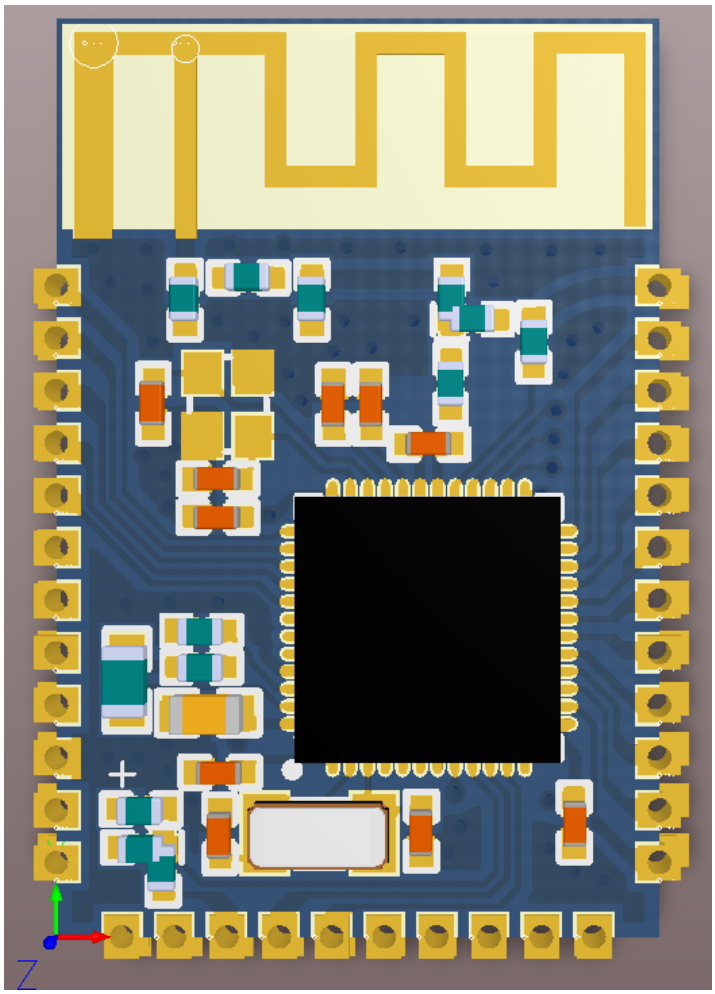
MKBN02 series BLE Module Datasheet

1. Product Description

MKBN02 series BLE module is a highly integrated BLE® 4.0 module with NFC function, it was designed for high data rate, short-range wireless communication in the 2.4GHz ISM band. The module is designed based on Nordic® Semiconductor nRF52832 radio Transceiver IC, has a 32 bit ARM® Cortex-M4 CPU, flash memory and analog and digital peripherals. MKBN02 provides a low power and ultra-low cost BLE and proprietary protocols for wireless transmission applications.



2. Product Classification

Product Model	PCB Antenna	External Antenna	LED
MKBN02A00	YES	NONE	YES
MKBN02A01	NONE	YES	NONE

3. Key Features

- 32 bits ARM® Cortextm-M4 @ 16MHz
- 2.4GHz multi-protocol transceiver
- 64KB SRAM
- 512KB Flash
- 30 configurable I/O pins, 22 General Purpose I/O pins（MKBN02A00）

- One 32 and two 16 bit timers with counter mode
- 20 channel CPU independent Programmable Peripheral Interconnect (PPI)
- Encryption -128 bit AES ECB/CCM/AAR co-processor
- RNG, RTC
- Temperature sensor
- Digital interfaces SPI Master/Slave, 2-wire Master (I2C compatible), UART (CTS/RTS),IIS,PDM
- Quadrature decoder
- 12bit 200KSPS ADC - 8 configurable channels
- Low power comparator
- -96dBm sensitivity
- Single-ended antenna
- NFC-A tag
- Tx Power -40 to +4 dBm in 8 dB steps
- 7.5mA TX at +4dBm
- Operating voltage : 1.8V to 3.6V
- Dimension :23x13.8x0.8mm

4. Applications

- Computer peripherals and I/O devices Mouse Keyboard Multi-touch trackpad
- Interactive entertainment devices Remote control 3D Glasses Gaming controller
- Personal Area Networks Health/fitness sensor and monitor devices Medical devices Key-fobs + wrist watches
- Remote control toys
- Beacons
- Bluetooth Gateway
- Indoor Location

5. Interfaces

5.1 Power Supply

Regulated power for the **MKBN02** is required. The input voltage VCC range should be 1.8V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2 System Function Interfaces

5.2.1 GPIOs

The general purpose I/O is organized as one port with up to 22 I/Os enabling access and control of up to 22 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

◆ Input/output direction

◆ Output drive strength

◆ Internal pull-up and pull-down resistors

◆ Wake-up from high or low level triggers on all pins

◆ Trigger interrupt on all pins

◆ All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

◆ All pins can be individually configured to carry serial interface or quadrature demodulator signals

◆ All pins can be configured as PWM signal

5.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps ,250kbps and 400 kbps. The module has 2 TWI ports and they properties like following table.

Instance	Master/Slave
TWI 0	Master
TWI 1	Master

5.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non- intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

5.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. Support the following baudrate in bps unit: 1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200. * Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configed independently.

5.2.6 Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit). * Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

MKBN02 Pin Number	Pin Number	Description
4	P0.28	Digital I/O; Analog input 4
5	P0.29	Digital I/O; Analog input 5
6	P0.30	Digital I/O; Analog input 6
7	P0.31	Digital I/O; Analog input 7
8	P0.02	Digital I/O; Analog input 0
11	P0.03	Digital I/O; Analog input 1
12	P0.04	Digital I/O; Analog input 2
13	P0.05	Digital I/O; Analog input 3

5.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8 Reset

The reset pin of the MKBN02 series module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be reserved .

5.2.9 NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum. Listed here are the main features for the NFC peripheral:

◆NFC-A listen mode operation

◆13.56 MHz input frequency

◆Bit rate 106 kbps

◆Wake-on-field low power field detection (SENSE) mode

◆Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum

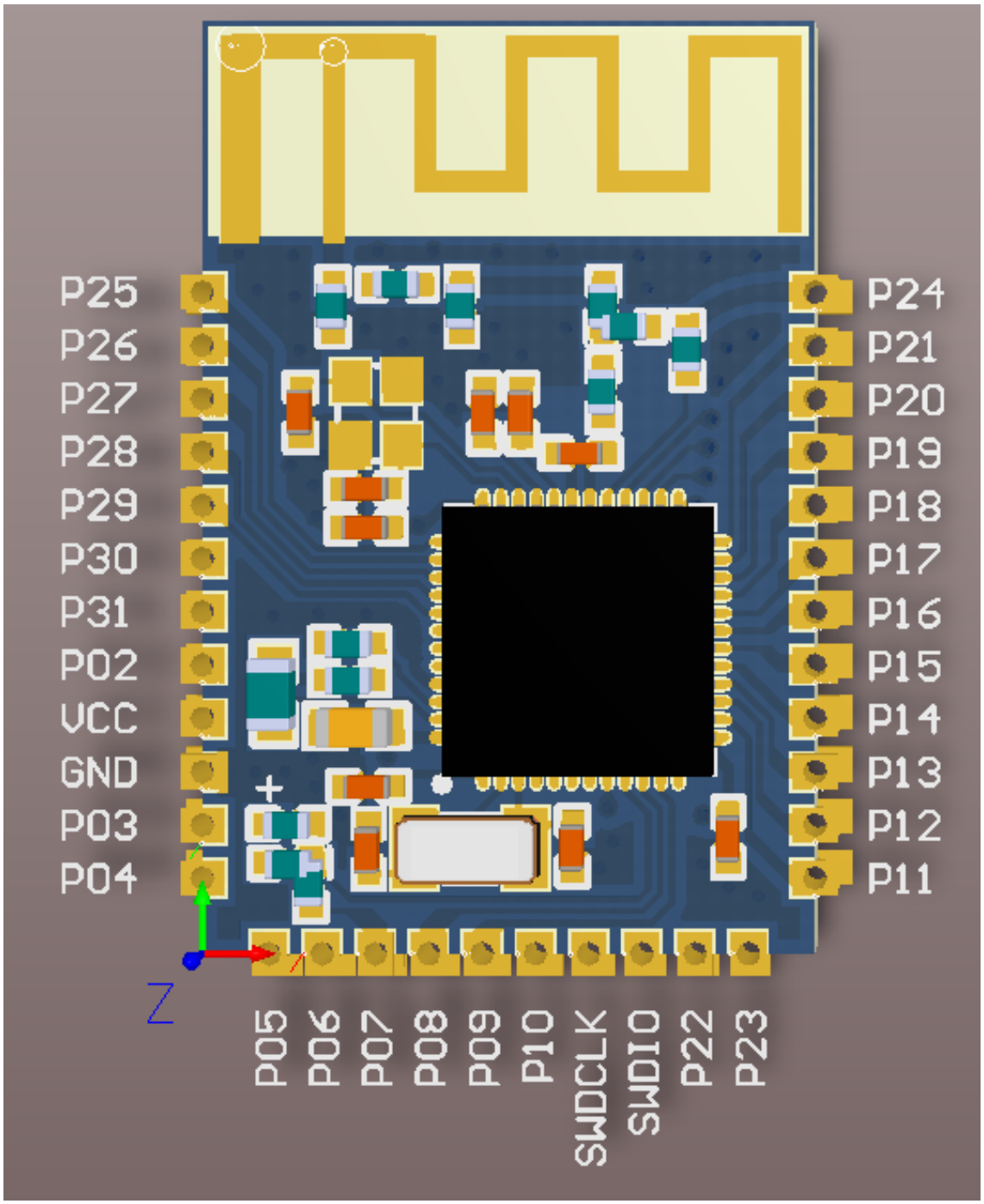
◆Programmable frame timing controller

◆Integrated automatic collision resolution, CRC and parity functions

MKBN04A00 Pin Number	Pin Number	Description
17	P0.09	Digital I/O; NFC1
18	P0.10	Digital I/O; NFC2

6. Module Pinout and Pin Description

6.1 Module Pinout



6.2 Pin Description

Pin NO.	Pin Name	Description	Remark
1	P0.25	General Purpose I/O	Digital I/O
2	P0.26	General Purpose I/O	Digital I/O
3	P0.27	General Purpose I/O	Digital I/O
4	P0.28	Digital I/O; Analog input 4	SAADC/COMP/LPCOMP input
5	P0.29	Digital I/O; Analog input 5	SAADC/COMP/LPCOMP input
6	P0.30	Digital I/O; Analog input 6	SAADC/COMP/LPCOMP input
7	P0.31	Digital I/O; Analog input 7	SAADC/COMP/LPCOMP input

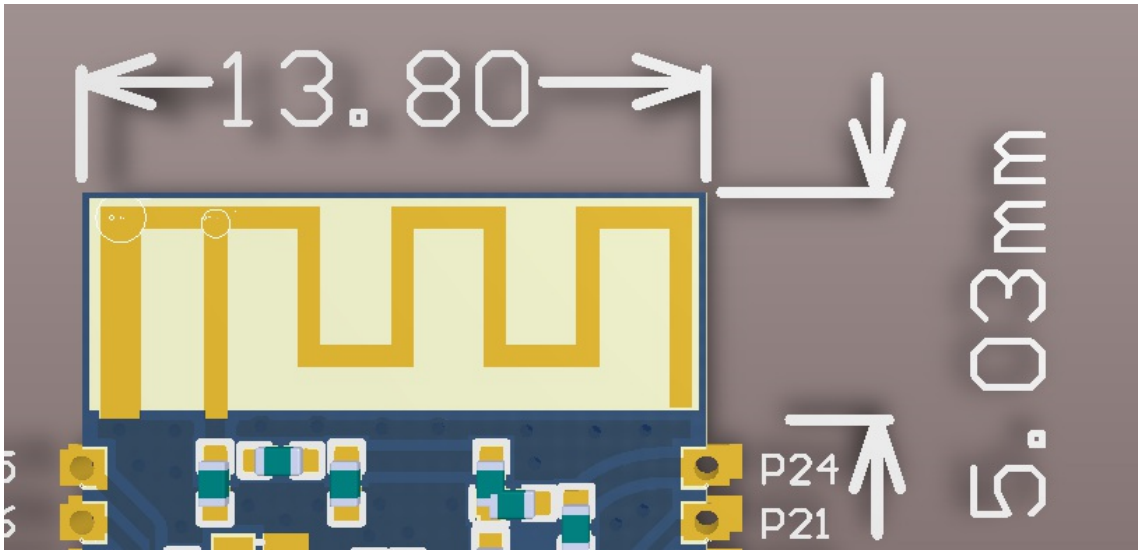
8	P0.02	Digital I/O; Analog input 0	SAADC/COMP/LPCOMP input
9	VCC	Power Supply	1.8V-3.6V
10	GND	Ground	-
11	P0.03	Digital I/O; Analog input 1	SAADC/COMP/LPCOMP input
12	P0.04	Digital I/O; Analog input 2	SAADC/COMP/LPCOMP input
13	P0.05	Digital I/O; Analog input 3	SAADC/COMP/LPCOMP input
14	P0.06	General Purpose I/O	Digital I/O
15	P0.07	General Purpose I/O	Digital I/O / LED
16	P0.08	General Purpose I/O	Digital I/O
17	P0.09/NFC1	General Purpose I/O; NFC1	Digital I/O
18	P0.10/NFC2	General Purpose I/O; NFC2	Digital I/O
19	SWDCLK	Digital input	Hardware Debug and Flash Program I/O
20	SWDIO	Digital I/O	Hardware Debug and Flash Program I/O
21	P0.22	General Purpose I/O	Digital I/O
22	P0.23	General Purpose I/O	Digital I/O
23	P0.11	General Purpose I/O	Digital I/O
24	P0.12	General Purpose I/O	Digital I/O
25	P0.13	General Purpose I/O	Digital I/O
26	P0.14	General Purpose I/O	Digital I/O
27	P0.15	General Purpose I/O	Digital I/O
28	P0.16	General Purpose I/O	Digital I/O
29	P0.17	General Purpose I/O	Digital I/O
30	P0.18	General Purpose I/O	Digital I/O
31	P0.19	General Purpose I/O	Digital I/O
32	P0.20	General Purpose I/O	Digital I/O
33	P0.21/RESET	General Purpose I/O; nRESET	Digital I/O
34	P0.24	General Purpose I/O	Digital I/O External antenna（MKBN02A01）

REMARK:

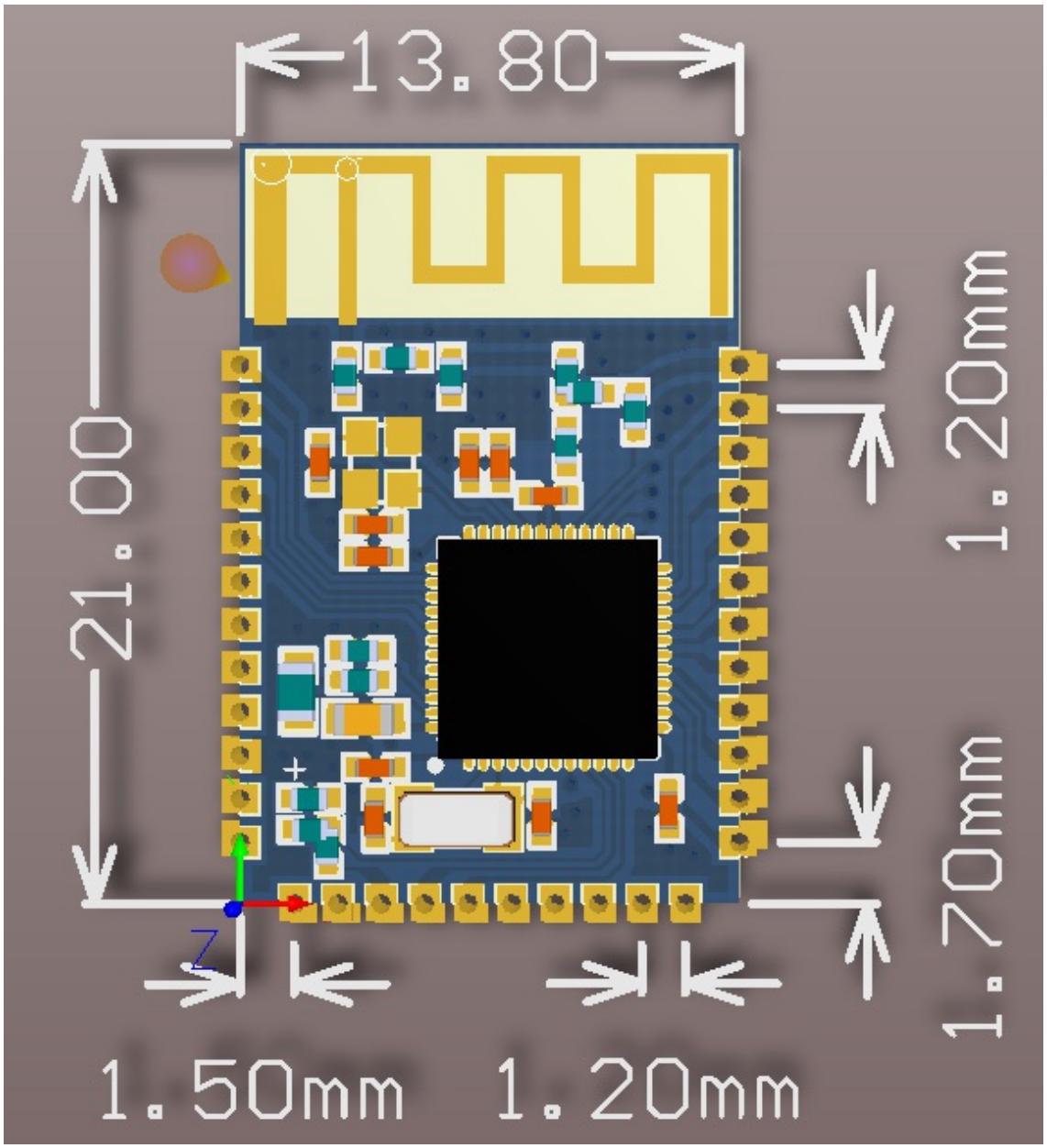
1. P07 is for LED. The user can request to remove the LED and use P07 as General Purpose I/O;
2. User can choose P24 to lead external antenna. If P24 is used to lead external antenna, the PCB antenna will not work and P24 can not be used as General Purpose I/O. The module with external antennal is named MKBN02A01. User needs to select the appropriate external antenna to match the module.

7. PCB Design Guide（MKBN02A00）

Please reserve empty area for PCB antenna when you are going to design a device's board, the empty range minimum size : 13.8×5.03mm , please kindly check the picture below for reference.



8. PCB Footprint and Dimensions


13.80
21.00
1.20mm
1.70mm
1.50mm
1.20mm

9. Host Information

The host will Satisfy Class I or Class Ⅱ permissive change based this module FCC ID. The host will be electronic product that uses the BLE function of the MKBN02 series module.

10. FCC Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits aredesigned to provide reasonable protection against harmful interference in aresidential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. If the FCC identification number is not visible when the module is installed inside the host, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains Transmitter Module Contains FCC ID:2AO94-MKBN02” or “Contains FCC ID: 2AO94-MKBN02 Any similar wording that expresses the same meaning may be used. RF warning statement: The device has been evaluated to meet general RF exposure requirement. The device can be used

in public exposure condition without restriction.

FCC RF warning statement:

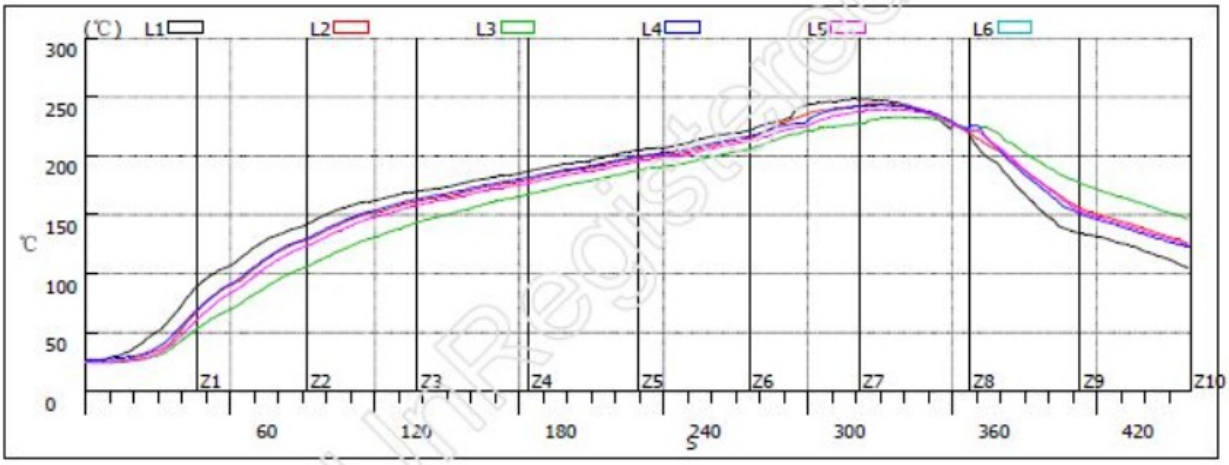
The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction.

11. Information for Manufacture

PROFILE CHECK

Date Time: 2018/11/1 12:51:23
Customer Name: 华创恒达科技有限公司
PCB Name: MKBN02 FR4
Oven Type: B线
Speed: 75cm/min
Zones setting (℃)

Zones	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Top	130	155	165	175	180	190	200	230	260	250	0	0	0	0
Bottom	130	155	165	175	180	190	200	230	260	250	0	0	0	0



TCS	Peak(℃)	Peak difference	Peak At Time(S)	190(℃)Time above	Preheat 50-150 Time	Preheat 50-150 Slope	Soak 150-200 Time	Soak 150-200 Slope	Reflow 220-255 Time	Reflow 220-255 Slope	Liquid phase (220)time	Cooling 255-170 Time	Cooling 255-170 Slope
line1	248.5	15.25	324	190	1.41	71	0.43	116	0.67	52	93	115	-1.17
line2	244		331	177	1.30	77	0.42	118	0.70	50	85	128	-1.05
line3	233.25		336	164	0.93	107	0.45	112	0.90	39	81	123	-1.10
line4	243.5		330	181	1.30	77	0.43	117	0.71	49	91	129	-1.05
line5	240.25		334	172	1.19	84	0.41	121	0.73	48	84	125	-1.08

Operation Name: 李文茜 Confirmor: 陆克明 Checker: 别勇刚

Temperature analysis report

12. Declaration

The contents of this datasheet are subject to change without prior notice for further improvement. MOKO team reserves all the rights for the final explanation. Please contact MOKO sales team or visit http://www.mokosmart.com to get more related information if needed.

Contact Information

MOKO TECHNOLOGY LTD. Address : 4F,Buidling2, Guanghui Technology Park, MinQing Rd, Longhua, Shenzhen, Guangdong, China
Telephone : 86-75523573370 Fax : 86-75523573370-808
Website : http://www.mokosmart.com

Revision History

Revision	Description of changes	Approved	Revision Date
V1.0	Initial Release	Kevin	2018.06
V1.1	Added product classification	Kevin	2018.07.18