

PCB MARK & LABEL

Heat Sink	
Optical Marks	T1 MARK T2 MARK T3 MARK T4 MARK T5 MARK T6 MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK
Label Outline	SN&MAC ☐ H1 20mm X 10mm Lot Number ☐ H2 10mm X 10mm
Silkscreen	PCB Name & Version EL03399 (E679524) (USB-C) ☐ ENG Version A20xxx ☐ A20xxx
Mounting Hole	只保留7个螺丝固定孔 H5~H12: 螺丝固定孔; H13~H15: 板卡定位柱固定孔, 2.4mm直径的NPTN过孔 H16: 板卡定位柱固定孔, 11mm直径的NPTN过孔

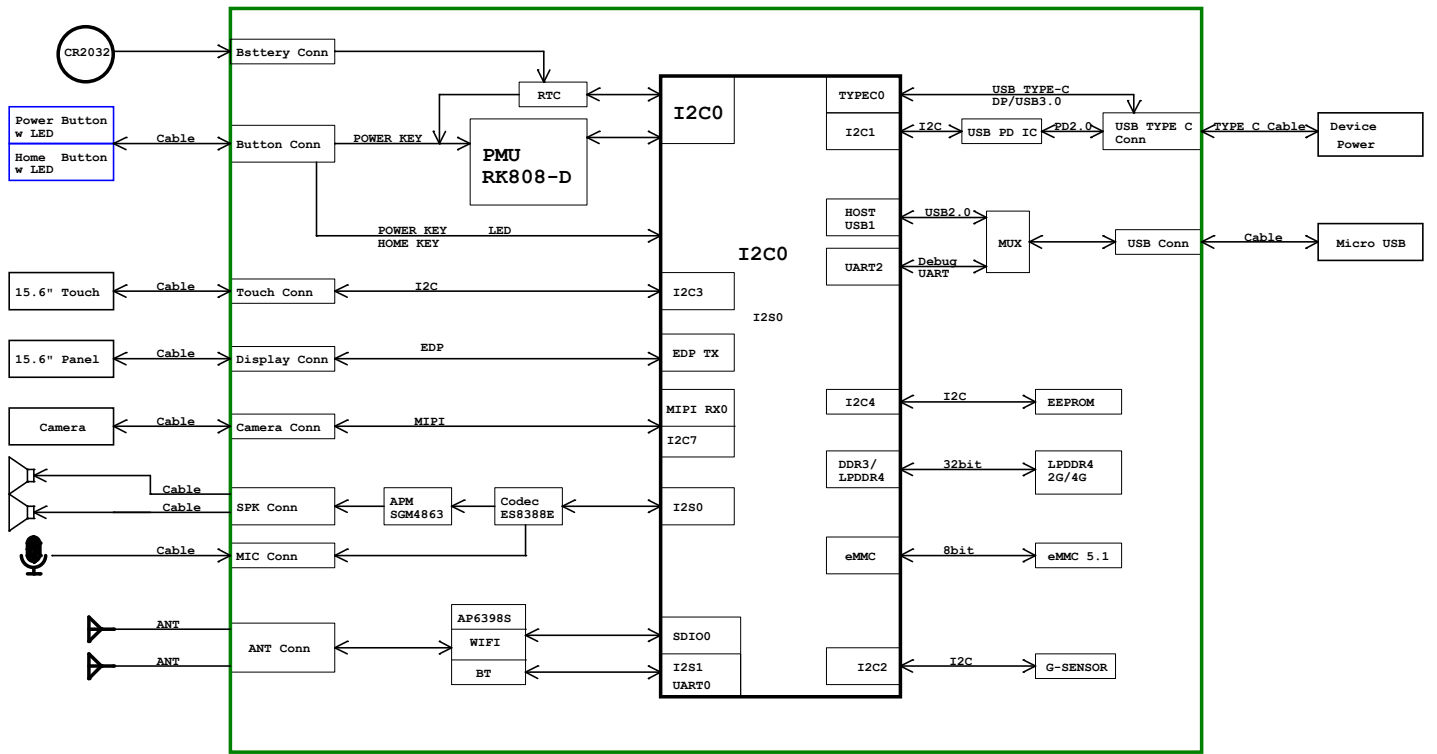
SIGNWAY			
Project:	E679524		
File:	01.Msc		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhanghui	Sheet:	1 of 32

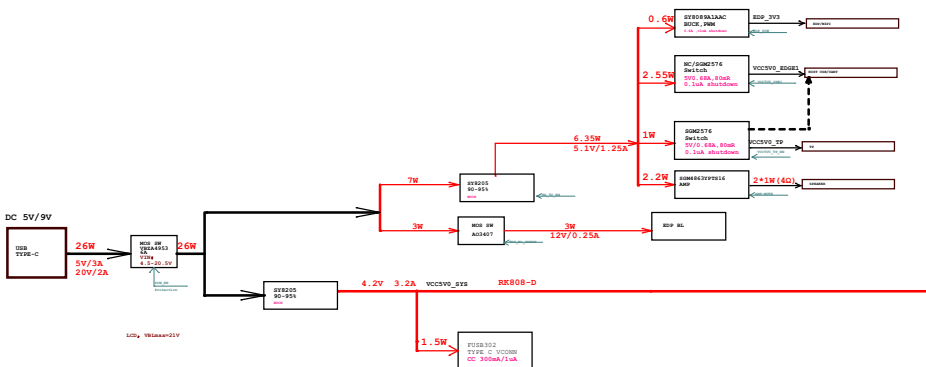
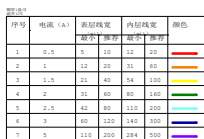
Change List

Version	Date	Author	Change Note	Approved
V0.5	August 02, 2020	ZHangliubin	First edition.	ZHangbo
V1.0	August 20, 2020	ZHangliubin	Adjust the power scheme.	ZHangbo
V1.1	August 27, 2020	ZHangliubin	Adjust the Panle power supply U35	ZHangbo
V1.2	September 2, 2020	ZHangliubin	Modify the Block Diagram	ZHangbo



Project: E679524			
File:		02.Change List	
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangliubin	Sheet:	2 of 32



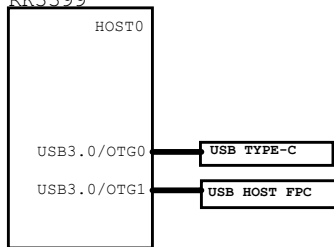


I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GP101_B7/SP13_RXD/I2C0_SDA GP101_C0/SP13_TXD/I2C0_SCL	PMU102	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SY8377FNC	0x40	DC-DC Buck	100kHz,400KHz,3.4MHz
					SY8388FNC	0x41	DC-DC Buck	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GP104_A1/I2C1_SDA GP104_A2/I2C1_SCL	API05	I2C1_SDA_V18 I2C1_SCL_V18	VCC_V18	ES8388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB302MFX/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
								100kHz
I2C2	GP102_A0/VOP_D0/CI/F_D0/I2C2_SDA GP102_A1/VOP_D1/CI/F_D1/I2C2_SCL	API02	I2C2_SDA_V18 I2C2_SCL_V18	VCC_V18	MMA8452Q/1.8V	0x1d,0x1e	G-SENSOR	100kHz,400KHz,
I2C3	GP104_C0/I2C3_SDA/UART2B_RX GP104_C1/I2C3_SCL/UART2B_TX	API04	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TD0	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GP101_B3/I2C4_SDA GP101_B4/I2C4_SCL	PMU102	I2C4_SDA I2C4_SCL	VCC_3V0	SM201/3.0V	0xa0 0xe0	EEPROM	10kHz
I2C5	GP103_B2/MAC_RXRX/I2C5_SDA GP103_B3/MAC_CLK/I2C5_SCL	API01	MAC USB					
I2C6	GP102_B1/SP12_RXD/CI/F_HREF/I2C6_SDA GP102_B2/SP12_TXD/CI/F_CLKIN/I2C6_SCL	API02	I2C6_SDA_V18 I2C6_SCL_V18	VCC_V18				20kHz
I2C7	GP102_A7/VOP_D7/CI/F_D7/I2C7_SDA GP102_B0/VOP_CLK/CI/F_VSYNC/I2C7_SCL	API02	I2C7_SDA_V18 I2C7_SCL_V18	VCC_V18	MIP1_CSI /1.8V			100kHz

USB MAP

RK3399

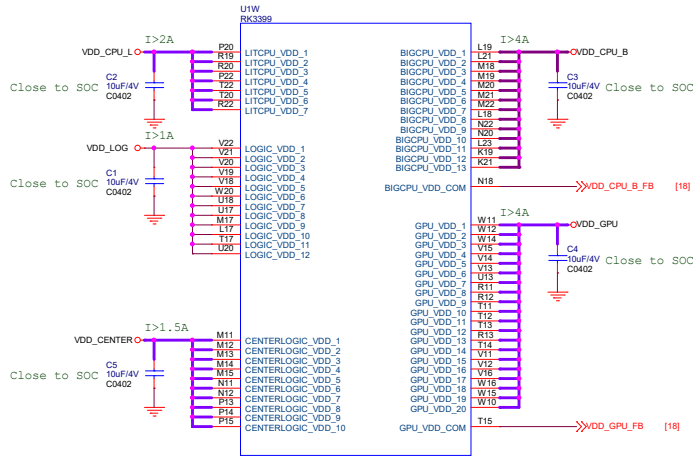


SIGNWAY			
Project: ES79534			
File: 05I2C&USB Map			
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangshun	Sheet:	5 of 32

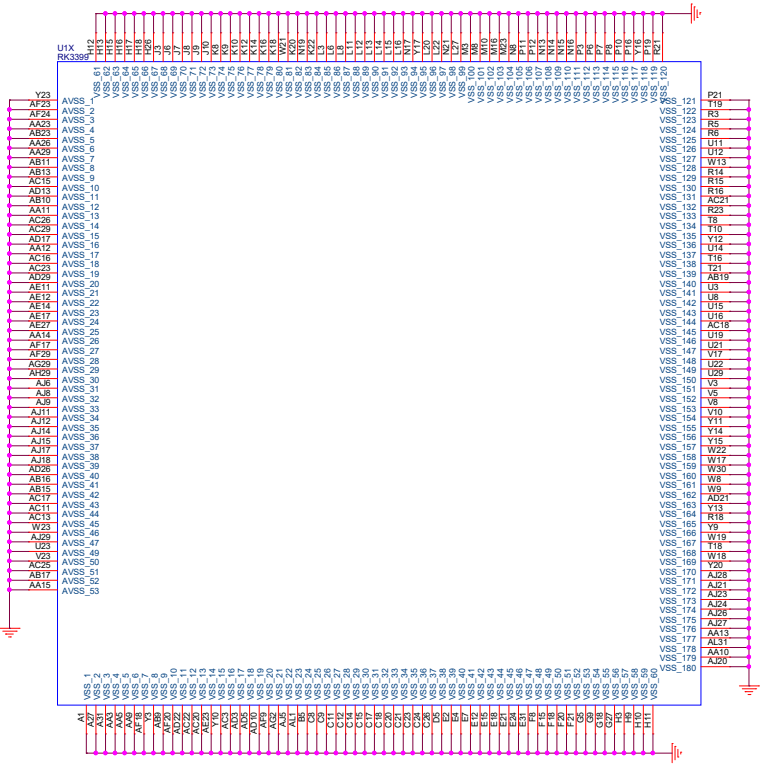
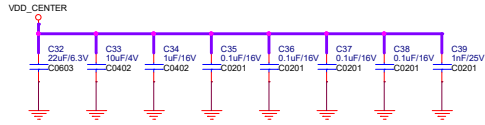
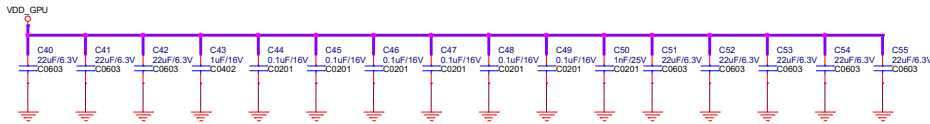
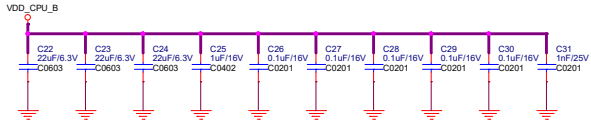
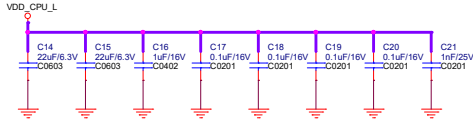
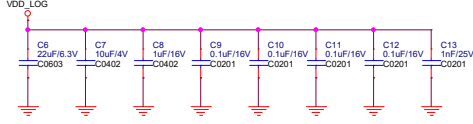
Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUI01	pmui01_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLD03
Part E	PMUI02/PART E	pmui830_gpiolabcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLD06
Part I	API01	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	API02	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLD03
Part G	API03	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	API04	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLD06 RK808-D VLD08
Part J	API05/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLD01
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLD04

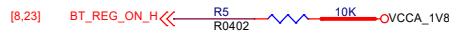
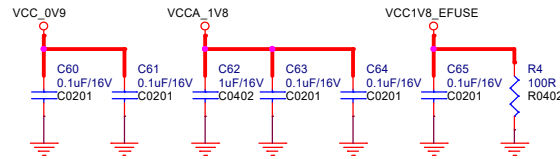
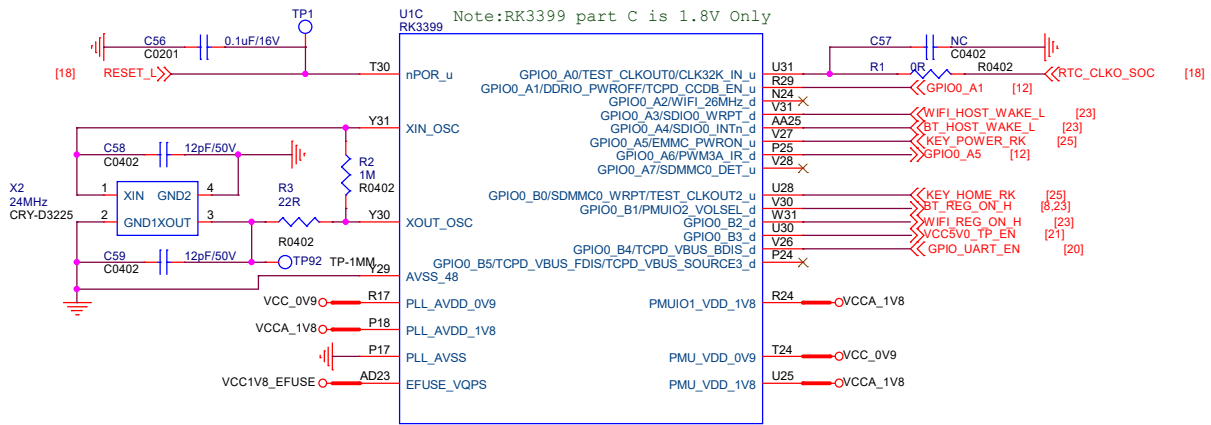
			
Project:	E679524		
File:	06.Power Domain Map		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhanglilin	Sheet:	6 of 32



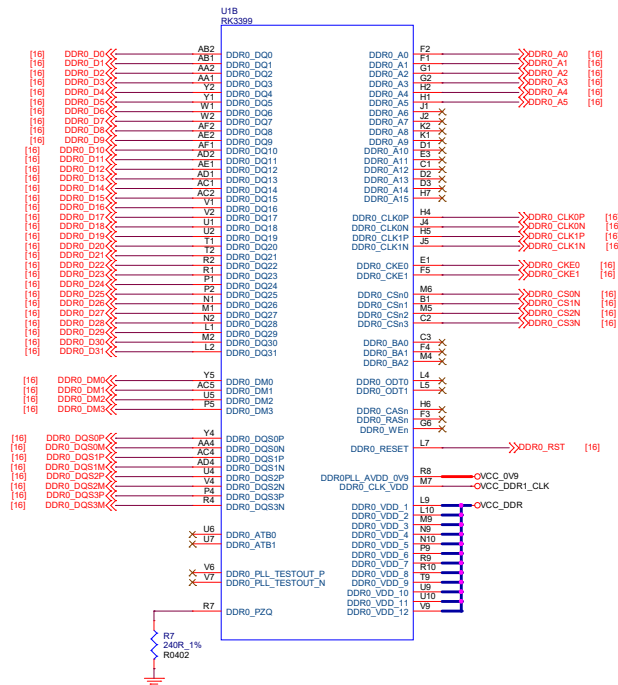
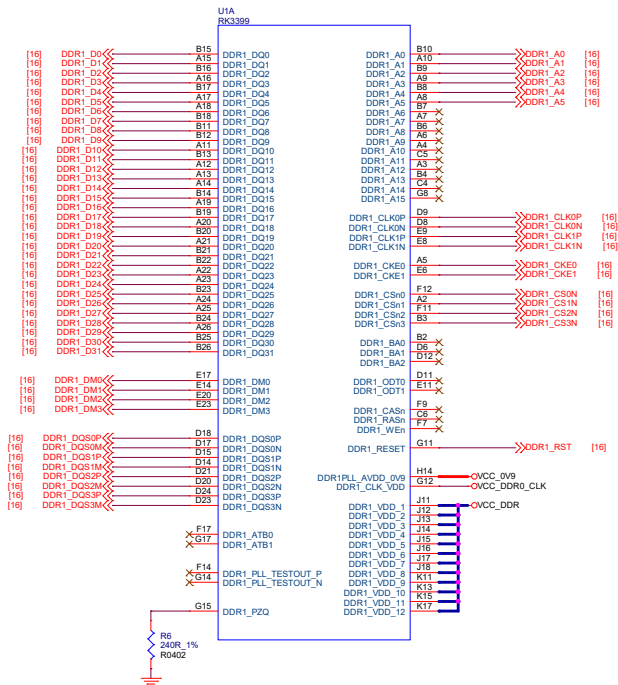
Note: Power filter CAP please place back of SOC or close to SOC



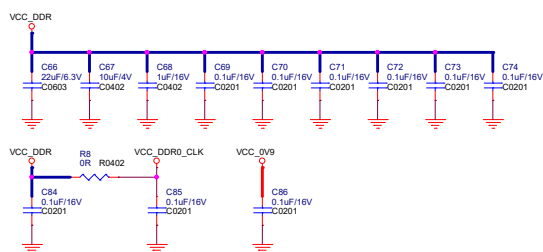
SIGNWAY			
Project: E879534			
File: 07 RK3399 Power			
Date: Monday, December 20, 2021	Rev: A0		
Designed by: Zhongbin	Sheet: 7	of 32	



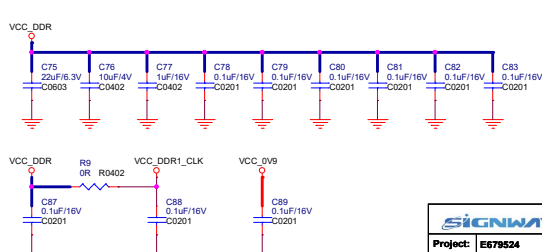
SIGNWAY			
Project:	E679524		
File:	08.RK3399 PMU Controller		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangliubin	Sheet:	8 of 32



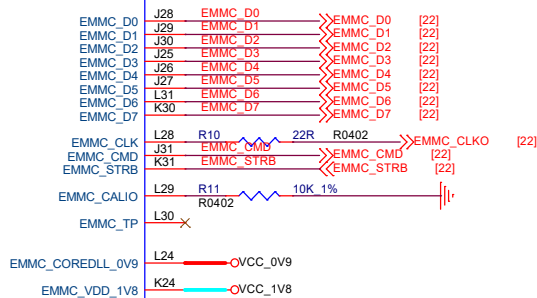
DDR FILTER Note:R10 cannot be deleted



DDR FILTER Note:R11 cannot be deleted

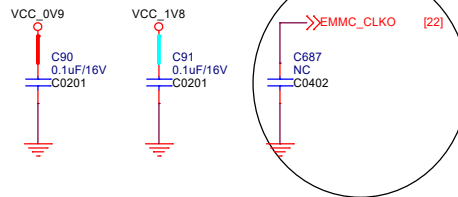


U1H
RK3399

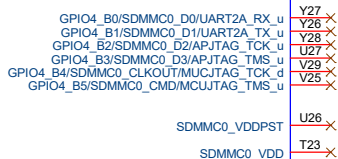


EMMC design rule:

- 1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;
- 6.R11 close to SOC;



U1F
RK3399

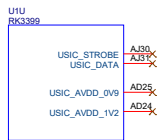


SDMMC design rule:

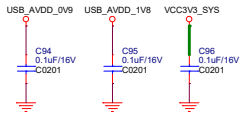
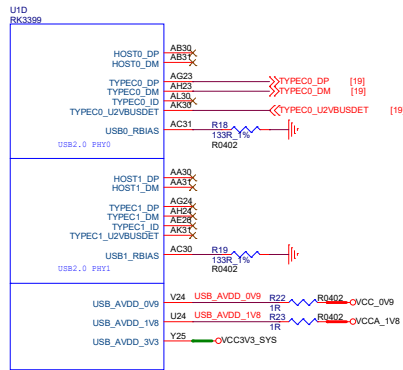
- 1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

SIGNWAY

Project:	E679524		
File:	10.RK3399 Flash&SDMMC Controler		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangliubin	Sheet:	10 of 32



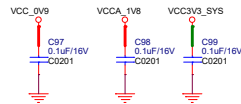
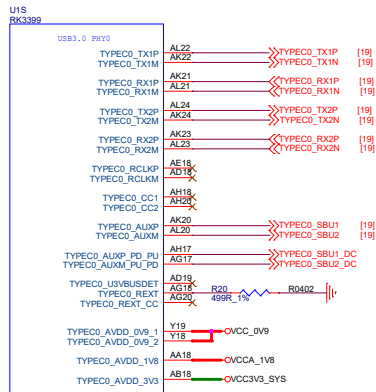
USB2.0



USB2.0 design rule:

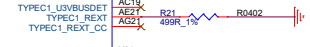
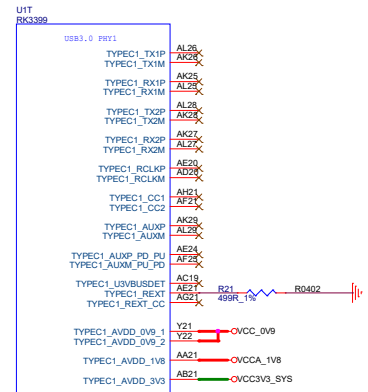
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

USB3.0



USB3.0 design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between TX and RX < 1.6 ns;
- 3.Max trace length < 6 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 90ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;



DP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E879534		
File:	11.RK3399 USB/USBC Controller		
Date:	Monday, December 28, 2021	Rev:	A0
Designed by:	Zhangshubin	Sheet:	11 of 32

U1V
RK3399

ADC_IN0
ADC_IN1
ADC_IN2
ADC_IN3
ADC_IN4

AG28
AH28
AG25
AG28
AH27

ADC_AVDD

AC24

VCCA_1V8

C100

0.1uF/16V

C0201

C404

1nF/25V

C0402

PD_VBUS_TYPEC0_ADC [19]

布线较长，预留电容，防止电压波动，
影响ADC检测的稳定性；
靠近cpu引脚放置
20200804

HW Version

VCCA_1V8

R357

NC

R0402

TP63

TP-1MM

HW_VER2

GPIO0_A5 [8]

R307

10K

R0402

VCCA_1V8

R308

NC

R0402

TP68

TP-1MM

HW_VER1

GPIO3_D6 [8]

R309

10K

R0402

VCCA_1V8

R311

10K

R0402

TP10

TP-1MM

HW_VER0

GPIO2_D4 [15]

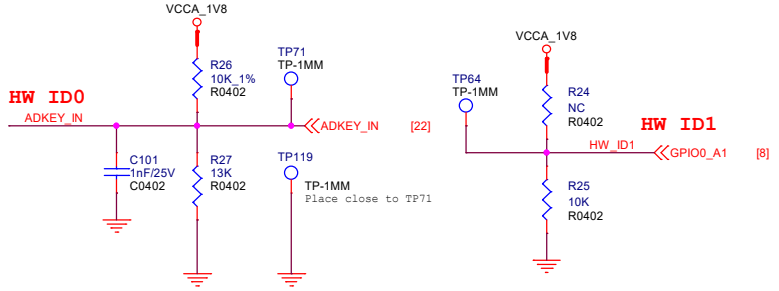
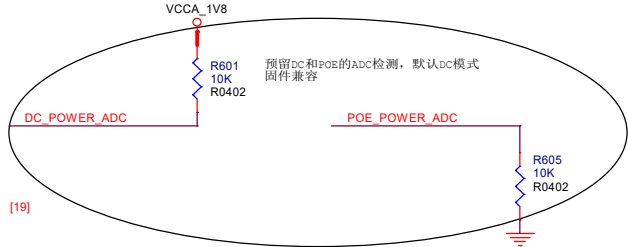
R310

NC

R0402

E472673 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1 (EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	TBD
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD



RK3399 project hardware ID definiton

ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
ADC1 Function2: Secondary definiton of product hardware ID.
GPIO0_A1: Main definiton of of product hardware ID.

Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673(15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828(21.5)	
03.	Low	39K	1.433V	E473060(10.1)	
04.	Low	22K	1.238V	E473261 (BACKPACK)	
05.	Low	13K	1.017V	E679524(USB-C)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

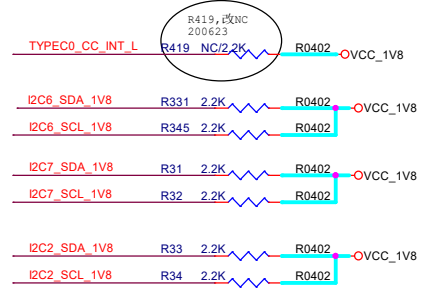
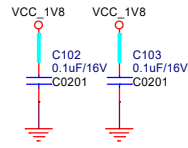
SiGNWAY

Project:	E679524		
File:	12.RK3399 SARADC/Key		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangliubin	Sheet:	12 of 32

U1L
RK3399

GPI02_A0/VOP_D0/CIF_D0/I2C2_SDA_u G31 << I2C2_SDA_1V8 [29]
GPI02_A1/VOP_D1/CIF_D1/I2C2_SCL_u H25 << I2C2_SCL_1V8 [29]
GPI02_A2/VOP_D2/CIF_D2_d F30 >> DVP_PWR [30]
GPI02_A3/VOP_D3/CIF_D3_d F28 >> Camera_RST_L [30]
GPI02_A4/VOP_D4/CIF_D4_d H29 X
GPI02_A5/VOP_D5/CIF_D5_d F29 X << TYPEC0_CC_INT_L [19]
GPI02_A6/VOP_D6/CIF_D6_d H27 X
GPI02_A7/VOP_D7/CIF_D7/I2C7_SDA_u G30 X << I2C7_SDA_1V8 [30]
GPI02_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL_u H28 << I2C7_SCL_1V8 [30]
GPI02_B1/SPI2_RXD/CIF_HREF/I2C6_SDA_u F30 << I2C6_SDA_1V8 [30]
GPI02_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL_u H24 << I2C6_SCL_1V8 [30]
GPI02_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA_u H31 << CIF_CLKO [30]
GPI02_B4/SPI2_CSn0_u F31 >> DVP_PDN0_H [30]

APIO2_VDDPST J24 << VCC_1V8
APIO2_VDD K23 << VCC_1V8



U1R
RK3399

MIPI_RX0_D0P AK15 << MIPI_RX0_D0P [30]
MIPI_RX0_D0N AL15 << MIPI_RX0_D0N [30]
MIPI_RX0_D1P AK14 << MIPI_RX0_D1P [30]
MIPI_RX0_D1N AL14 << MIPI_RX0_D1N [30]
MIPI_RX0_CLKP AK13 << MIPI_RX0_CLKP [30]
MIPI_RX0_CLKN AL13 << MIPI_RX0_CLKN [30]
MIPI_RX0_D2P AK12 X
MIPI_RX0_D2N AL12 X
MIPI_RX0_D3P AK11 X
MIPI_RX0_D3N AL11 X
MIPI_RX0_REXT AF14 R35 4.02K 1% R0402
MIPI_RX0_AVDD_1V8 AB14 << OVCCA1V8_HDMI



U1P
RK3399

MIPI_TX1/RX1_D0P AK6 X
MIPI_TX1/RX1_D0N AL6 X
MIPI_TX1/RX1_D1P AK7 X
MIPI_TX1/RX1_D1N AL7 X
MIPI_TX1/RX1_CLKP AK8 X
MIPI_TX1/RX1_CLKN AL8 X
MIPI_TX1/RX1_D2P AK9 X
MIPI_TX1/RX1_D2N AL9 X
MIPI_TX1/RX1_D3P AK10 X
MIPI_TX1/RX1_D3N AL10 X
MIPI_TX1/RX1_REXT AF11 X
MIPI_TX1/RX1_AVDD_1V8 AC10 X

SIGNWAY

Project: E679524

File: 13.RK3399 DVP Interface

Date: Monday, December 20, 2021

Rev: A0

Designed by: Zhangliubin

Sheet: 13 of 32

U1N
RK3399

HDMI_TX0P AK17
HDMI_TX0N AL17
HDMI_TX1P AK18
HDMI_TX1N AL18
HDMI_TX2P AK19
HDMI_TX2N AL19
HDMI_T0P AK16
HDMI_T0N AL16
HDMI_HP0 AE15
HDMI_REXT AF15

HDMI_AVDD_0V9_1 AA16
HDMI_AVDD_0V9_2 AA17
HDMI_AVDD_1V8 AD16

HDMI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

U1Q
RK3399

MIPI_TX0_D0P AG15
MIPI_TX0_D0N AH15
MIPI_TX0_D1P AG14
MIPI_TX0_D1N AH14
MIPI_TX0_CLKP AG12
MIPI_TX0_CLKN AH12
MIPI_TX0_D2P AG11
MIPI_TX0_D2N AH11
MIPI_TX0_D3P AG9
MIPI_TX0_D3N AH9
MIPI_TX0_REXT AF12
MIPI_TX0_AVDD_1V8 AB12

U1M
RK3399

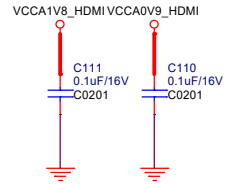
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EDP_TX0N A29 C107 0.1uF/16V C0201 EDP_TX0N [28]
EDP_TX1P B30 C108 0.1uF/16V C0201 EDP_TX1P [28]
EDP_TX1N A30 C109 0.1uF/16V C0201 EDP_TX1N [28]
EDP_TX2P C30
EDP_TX2N C31
EDP_TX3P D30
EDP_TX3N D31
EDP_AUXP B28 EDP_AUXP [28]
EDP_AUXN A28 EDP_AUXN [28]
EDP_DC_TP G20
EDP_CLK24M_IN H21
EDP_REXT G21 R37 6.04K 1% R0402
EDP_AVDD_0V9 H20 EDP_AVDD_0V9 VCCA0V9_HDMI
EDP_AVDD_1V8_1 J19 EDP_AVDD_1V8 VCCA1V8_HDMI
EDP_AVDD_1V8_2 J20 EDP_AVDD_1V8 VCCA1V8_HDMI
EDP_AVSS_1 B31
EDP_AVSS_2 C28
EDP_AVSS_3 C29
EDP_AVSS_4 D29
EDP_AVSS_5 H19
EDP_AVSS_6 J21

eDP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

MIPI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;



SIGNWAY

Project: E679524

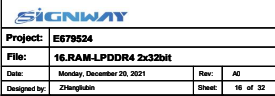
File: 14.RK3399 Display Interface

Date: Monday, December 20, 2021

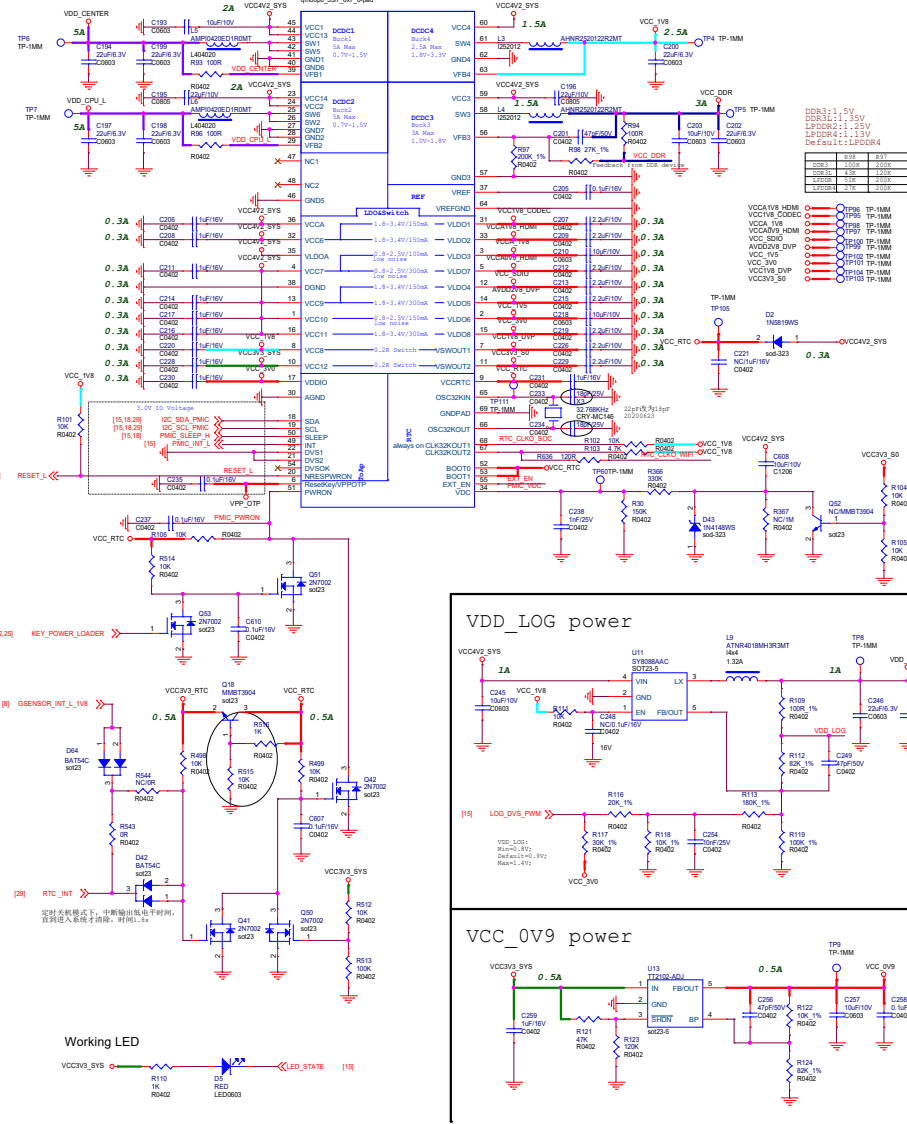
Rev: A0

Designed by: ZHANGJUN

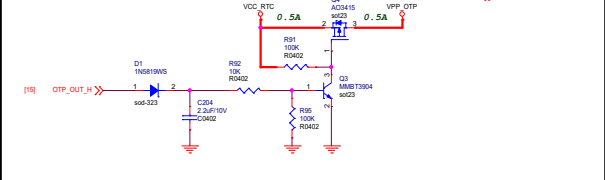
Sheet: 14 of 32



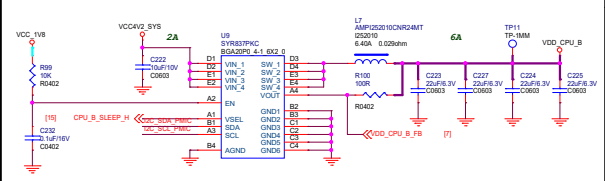
PMIC



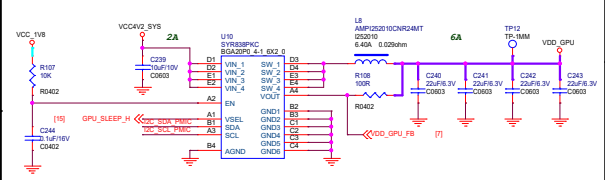
Over-temperature
Protection



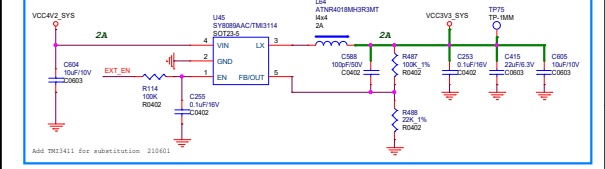
VDD_CPU_B power



VDD_GPU power

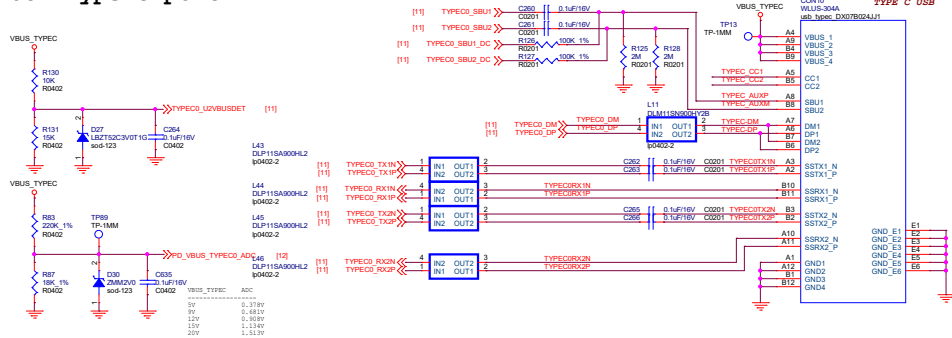


VCC3V3_SYS power

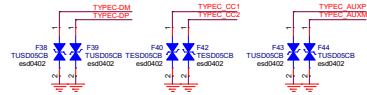
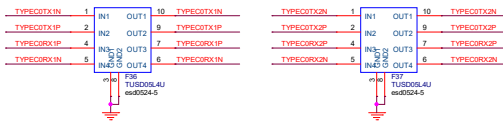
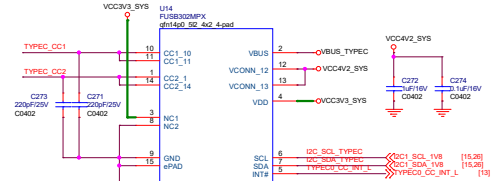


序号	电流 (A) 留焊区可 最小10%	表层线宽		内层线宽		颜色
		最小 (mil)	推荐 (mil)	最小 (mil)	推荐 (mil)	
1	0.5	5	10	12	20	
2	1	12	20	31	60	
3	1.5	21	40	54	100	
4	2	31	60	80	160	
5	2.5	42	80	110	200	
6	3	60	120	140	300	
7	5	110	200	284	500	

SD

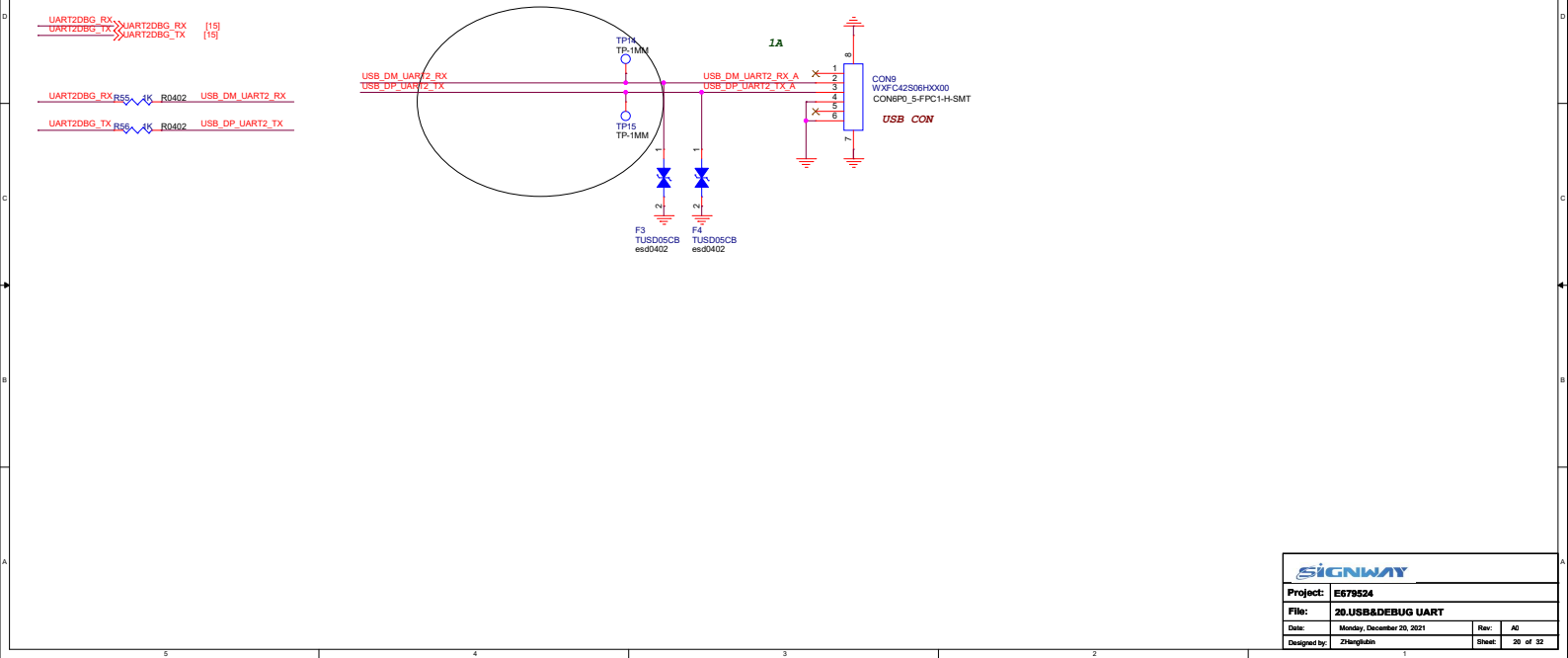


CC CTRL

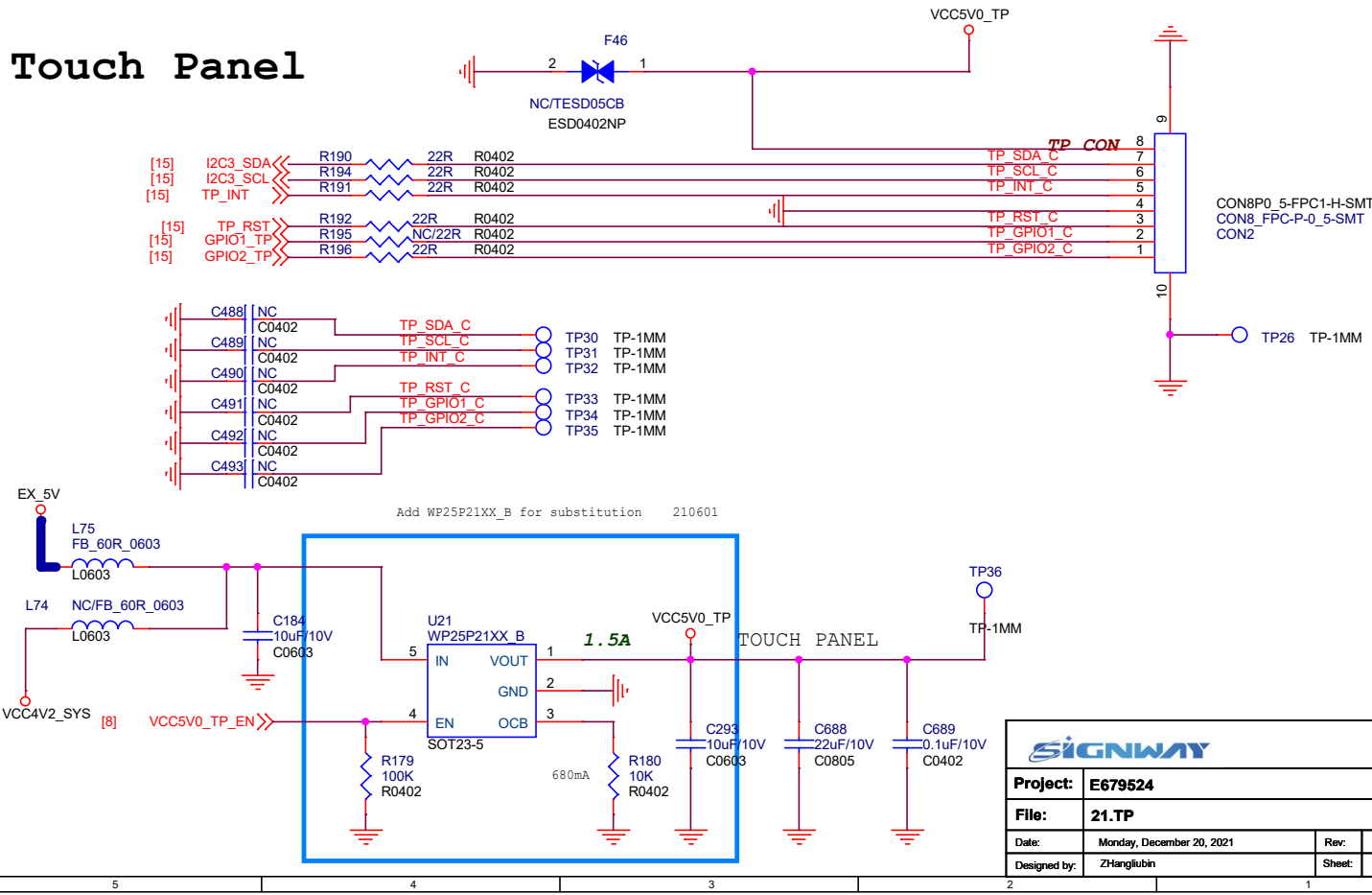


			
Project:	E679524		
File:	19.TYPE-C		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhangbin	Sheet:	19 of 32

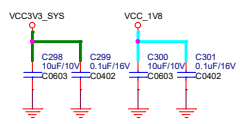
OTG USB & DEBUG UART



Touch Panel

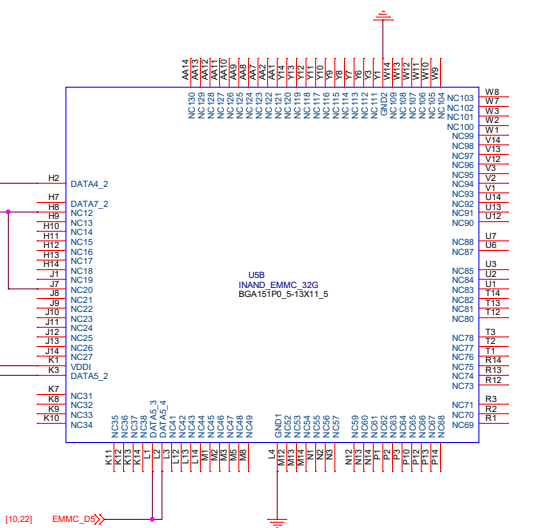
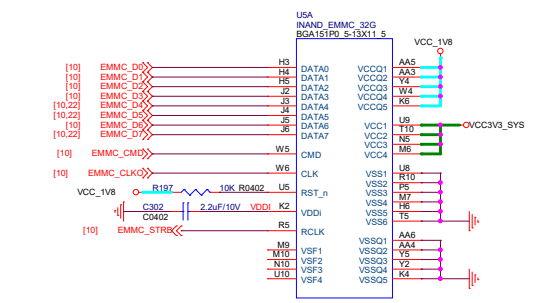
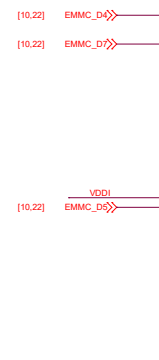
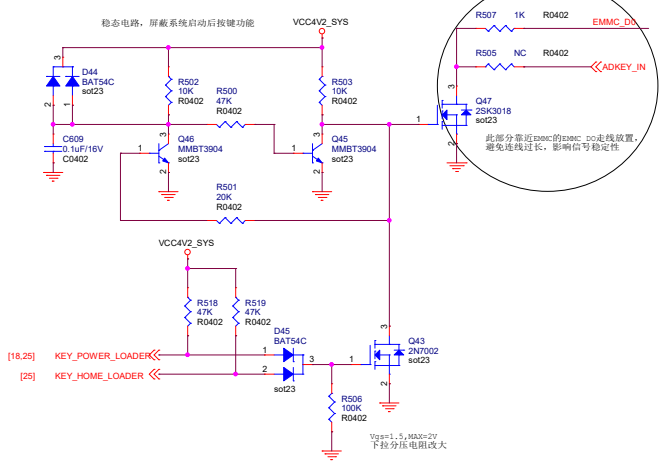


eMMC FLASH



Note: All the Power filter capacitors should be placed close to the power pins of eMMC

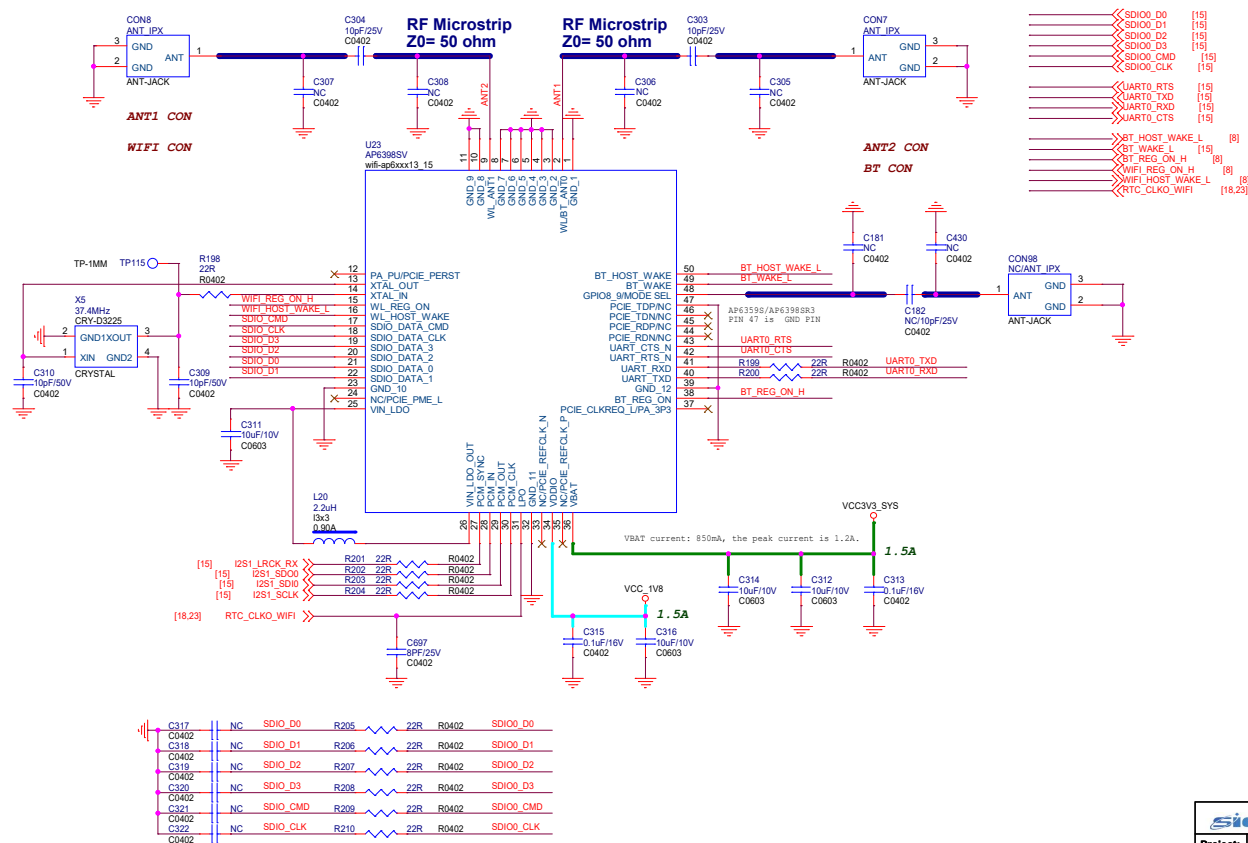
Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=UV at power-on reset,
then system will enter into Maskrom mode.



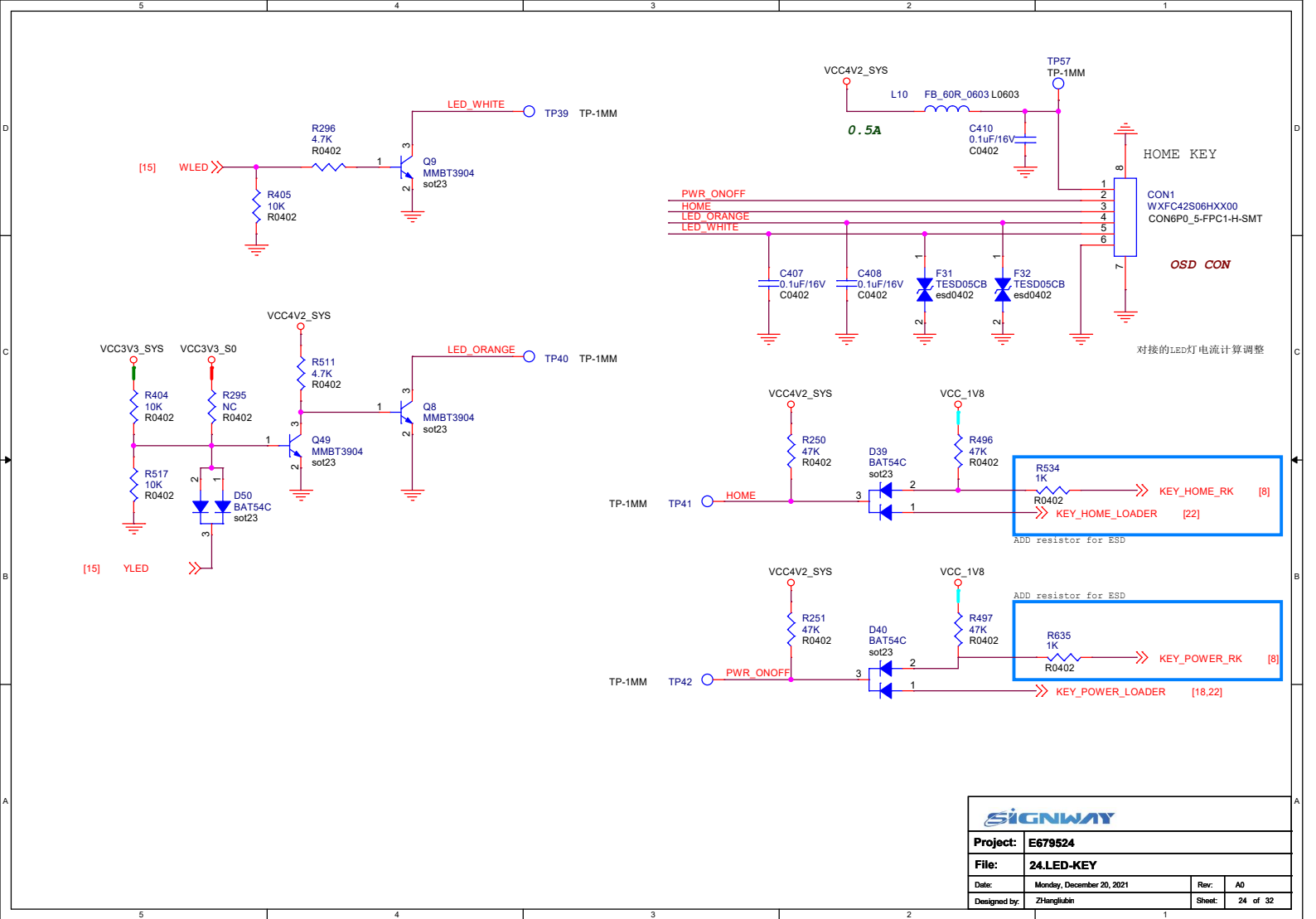
SIGNWAY			
Project: ES79534			
File: 22.Memory-eMMC			
Date: Monday, December 20, 2021	Rev: A0		
Designed by: Zhongshun	Sheet: 22 of 32		

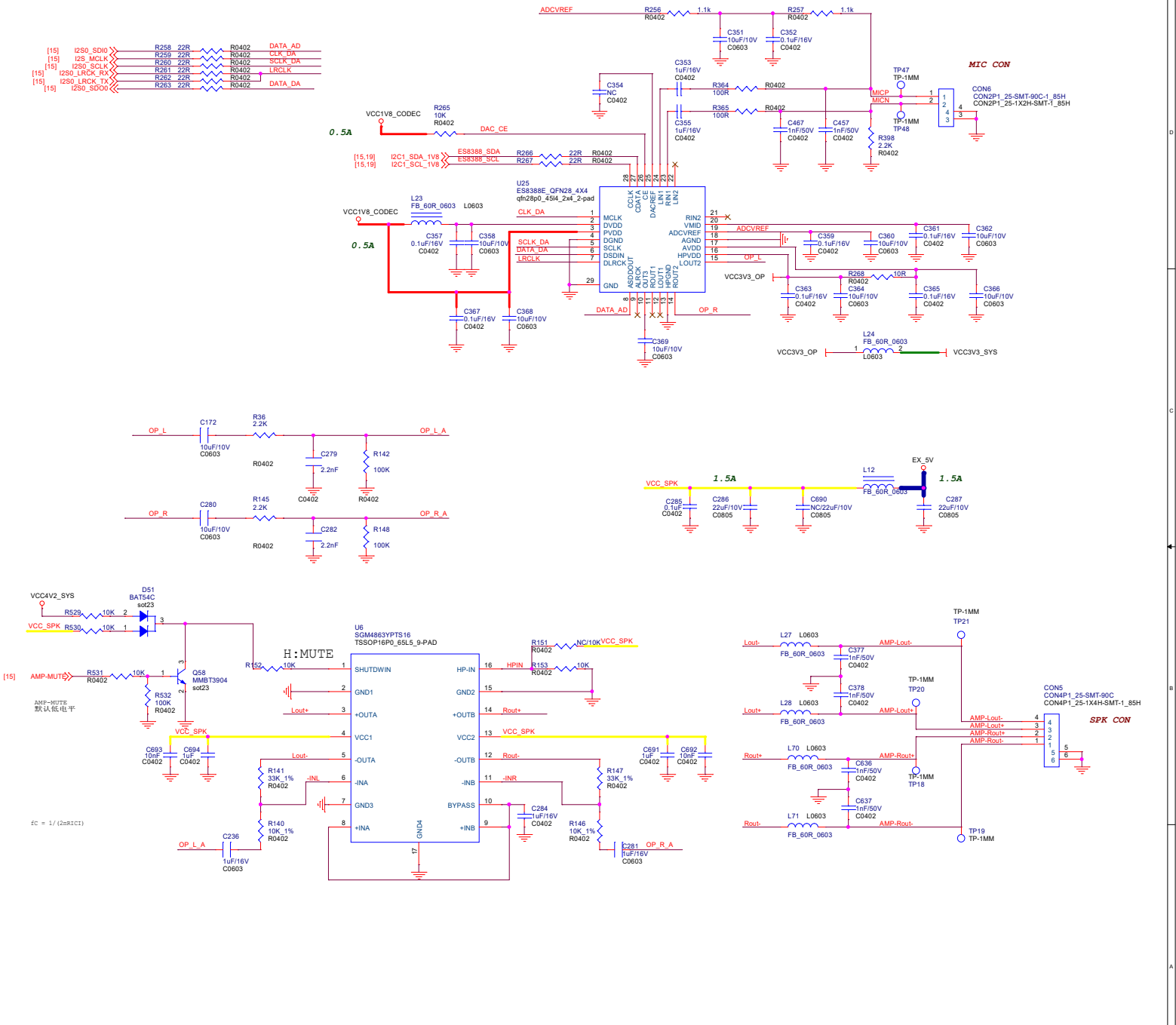
SDIO WIFI/BT MODULE-MIMO

Note:VBAT power supply range is 3.0V~4.8V.

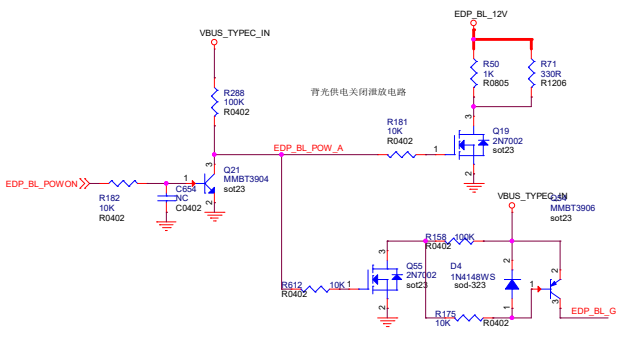
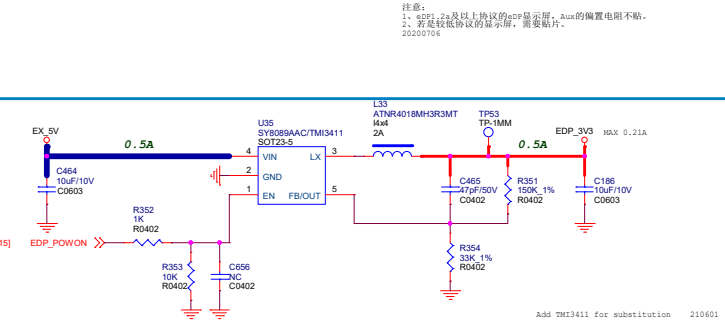
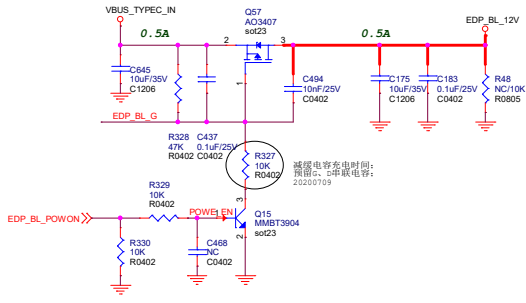
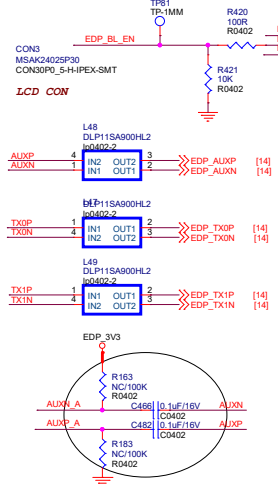
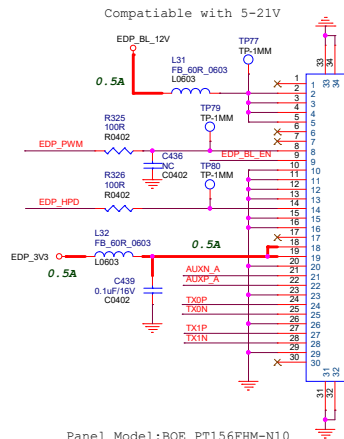


SIGNWAY			
Project: E679524			
File: 23.WIFI/BT-AP6398SV			
Date: Monday, December 20, 2021	Rev: A0		
Designed by: Zhenghubin	Sheet: 29 of 32		





SIGNWAY			
Project: E678524			
File: 25.E68388/OP			
Date: Monday, December 20, 2021	Rev: A0	Sheet: 25 of 32	
Designed by: Zhenqiang			



SIGNWAY			
Project: E679524			
File: 26.Edp Display			
Date: Monday, December 20, 2021	Rev: A0		
Designed by: Zhenqun	Sheet: 26 of 32		

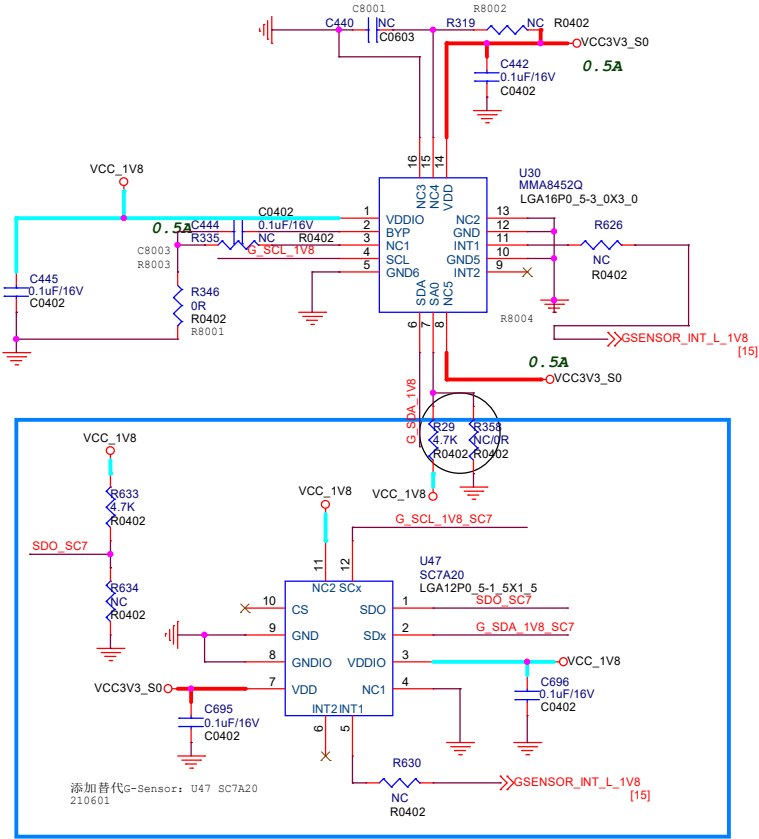
SY8089AAC的最小压降??

注意:
1、eDP1.2及以上协议的eDP显示屏，Aux的偏置电阻不贴。
2、若是较低协议的显示屏，需要贴片。
20200706

Add TH13411 for substitution 210601

	LIS3DH	MMA8452Q	ISM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	0R
R8004	NC	NC	0R

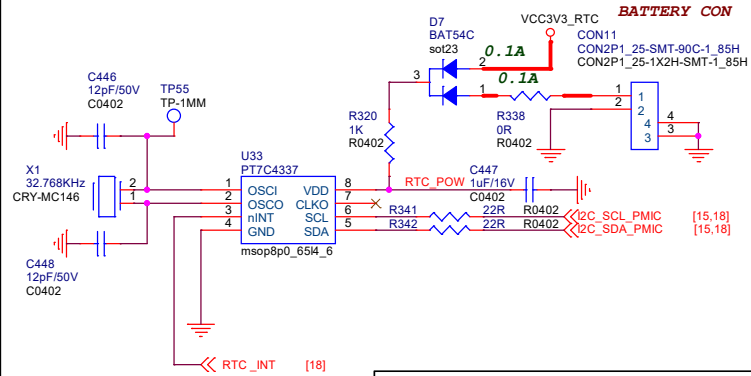
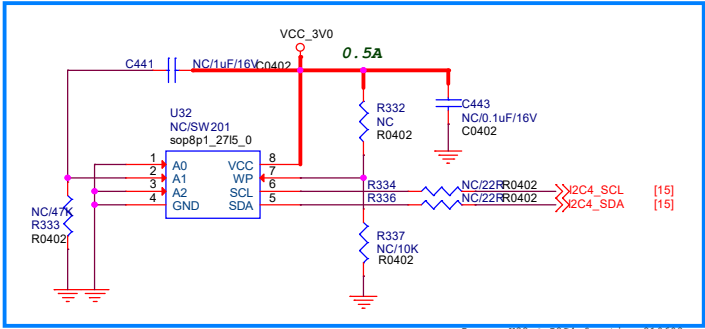
The MMA8452Q's standard slave address is a choice between the two sequential addresses 001100 and 001101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are programmed and alternate addresses are available at customer request



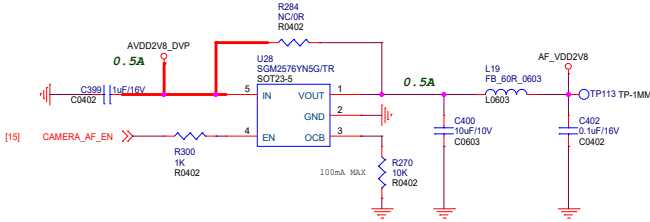
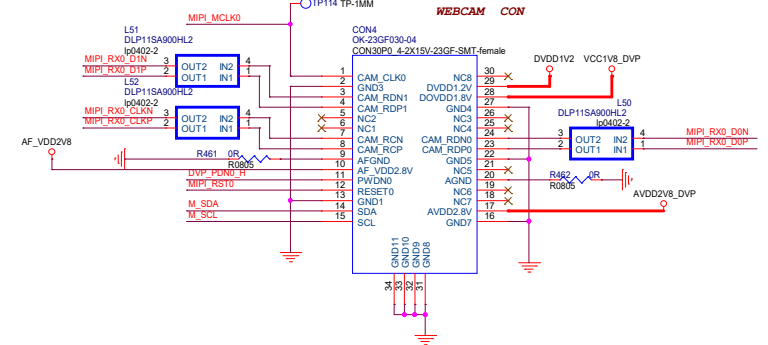
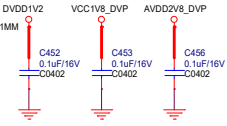
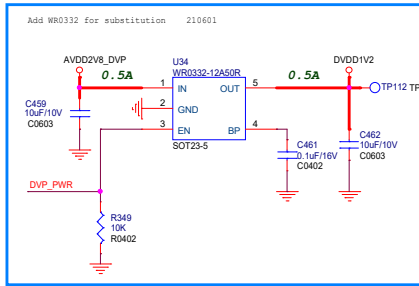
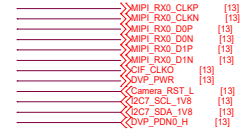
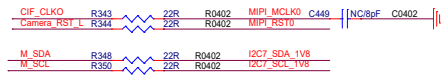
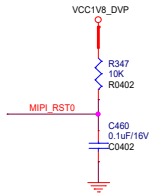
G_SCL_1V8 R339 NC/22R R0402 I2C2_SCL_1V8 [13]
G_SDA_1V8 R340 NC/22R R0402 I2C2_SDA_1V8 [13]

G_SCL_1V8_SC7 R631 22R R0402 I2C2_SCL_1V8 [13]
G_SDA_1V8_SC7 R632 22R R0402 I2C2_SDA_1V8 [13]

Add for U47 210601



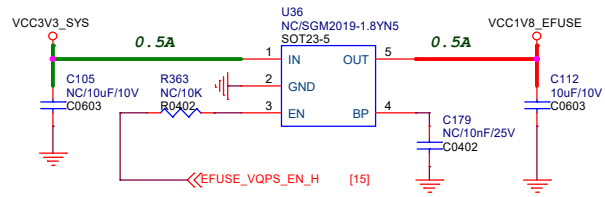
Project:	E679524		
File:	27.G-sensor&RTC		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhanglilin	Sheet:	27 of 32



SIGNWAY			
Project: E679524			
File: 28.MIPI Camera			
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhanghui	Sheet:	28 of 32

eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE.



SIGNWAY

Project:	E679524		
File:	29.eFUSE		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	Zhanglubin	Sheet:	29 of 32