AF51Y Hardware Design

Wi-Fi&Bluetooth Module Series

Version: 1.0.1

Date: 2021-07-19

Status: Preliminary

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Revision	Date	Author	Description
-	2020-12-22	Wilson PAN/ Lucas HUANG	Creation of the document
1.0.0	2020-12-24	Wilson PAN/ Lucas HUANG	Preliminary
1.0.1	2021-07-19	Wilson PAN/ Lucas HUANG	Preliminary: 1. Updated Bluetooth 5.1 to Bluetooth 5.2. 2. Added Time Sequence (Chapter 3.4.1). 3. Updated RF Performances (Chapter 4.5) 4. Updated data of transmitting power in Key Features (Table 2). 5. Deleted VDD_RF (Figure 1, Table 4&5). 6. Updated Pin 64 in Pin Assignment (Table 4). 7. Updated Pin Description, deleted VDD_RF (Table 4). 8. Updated Current consumption data (Table 22). 9. Updated RF0_ANT, RF1_ANT, BT_ANT into ANT_WIFI1, ANT_WIFI0 and ANT_BT (Figure 1). 10. Updated CTS and RTS of the HOST (Figure 8). 11. Updated Top & Bottom Views of the Module (Figure 21).

Contents

Table Index

Figure Index

1 Introduction

This document, describing AF51Y module and its air interface and hardware interfaces connected to your applications, informs you of the interface specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Concept

2.1. General Description

AF51Y is an automotive grade Wi-Fi and Bluetooth module with low power consumption. It is a single-die WLAN (Wireless Local Area Network) and Bluetooth combo solution, complying with IEEE 802.11a/b/g/n/ac 2.4 GHz & 5 GHz WLAN standards and Bluetooth 5.2 standard, which enables seamless integration of WLAN and Bluetooth Low Energy technologies.

AF51Y supports a low-power PCIe Gen 2 interface for WLAN and a UART/PCM interface for Bluetooth, and it also supports LTE & WLAN/Bluetooth coexistence interface. It is designed to be used in conjunction with Quectel AG52xR series and AG55xQ series, to provide AG52xR series and AG55xQ series with WLAN and Bluetooth functions.

2.2. Key Features

The following table describes the key features of AF51Y module.

Table 2: Key Features

Features	Details
Power Supply	● Core supply voltage: 1.8 V ● I/O supply voltage: 1.8 V ● VDD PA supply voltage: 2.2 V
Operating Frequency	● 2.4 GHz WLAN: 2.400–2.4835 GHz ● 5 GHz WLAN: 5.150–5.850 GHz ● Bluetooth: 2.402–2.480 GHz
Transmission Data Rates	● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps ● 802.11a/g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps ● 802.11n: HT20 (MCS0–7), HT40 (MCS0–7) ● 802.11ac: VHT20 (MCS0–8), VHT40 (MCS0–9), VHT80 (MCS0–9)

Protocol Features	● IEEE 802.11a/b/g/n/ac ● Bluetooth 5.2
Operation Mode	AP, STA
Modulation	CCK, BPSK, QPSK, 16QAM, 64QAM, 256QAM
WLAN Interface	PCIe
Bluetooth Interface	UART and PCM
Antenna Interfaces	● Wi-Fi&Bluetooth antenna interfaces ● 50 Ω impedance
Physical Characteristics	● Size: (19.5 ±0.2) mm × (21.5 ±0.2) mm × (2.5 ±0.2) mm ● Package: LGA ● Weight: TBD
Temperature Range	● Operating temperature range: -40 °C to +85 °C ● Storage temperature range: -40 °C to +95 °C
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of AF51Y module.

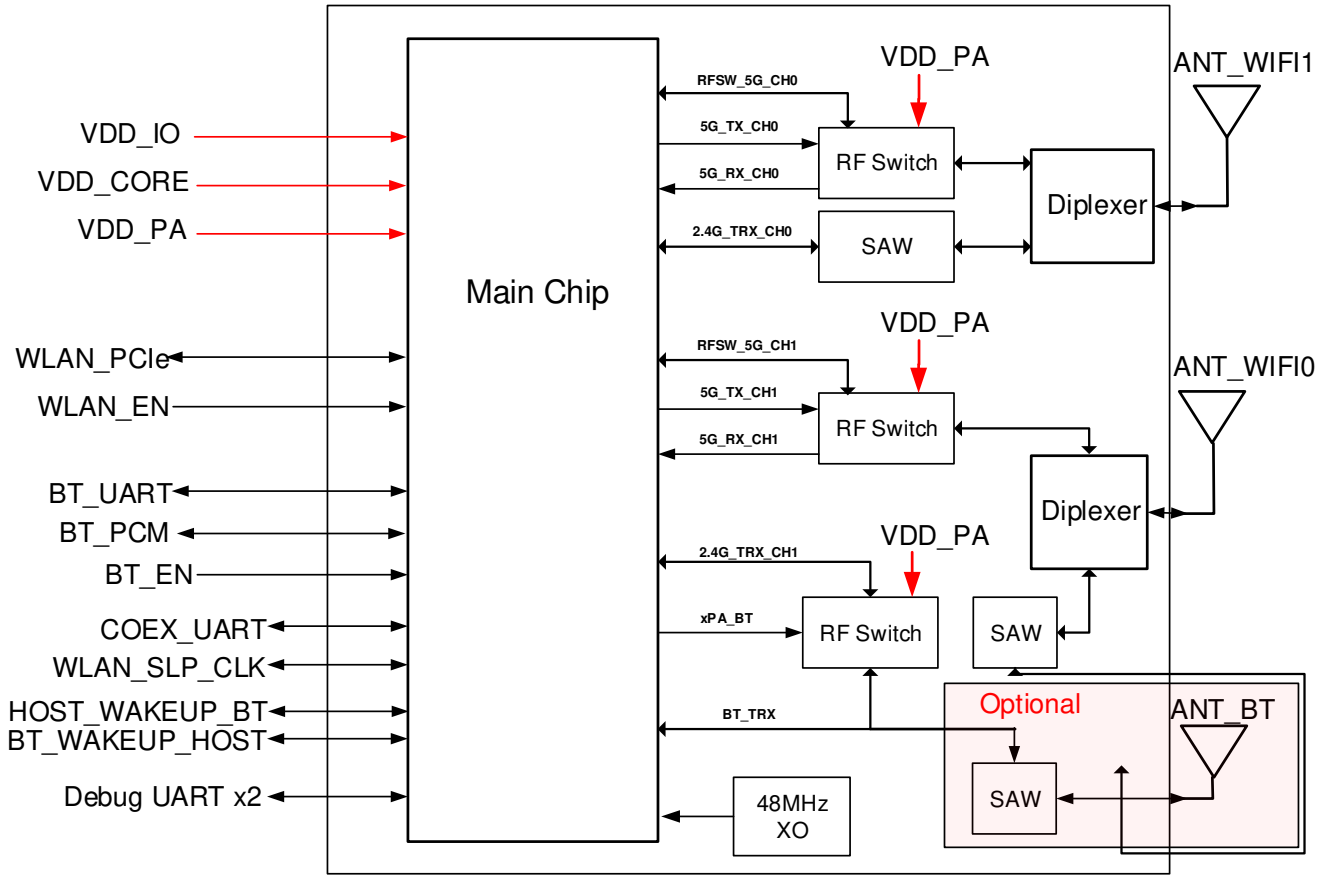


Figure 1: Functional Diagram of AF51Y Module

2.4. Evaluation Board

In order to help you develop applications with AF51Y module conveniently, Quectel supplies the evaluation board (EVB), USB to RS232 converter cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

AF51Y module is equipped with 108 LGA pins that can be connected to the cellular application platform. The subsequent chapters will provide a detailed introduction to the following interfaces and pins of the module:

- Power supply
- WLAN interface
- Bluetooth interface
- Control signal pins*
- Coexistence interfaces
- WLAN_SLP_CLK interface
- RF antenna interfaces

3.2. Pin Assignment

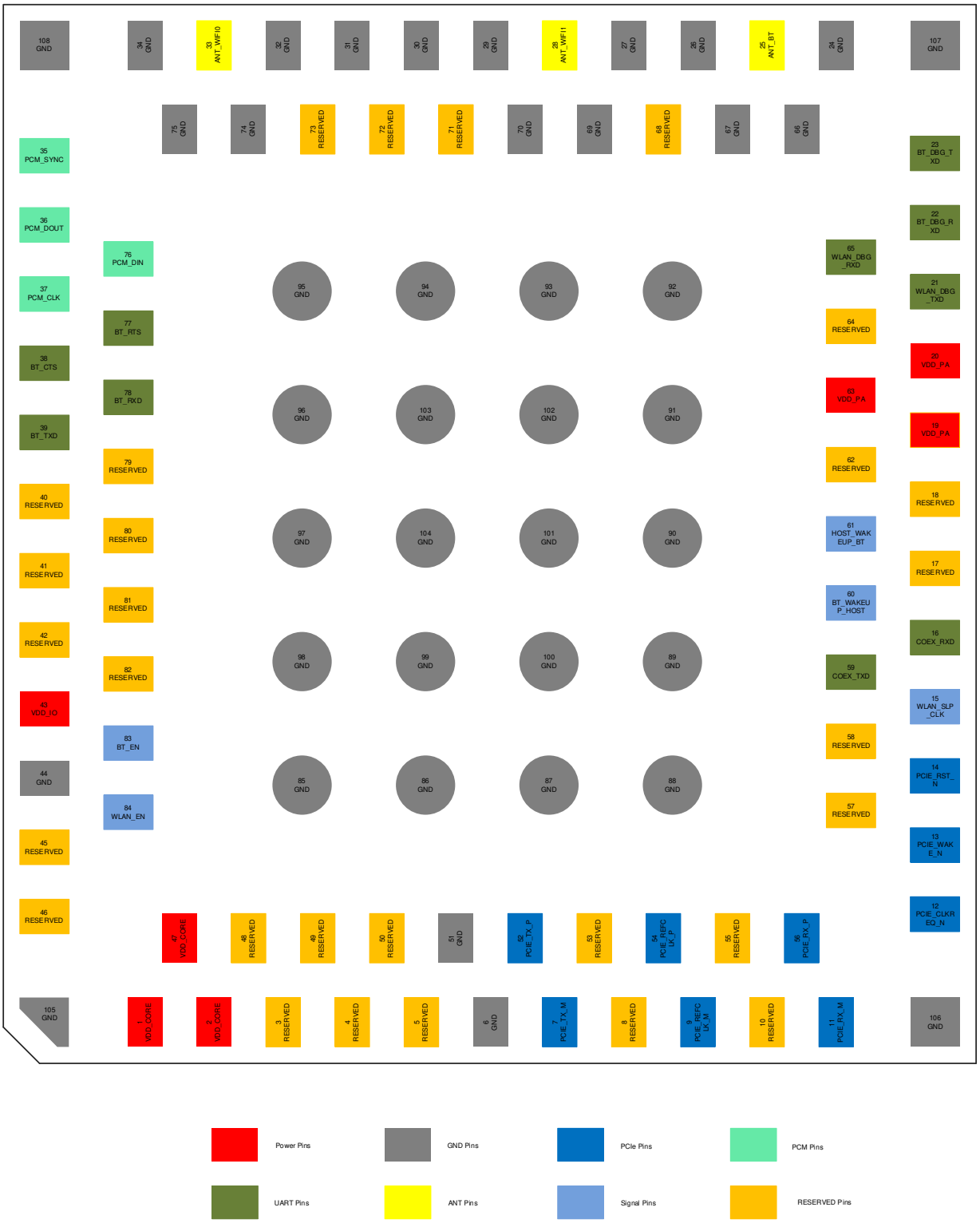


Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED pins open.

3.3. Pin Description

The following tables show the pin description of AF51Y module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

Table 4: Pin Description

Power Supply				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
VDD_CORE	1, 2, 47	PI	Voltage for core	It must be provided with sufficient current up to 1.3 A.
VDD_PA	19, 20, 63	PI	Voltage for power amplifier	It must be provided with sufficient current up to 1.5 A.
VDD_IO	43	PI	Voltage supply for I/O	It must be provided with sufficient current up to 50 mA.
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85–108			
WLAN Interface				

Pin Name	Pin No.	I/O	Description	Comment
WLAN_EN	84	DI	WLAN enable control	1.8 V power domain. Active high.
PCIE_REFCLK_P	54	AI	PCIe reference clock (+)	Require differential impedance of 100 Ω.
PCIE_REFCLK_M	9	AI	PCIe reference clock (-)	
PCIE_TX_P	52	AO	PCIe transmit (+)	
PCIE_TX_M	7	AO	PCIe transmit (-)	
PCIE_RX_P	56	AI	PCIe receive (+)	
PCIE_RX_M	11	AI	PCIe receive (-)	
PCIE_CLKREQ_N	12	DO	PCIe clock request	
PCIE_RST_N	14	DI	PCIe reset	1.8 V power domain
PCIE_WAKE_N	13	DO	PCIe wakes up host	1.8 V power domain
WLAN_DBG_TXD	21	DO	WLAN debug UART transmit	1.8 V power domain
WLAN_DBG_RXD	65	DI	WLAN debug UART receive	1.8 V power domain. If unused, keep this pin open.
Bluetooth Interface				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
BT_EN	83	DI	Bluetooth enable control	1.8 V power domain. Active high.
PCM_DIN*	76	DI	PCM data input	1.8 V power domain
PCM_SYNC*	35	DI	PCM data frame sync	1.8 V power domain
PCM_CLK*	37	DI	PCM clock	1.8 V power domain
PCM_DOUT*	36	DO	PCM data output	1.8 V power domain
BT_RTS	77	DO	Bluetooth UART request to send	1.8 V power domain
BT_CTS	38	DI	Bluetooth UART clear to send	1.8 V power domain
BT_TXD	39	DO	Bluetooth UART transmit	1.8 V power domain

BT_RXD	78	DI	Bluetooth UART receive	1.8 V power domain
BT_DBG_TXD	23	DO	Bluetooth debug UART transmit	1.8 V power domain. If unused, keep this pin open.
BT_DBG_RXD	22	DI	Bluetooth debug UART receive	1.8 V power domain. If unused, keep this pin open.
Control Signal Pins*				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
HOST_WAKEUP_BT	61	DI	Host wakes up Bluetooth	1.8 V power domain. If unused, keep this pin open.
BT_WAKEUP_HOST	60	DO	Bluetooth wakes up the host	1.8 V power domain. If unused, keep this pin open.
Coexistence Interface				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
COEX_TXD	59	DO	LTE & WLAN & Bluetooth coexistence transmit	1.8 V power domain. If unused, keep this pin open.
COEX_RXD	16	DI	LTE & WLAN & Bluetooth coexistence receive	1.8 V power domain. If unused, keep this pin open.
RF Antenna Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
ANT_WIFI1	28	AIO	Bluetooth and 2.4G & 5G WLAN antenna interface 0	50 Ω impedance
ANT_WIFI0	33	AIO	2.4G & 5G WLAN antenna interface 1	50 Ω impedance
ANT_BT	25	AIO	Reserved dedicated Bluetooth antenna interface	50 Ω impedance
WLAN_SLP_CLK Interface*				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
WLAN_SLP_CLK	15	DI	External 32.768 kHz sleep clock input	1.8 V power domain
RESERVED Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**

RSERVED	3, 4, 5, 8, 10, 17, 18, 40, 41, 42, 45, 46, 48, 49, 50, 53, 55, 57, 58, 62, 64, 68, 71, 72, 73, 79, 80, 81, 82	Keep these pins open.

NOTE

Please keep all RESERVED and unused pins open.

3.4. Power Supply

The following table shows the power supply pins and ground pins of AF51Y module.

Table 5: Definition of Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VDD_CORE	1, 2, 47	Voltage for core	1.71	1.8	1.89	V
VDD_PA	19, 20, 63	Voltage for power amplifier	2.09	2.2	2.31	V
VDD_IO	43	Voltage supply for I/O	1.62	1.8	1.98	V
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85–108	Ground	-	-	-	V

3.4.1. Power on and off Scenarios

The power on scenario is illustrated in the following figure.

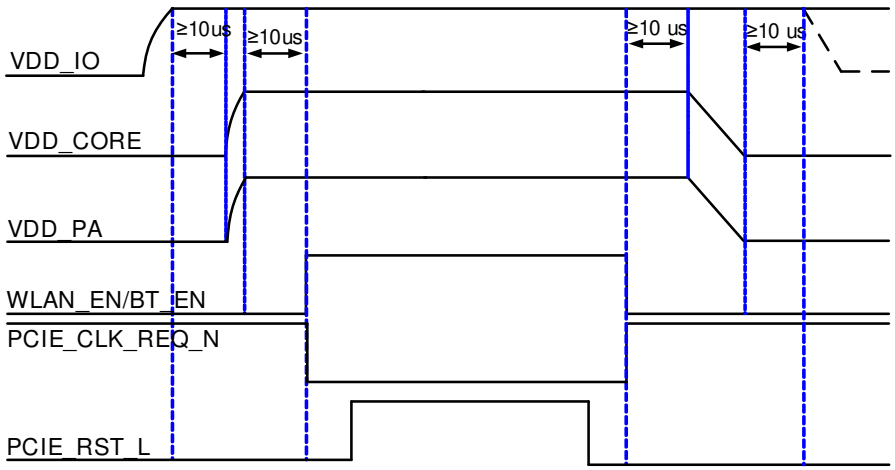


Figure 3: Time Sequence

3.5. WLAN Application Interface

The following figure shows the WLAN application interface connection between AF51Y and host.

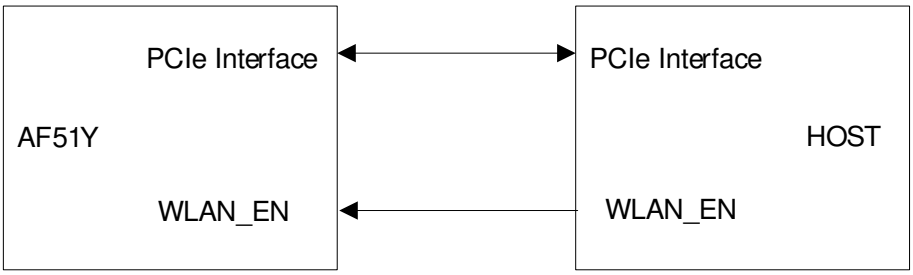


Figure 4: WLAN Interface Connection

3.5.1. WLAN_EN

WLAN_EN is used to control the WLAN function of AF51Y module. WLAN function will be enabled when WLAN_EN is at high level.

Table 6: Pin Definition of WLAN_EN

Pin Name	Pin No.	I/O	Description	Comment
WLAN_EN	84	DI	WLAN enable control	Active high

NOTE

WLAN_EN is a sensitive signal, and it should be ground shielded and routed as close as possible to AF51Y module.

3.5.2. PCIe Interface

Table 7: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	54	AI	PCIe reference clock (+)	Require differential impedance of 100 Ω.
PCIE_REFCLK_M	9	AI	PCIe reference clock (-)	
PCIE_TX_P	52	AO	PCIe transmit (+)	
PCIE_TX_M	7	AO	PCIe transmit (-)	
PCIE_RX_P	56	AI	PCIe receive (+)	
PCIE_RX_M	11	AI	PCIe receive (-)	
PCIE_CLKREQ_N	12	DO	PCIe clock request	1.8 V power domain
PCIE_RST_N	14	DI	PCIe reset	
PCIE_WAKE_N	13	DO	PCIe wakes up host	

The following figure shows the PCIe interface connection between AF51Y and the host.

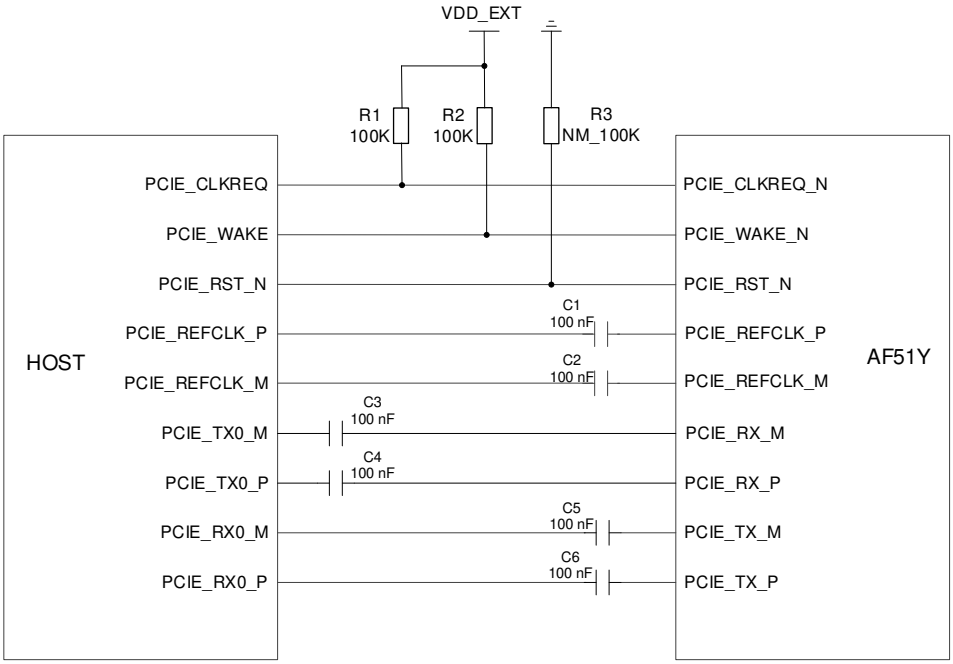


Figure 5: PCIe Interface Connection

In order to ensure the signal integrity of PCIe interface, C3 and C4 should be placed close to the host module, and C5 and C6 should be placed close to the AF51Y module. The extra stubs of traces must be as short as possible. A couple of 100 nF capacitors (C1/C2) must be added when the host is I.MX serial, because the differential clock of I.MX serial does not meet PCIe compliance standard.

The following principles of PCIe interface design should be complied with, to meet PCIe Gen2 specifications.

- It is important to route the PCIe signal traces as differential pairs with total grounding. And the differential impedance is 100 Ω ±10 %.
- For PCIe signal traces, the maximum length of each differential data pair (PCIE_TX/PCIE_RX/PCIE_REFCLK) is recommended to be less than 300 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- Spacing to all other signals (inter-interface) is four times of trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices, or RF signal traces. It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces with ground on that layer and with ground planes above and below.

3.6. Bluetooth Application Interface

The following figure shows the block diagram of Bluetooth interface connection between AF51Y and the host.

If Bluetooth function of AF51Y module is used, the UART and PCM interfaces of AF51Y must be connected to that of the host.

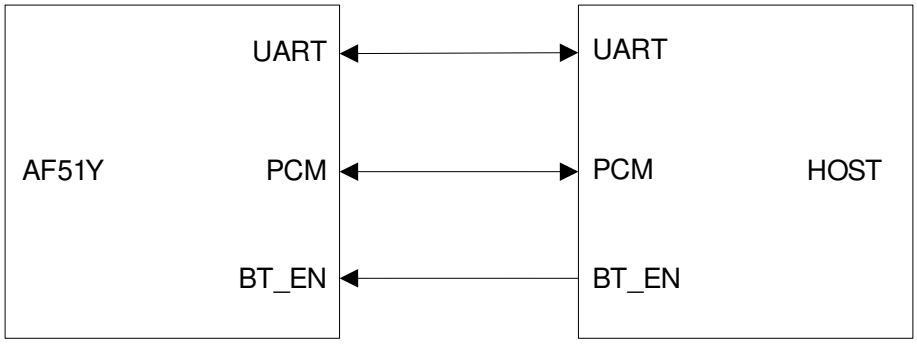


Figure 6: Block Diagram of Bluetooth Interface Connection

3.6.1. BT_EN

BT_EN is used to control the Bluetooth function of AF51Y module. Bluetooth function will be enabled when BT_EN is at high level.

Table 8: Pin Definition of BT_EN

Pin Name	Pin No.	I/O	Description	Comment
BT_EN	83	DI	Bluetooth enable control	Active high.

3.6.2. PCM Interface*

Table 9: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	76	DI	PCM data input	1.8 V power domain
PCM_SYNC	35	DI	PCM data frame sync	1.8 V power domain

PCM_CLK	37	DI	PCM clock	1.8 V power domain
PCM_DOUT	36	DO	PCM data output	1.8 V power domain

The following figure shows the PCM interface connection between AF51Y and the host.

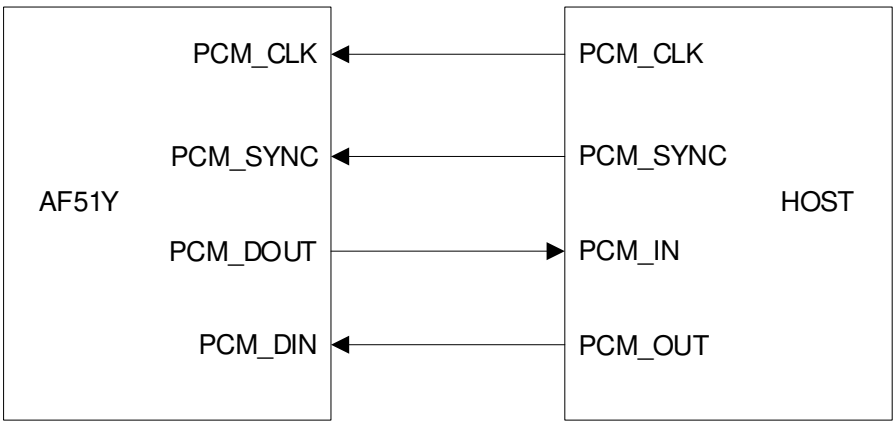


Figure 7: PCM Interface Connection

3.6.3. UART Interface

Table 10: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_RTS	77	DO	Bluetooth UART request to send	1.8 V power domain
BT_CTS	38	DI	Bluetooth UART clear to send	1.8 V power domain
BT_TXD	39	DO	Bluetooth UART transmit	1.8 V power domain
BT_RXD	78	DI	Bluetooth UART receive	1.8 V power domain

The following figure shows the reference design for UART interface connection between AF51Y and the host.

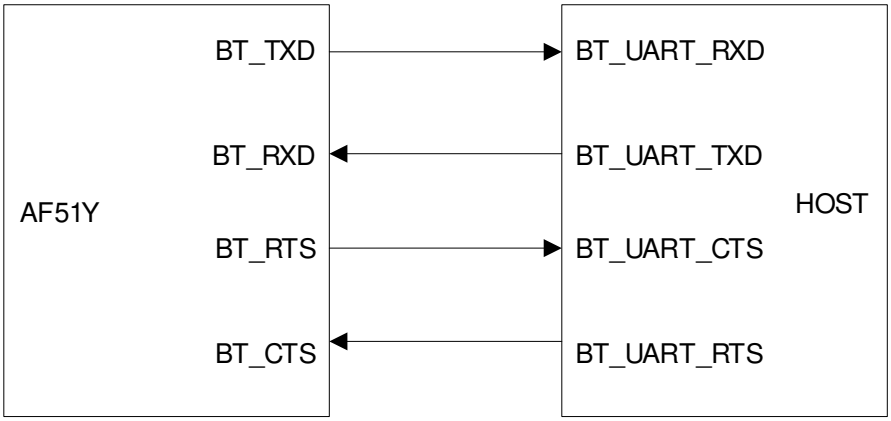


Figure 8: UART Interface Connection

3.7. Control Signal Pins*

3.7.1. HOST_WAKEUP_BT and BT_WAKEUP_HOST

Table 11: Pin Definition of HOST_WAKEUP_BT and BT_WAKEUP_HOST

Pin Name	Pin No.	I/O	Description	Comment
HOST_WAKEUP_BT	61	DI	Host wakes up Bluetooth	1.8 V power domain. If unused, keep this pin open .
BT_WAKEUP_HOST	60	DO	Bluetooth wakes up the host	1.8 V power domain. If unused, keep this pin open .

3.8. Coexistence Interfaces

3.8.1. UART Coexistence Interface

Table 12: Pin Definition of UART Coexistence Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_TXD	59	DO	LTE & WLAN & Bluetooth coexistence transmit	If unused, keep this pin open.
COEX_RXD	16	DI	LTE & WLAN & Bluetooth coexistence receive	If unused, keep this pin open.

AF51Y module supports LTE & WLAN coexistence and LTE & Bluetooth coexistence. The following figure shows the UART coexistence interface connection between AF51Y and AG52xR series and AG55xQ series modules.

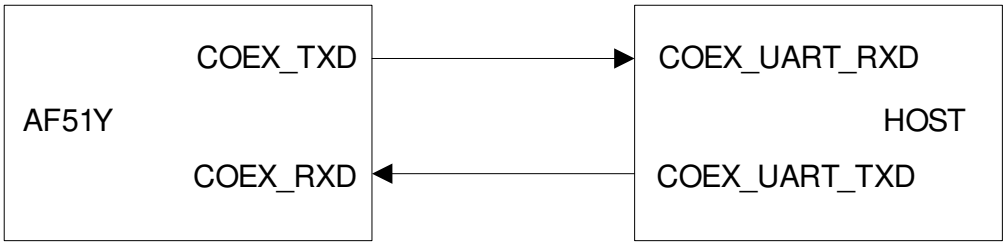


Figure 9: UART Coexistence Interface Connection

3.9. WLAN_SLP_CLK Interface*

An external 32.768 kHz sleep clock connecting to WLAN_SLP_CLK is necessary. AF51Y is unable to boot up and work without sleep clock.

Table 13: Pin Definition of WLAN_SLP_CLK Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	15	DI	External 32.768 kHz sleep clock input	1.8 V power domain

3.10. RF Antenna Interfaces

Table 14: Pin Definition of RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI1	28	AIO	Bluetooth and 2.4G & 5G WLAN antenna interface 0	50 Ω impedance
ANT_WIFI0	33	AIO	2.4G & 5G WLAN antenna interface 1	50 Ω impedance
ANT_BT	25	AIO	Reserved dedicated Bluetooth antenna interface	50 Ω impedance

3.10.1. Operating Frequency

Table 15: Operating Frequency of the Module

Feature	Frequency	Unit
2.4 GHz WLAN	2.400–2.4835	GHz
5 GHz WLAN	5.150–5.850	GHz
Bluetooth	2.402–2.480	GHz

3.10.2. Reference Design of RF Antenna Interfaces

AF51Y module provides three RF antenna interfaces for antenna connection. A reference circuit design for an RF antenna interface is shown below.

It is recommended to reserve a π-type and notch matching circuit for better RF performance, and the π-type matching components (C3, C4, and R1) and the notch (C1, C2, L1 and L2) should be placed as close to the antenna as possible. The capacitors and inductors are not mounted by default.

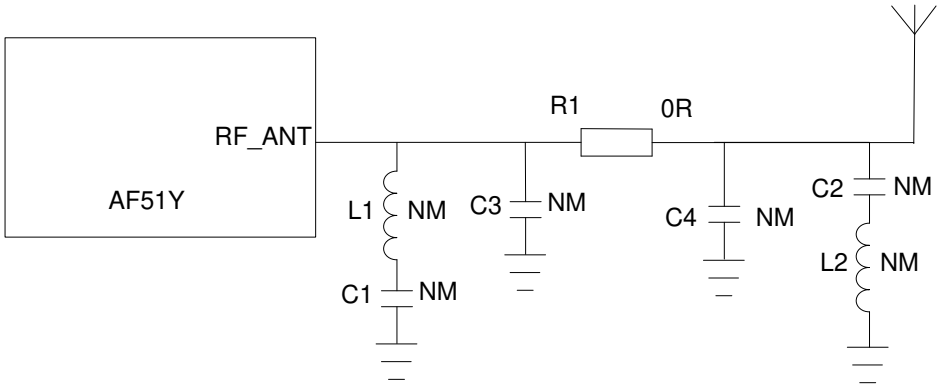


Figure 10: Reference Circuit for RF Antenna Interfaces

3.10.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

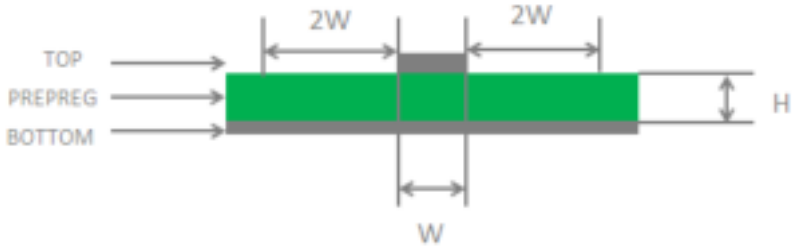


Figure 11: Microstrip Design on a 2-layer PCB

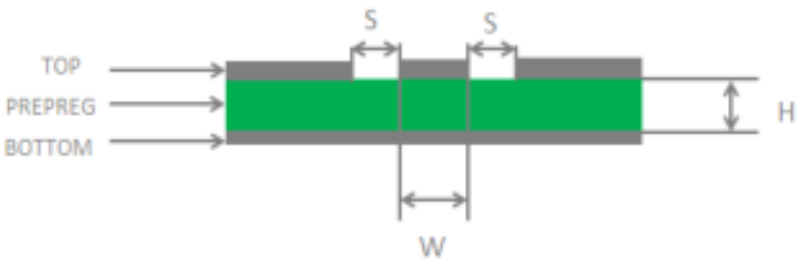


Figure 12: Coplanar Waveguide Design on a 2-layer PCB

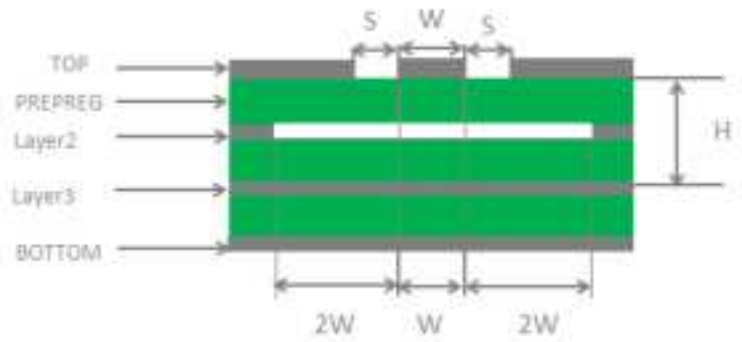


Figure 13: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

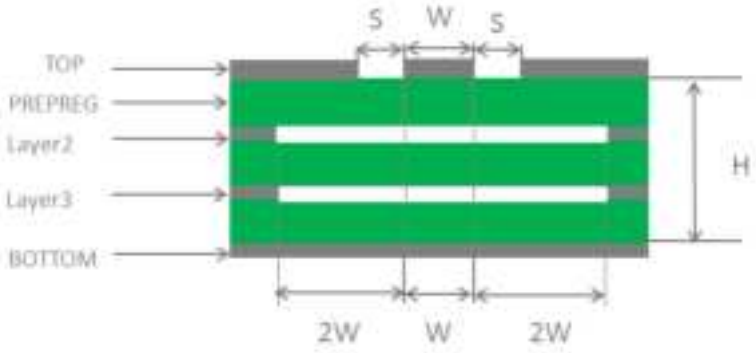


Figure 14: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

3.10.4. Antenna Requirements

The following tables show the requirements on antenna cables and antennas.

Table 16: Antenna Cable Requirements

Type	Requirements
2.400–2.4835 GHz	Cable insertion loss: <1 dB
5.150–5.850 GHz	Cable insertion loss: <1 dB

Table 17: Antenna Requirements

Type	Requirements
Frequency Range (GHz)	2.400–2.4835 5.150–5.850
VSWR	< 2:1 recommended
Gain (dBi)	Typical 1
Max Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

3.10.5. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

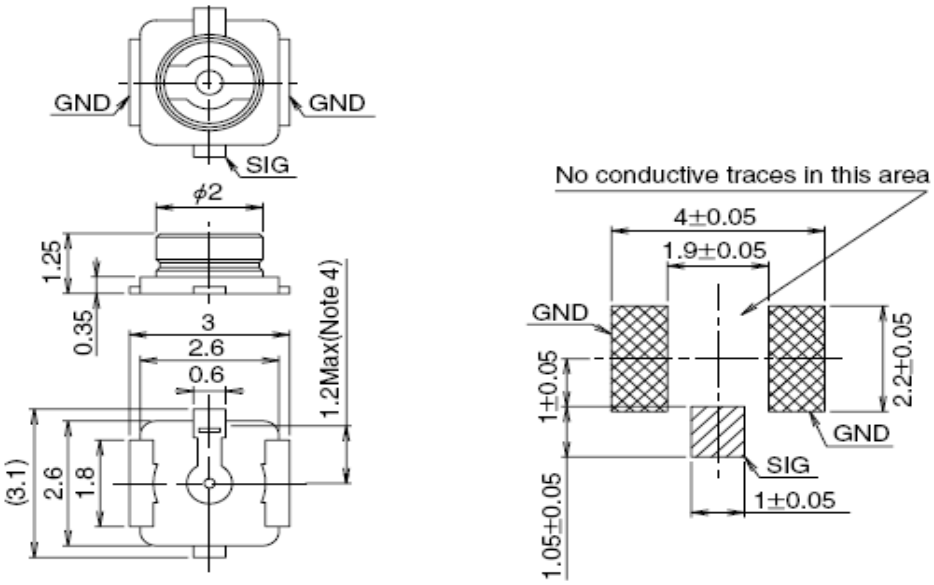


Figure 15: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

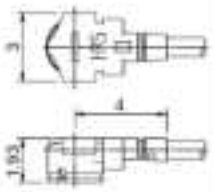
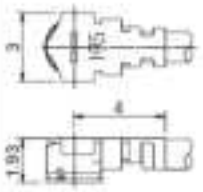
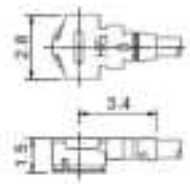
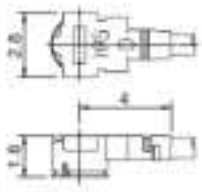
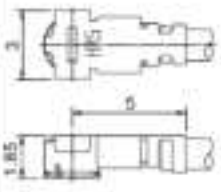
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 16: Mechanicals of UF.L-LP Connectors (Unit: mm)

The following figure describes the space factor of mated connector

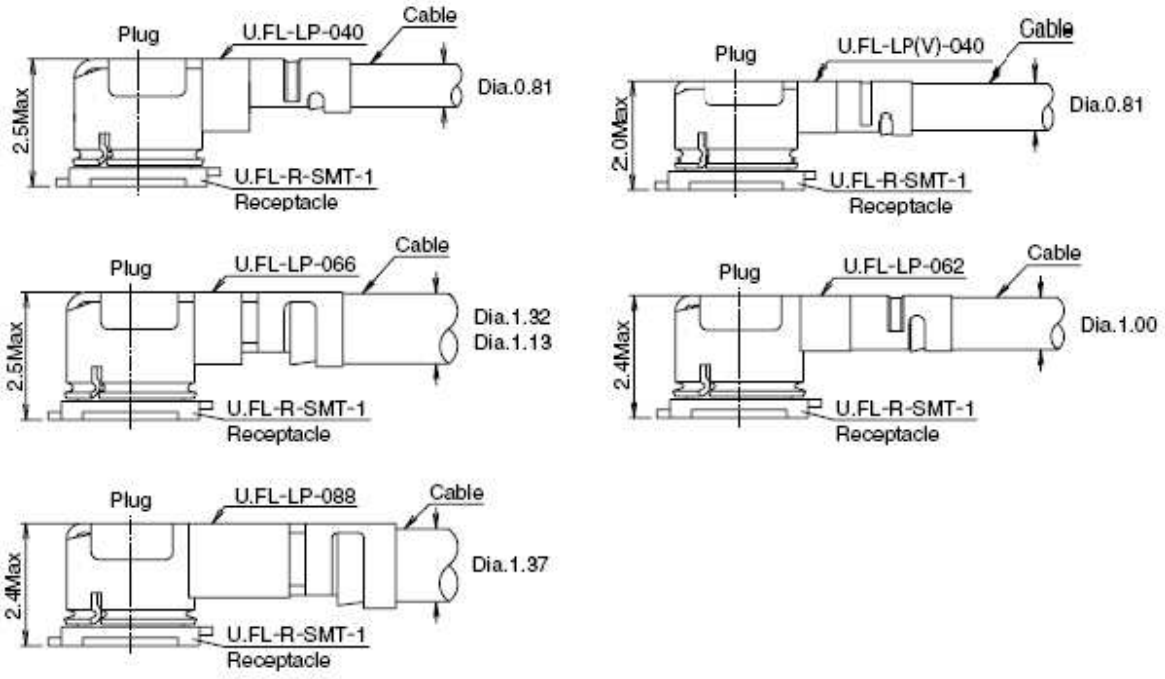


Figure 17: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

4 Reliability, Radio and Electrical Characteristic

4.1. General Description

This chapter mainly introduces electrical and radio frequency characteristics of AF51Y module. The details are listed in the subsequent chapters.

4.2. Electrical Characteristics

Table 18: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VDD_CORE	-0.3	V_{DDX} + 0.2	V
VDD_PA	-0.3	V_{DDX} + 0.2	V
VDD_IO	-0.3	V_{DDX} + 0.2	V
Digital I/O Input Voltage	-0.3	VDD_IO + 0.2	V

NOTE

V_{DDX} is the supply voltage associated with the input pin to which the test voltage is applied.

The following table shows the recommended operating conditions of AF51Y module.

Table 19: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VDD_CORE	1.71	1.8	1.89	V
VDD_PA	2.09	2.2	2.31	V
VDD_IO	1.62	1.8	1.98	V

4.3. I/O Interface Characteristics

The following table shows the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 20: General DC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	High Level Input Voltage	0.65 × VDD_IO	VDD_IO + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.35 × VDD_IO	V
V_{OH}	High Level Output Voltage	VDD_IO - 0.45	VDD_IO	V
V_{OL}	Low Level Output Voltage	0	0.45	V
I_{IL}	Input Leakage Current	TBD	TBD	μA

4.4. Current Consumption

Table 21: Current Consumption of the Module (Low Power Modes)

Conditions	I_{VDD_CORE}	I_{VDD_IO}	I_{VDD_PA}	Unit
AT+QWIFI=0	TBD	TBD	TBD	mA
AT+QWIFI=1	TBD	TBD	TBD	mA

Table 22: Current Consumption of the Module (Normal Operation)

Description	Conditions	I_{VDD_CORE}	I_{VDD_IO}	I_{VDD_PA}	Unit
802.11b	TX 1 Mbps	296.51	4.51	483.47	mA
	TX 11 Mbps	303.32	4.41	475.61	mA
802.11g	TX 6 Mbps	317.34	4.36	467.53	mA
	TX 54 Mbps	330.46	4.52	377.17	mA
802.11n (2.4G)	TX HT20-MCS0	320.44	4.34	461.51	mA
	TX HT20-MCS7	334.63	4.64	359.71	mA
	TX HT40-MCS0	332.38	4.51	443.62	mA
	TX HT40-MCS7	343.47	4.43	231.70	mA
802.11a	TX 6 Mbps	330.27	4.51	488.71	mA
	TX 54 Mbps	360.58	4.37	382.78	mA
802.11n (5G)	TX HT20-MCS0	342.22	4.28	472.62	mA
	TX HT20-MCS7	359.91	4.32	365.83	mA
	TX HT40-MCS0	378.65	4.31	467.85	mA
	TX HT40-MCS7	381.73	4.33	264.71	mA
802.11ac	TX VHT20 MCS0	342.72	4.27	473.15	
	TX VHT20 MCS8	364.76	4.38	348.54	mA

	TX VHT40 MCS0	378.70	4.39	467.86	mA
	TX VHT40 MCS9	378.68	4.32	230.11	mA
	TX VHT80 MCS0	434.65	4.74	434.39	mA
	TX VHT80 MCS9	380.91	4.37	161.64	mA

4.5. RF Performances

The following tables summarize the transmitting and receiving performances of AF51Y.

4.5.1. Conducted RF Output Power

Table 23: Conducted RF Output Power at BT

Frequency	Min.	Typ.	Unit
Classic	8	10	dBm
BLE	5	7	dBm

Table 24: Conducted RF Output Power at 2.4 GHz

Frequency	Min.	Typ.	Unit
802.11b @ 1 Mbps	15.5	17.5	dBm
802.11g @ 6 Mbps	15	17	dBm
802.11n, HT20 @ MCS0	15	17	dBm
802.11n, HT40 @ MCS0	11	13.5	dBm

Table 25: Conducted RF Output Power at 5 GHz

Frequency	Min.	Typ.	Unit
802.11a @ 6 Mbps	13.5	15.5	dBm

802.11n, HT20 @ MCS0	13.5	15.5	dBm
802.11n, HT40 @ MCS0	13	15	dBm
802.11ac, VHT20 @ MCS0	13.5	15.5	dBm
802.11ac, VHT40 @ MCS0	13	15	dBm
802.11ac, VHT80 @ MCS0	12.5	14.5	dBm

4.5.2. Conducted RF Receiving Sensitivity

Table 26: Conducted RF Receiving Sensitivity at 2.4 GHz

Frequency	Receiving Sensitivity (Typ.)
802.11b, 1 Mbps	93 dBm
802.11b, 11 Mbps	84 dBm
802.11g, 6 Mbps	87 dBm
802.11g, 54 Mbps	70 dBm
802.11n, HT20, MCS0	87 dBm
802.11n, HT20, MCS7	69 dBm
802.11n, HT40, MCS0	84 dBm
802.11n, HT40, MCS7	67 dBm

Table 27: Conducted RF Receiving Sensitivity at 5 GHz

Frequency	Receiving Sensitivity (Typ.)
802.11a, 6 Mbps	90 dBm
802.11a, 54 Mbps	73 dBm
802.11n, HT20, MCS0	90 dBm
802.11n, HT20, MCS7	72 dBm

802.11n, HT40, MCS0	87 dBm
802.11n, HT40, MCS7	70 dBm
802.11ac, VHT20, MCS0	90 dBm
802.11ac, VHT20, MCS8	68 dBm
802.11ac, VHT40, MCS0	87 dBm
802.11ac, VHT40, MCS9	64 dBm
802.11ac, VHT80, MCS0	84 dBm
802.11ac, VHT80, MCS9	60 dBm

4.6. Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

5 Mechanical Dimensions

This chapter describes the mechanical dimensions of AF51Y module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

5.1. Mechanical Dimensions of the Module

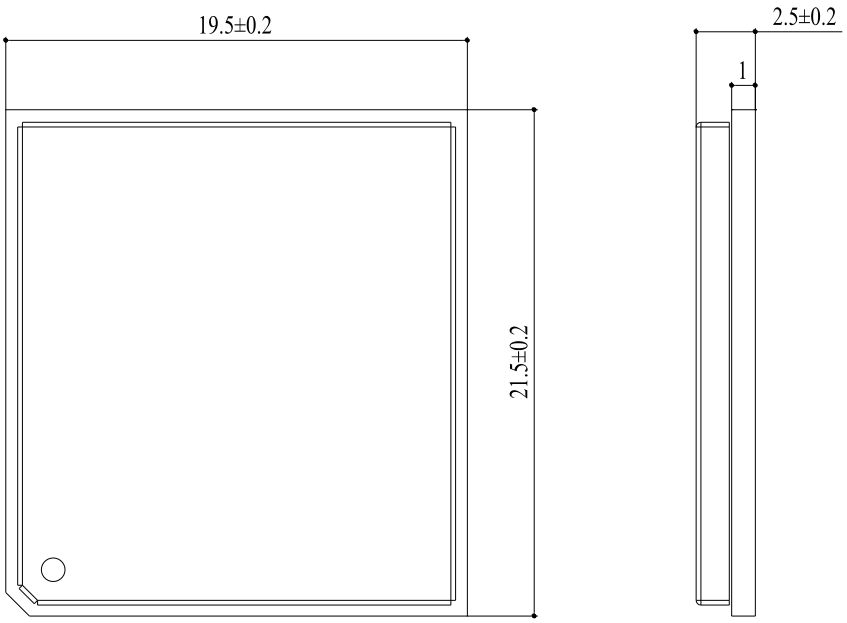


Figure 18: AF51Y Top and Side Dimensions

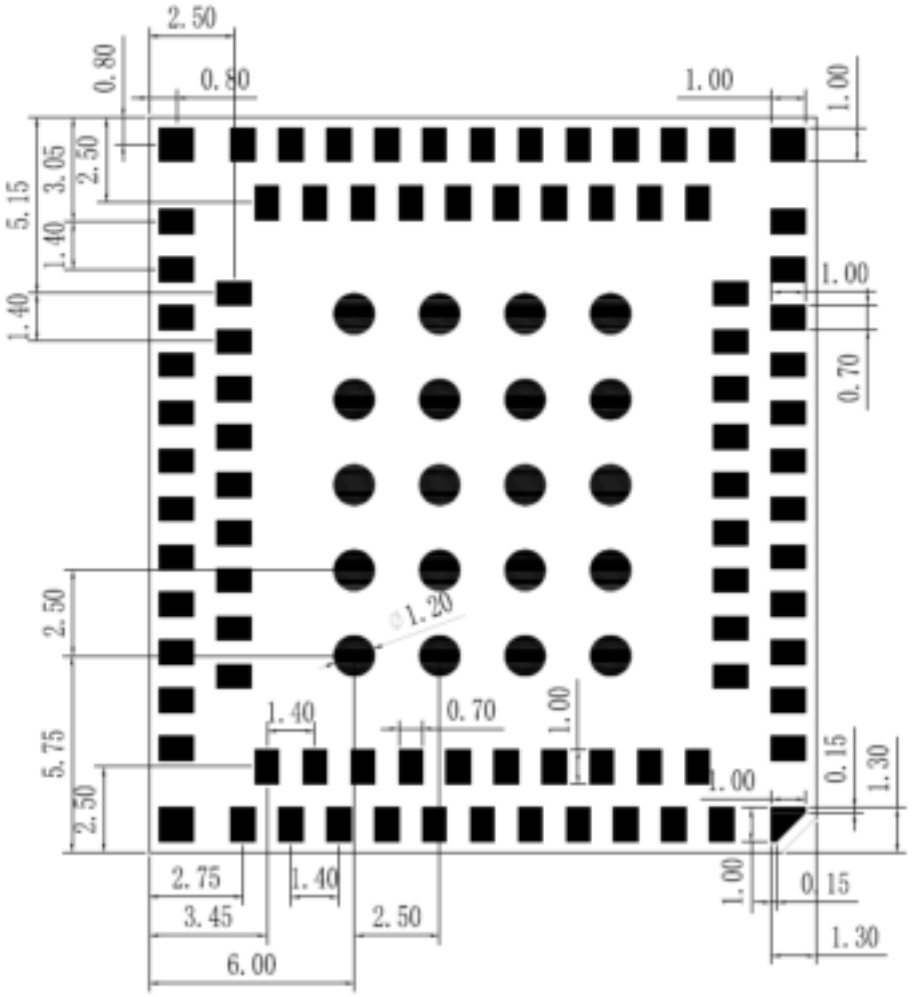


Figure 19: AF51Y Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

5.2. Recommended Footprint

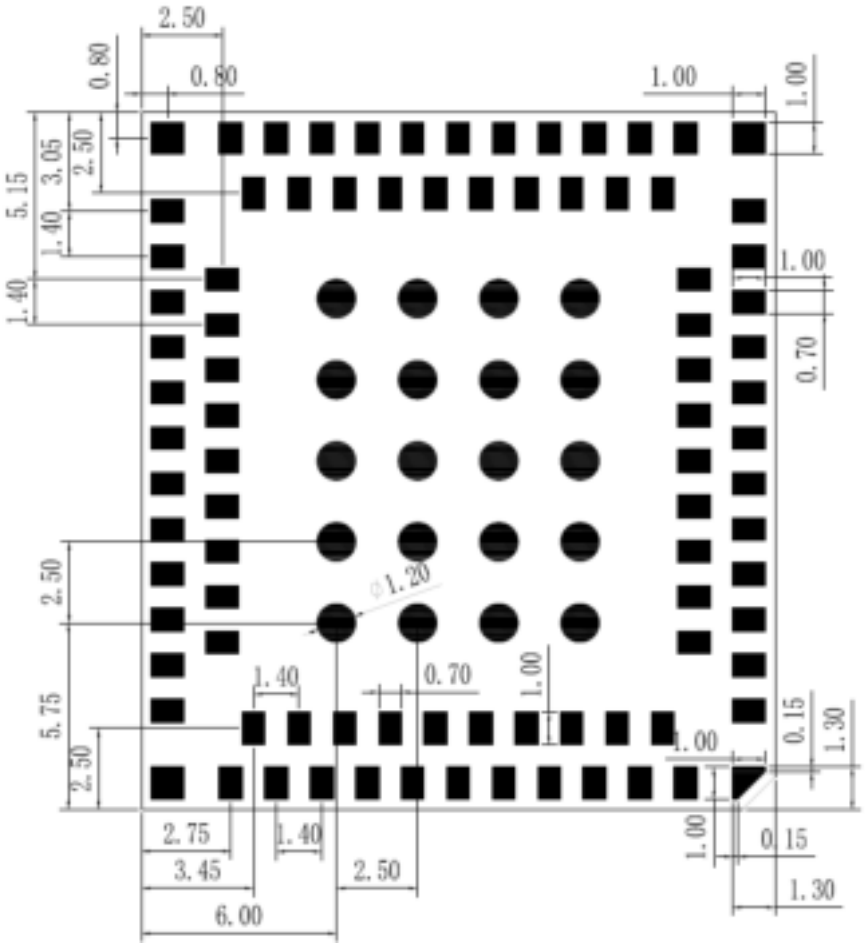


Figure 20: Recommended Footprint (Bottom View)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. Keep all RESERVED pins open.

5.3. Top and Bottom Views of the Module

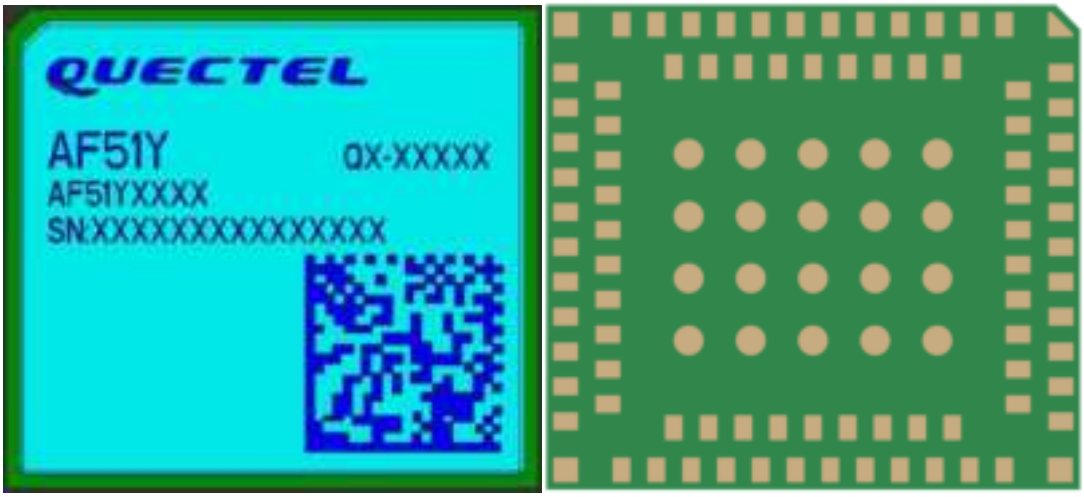


Figure 21: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

6 Storage, Manufacturing and Packaging

6.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:
   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[1] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

6.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [3]***.

The peak reflow temperature should be 238–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

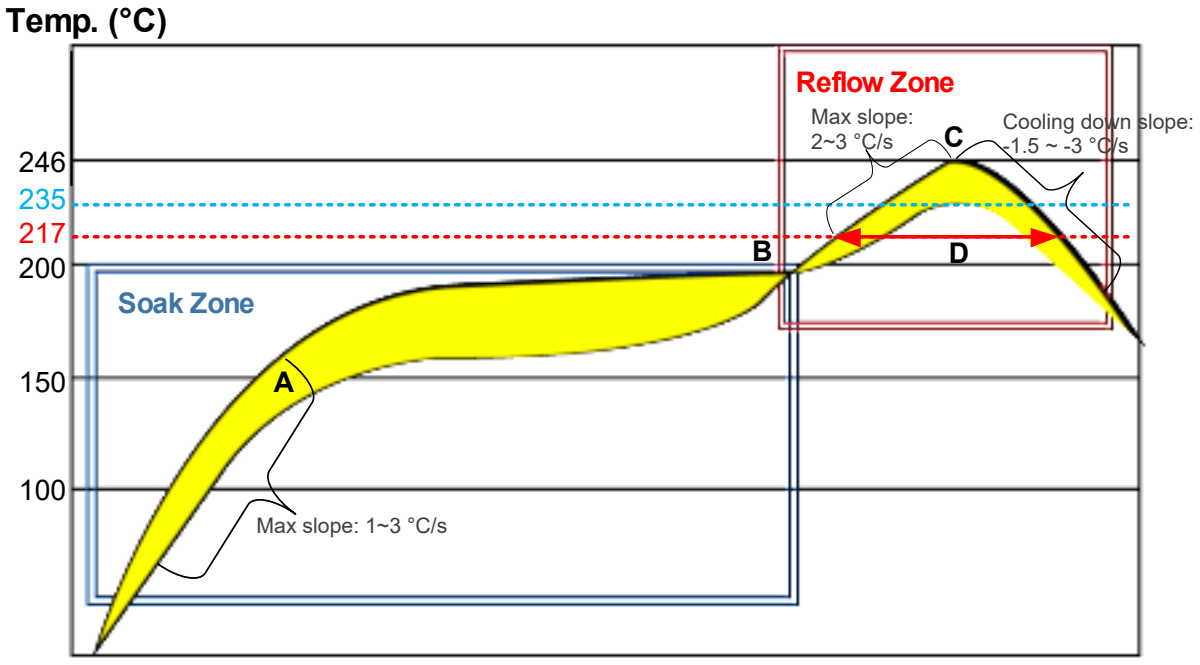


Figure 22: Recommended Reflow Soldering Thermal Profile

Table 28: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

6.3. Packaging

AF51Y module is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

AF51Y is packaged in tape and reel carriers.

Table 29: Reel Packaging

Model Name	MOQ for MP	Minimum Package: TBD	Minimum Package TBD
AF51Y	TBD	Size: TBD N.W: TBD G.W: TBD	Size: TBD N.W: TBD G.W: TBD

7 Worning

7.1. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

Important Note notice that any deviation(s) from the defined parameters of the antenna trace, as described by the
instructions, require that the host product manufacturer must notify to Quectel Wireless Solutions Co., Ltd.. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR202303AF51Y”
The FCC ID can be used only when all FCC mpliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.
(4) The max allowed antenna gain is 3.76dBi for external monopole antenna.
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

7.2. FCC Statement

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

7.3. IC Statement

This device complies with Industry Canada's licence exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device.
Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.
L'exploitation est autorisée aux deux conditions suivantes (1) l'appareil ne doit pas produire de brouillage, et.
(2) l' utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This device complies with the Canadian ICES-003 Class B specifications. CAN ICES-3(B)/ NMB-3(B).
Cet appareil numérique de la Canadian ICES-003. Cet appareil num rique de la classe B est conforme à la norme NMB-003 du Canada.

8 Appendix References

Table 30: Related Documents

Document Name
[1] Quectel_V2X&5G_EVB_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_Secondary_SMT_User_Guide

Table 31: Terms and Abbreviations

Abbreviation	Description
AP	Access Point
BPSK	Binary Phase Shift Keying
Bluetooth	Bluetooth
CCK	Complementary Code Keying
CTS	Clear To Send
ESD	Electrostatic Discharge
GND	Ground
HT	High Throughput
IEEE	Institute of Electrical and Electronics Engineers
I_{IL}	Input Leakage Current
I/O	Input/Output
LTE	Long Term Evolution

Mbps	Megabits per second
MCS	Modulation and Coding Scheme
MOQ	Minimum Order Quantity
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
TBD	To Be Determined
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VHT	Very High Throughput
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
$V_{OH}min$	Minimum High-level Output Voltage
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless-Fidelity
WLAN	Wireless Local Area Network