WGM160P Wi-Fi® Module Data Sheet

The WGM160P is an ultra low power all-inclusive Wi-Fi® module targeted for applications requiring excellent RF performance, low power consumption, high security, integrated customer applications and fast time to market.

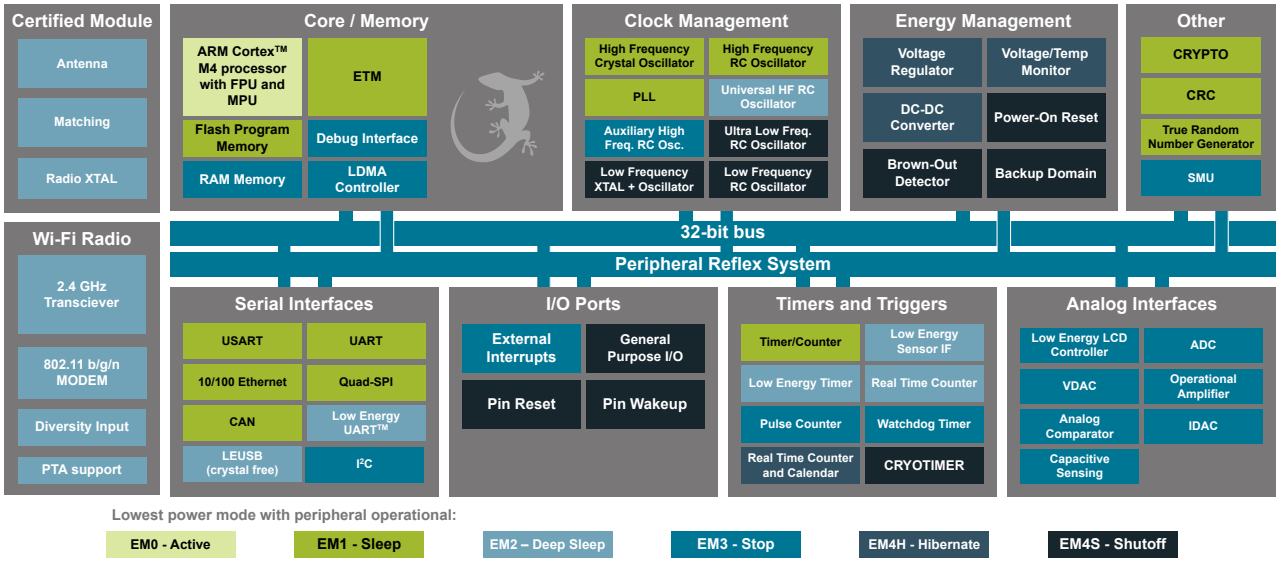
The WGM160P module integrates all of the necessary elements required for a cloud connected IoT Wi-Fi application, including 802.11b/g/n radio, integrated chip antenna, certifications, microcontroller, Wi-Fi and IP stacks, HTTP server, and multiple protocols, such as TCP and UDP. Co-existence with external 2.4GHz transceivers is supported.

WGM160P can be configured to concurrently act as a Wi-Fi client and a Wi-Fi access point, which is ideal for user friendly device provisioning. WGM160P can natively host C-applications, removing the need for an external host controller. Alternatively, the Wi-Fi Module can run in Network Co-Processor (NCP) mode, leaving the complexity of TCP/IP networking to the module so that the customer's own host controller can be fully dedicated to processing the customer application tasks. The WGM160P module has highly flexible host and peripheral hardware interfaces for wide application use.

This module also supports Gecko OS, a comprehensive software suite designed to simplify your Wi-Fi, application, device management and cloud connectivity development process.

KEY POINTS

- Available with integrated chip antenna or an RF pin
- Antenna diversity supported via secondary RF pin
- IEEE 802.11 b/g/n compliant
- TX power: +16 dBm
- RX sensitivity: -96 dBm
- CPU core: 32-bit ARM® Cortex-M4
- Flash memory: 2 MB
- RAM: 512 kB
- Concurrent mode: Wi-Fi AP and STA
- Ultra low power consumption
- Wi-Fi Alliance certified (pending)
- Modular certification
  - CE, FCC, ISED
  - Japan, KC (pending)
- End-to-end security
- Built-in 10/100 Ethernet Support
- Gecko OS support
- Size: 23.8 mm x 14.2 mm x 2.3 mm



1. Key Features

The key features of the WGM160P module are listed below.

Radio Features

- Built-in Antenna (optional)
- TX Power: +16 dBm
- RX Sensitivity: -96 dBm
- Superior blocking performance

Wi-Fi Features

- 802.11: b/g/n
- Bit rate: up to 72.2 Mbps
- 802.11 Security: WPA2/WPA Personal
- STA (Station Mode)
- SoftAP (Soft Access Point Mode)

Electrical Characteristics

- Supply voltage: 3.0V to 3.6V

Environmental specifications

- Temperature range: -40°C to +85°C

Modular certification (pending)

- Wi-Fi Alliance
- CE, FCC, ISED, KC, Japan
- RoHS/REACH compliant

Dimensions

- L x W x H: 23.8 mm x 14.2 mm x 2.3 mm

MCU Features

- ARM® Cortex-M4, 72MHz
- 512 kB RAM
- 2 MB Flash

Hardware Interfaces

- Host interface: UART/SPI/USB
- Peripheral interfaces
  - 2 x USART (UART/SPI/I2S)
  - QSPI with Execute In Place (XIP) support
  - SD Card support (SPI)
  - Capacitive Touch Sensing in all GPIOs
  - LESENSE
  - 10/100 Ethernet MAC with RMII interface
  - USB device (2.0 Full speed)
  - I^2C peripheral interfaces
  - CAN
- Up to 31 x GPIO with interrupts
- 2 x 12-bit ADC
- 2 x 12-bit DAC
- Rich selection of timers, inc. Real-time counters
- Co-existence interface (PTA: 2, 3, 4 wire)

2. Ordering Information

Table 2.1. Ordering Information

Part Number	Protocol	Max TX Power	Flash/Ram (kB)	LF XTAL	Antenna	GPIO	Carrier
WGM160PX22KGA2	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	Included	Built-in	Up to 31	Cut Tape
WGM160PX22KGA2R	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	Included	Built-in	Up to 31	Reel
WGM160P022KGA2	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	None	Built-in	Up to 31	Cut Tape
WGM160P022KGA2R	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	None	Built-in	Up to 31	Reel
WGM160PX22KGN2	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	Included	External (RF Pin)	Up to 31	Cut Tape
WGM160PX22KGN2R	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	Included	External (RF Pin)	Up to 31	Reel
WGM160P022KGN2	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	None	External (RF Pin)	Up to 31	Cut Tape
WGM160P022KGN2R	Wi-Fi (802.11 b/g/n)	16 dBm	2048 / 512	None	External (RF Pin)	Up to 31	Reel

Note:

1. WGM160P modules come pre-programmed with the Gecko OS Kernel. Devices ship with the debug interface locked. Devices may be reprogrammed via serial or OTA DFU and preserve the device credentials. Unlocking the debug interface will result in loss of pre-programmed firmware, including Gecko OS Kernel and device credentials.
2. SLWSTK6121A Wireless Starter Kit and SLWRB4321A Radio Board are available to start developing with WGM160P Wi-Fi modules.
3. Devices listed may be referred to by the product family name (WGM160P), model name (WGM160P22A / WGM160P22N) or the full orderable part number throughout this document.

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3. System Overview

3.1 Introduction

The WGM160P module combines the WF200 Wi-Fi transceiver with an EFM32GG11 microcontroller to deliver a complete and certified standalone Wi-Fi solution, with the ability to run customer application on an Cortex M4 processor.

This device supports Gecko OS, a comprehensive software solution that simplifies the Wi-Fi , application and cloud connectivity development process to reduce time to market. For more details on the software platform, please consult our online documentation.

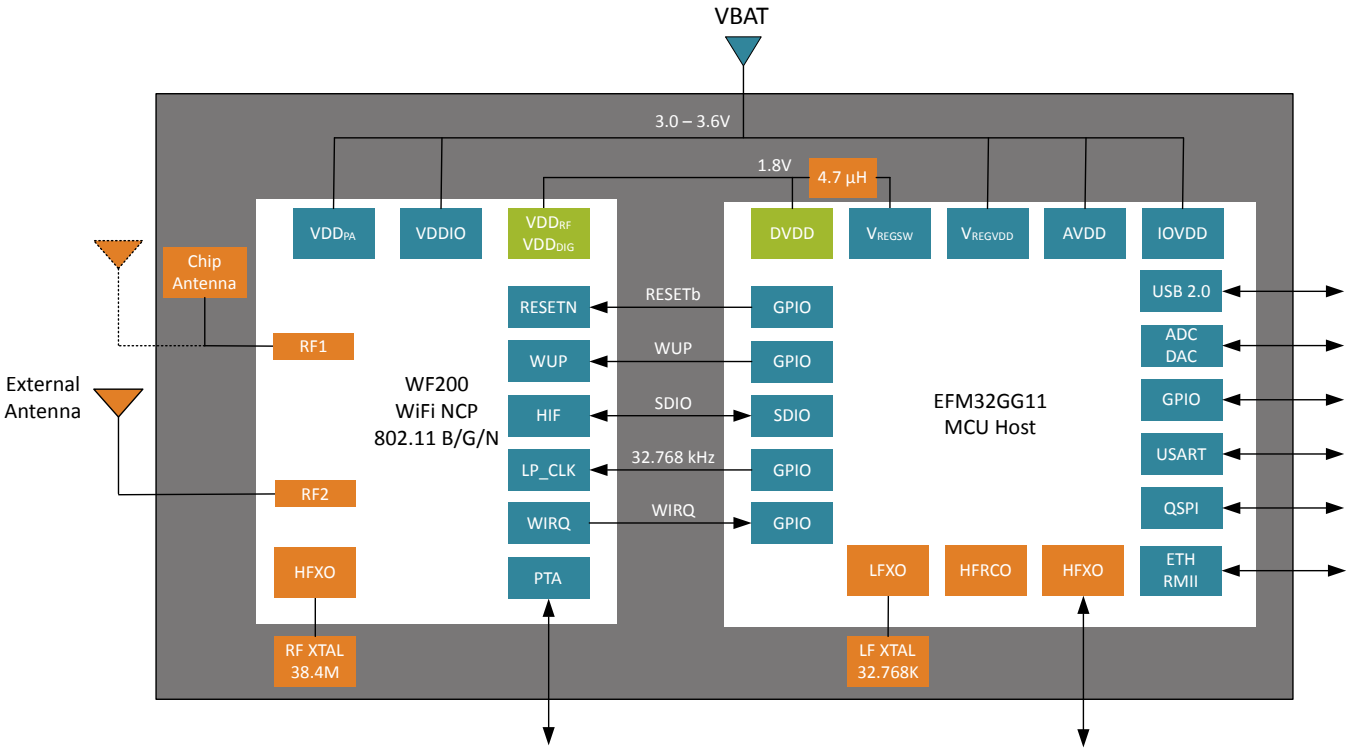


Figure 3.1. WGM160P Block Diagram

3.2 Wi-Fi Supported 2.4 GHz ISM Modulations, BW, and Channels

Table 3.1. Supported Wi-Fi Modulations, BW, and Channels

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Channel Center Frequency	CHAN	Subject to Regulatory Agency	2412	2437	2484	MHz
Channel Bandwidth	BW		—	20	—	MHz

4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB} = 25 °C; V_{VBAT} = 3.3V; Center Frequency = 2,437 MHz.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna port. Conducted RF measurements include additional output power reductions to guarantee WiFi and regulatory emissions compliance while connected to the specified antennas which have non-ideal impedance loading.

Refer to Section 4.2 Operating Conditions for more details about operational supply and temperature limits.

4.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_{STG}		-40	—	105	°C
RF power level at RF1 and RF2 ports	P_{RFMAX}	Max power that can be applied to input of recommended matching network connected to RF1 and RF2 pins.	—	—	10	dBm
Maximum supply voltage to VBAT	$VBAT_{MAX}$		-0.3	—	3.6	V
DC voltage on I/O pins	VG_{MAX}	5 V tolerant GPIO (PF0, PF1, PF10, PF11)[1] [2]	-0.3	—	Min of 5.25 and VBAT +2	V
		All other GPIO and PTA pins	-0.3	—	VBAT + 0.3	V
Current into any GPIO pin	IO_{MAX}		—	—	20	mA
Sum of current into all GPIO pins	IO_{ALLMAX}		—	—	150	mA
Range of load impedance at RF1 and RF2 pins during TX	$LOAD_{TX}$		—	—	10:1	VSWR

Note:

1. When a GPIO is used for analog functions via the APORT, the maximum voltage is VBAT.
2. To operate above the VBAT supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as all other GPIO (max = VBAT + 0.3 V).

4.2 Operating Conditions

Table 4.2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient operating temperature	TA_{OP}		-40	—	85	°C
Nominal supply voltage to VBAT[1]	V_{VBAT}		3.0	3.3	3.6	V

Note:

1. Operating outside of the recommended voltage supply range is not supported. The module may disable WiFi transmit functions when operating outside of this range in order to guarantee regulatory emissions compliance.

4.3 Power Consumption

All currents measured with VBAT = 3.3 V.

Table 4.3. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Continuous TX current, 1 Mbps, max power setting	ITX_{MAX}		—	141.3	—	mA
Continuous TX current, MCS7, max power setting	ITX_{MAX_N}		—	131.4	—	mA
Continuous RX listen current	IRX_{MAX}		—	36.6	—	mA
Continuous RX receive current, 1 Mbps	IRX_{MAXR}		—	34.5	—	mA
Continuous RX receive current, MCS7	IRX_{MAXR_N}		—	38.5	—	mA
Idle associated current, DTIM=1	I_{DTIM1}	UART off	—	TBD	—	mA
Idle associated current, DTIM=3	I_{DTIM3}	UART off	—	TBD	—	mA
Idle associated current, DTIM=10	I_{DTIM10}	UART off	—	TBD	—	mA
Sleep mode current	I_{SLEEP}		—	TBD	—	mA
Idle current average	I_{IDLE}		—	TBD	—	mA

4.4 Digital I/O Specifications

Table 4.4. Digital I/O Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage input high (relative to VBAT)	V_{IH}		70	—	—	%
Voltage input low (relative to VBAT)	V_{IL}		—	—	30	%
Logic low output voltage (relative to VBAT)	V_{OL}	PTA Pins, Sinking 5 mA	—	—	25	%
		GPIO Pins, Sinking 20 mA, DRIVESTRENGTH = STRONG	—	—	20	%
Logic high output voltage (relative to VBAT)	V_{OH}	PTA Pins, Sourcing 5 mA	80	—	—	%
		GPIO Pins, Sourcing 20 mA, DRIVESTRENGTH = STRONG	80	—	—	%
Input leakage current	I_{Leak}	All I/O when GPIO voltage ≤ VBAT	—	1	—	nA
		5 V Tolerant I/O (PF0, PF1, PF10, PF11) when VBAT < GPIO voltage ≤ VBAT + 2 V	—	3.3	15	µA
Pullup resistance	R_{PU}		30	43	65	kΩ
Pulldown resistance	R_{PD}		30	43	65	kΩ
Output fall time from V_{OH} to V_{OL}	T_{OF}	50 pF load	—	15	TBD	ns
Output rise time from V_{OL} to V_{OH}	T_{OR}	50 pF load	—	15	TBD	ns
Required external series resistor on USB D+ and D-	R_{USB}		—	33 +/-10%	—	Ω

4.5 RF Transmitter General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2,437 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made at the 50 Ω Antenna Port. See Section 5.1.1 Antenna Ports. Conducted RF measurements include additional output power reductions to guarantee WiFi and regulatory emissions compliance while connected to the specified antennas which have non-ideal impedance loading.

Table 4.5. RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum RMS Output Power at Antenna (High Power PA)[1] [2]	$POUT_{MAX\_RMS\_HPPA}$	802.11b: 1 Mbps	—	16.1	—	dBm
		802.11b: 11 Mbps	—	15.1	—	dBm
		802.11g: 6 Mbps	—	14.7	—	dBm
		802.11g: 54 Mbps	—	9.1	—	dBm
		802.11n: MCS=0	—	14.4	—	dBm
		802.11n: MCS=7	—	5.8	—	dBm
Carrier frequency error	$CARR_{FREQ\_ERROR}$	Across temperature	-25	—	25	ppm
POUT variation over supply voltage range, relative to nominal 3.3 V	$POUT_{VAR\_V}$	VBAT = 3.0-3.6 V	—	+0.3 / -1.1	—	dB
POUT variation over frequency range, relative to average[2]	$POUT_{VAR\_F}$	CH1 to CH14	—	+/-0.15	—	dB
POUT variation over temperature range, relative to 25C	$POUT_{VAR\_T}$	-40 to +85C	—	+0.1 / -1.2	—	dB

Note:

1. VBAT should be at least 3.0 V to achieve the rated RF transmitter output power levels.
2. Rated power levels may not apply to the edge channels, which may need additional backoff for FCC compliance.

4.6 RF Receiver General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2,437 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made at the 50 Ω Antenna Port. See Section 5.1.1 Antenna Ports.

Table 4.6. RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity for 8% FER (1024 Octet)	$SENS_B$	802.11b: 1 Mbps	—	-96.4	—	dBm
		802.11b: 11 Mbps	—	TBD	—	dBm
RX Sensitivity for 10% PER (1024 Octet)	$SENS_G$	802.11g: 6 Mbps	—	TBD	—	dBm
		802.11g: 54 Mbps	—	TBD	—	dBm
RX Sensitivity for 10% PER (4096 Octet)	$SENSE_N$	802.11n: MCS=0	—	TBD	—	dBm
		802.11n: MCS=7	—	TBD	—	dBm
RX Max Strong Signal for 8% FER (1024 Octet)	RX_{SAT_B}	802.11b: 1 Mbps	—	-4.0	—	dBm
		802.11b: 11 Mbps	—	-10.0	—	dBm
RX Max Strong Signal for 10% PER (1024 Octet)	RX_{SAT_G}	802.11g: 6 Mbps	—	-9.0	—	dBm
		802.11g: 54 Mbps	—	-9.0	—	dBm
RX Max Strong Signal for 10% PER (4096 Octet)	RX_{SAT_N}	802.11n: MCS=0	—	-9.0	—	dBm
		802.11n: MCS=7	—	-9.0	—	dBm
Sensitivity variation across frequency range, CH1 to CH14	$SENS_{VAR\_V}$	802.11b 1 Mbps	—	+/-0.5	—	dB
Sensitivity variation over temperature range, -40 to 85C	$SENS_{VAR\_TEMP}$	802.11b 1 Mbps	—	+/-1.3	—	dB
RX Channel power Indicator Step Size	$RCPI_{STEP}$	802.11b: 1 Mbps	—	0.5	—	dBm

4.7 Radiated Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2437 MHz, using the integrated antenna, and measured with the ideal application board size for 2.4 GHz radiation.

Table 4.7. Radiated Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Application board size, radiated edge "X" dimension[1]	PCB_{X_MM}		35	50	—	mm
Antenna Efficiency	ANT_{EFF}	Optimal application board design	—	-1.4	—	dB

Note:

1. Refer to "UG384: WGM160P Hardware Design Users Guide" for more PCB layout details.

4.8 Microcontroller Peripherals

WGM160P offers an extensive list of peripherals, some of which are listed below:

- 12-bit ADC
- 12-bit DAC
- GPIO
- USART (UART/SPI/I2S)
- QSPI with Execute In Place (XIP) support
- Capacitive Touch Sensing in all GPIOs
- LESENSE
- 10/100 Ethernet MAC with RMII interface (50 MHz external crystal required)
- USB device (2.0 Full speed)
- I^2C peripheral interfaces
- CAN
- Timers
- LCD Driver

For more information on the pins these peripherals are availabile on, please consult: 7.2 GPIO Functionality Table and 7.3 Alternate Functionality Overview.

For details on the electrical performance of these peripherals, please consult the relevant portions of Section 4 in the EFM32GG11 Family Datasheet.

5. Typical Applications and Connections

5.1 RF Connections

5.1.1 Antenna Ports

The WGM160P offers two RF ports that support antenna diversity using an internal switch. In applications with only one antenna, the unused port should be terminated to ground with a 47-51 Ω resistor. Leaving the unused port floating or tying directly to ground will result in degraded performance. An external antenna connected to either RF port needs to be properly matched with at least -10dB return loss (VSWR < 2).

5.1.2 Antenna Diversity

In applications where multipath fading is a potential issue, such as indoors, a second antenna can be connected. A firmware feature can be enabled to automatically determine which of the two antennas gives a better signal, allowing significant improvement in link reliability.

5.2 Multi-Protocol Co-Existance

Packet Transmit Arbitration (PTA) pins are provide to share antenna and optimize co-existence performance with other networks including other protocols. See Application Notes "AN1128 Bluetooth Coexistance with Wi-Fi" and "AN1017 Zigbee and Thread Coexistance with Wi-Fi" for more information.

5.3 Example Schematic

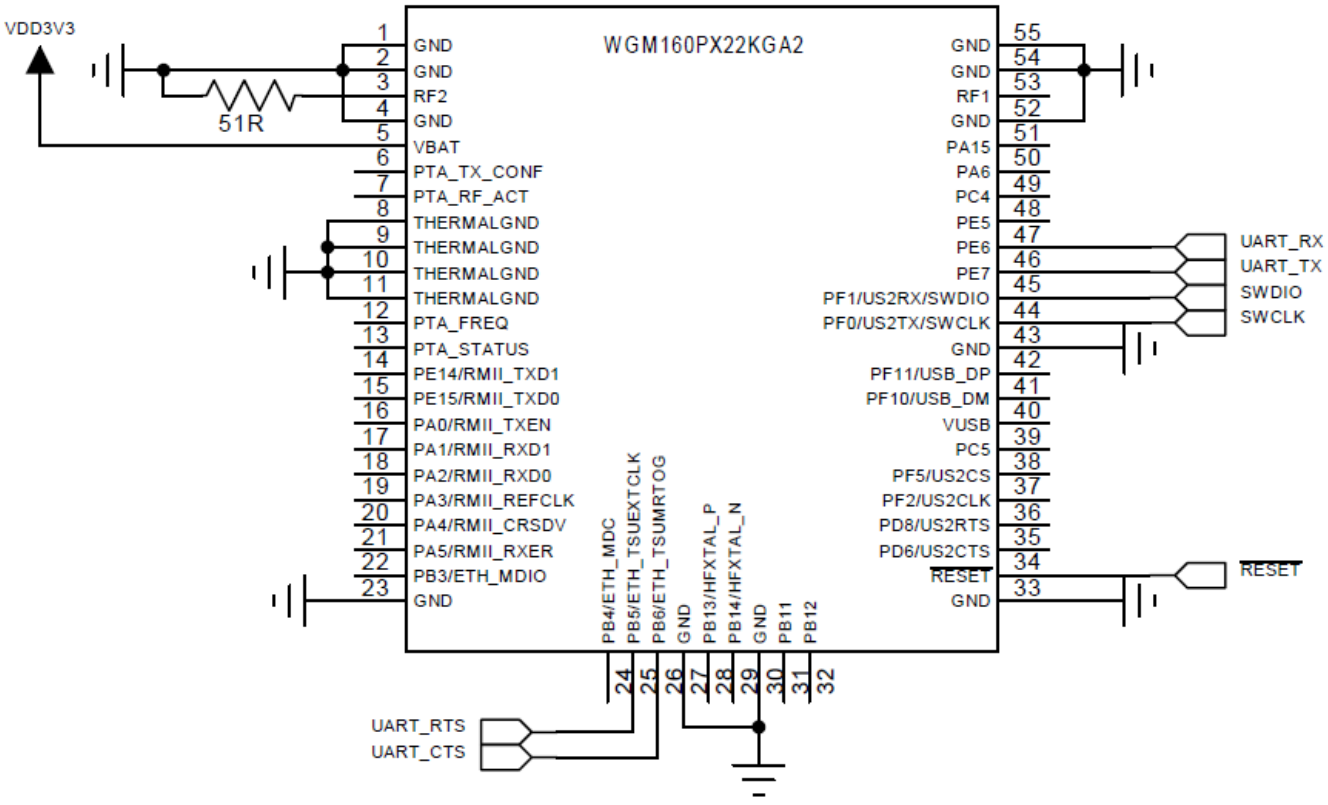


Figure 5.1. Example Schematic for NCP Application

6. Gecko OS Features

The Gecko OS software supplied with the WGM160P provides a wide range of features beyond the underlying hardware, and supports application development via its command API.

For complete documentation of Gecko OS, see https://docs.silabs.com/gecko-os/.

Software APIs

- Gecko OS Command API
- Gecko OS Native C API

Interfaces

- Serial (UART, remote terminal)
- SoftAP and WLAN client (concurrent)
- I2C master
- SPI master

Servers

- TCP/TLS, UDP, HTTP(S), DHCP, DNS
- HTTP(S) Server with RESTful API and Websockets

Clients

- TCP/TLS, UDP, NTP, Secure-SMTP, DHCP, DNS
- HTTP(S) client
- Websocket client

Setup

- Multiple Wi-Fi setup options, including via serial command and Web setup with SoftAP

Peripherals and Sensors

- GPIOs for control, indication and monitoring
- I2C-master API for interfacing to external peripherals
- SPI-master API for interfacing to external peripherals
- Automated broadcast and streaming of sensor data
- Local caching of sensor data

Update and Recovery

- Wireless OTA (Over-the-Air) update to remote manage firmware using the Zentri DMS (Device Management Service)

System Management

- System configuration and monitoring via setting and getting a wide range of variables
- Configurable power states
- Sleep/wake timers

File System

- Read/write file system with appendable log files
- Storage of large files
- Optional additional bulk serial flash
- HTTP download to file system, HTTP upload from file system

7. Pin Descriptions

7.1 WGM160P Device Pinout

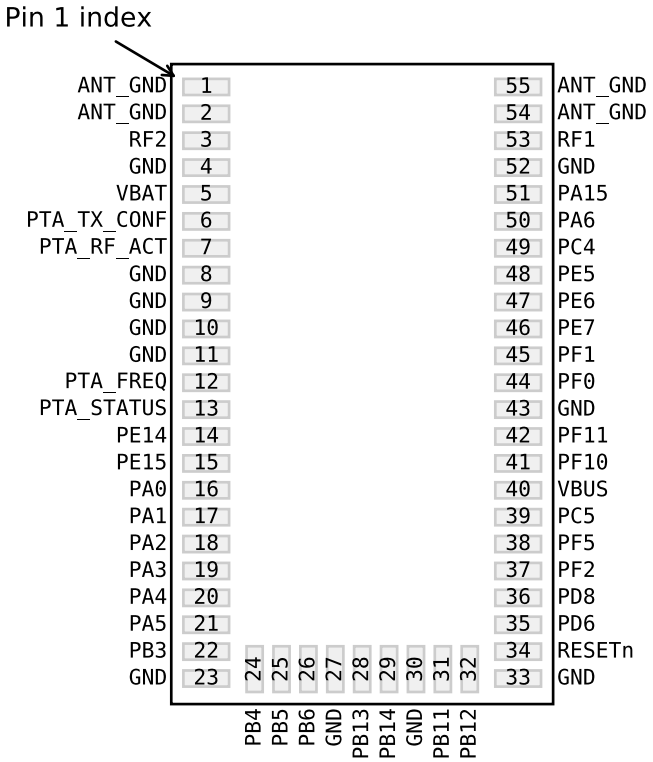


Figure 7.1. WGM160P Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 7.2 GPIO Functionality Table or 7.3 Alternate Functionality Overview.

Table 7.1. WGM160P Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
ANT_GND	1 2 54 55	Antenna ground.	RF2	3	External antenna connection for diversity antenna. Terminate to ground with 47-51 Ohms if not connected to an antenna.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
GND	4 8 9 10 11 23 27 30 33 43 52	Ground. Connect all ground pins to ground plane.	VBAT	5	Module power supply
PTA_TX_CONF	6	PTA TX_CONF pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_RF_ACT	7	PTA RF_ACT pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PTA_FREQ	12	PTA FREQ pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_STATUS	13	PTA STATUS pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PE14	14	GPIO	PE15	15	GPIO
PA0	16	GPIO	PA1	17	GPIO
PA2	18	GPIO	PA3	19	GPIO
PA4	20	GPIO	PA5	21	GPIO
PB3	22	GPIO	PB4	24	GPIO
PB5	25	GPIO	PB6	26	GPIO
PB13	28	GPIO	PB14	29	GPIO
PB11	31	GPIO	PB12	32	GPIO
RESETn	34	Reset input, active low. This pin is internally pulled up to VBAT. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PD6	35	GPIO
PD8	36	GPIO	PF2	37	GPIO
PF5	38	GPIO	PC5	39	GPIO
VBUS	40	USB VBUS signal and auxiliary input to 5 V regulator. May be left disconnected if USB is unused.	PF10	41	GPIO (5V)
PF11	42	GPIO (5V)	PF0	44	GPIO (5V)
PF1	45	GPIO (5V)	PE7	46	GPIO
PE6	47	GPIO	PE5	48	GPIO
PC4	49	GPIO	PA6	50	GPIO
PA15	51	GPIO	RF1	53	External antenna connection on WGM160P22N. Not connected on WGM160P22A.

Note:

1. GPIO with 5V tolerance are indicated by (5V).

7.2 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 7.3 Alternate Functionality Overview for a list of GPIO locations available for each function.

Full peripheral features and flexibility are not supported with all software architectures. In particular, some restrictions apply when using Gecko OS. Refer to “UG384 WGM160P Hardware Design Users Guide” for more details.

Table 7.2. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PA0	BUSBY BUSAX LCD_SEG13	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN US1_RX #5 US3_TX #0 QSPI0_CS0 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 GPIO_EM4WU0
PA1	BUSAY BUSBX LCD_SEG14	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 US3_RX #0 QSPI0_CS1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1
PA2	BUSBY BUSAX LCD_SEG15	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 US1_RX #6 US3_CLK QSPI0_DQ0	CMU_CLK0 #0 PRS_CH8 ETM_TD0 #3
PA3	BUSAY BUSBX LCD_SEG16	TIM0_CDTI0 TIM3_CC0 #5	ETH_RMIIREFCLK US3_CS U0_TX #2 QSPI0_DQ1	CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 ETM_TD1
PA4	BUSBY BUSAX LCD_SEG17	TIM0_CDTI1 TIM3_CC1 #5	ETH_RMIICRSDV US3_CTS #0 U0_RX #2 QSPI0_DQ2	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PA5	BUSAY BUSBX LCD_SEG18	TIM0_CDTI2 #0 TIM3_CC2 #5 PCNT1_S0IN #0	ETH_RMIIRXER US3_RTS U0_CTS QSPI0_DQ3 LEU1_TX #1	LES_ALTEX4 PRS_CH17 #0 ACMP1_O #7 ETM_TD3 #3

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PA6	BUSBY BUSAX LCD_SEG19	TIM3_CC0 #6 WTIM0_CC0 #1 LETIM1_OUT1 #0 PCNT1_S1IN #0	ETH_MDC #3 U0_RTS #2 LEU1_RX #1	PRS_CH6 #0 ACMP0_O #4 ETM_TCLK GPIO_EM4WU1
PA15	BUSAY BUSBX LCD_SEG12	TIM3_CC2 #0	ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MDIO #0 US2_TX #1 US3_TX #2 QSPI0_DQ4	PRS_CH19 #0 ACMP0_O #7
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MDC #0 US2_RX #1 QSPI0_DQ5 LEU1_TX #4	PRS_CH20
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	WTIM0_CC2 #6 LETIM1_OUT0 PCNT0_S0IN #6	ETH_TSUEXTCLK US0_RTS #4 US2_CLK #1 QSPI0_DQ6 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 LETIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG US0_CTS #4 US2_CS #1 QSPI0_DQ7	PRS_CH12 #1
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT IDAC0_OUT	TIM0_CDTI2 #4 TIM1_CC2 WTIM2_CC2 LETIM0_OUT0 #1 PCNT0_S1IN #7 PCNT1_S0IN #6	US0_CTS #5 US1_CLK #5 US2_CS #3 U1_CTS #2 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLKI0 #7 PRS_CH21 #2 ACMP0_O #3 GPIO_EM4WU7
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	TIM1_CC3 #3 WTIM2_CC0 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PB13	BUSAY BUSBX HFXTAL_P	TIM6_CC0 WTIM1_CC0 #0 PCNT2_S0IN #2	US0_CLK #4 US1_CTS LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0
PB14	BUSBY BUSAX HFXTAL_N	TIM6_CC1 WTIM1_CC1 PCNT2_S1IN #2	US0_CS US1_RTS LEU0_RX #1	PRS_CH6 #1
PC4	BUSACMP0Y BUSACMP0X OPA0_P	TIM0_CC0 #5 TIM0_CDTI2 #3 TIM2_CC2 LETIM0_OUT0 #3 PCNT1_S0IN #3	US2_CLK #0 U0_TX #4 U1_CTS #4 I2C1_SDA #0	LES_CH4 PRS_CH18 GPIO_EM4WU6
PC5	BUSACMP0Y BUSACMP0X OPA0_N	TIM0_CC1 #5 LETIM0_OUT1 #3 PCNT1_S1IN #3	US2_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT ADC1_EXTP OPA1_P	TIM1_CC0 #4 TIM6_CC2 WTIM0_CDTI2 WTIM1_CC0 #2 LETIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_ALTEX0 PRS_CH5 ACMP0_O #2 ETM_TD0 #0
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O
PE5	BUSCY BUSDX LCD_COM1	TIM3_CC0 #3 TIM3_CC2 #2 TIM5_CC1 #0 TIM6_CDTI1 WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 U1_RTS #3 I2C0_SCL #7	PRS_CH17 #2
PE6	BUSDY BUSCX LCD_COM2	TIM3_CC1 #3 TIM5_CC2 #0 TIM6_CDTI2 WTIM0_CC2 #0 WTIM1_CC3	US0_RX US3_TX #1	PRS_CH6 #2

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PE7	BUSCY BUSDX LCD_COM3	TIM3_CC2 #3 TIM5_CC0 WTIM1_CC0 #5	US0_TX US3_RX #1	PRS_CH7 #2
PE14	BUSDY BUSCX LCD_SEG10	TIM2_CDTI1 TIM3_CC0 #0	ETH_RMIITXD1 US0_CTS #0 QSPI0_SCLK LEU0_TX #2	PRS_CH13 ETM_TD2 #4
PE15	BUSCY BUSDX LCD_SEG11	TIM2_CDTI2 TIM3_CC1 #0	ETH_RMIITXD0 US0_RTS #0 QSPI0_DQS LEU0_RX #2	PRS_CH14 ETM_TD3 #4
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LETIM0_OUT0 #2	US2_TX #5 CAN0_RX US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LETIM0_OUT1 #2	US2_RX #5 US1_CS U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX US1_TX U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO GPIO_EM4WU4
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 DBG_TDI
PF10	BUSDY BUSCX	TIM5_CC1 #6 WTIM3_CC1 PCNT2_S0IN #3	U1_TX I2C2_SDA USB_DM	
PF11	BUSCY BUSDX	TIM5_CC2 #6 WTIM3_CC2 PCNT2_S1IN #3	U1_RX I2C2_SCL #2 USB_DP	

7.3 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 7.2 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 7.3. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	2: PD6 3: PB11	4: PA6 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2	7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8		Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0		Analog comparator ACMP3, digital output.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
CAN0_RX	1: PF0		CAN0 RX.
CAN0_TX	1: PF2		CAN0 TX.
CMU_CLK0	0: PA2	4: PF2	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8	5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.
CMU_CLKI0	1: PA3 3: PB13	7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2		Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
ETH_MDC	0: PB4 3: PA6		Ethernet Management Data Clock.
ETH_MDIO	0: PB3 3: PA15		Ethernet Management Data I/O.
ETH_RMIICRSDV	0: PA4		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5		Ethernet IEEE1588 External Reference Clock.
ETH_TSUTMR-TOG	0: PB6		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	3: PA6		Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 3: PA2		Embedded Trace Module ETM data 0.
ETM_TD1	3: PA3		Embedded Trace Module ETM data 1.
ETM_TD2	3: PA4	4: PE14	Embedded Trace Module ETM data 2.
ETM_TD3	3: PA5	4: PE15	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
HFXTAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1	5: PF1 7: PE5	I2C0 Serial Clock Line input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
I2C0_SDA	0: PA0 1: PD6	5: PF0	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12	4: PF2	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11		I2C1 Serial Data input / output.
I2C2_SCL	0: PF5 2: PF11		I2C2 Serial Clock Line input / output.
I2C2_SDA	2: PF10		I2C2 Serial Data input / output.
IDAC0_OUT	0: PB11		IDAC0 output.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG10	0: PE14		LCD segment line 10.
LCD_SEG11	0: PE15		LCD segment line 11.
LCD_SEG12	0: PA15		LCD segment line 12.
LCD_SEG13	0: PA0		LCD segment line 13.
LCD_SEG14	0: PA1		LCD segment line 14.
LCD_SEG15	0: PA2		LCD segment line 15.
LCD_SEG16	0: PA3		LCD segment line 16.
LCD_SEG17	0: PA4		LCD segment line 17.
LCD_SEG18	0: PA5		LCD segment line 18.
LCD_SEG19	0: PA6		LCD segment line 19.
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_CH4	0: PC4		LESENSE channel 4.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH5	0: PC5		LESENSE channel 5.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4		Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	1: PB12 2: PF1 3: PC5		Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0		4: PB5	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6	4: PB6	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	1: PB14 2: PE15 3: PF1	4: PA0	LEUART0 Receive input.
LEU0_TX	1: PB13 2: PE14 3: PF0	4: PF2	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	1: PA6	4: PB5	LEUART1 Receive input.
LEU1_TX	1: PA5	4: PB4	LEUART1 Transmit output. Also used as receive input in half duplex communication.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
PCNT0_S0IN	3: PD6	4: PA0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN		4: PA1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 3: PC4	6: PB11	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 3: PC5	6: PB12	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	2: PB13 3: PF10		Pulse Counter PCNT2 input number 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PCNT2_S1IN	2: PB14 3: PF11		Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1		Peripheral Reflex System PRS, channel 1.
PRS_CH2	1: PF5		Peripheral Reflex System PRS, channel 2.
PRS_CH3	3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PB13 2: PE7		Peripheral Reflex System PRS, channel 7.
PRS_CH8	1: PA2		Peripheral Reflex System PRS, channel 8.
PRS_CH9	1: PA3		Peripheral Reflex System PRS, channel 9.
PRS_CH12	1: PB6 2: PD8		Peripheral Reflex System PRS, channel 12.
PRS_CH13	2: PE14		Peripheral Reflex System PRS, channel 13.
PRS_CH14	2: PE15		Peripheral Reflex System PRS, channel 14.
PRS_CH15	0: PA15 2: PF0		Peripheral Reflex System PRS, channel 15.
PRS_CH16	0: PA4 1: PB12		Peripheral Reflex System PRS, channel 16.
PRS_CH17	0: PA5 2: PE5		Peripheral Reflex System PRS, channel 17.
PRS_CH18	2: PC4		Peripheral Reflex System PRS, channel 18.
PRS_CH19	0: PB3 2: PC5		Peripheral Reflex System PRS, channel 19.
PRS_CH20	0: PB4		Peripheral Reflex System PRS, channel 20.
PRS_CH21	0: PB5 2: PB11		Peripheral Reflex System PRS, channel 21.
QSPI0_CS0	1: PA0		Quad SPI 0 Chip Select 0.
QSPI0_CS1	1: PA1		Quad SPI 0 Chip Select 1.
QSPI0_DQ0	1: PA2		Quad SPI 0 Data 0.
QSPI0_DQ1	1: PA3		Quad SPI 0 Data 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ2	1: PA4		Quad SPI 0 Data 2.
QSPI0_DQ3	1: PA5		Quad SPI 0 Data 3.
QSPI0_DQ4	1: PB3		Quad SPI 0 Data 4.
QSPI0_DQ5	1: PB4		Quad SPI 0 Data 5.
QSPI0_DQ6	1: PB5		Quad SPI 0 Data 6.
QSPI0_DQ7	1: PB6		Quad SPI 0 Data 7.
QSPI0_DQS	1: PE15		Quad SPI 0 Data S.
QSPI0_SCLK	1: PE14		Quad SPI 0 Serial Clock.
TIM0_CC0	0: PA0 3: PB6	4: PF0 5: PC4 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1	4: PF1 5: PC5 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2	4: PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3		Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4		Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0		4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.
TIM1_CC2	3: PB11		Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	2: PB3 3: PB12	6: PF5	Timer 1 Capture Compare input / output channel 3.
TIM2_CC0	3: PF2	4: PB6	Timer 2 Capture Compare input / output channel 0.
TIM2_CC2		5: PC4	Timer 2 Capture Compare input / output channel 2.
TIM2_CDTI1	2: PE14		Timer 2 Complimentary Dead Time Insertion channel 1.
TIM2_CDTI2	2: PE15		Timer 2 Complimentary Dead Time Insertion channel 2.
TIM3_CC0	0: PE14 3: PE5	4: PA0 5: PA3 6: PA6	Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	0: PE15 3: PE6	4: PA1 5: PA4	Timer 3 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM3_CC2	0: PA15 2: PE5 3: PE7	4: PA2 5: PA5	Timer 3 Capture Compare input / output channel 2.
TIM4_CC0	2: PF5		Timer 4 Capture Compare input / output channel 0.
TIM5_CC0	1: PE7		Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5	6: PF10	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6	6: PF11	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0		5: PB13	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1		5: PB14	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2		7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI1	2: PE5		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	2: PE6		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	2: PA5		UART0 Clear To Send hardware flow control input.
U0_RTS	2: PA6	5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	2: PA4	4: PC5 5: PF2	UART0 Receive input.
U0_TX	2: PA3	4: PC4 5: PF1	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	2: PB11	4: PC4	UART1 Clear To Send hardware flow control input.
U1_RTS	2: PB12 3: PE5	4: PC5	UART1 Request To Send hardware flow control output.
U1_RX	1: PF11		UART1 Receive input.
U1_TX	1: PF10		UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	1: PE5	4: PB13	USART0 clock input / output.
US0_CS		4: PB14	USART0 chip select input / output.
US0_CTS	0: PE14	4: PB6 5: PB11	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15	4: PB5 5: PD6	USART0 Request To Send hardware flow control output.
US0_RX	1: PE6		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	1: PE7		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	2: PF0	5: PB11 6: PE5	USART1 clock input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CS	2: PF1		USART1 chip select input / output.
US1_CTS		5: PB13	USART1 Clear To Send hardware flow control input.
US1_RTS		5: PB14	USART1 Request To Send hardware flow control output.
US1_RX	2: PD6	5: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
		6: PA2	
US1_TX		5: PF2	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 3: PA15	5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 3: PB11	5: PF5	USART2 chip select input / output.
US2_CTS	1: PB12	5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS		5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	1: PB4	5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	1: PB3	5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2		USART3 clock input / output.
US3_CS	0: PA3		USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6		USART3 Clear To Send hardware flow control input.
US3_RTS	0: PA5		USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7		USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3		USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
WTIM0_CC0	1: PA6	6: PB3	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5	4: PF0 6: PB4	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PE6	4: PF1 6: PB5	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI2		4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 2: PD6	5: PE7	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14		Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3		4: PE6	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	3: PB12		Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC2	2: PB11		Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0		6: PB6	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	3: PF10		Wide timer 3 Capture Compare input / output channel 1.
WTIM3_CC2	3: PF11		Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 7.4. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3	High Speed
CMU_CLKI0	1: PA3	High Speed
ETH_RMIICRSDV	0: PA4	High Speed
ETH_RMIIREFCLK	0: PA3	High Speed
ETH_RMIIRXD0	0: PA2	High Speed
ETH_RMIIRXD1	0: PA1	High Speed
ETH_RMIIRXER	0: PA5	High Speed
ETH_RMIITXD0	0: PE15	High Speed
ETH_RMIITXD1	0: PE14	High Speed

Alternate Functionality	Location	Priority
ETH_RMIITXEN	0: PA0	High Speed
TIM0_CC0	3: PB6	Non-interference
US2_CLK	5: PF2	High Speed
US2_CS	5: PF5	High Speed
US2_RX	5: PF1	High Speed
US2_TX	5: PF0	High Speed

8. Package Specifications

8.1 Package Outline

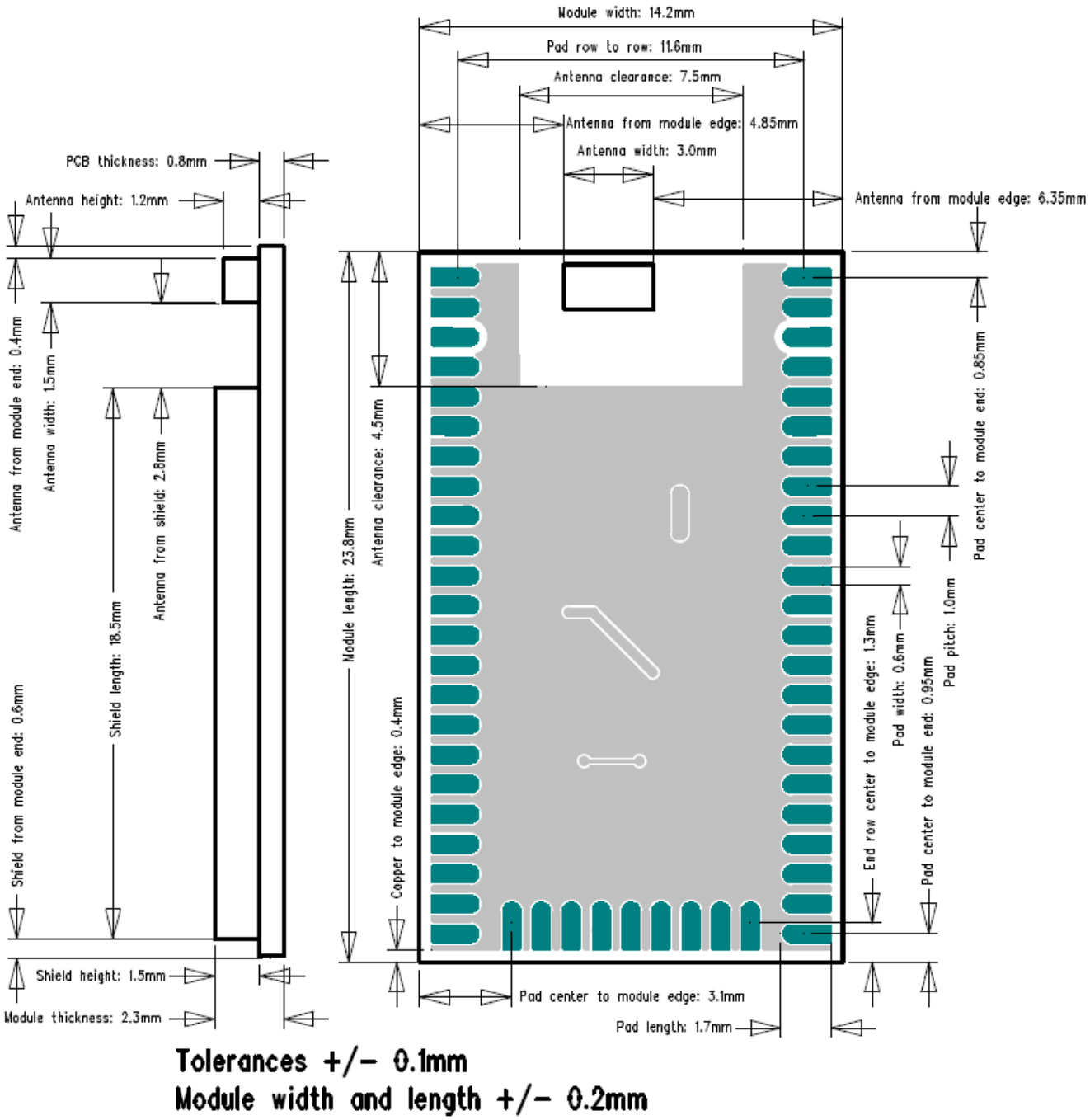


Figure 8.1. WGM160P Package Outline

8.2 Recommended PCB Land Patterns

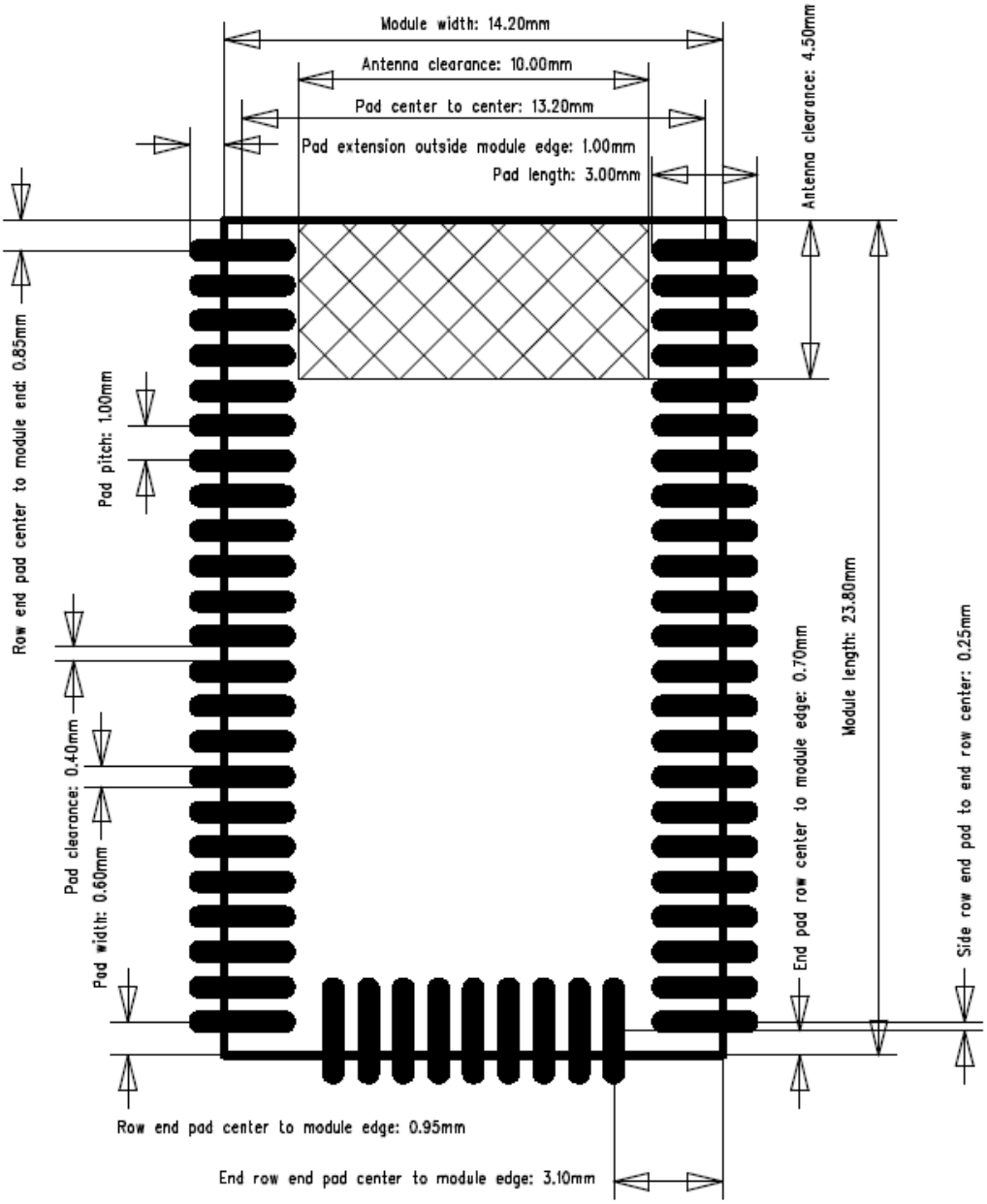


Figure 8.2. WGM160P22A Land Pattern

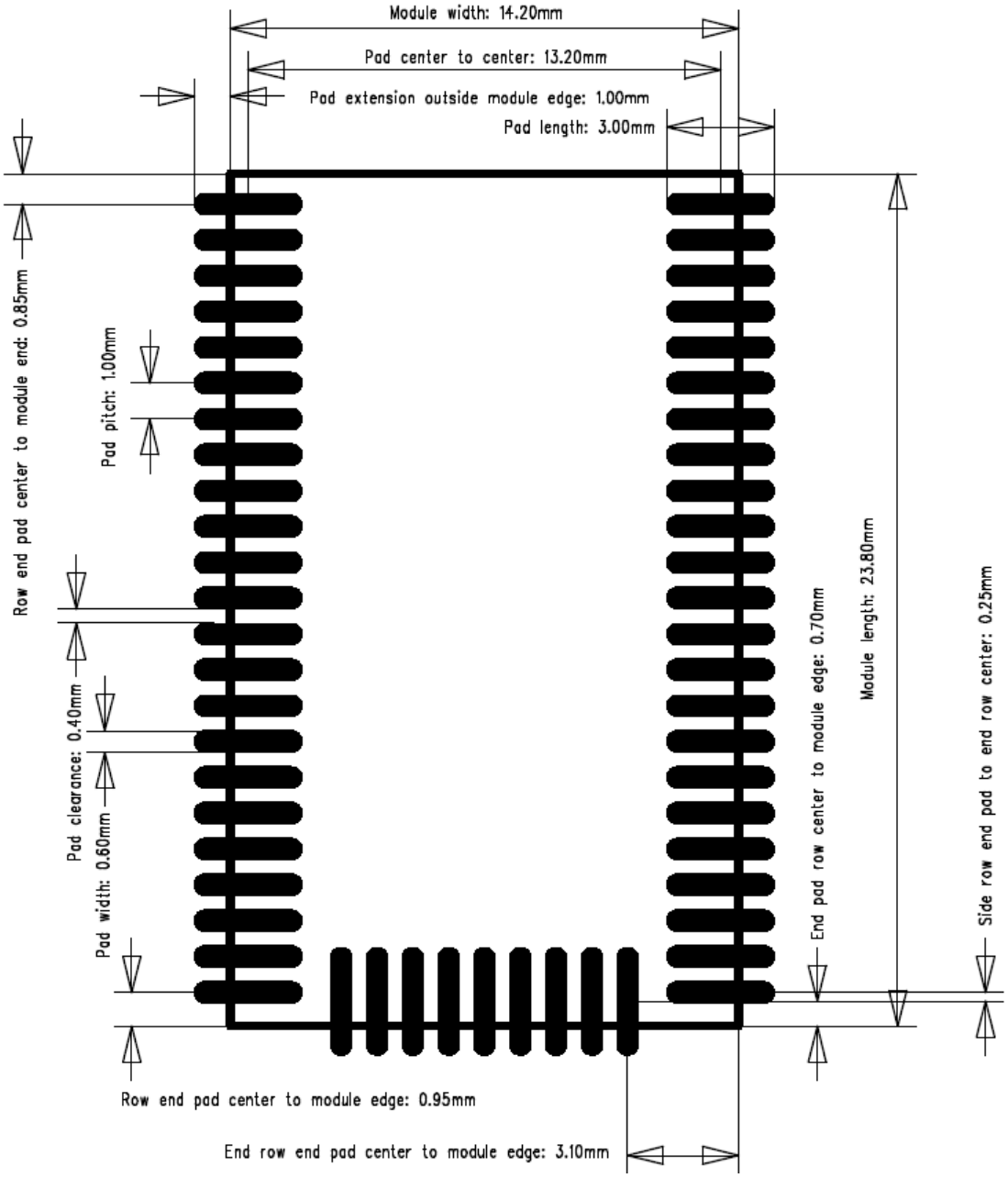


Figure 8.3. WGM160P22N Land Pattern

8.3 Package Marking

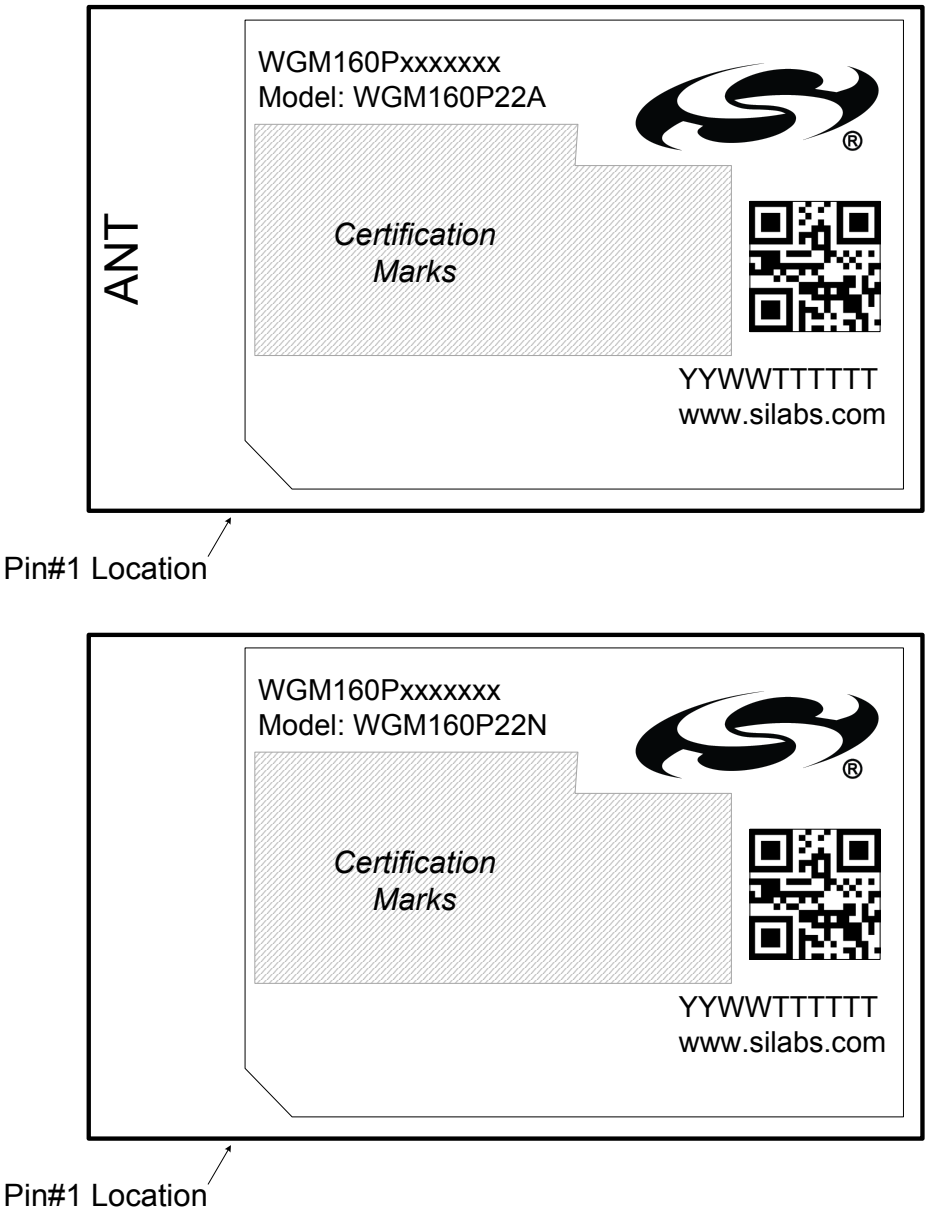


Figure 8.4. Package Marking

The package marking consists of:

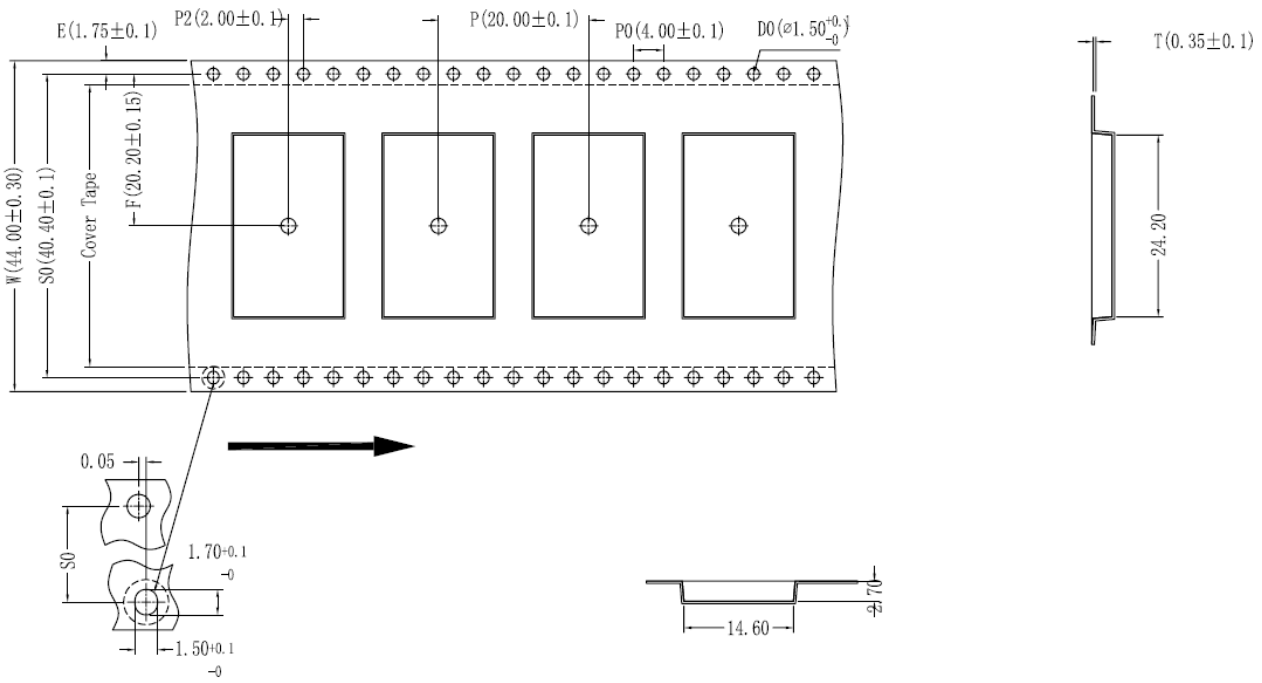
- WGM160Pxxxxxxx - Part number designation
- Model: WGM160Pxxx - Model number designation
- Certification Marks - All certification marks will be printed in this area according to regulatory body requirements.
- QR Code: YYWWMMABCDE
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first letter is the device revision.

9. Soldering Recommendations

The WGM160P is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

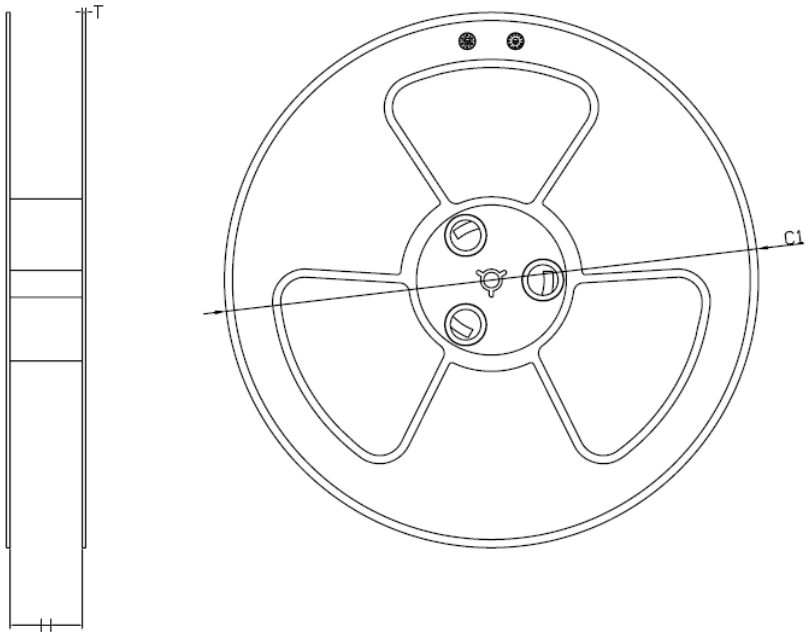
- Refer to technical documentations of particular solder paste for profile configurations.
- Avoid using more than two reflow cycles.
- Aperture size of the stencil should be 1:1 with the pad size.
- A no-clean, type-3 solder paste is recommended.
- For further recommendation, please refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.
- Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

10. Tape and Reel Dimensions



All dimensions in mm unless otherwise indicated.

Figure 10.1. Carrier Tape Dimensions



spec	13″
c1±1	ϕ330
A±0.2	2.6
B±0.2	10.8
T±0.2	2.2
H±0.5	44.5

All dimensions in mm unless otherwise indicated.

Figure 10.2. Reel Dimensions

11. Certifications

This section details certification status of the module in various regions.

The manufacturer address for the modules is:

SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

11.1 Qualified External Antenna Types

This device has been certified with an integrated chip antenna as well as external antennas connected to either RF port or both. The required antenna impedance is 50 Ω.

Table 11.1. Qualified Antennas for WGM160P

Antenna Type	Maximum Gain
Connectorized Coaxial Dipole	2.14 dBi

Any antenna that is of the same general type and of equal or less directional gain as listed in the above table can be used without a need for retesting in the regulatory areas that have a full modular radio approval (USA, Canada, Korea, Japan). In countries applying the ETSI standards, like the EU countries, the radiated emissions are always tested with the end-product and the antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

If an antenna of a different type (such as a chip antenna, a PCB trace antenna or a patch) with a gain less than or equal to 2.14 dBi is needed, it can be added as a permissive change, requiring some radiated emission testing. Antenna types with more gain than 2.14 dBi may require a fully new certification. Since the exact permissive change procedure is chosen on a case by case basis, please consult your test house, for example while performing with them the EMC testing of the end-product.

11.2 CE

The WGM160P22A and WGM160P22N module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU). Please note that every application using the WGM160P22A and WGM160P22N will need to perform the radio EMC tests on the end product, according to EN 301 489-17. It is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product. The specific product assembly may have an impact to RF radiated characteristics, and manufacturers should carefully consider RF radiated testing with the end-product assembly. A formal Declaration of Conformity (DoC) is available via https://www.silabs.com/products/wireless/wi-fi/wgm160p-wifi-module.

11.3 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations:

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

- With WGM160P22A and WGM160P22N the antenna(s) must be installed such that a minimum separation distance of 40 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

Important Note:

In the event that these conditions cannot be met, then for the FCC authorization to remain valid the final product will have to undergo additional testing to evaluate the RF exposure, and a permissive change will have to be applied with the help of the customer's own Telecommunication Certification Body.

End Product Labeling

The variants of WGM160P Modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQWGM160P"

Or

"Contains FCC ID: QOQWGM160P"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

Class B device notice:

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help.

11.4 ISED Canada

ISED

This radio transmitter (IC: 5123A-WGM160P) has been approved by Industry Canada to operate with the antenna types listed above, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

This device complies with ISED license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The models WGM160P22A and WGM160P22N meet the given exemption requirements when the minimum separation distance to human body is 40 mm.

In other words, RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR when using the module at its highest transmission power.

OEM Responsibilities to comply with IC Regulations

The WGM160P modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE

In the event that these conditions cannot be met, then for the ISED authorization to remain valid the final product will have to undergo additional testing to evaluate the RF exposure, and a permissive change will have to be applied with the help of the customer's own Telecommunication Certification Body.

End Product Labeling

The WGM160P module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 5123A-WGM160P** ”

or

“**Contains IC: 5123A-WGM160P”**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

CAN ICES-003 (B):

This Class B digital apparatus complies with Canadian ICES-003

ISED (Français)

Industrie Canada a approuvé l'utilisation de cet émetteur radio (IC: 5123A-WGM160P) en conjonction avec des antennes de type dipolaire à 2.14dBi ou des antennes embarquées, intégrée au produit. L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industrie Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d'interférences.
2. Ce composant doit pouvoir est soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Les modules WGM160P22A and WGM160P22N répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 40 mm.

La déclaration d'exposition RF ou l'évaluation SAR n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus. Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procédé à une évaluation SAR.

Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module WGM160P a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n'est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

REMARQUE IMPORTANTE

ans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation ISED n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d'une autorisation ISED distincte.

Étiquetage des produits finis

Les modules WGM160P sont étiquetés avec leur propre ID IC. Si l'ID IC n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaitre les référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

"**Contient le module transmetteur: 5123A-WGM160P** "

or

"**Contient le circuit: 5123A-WGM160P"**

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

11.5 Locating the Module Close to Human Body

When using the module in an application where the radio is located close to human body, the human RF exposure must be evaluated. FCC, IC, and CE all have different standards for evaluating the RF exposure, and because of this, each standard will require a different minimum separation distance between the module and human body. Certification of WGM160P allows for the minimum separation distances detailed in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 41 in portable use cases (less than 20 cm from human body). The module is approved for the mobile use case (more than 20 cm) without any need for RF exposure evaluation.

Table 11.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	WGM160P with integrated antenna	WGM160P with external reference dipole antenna
FCC	40 mm	40 mm
ISED	30 mm	40 mm
CE	The RF exposure must always be evaluated using the end-product when transmitting with power levels higher than 20 mW = 13 dBm.	

For FCC and ISED, using the module in end products where the separation distance is smaller than those listed above is allowed but requires evaluation of the RF exposure in the final assembly and applying for a *Class 2 Permissive Change* or *Change of ID* to be applied to the existing FCC/ISED approvals of the module. For CE, RF exposure must be evaluated using the end-product in all cases.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus reducing range.

12. Revision History

Revision 0.3

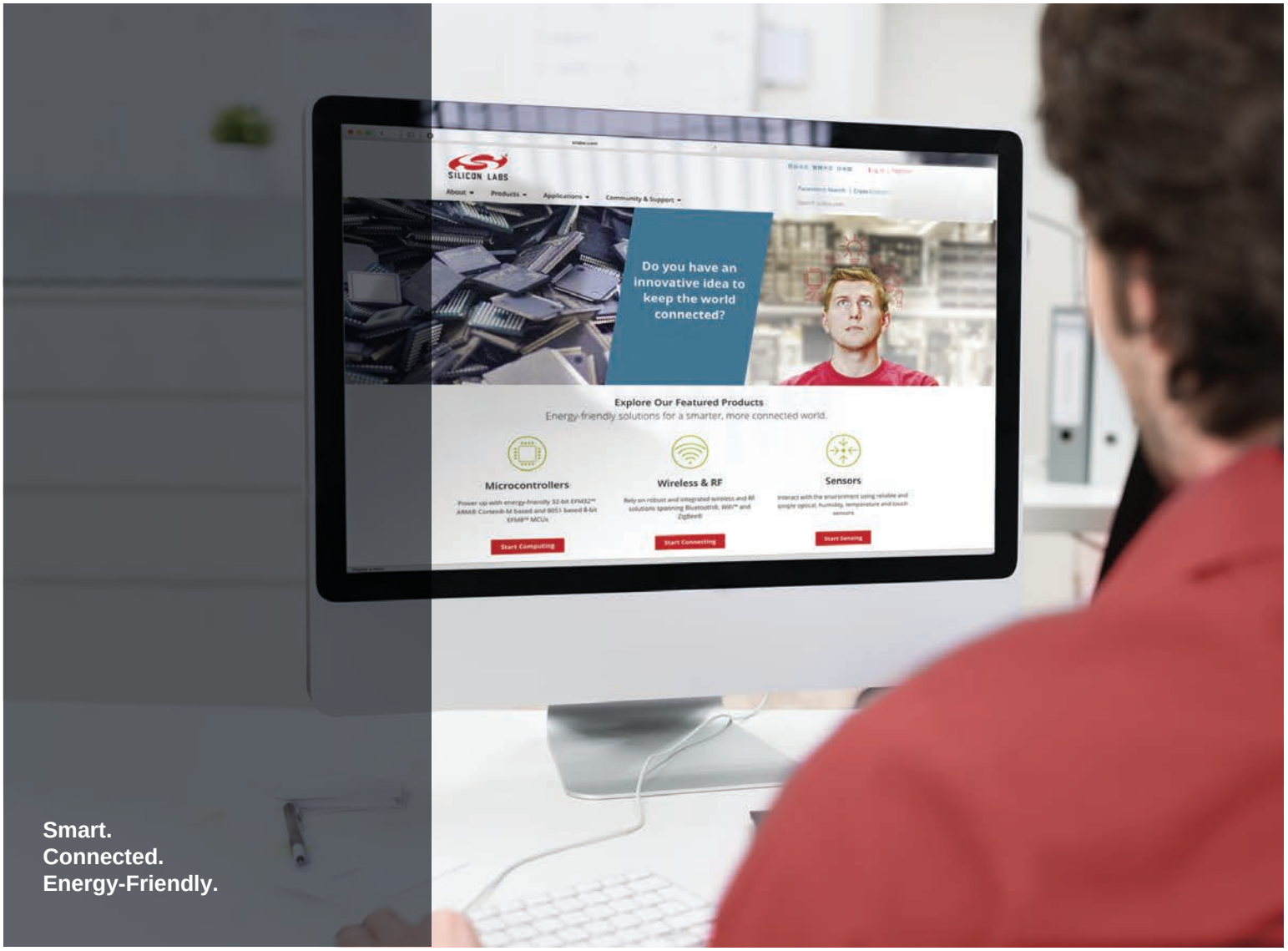
Feb 2019

- Updated top-level device details throughout document.
- Removed software details from 1. Key Features (moved to 6. Gecko OS Features).
- Updated 2. Ordering Information to expand all OPN details.
- Corrected details in Figure 3.1 WGM160P Block Diagram on page 6.
- Updated all tables in 4. Electrical Specifications with latest nomenclature and characterization data.
- Added 5.3 Example Schematic.
- Added 6. Gecko OS Features.
- Updated pinout details in 7. Pin Descriptions.
- Removed functions not pinned out from 7.2 GPIO Functionality Table and 7.3 Alternate Functionality Overview.
- Updated 8. Package Specifications with additional landing diagram and package marking details.
- Added 9. Soldering Recommendations.
- Added 10. Tape and Reel Dimensions.
- Added 11. Certifications.

Revision 0.2

November 2018

- Initial release.



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<ug384>: WGM160P Hardware Design User's Guide

The purpose of this guide is to help users design WiFi applications using WGM160P.

This guide includes information for schematics and layout. Some options available with WGM160P hardware are not available with all software architectures, so the pin features versus software are detailed.

KEY FEATURES

- Schematics guidelines
- Package information
- Layout guideline

1 Table of Content

Contents

2 WGM160P Pinout

WGM160P is a 23.8 mm x 14.2 mm x 2.2mm PCB module.

The diagram below describes pinout (top view)

As shown below, insert Figure 7.1 WGM160 Device Pinout from WGM160P Data Sheet

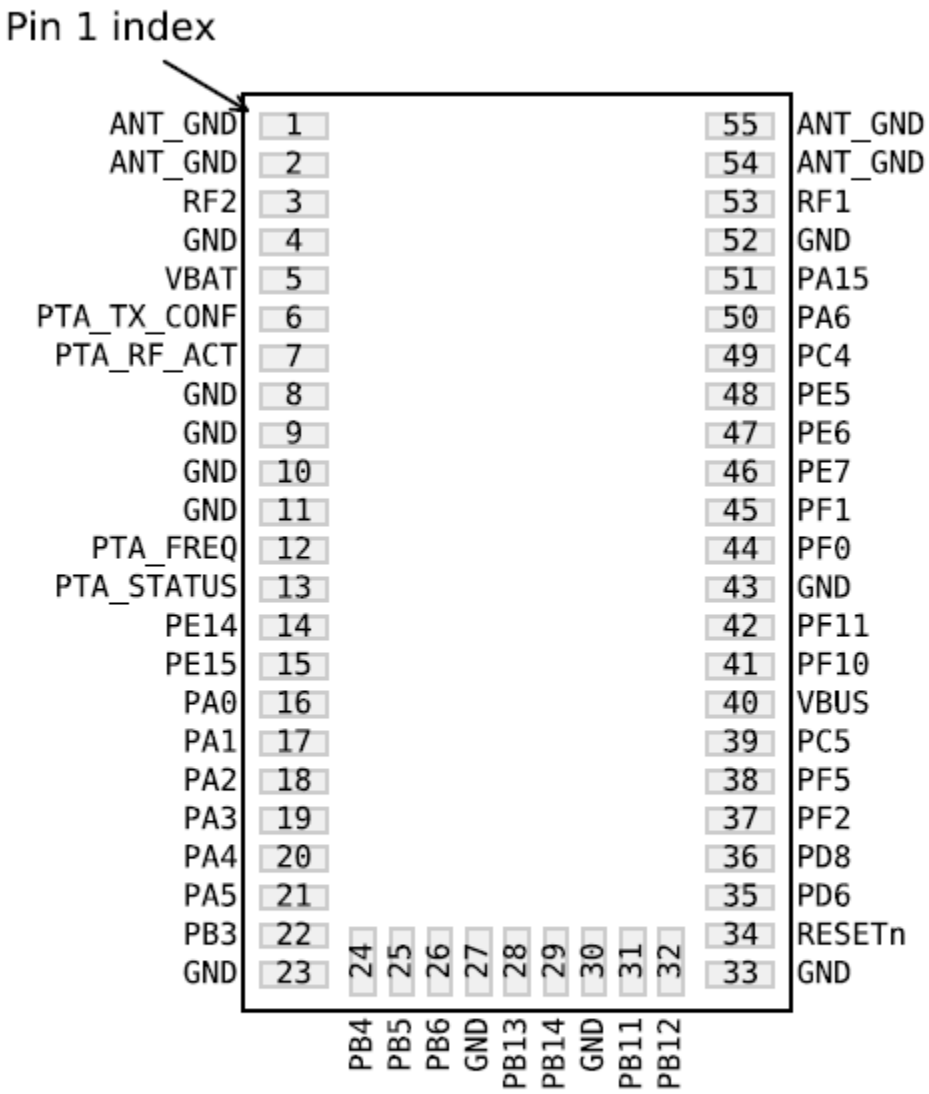

Figure 2.1 WGM160P Device Pinout

3 WGM160P pin description

3.1 Pins table

As shown below, insert Table 7.1 WGM160 Device Pinout from WGM160P Data Sheet

Table 3.1 WGM160P Pin Description

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
ANT_GND	1 2 54 55	Antenna ground.	RF2	3	External antenna connection for diversity antenna. Terminate to ground with 47-51 Ohms if not connected to an antenna.
GND	4 8 9 10 11 23 27 30 33 43 52	Ground. Connect all ground pins to ground plane.	VBAT	5	Module power supply
PTA_TX_CONF	6	PTA TX_CONF pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_RF_ACT	7	PTA RF_ACT pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PTA_FREQ	12	PTA FREQ pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_STATUS	13	PTA STATUS pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PE14	14	GPIO	PE15	15	GPIO
PA0	16	GPIO	PA1	17	GPIO
PA2	18	GPIO	PA3	19	GPIO
PA4	20	GPIO	PA5	21	GPIO
PB3	22	GPIO	PB4	24	GPIO
PB5	25	GPIO	PB6	26	GPIO
PB13	28	GPIO	PB14	29	GPIO
PB11	31	GPIO	PB12	32	GPIO
RESETn	34	Reset input, active low. This pin is internally pulled up to VBAT. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PD6	35	GPIO
PD8	36	GPIO	PF2	37	GPIO
PF5	38	GPIO	PC5	39	GPIO
VBUS	40	USB VBUS signal and auxiliary input to 5 V regulator. May be left disconnected if USB is unused.	PF10	41	GPIO (5V)
PF11	42	GPIO (5V)	PF0	44	GPIO (5V)
PF1	45	GPIO (5V)	PE7	46	GPIO
PE6	47	GPIO	PE5	48	GPIO
PC4	49	GPIO	PA6	50	GPIO
PA15	51	GPIO	RF1	53	External antenna connection on WGM160P22N. Not connected on WGM160P22A.

Note:
1. GPIO with 5V tolerance are indicated by (5V).

3.2 Power pin

The WGM160P module is supplied through VBAT pin. There is no need for external bypass capacitors as ICs decoupling is performed within the module. Note that although VBAT supply is variable, the maximum TX output power can be achieved only when supply is set to 3.3V or above.

Note that pin VBUS cannot be used to supply the module.

3.3 RESETn pin

WGM160P module is reset by driving the RESETn pin low. A weak internal pull-up resistor holds the RESETn pin high, allowing it to be left unconnected if no external reset source is required.

Note that when WGM160P is not powered, RESETn must not be connected to an active supply through an external pull-up resistor as this could damage the device.

Note also that WGM160P features Power On Reset to keep WGM160P in reset mode until VBAT is high enough. For more details, refer to MCU EFM32GG11 reference manual.

3.4 RF pins

The WGM160P module is available with 2 RF configurations.

Table 3.2 WGM160P RF Configuration

Part numbers	RF1	RF2
WGM160PX22KGA2 WGM160P022KGA2	Internal antenna. Pin RF1 is not connected.	RF port
WGM160PX22KGN2 WGM160P022KGN2	RF port	RF port

RF ports are internally matched to 50 Ohms. It is recommended to connect any unused RF port to ground through a 50 Ohms resistor. Any of the RF ports can be used in a similar way. However, performance obtained on RF1 is slightly better, so it is preferable to use this one.

Only one RF port is active at a given time, but the module can also achieve antenna diversity if the application requires it. Port selection and antenna diversity enablement are achieved through software configuration.

3.5 Clocks

The WGM160P module is available with 2 clock configurations.

Table 3.3 WGM160P Low Power Clock Configuration

Part numbers	Low Frequency Crystal
WGM160PX22KGA2 WGM160PX22KGN2	Internal 32.768kHz crystal
WGM160P022KGA2 WGM160P022KGN2	No crystal

A 32.768kHz clock source is required to enable the lowest power operation in WiFi power save modes. 32.768kHz can be generated either using internal Low Frequency RC oscillator or using internal crystal. As the frequency tolerance of this clock affects wake-up scheduling, power consumption in DTIM modes is optimized when using WGM160P with integrated 32.768kHz crystal.

For WGM160P applications requiring Ethernet, a 50MHz reference clock is required. This can be achieved either by connecting 50MHz external clock to module pin PB13 or by connecting a 50MHz crystal oscillator between pins PB13 (HFXTAL_P) and PB14 (HFXTAL_N).

As shown below, insert Table 4.13 High Frequency Crystal Oscillator of EFM32GG11 datasheet

Table 3.4 WGM160P 50MHz High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	No clock doubling	4	—	50	MHz
		Clock doubler enabled	4	—	25	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	50 MHz crystal	—	—	50	Ω
		24 MHz crystal	—	—	150	Ω
		4 MHz crystal	—	—	180	Ω
Nominal on-chip tuning cap range[1]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	8.7	—	51.7	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.084	—	pF
Startup time	t_{HFXO}	50 MHz crystal, ESR = 50 Ohm, C_L = 8 pF	—	350	—	µs
		24 MHz crystal, ESR = 150 Ohm, C_L = 6 pF	—	700	—	µs
		4 MHz crystal, ESR = 180 Ohm, C_L = 18 pF	—	3	—	ms
Current consumption after startup	I_{HFXO}	50 MHz crystal	—	880	—	µA
		24 MHz crystal	—	420	—	µA
		4 MHz crystal	—	80	—	µA

Note:

1. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

3.6 PTA pins

In case a RF transceiver using the same 2.4 GHz band (e.g. Bluetooth) is located next to WGM160P, Packet Transfer Arbitration (PTA) interface can be used to avoid mutual interference. In this case, PTA pins are connected to the other transceiver. PTA interface is highly programmable and can use 1, 2, 3, or 4 pins upon configuration. Depending on manufacturer, PTA signal names can vary so the table below shows the alternative naming.

Table 3.5 WGM160P PTA Configuration

WGM160P Pin #	WGM160P Pin name	Alternative naming
6	PTA_TX_CONF	GRANT
7	PTA_RF_ACT	REQUEST
13	PTA_STATUS	PRIORITY
12	PTA_FREQ	RHO

PTA interface configuration is achieved through software configuration. PTA operation will be detailed in an upcoming application note.

3.7 Multifunction pins

The multifunction pins refer to WGM160P pins directly connected to the embedded MCU EFM32GG11.

3.7.1 Software architecture consideration

The WGM160P module has a lot of flexibility regarding configuration of these MCU pins, as described in the data sheet, but all software architectures do not support all functions.

3.7.1.1 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.
WGM160P pin 44 (GG11 PF0) and pin 45 (GG11 PF1) provide respectively TX and RX access to bootloader.

3.7.1.2 Implementation with GG11 open software

Full flexibility can be achieved when using the source software based on the Full MAC driver provided by Silicon Labs. The configuration of multifunction pins is achieved within Simplicity Studio similarly to a software development for EFM32GG11. For more details regarding these pins, refer to tables 6.2 and 6.3 of WGM160P datasheet.

3.7.1.3 Implementation with Gecko OS

The table below provides the details on the various multifunction pin features supported through Gecko OS 4.0. Features such as SPI slave and USB will be supported in future release of Gecko OS.

Table 3.6 WGM160P Multifunction Pin Configuration With GeckoOS

WGM160P Pin	GG11 Port	Default Function	GPIO[1] (GOS_ GPIO_x)	UART[2] (GOS_ UART_x)	SPI[3] (GOS_ SPI_x)	I2C (GOS_ I2C_x)	ADC (GOS_ ADC_x)	PWM (GOS_ PWM_x)	Ethernet (RMII)
14	PE14	GPIO	0				0	0	TXD1
15	PE15	GPIO	1				-	1	TXD0
16	PA0	SPI Master MOSI	2		SPI0 MOSI		6	2	TXEN
17	PA1	SPI Master MISO	3		SPI0 MISO		-	3	RXD1
18	PA2	SPI Master CLK	4		SPI0 CLK		10	4	RXD0
19	PA3	GPIO	5				-	5	REFCLK
20	PA4	GPIO	6				11	6	CRSDV
21	PA5	GPIO	7				-	7	RXER
22	PB3	Bulk sflash MOSI or [4] UART TX (logging)	8	UART1 TX	SPI1 MOSI		-	8	

[1] The prefix _x in GOS_GPIO_x is replaced with the numbers in the column: GOS_GPIO_1, GOS_GPIO_2, etc. SDK have all those symbols defined in header files.

[2] all UART IO's are relevant to WGM160P, so when RX is used it means WGM160P receives, and TX means WGM160P transmits.

[3] SPI can be configured as master or slave. At the moment, only SPI master is supported in Gecko OS. SPI slave is coming in a future release. SPI interface does not define fixed SPI_CS pin. CS is configurable and any unused GPIO can be used for this function.

[4] PB3 and PB4 showing 2 default functions means that those pins can be assigned using Gecko OS command API (variables and command) to one of those functions. For example, "`set bus.data_bus uart1`" or "`set system.bflash.port spi1`". Once one of these variables is assigned, the other one will give an error that pins are already in use. UART (logging) is used to print Gecko OS log messages: https://docs.silabs.com/gecko-os/4/standard/latest/cmd/variables/bus#bus-log-bus

WGM160P Pin	GG11 Port	Default Function	GPIO[1] (GOS_ GPIO_x)	UART[2] (GOS_ UART_x)	SPI[3] (GOS_ SPI_x)	I2C (GOS_ I2C_x)	ADC (GOS_ ADC_x)	PWM (GOS_ PWM_x)	Ethernet (RMII)
24	PB4	Bulk sflash MISO or [4] UART RX (logging)	9	UART1 RX	SPI1 MISO		12	9	
25	PB5	UART RTS (Commands)	10	UART0 RTS			-	10	
26	PB6	UART CTS (Commands)	11	UART0 CTS			1	11	
28	PB13	GPIO	12				-	-	
29	PB14	GPIO	13				2	-	
31	PB11	I2C Master SDA	14			I2C0 SDA	-	12	
32	PB12	I2C Master SCL	15			I2C0 SCL	3	13	
35	PD6	Factory Reset[5] GPIO	16	UART1 CTS			4	14	
36	PD8	GPIO	17	UART1 RTS			-	15	
37	PF2	GPIO	18				5	16	
38	PF5	GPIO	19				-	17	
39	PC5	GPIO	20				-	18	
41	PF10	USB DM	21				7	-	
42	PF11	USB DP	22				-	-	
46	PE7	UART TX (Commands)	23	UART0 TX			-	19	
47	PE6	UART RX (Commands)	24	UART0 RX			8	20	
48	PE5	GPIO	25				-	21	
49	PC4	Bulk sflash SCLK	26		SPI1 CLK		-	22	
50	PA6	GPIO	27				9	23	MDC
51	PA15	GPIO	28				-	24	MDIO

[5] WGM160P PAD 35 is used as factory reset pin and resets all Gecko OS variables to defaults. Any of the spare GPIOs is expected to be configured as factory reset pin, default being GOS_GPIO_16. More about factory reset at https://docs.silabs.com/gecko-os/4/standard/latest/getting-started#performing-a-factory-reset

4 Application schematics recommendations

4.1 Power supply

WGM160P consists of two main blocks, the microcontroller EFM32GG11 and the Wi-Fi network co-processor WF200. The microcontroller contains an internal DC-DC converter that powers both the microcontroller core and the WiFi chip with a lower supply voltage to reduce overall power consumption. All the internal supplies are connected together and supplied by module pin VBAT.

Care should be taken that the supply source is capable of supplying enough current for the load peaks of the power amplifier which can go momentarily up to 200mA, so it is recommended to select a regulator capable of supplying 300 mA. The peaks can be very fast, and the power supply supplying the module should be capable of reacting to load changes within 5µs.

External high frequency bypass capacitors are not needed because the module contains the required supply filter capacitors. However, care should be taken to prevent strong switching noise from being superimposed on the supply lines. Such noise can be generated, for example, by on-board charge pump converters used in RS232 level shifters.

Note that there is a total of about 15 µF of low ESR ceramic capacitors inside the module connected directly on the supply input. When using external regulators to generate regulated supplies for the module, the stability of the regulator with the low ESR provided by these capacitors should be checked. Some low-drop linear regulators and some older switched mode regulators are not stable when using ceramic output capacitors. The datasheet of the regulator typically lists recommendations concerning suitable capacitors, including data on ESR range and/or stability curves. A regulator with a statement “stable with ceramic capacitors” is recommended.

4.2 RF part

When using WGM160P with an antenna external to the module, be they connectorized off-the-shelf antennas or PCB trace antennas, antenna impedance shall be well matched to 50 ohms, achieving better than -10dB return loss throughout the 2.4-2.48 GHz band to reduce distortion in the module power amplifier due to impedance mismatch.

The matching should be verified in the final enclosure and it is recommended to reserve SMD placeholders for external antenna tuning. The suggested external antenna matching structure is a 3-element PI network.

Unused RF ports (RF2 on both variants or RF1 on the variant without the chip antenna assembled) must be terminated to ground with a resistor between 47 and 51 ohms.

5 Typical applications schematics

The diagrams below show a simple application schematic with WGM160P and its internal antenna.

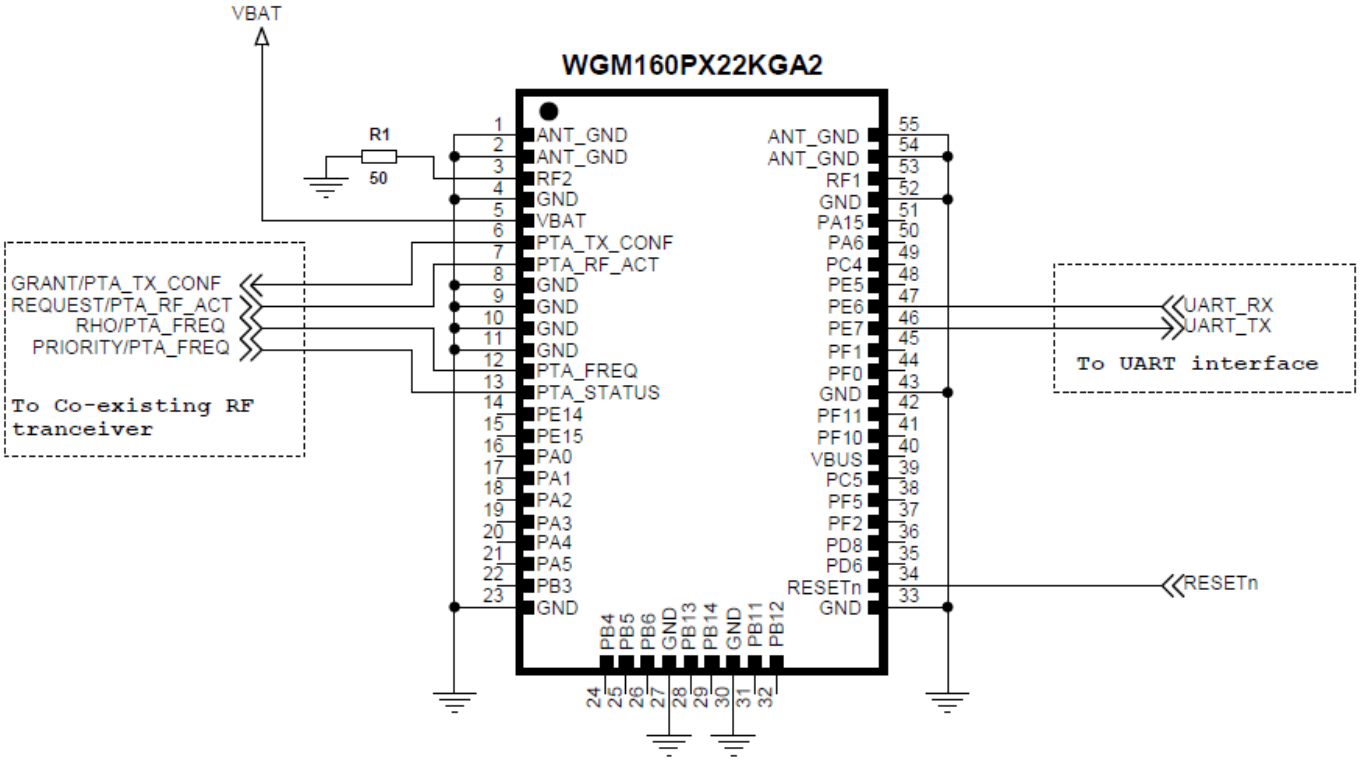

Figure 5.1 WFM160PX22KGA2 schematics

6 Layout recommendations

6.1 Generic RF Layout Considerations

For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design, because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required. The Silicon Labs development kit uses a 1.6 mm thick FR4 PCB with the following board stack-up.

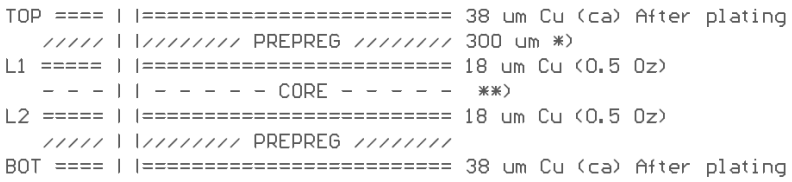

Figure 6.1 Reference design FR4 PCB stack-up

Use as much continuous and unified ground plane metallization as possible, especially on the top and bottom layers.

Use as many ground stitching vias, especially near the GND pins, as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.

Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic (the typical distance between vias on reference design is 1mm). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers, while keeping the GND pour metallization unbroken beneath the RF areas (between the antenna, matching network and the module). To benefit from parasitic decoupling capacitance, inner layer can be used to route power supply with wide VBAT sub-plane and traces to increase parasitic capacitance with nearby ground layers.

Avoid using long and/or thin transmission lines to connect the RF related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.

Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.

To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VBAT filtering. Any gap on each PCB layer should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to layout restrictions such as traces routed on other layers or components on the bottom side.

Use tapered line between transmission lines with different width (i.e., different impedance) to reduce internal reflections.

Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.

Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.

Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VBAT traces, to reduce their harmonic radiation caused by the fringing field.

Place any high-frequency (MHz-ranged) crystal as close to the module as possible. External crystal load capacitors are not needed, since there is an on-chip capacitance bank for this purpose. Thus, it is suggested that one select crystals with load capacitance requirements that can be supported by the module. This way, the crystal can be placed close to the chip pins and external capacitors are not needed. Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may be an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace. If possible, use an isolating ground metal between the crystal and any nearby supply traces to avoid any detuning effects on the crystal and to avoid the leakage of the crystal/clock signal and its harmonics to the supply lines. If possible, route traces between crystal and module pins as differential signals to minimize area of trace loop.

6.2 RF-pads including the diversity port and external antennas

With WGM160P variants without a chip antenna, the important properties are mainly to ensure that WGM160P ground pads are well connected to PCB ground plane to optimize thermal conductivity and to prevent unwanted emissions due to ground currents.

The RF pads and RF traces conducting the RF signal should be dimensioned to have a characteristic impedance of 50 ohms. It is vital that proper RF design principles are used when designing an application using the RF pads.

Antennas external to the module, be they connectorized off-the-shelf antennas or PCB trace antennas, must be well matched to 50 ohms. PCB size and layout recommendations from the antenna manufacturer shall be followed. Board size, ground plane size, plastic enclosures, metal shielding and components in close proximity to the antenna can affect antenna impedance and radiation pattern. Therefore, antenna matching should be verified in the final enclosure. Better than -10dB return loss throughout the 2.4-2.48 GHz band is recommended to prevent distortion in the module power amplifier due to impedance mismatch. PA distortion can cause significant packet loss and poor overall performance.

6.3 Module chip antenna

As is common for very small antennas, the antenna on WGM160P uses the ground plane edge to radiate, rather than just the antenna chip itself. The antenna on WGM160P is robust to the detuning effect of the proximity of various objects and makes the module easy to use with a consistent and reliable performance. All the antenna needs is a small patch free from copper under the antenna end of the module and a solid ground plane covering the whole PCB on at least one layer, especially the edge of the application board where the antenna is placed. To prevent the RF signal coupling to other, sensitive parts of the design, it is recommended to have a solid, board-wide ground plane.

For optimal performance of the WGM160P Module, please follow these guidelines:

1. Place the Module at the edge of the PCB with the antenna end flush against the application board edge. If it is necessary to place the module some distance from the edge, limit the copper plane edges to the level of the module antenna end
2. Place the module close to the center of the edge of the board
3. Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna
4. Connect all ground pads directly to a solid ground plane covering the whole PCB. The grounds closest to the antenna end conduct strong RF currents and are critical for good performance, while the rest of the ground pads are important for thermal conductivity.
5. Place multiple ground vias as close to the ground pads as possible. If possible, fill every unused area in all layers with ground-connected copper to improve thermal conductivity.
6. Terminate unused RF ports to ground with a resistor between 47 and 51 ohms.

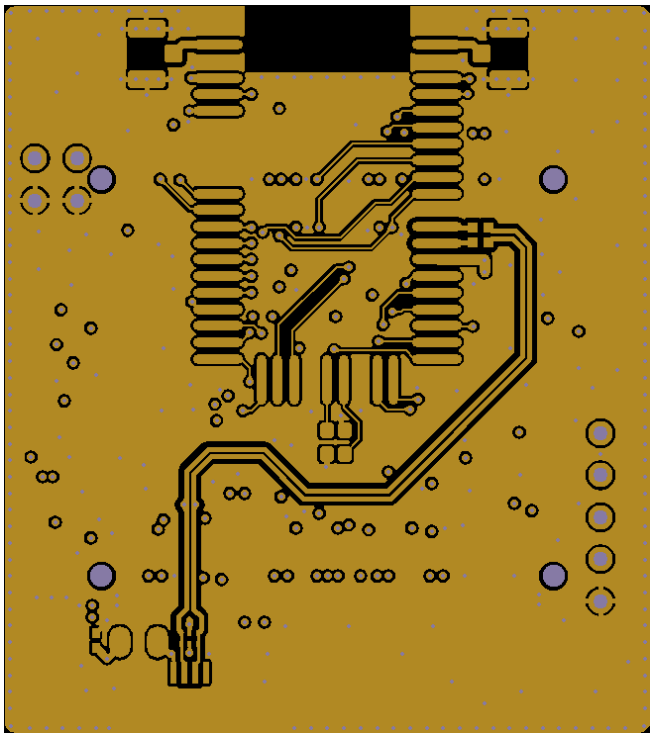

Figure 6.2 Top layer layout of WGM160P reference design

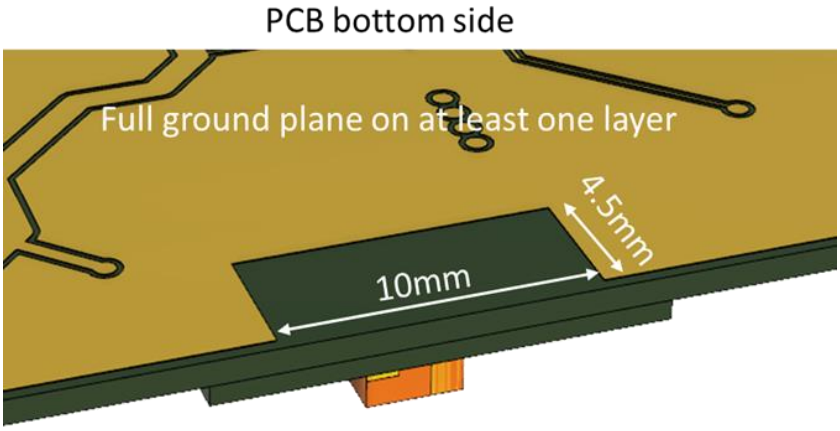

Figure 6.3 Details of the antenna ground clearance

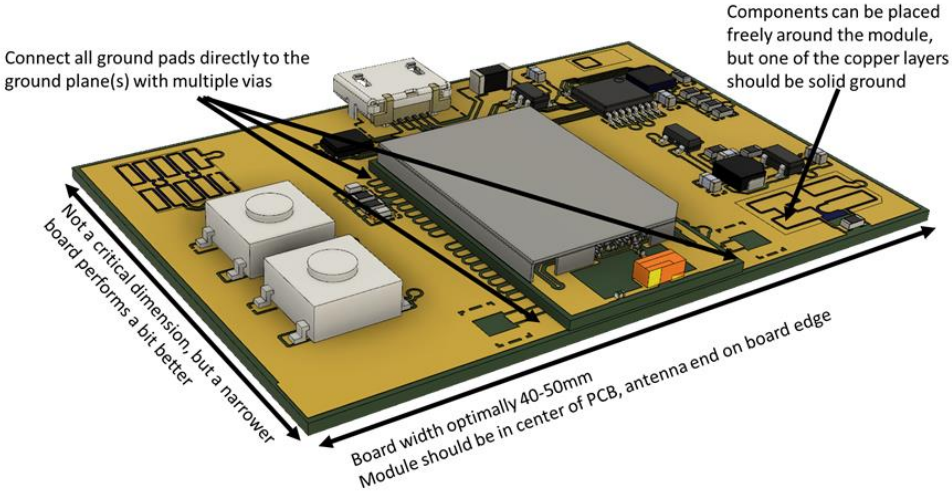

Figure 6.4 Details about board dimensions and module placement

Any metallic objects in close proximity to the antenna will distort the antenna electromagnetic fields and will cause the antenna center frequency to shift, reducing the performance. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes. Please note that even if the antenna center frequency is not shifted by a nearby metallic object, they prevent the antenna from radiating freely by distorting the radiating pattern. Metals are opaque to radio frequencies and may cause an equivalent of a shadow, a region of weaker performance, in the direction covered by the metal.

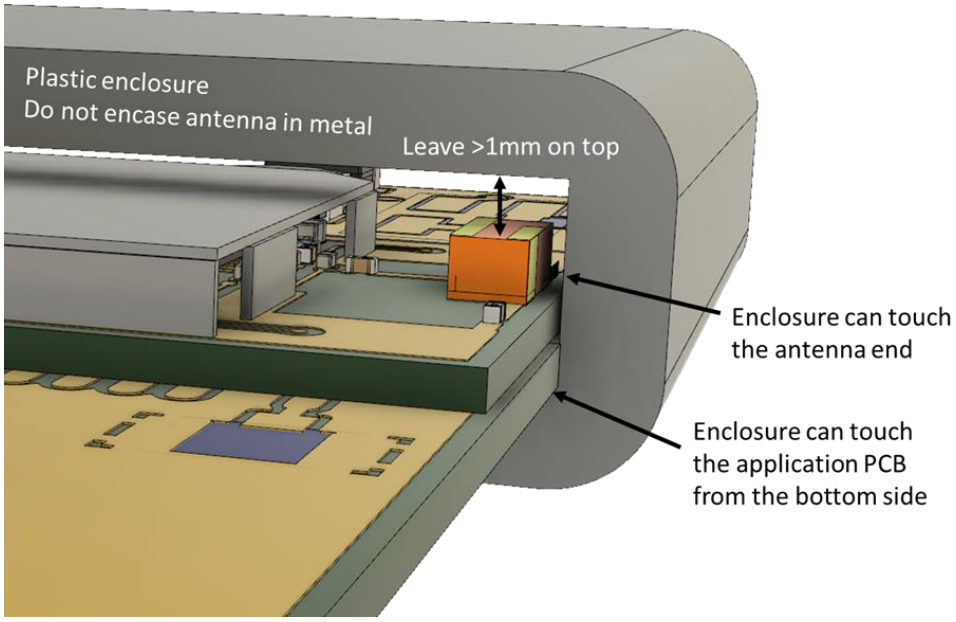

Figure 6.5 Enclosure clearance recommendations

Because the application board is part of the antenna circuit, its dimensions have an effect on the antenna efficiency and thus achievable range. Narrower ground planes can be used but will result in compromised RF performance.

7 Recommendations for certification

7.1 Module certification regarding port without integrated antenna

WGM160P has been certified with an integrated chip antenna as well as external antennas connected to either RF port or both. The required antenna impedance is 50 Ω.

Qualified external antenna type

Antenna type	Maximum gain
Connectorized coaxial dipole	2.14 dBi

Any antenna that is of the same general type and of equal or less directional gain as listed in the above table can be used without a need for retesting in the regulatory areas that have a full modular radio approval (USA, Canada, Korea, Japan). In countries applying the ETSI standards, like the EU countries, the radiated emissions are always tested with the end-product and the antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

If an antenna of a different type (such as a chip antenna, a PCB trace antenna or a patch) with a gain less than or equal to 2.14 dBi is needed, it can be added as a permissive change, requiring some radiated emission testing. Antenna types with more gain than 2.14 dBi may require a fully new certification. Since the exact permissive change procedure is chosen on a case by case basis, please consult your test house, for example while performing with them the EMC testing of the end-product.

7.2 Locating the Module Close to Human Body

When using the Module in an application where the radio is located close to human body, the human RF exposure must be evaluated. FCC, IC, and CE all have different standards for evaluating the RF exposure and, because of this, each standard will require a different minimum separation distance between the Module and human body. Certification of WGM160P allows for the minimum separation distances detailed in Table 7.1 below in portable use cases (less than 20 cm from human body). The module is approved for the mobile use case (more than 20 cm) without any need for RF exposure evaluation.

Table 7.1.WGM160P Minimum Allowed Separation Distance From Human Body

Certification	WGM160P with antenna	WGM160P without antenna[6]
FCC	24 mm	24 mm
ISED	30 mm	30 mm
CE	The RF exposure must be evaluated using the end product always when transmitting with power levels higher than 20mW=13dBm	The RF exposure must be evaluated using the end product always when transmitting with power levels higher than 20mW=13dBm

For FCC and ISED, using the Module in end products where the separation distance is smaller than those listed above is allowed but requires evaluation of the RF exposure in the final assembly and applying for a *Class 2 Permissive Change* or *Change of ID* to be applied to the existing FCC/ISED certificates of the Module. For CE certification, RF exposure must be evaluated using the end product in all cases.

Note: Placing the Module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus reducing range.

[6] With external reference dipole antenna

8 Package outline

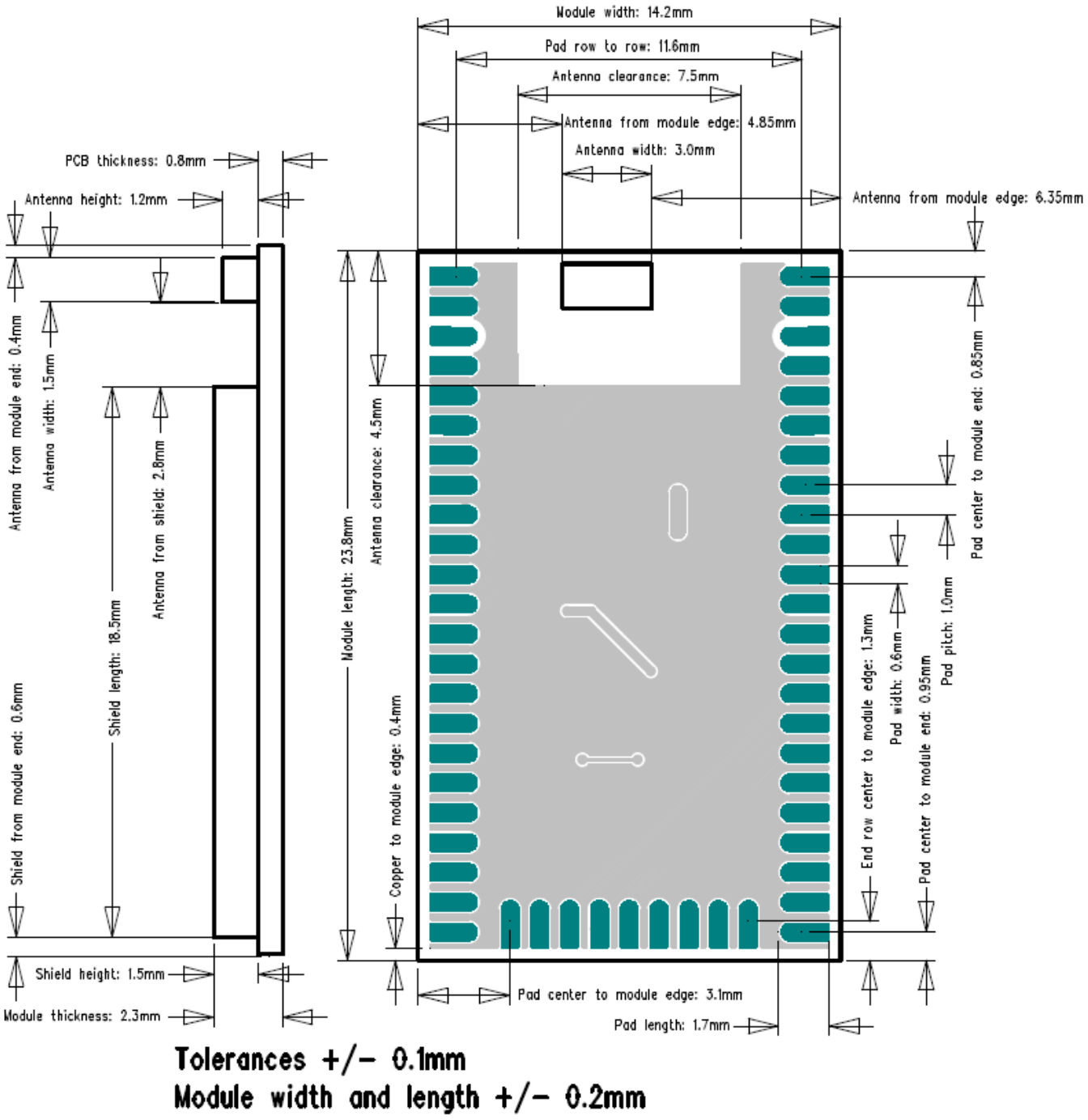

Figure 8.1 WGM160PX22KGA2 Package outline

9 Recommended PCB land pattern

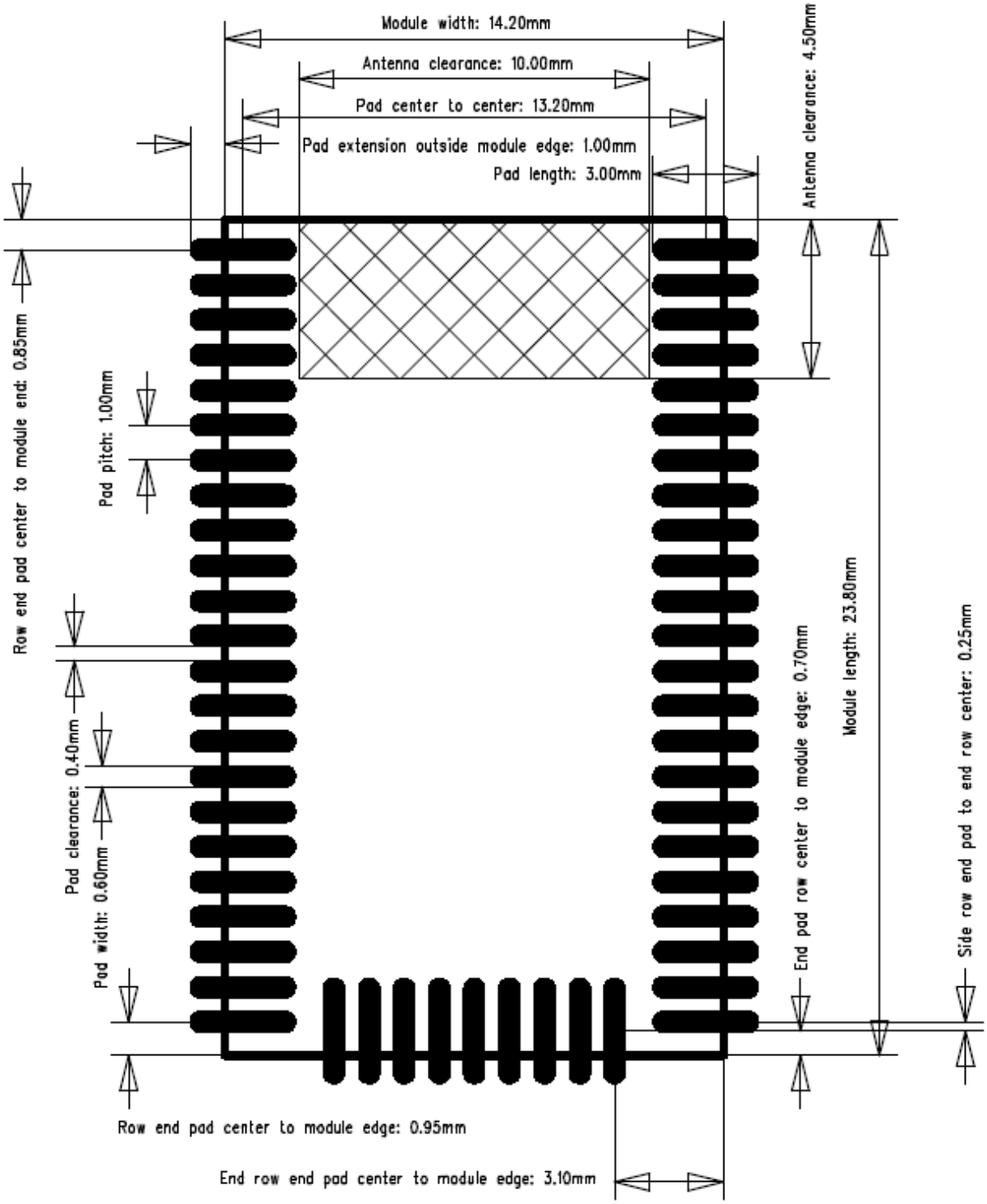

Figure 9.1 WGM160PX22KGA2/ WGM160P022KGA2 recommended land footprint

For WGM160P modules without antenna, there is no need of PCB antenna clearance.

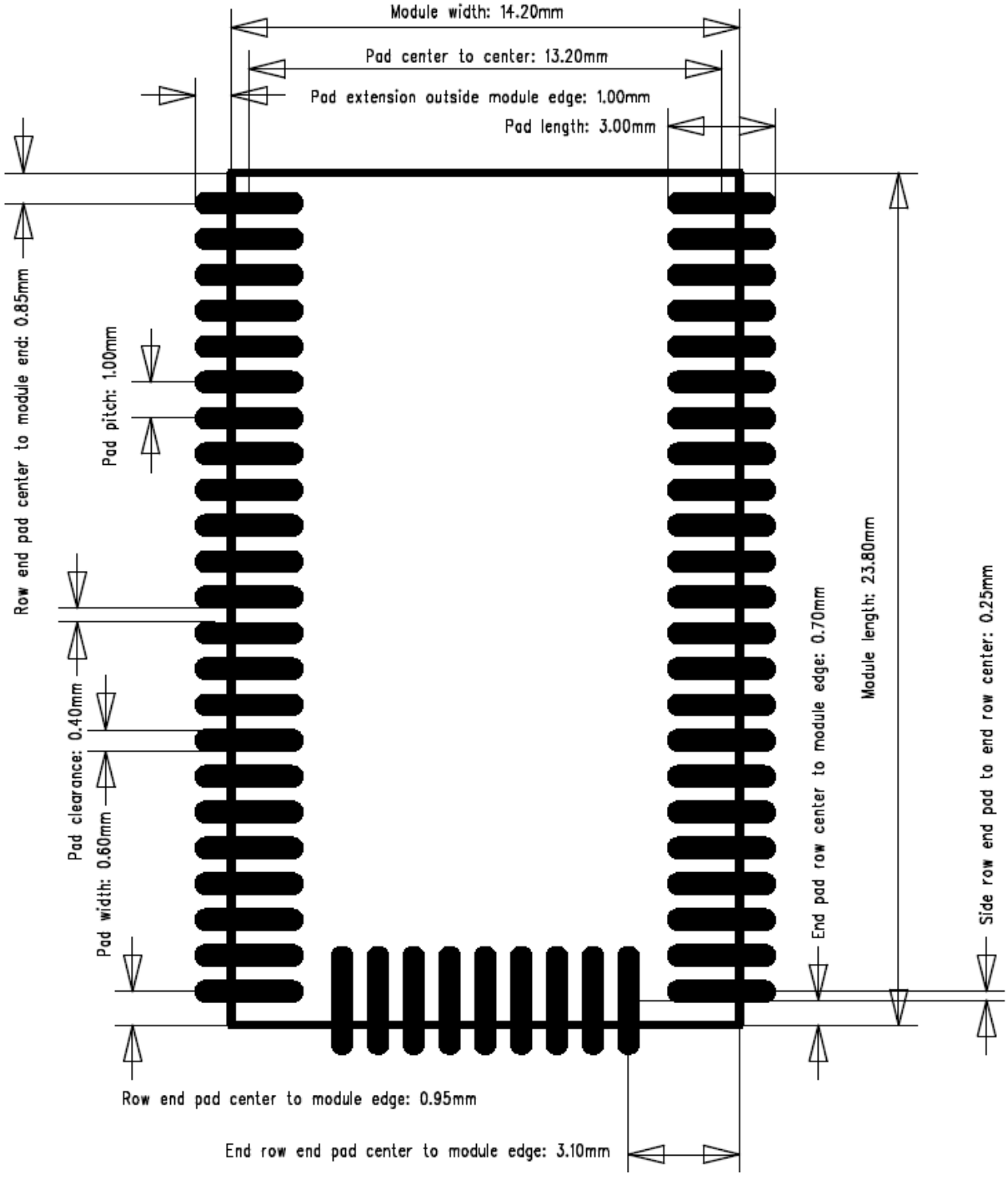

Figure 9.2 WGM160PX22KGN2/ WGM160P022KGN2 recommended land footprint