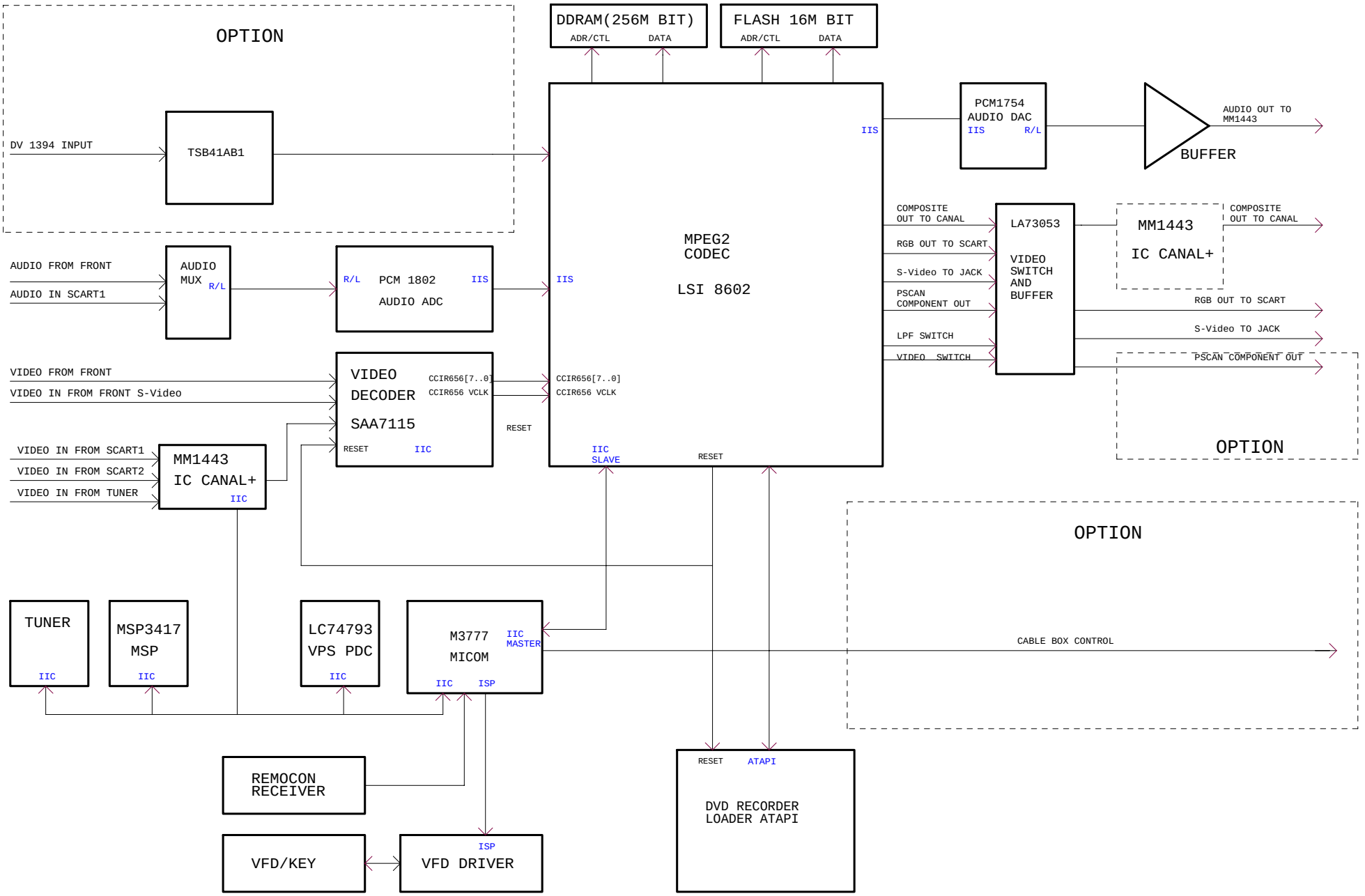
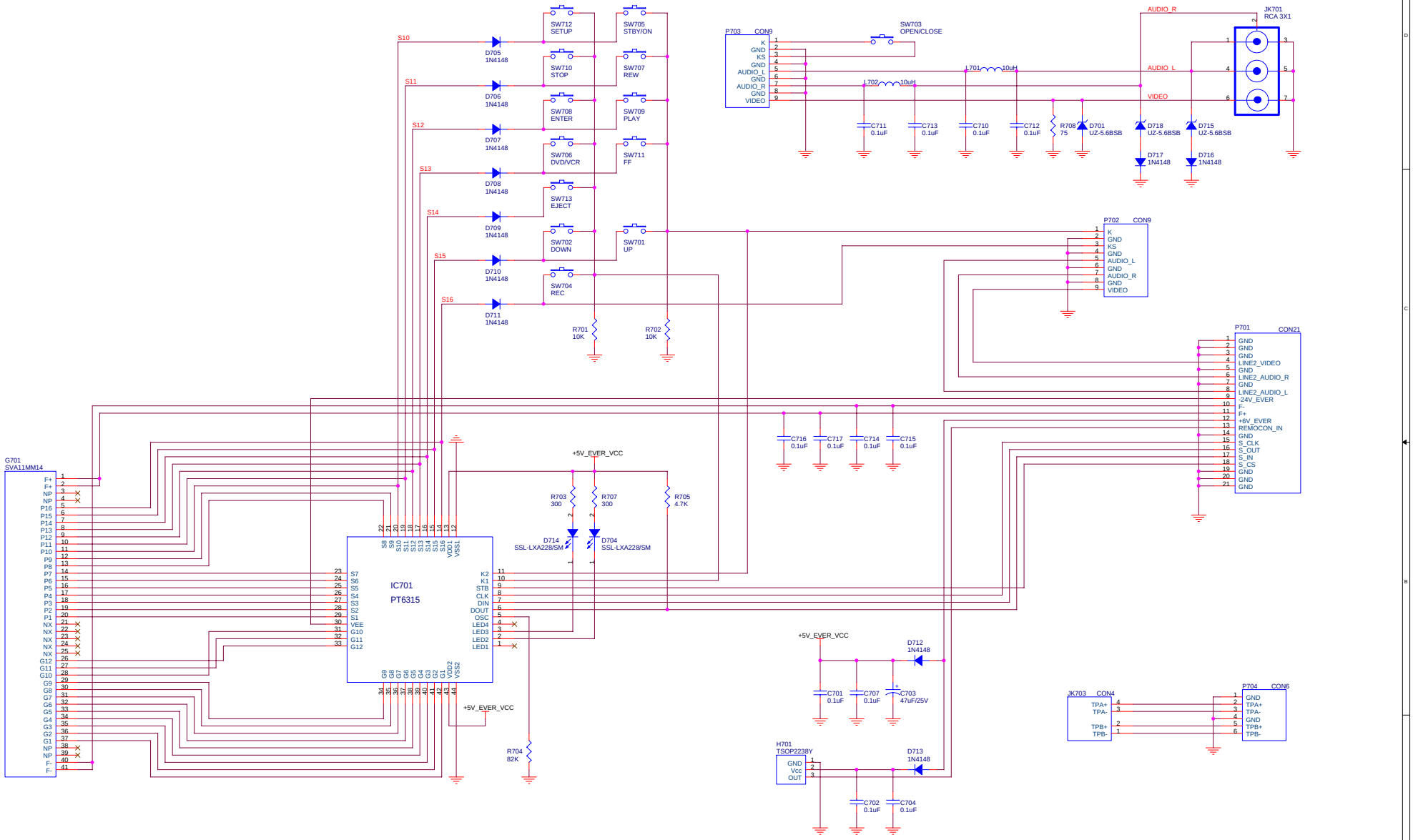
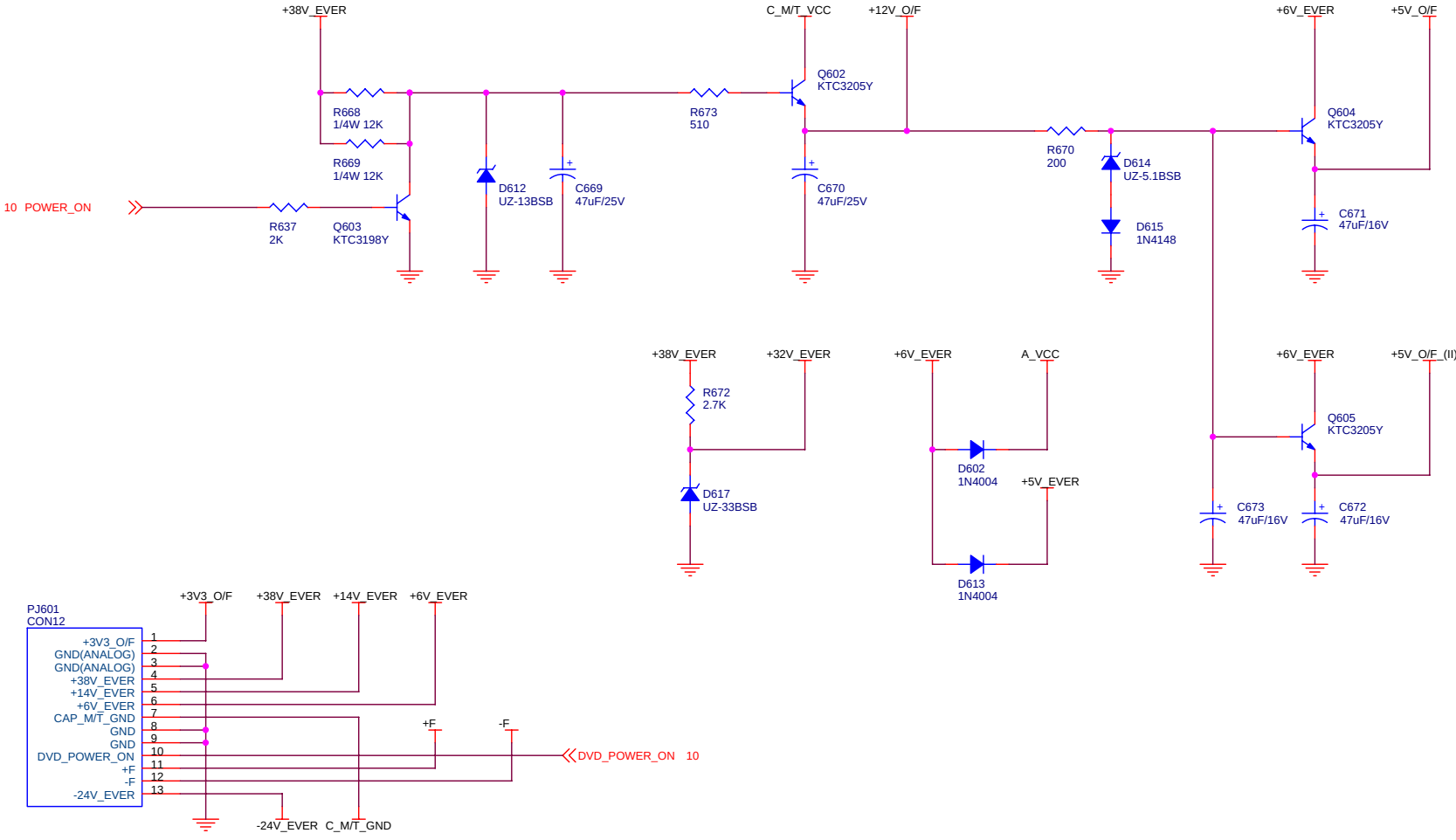


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
W.K.Ihm	W.K.Ihm	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO.	2.0
DAEWOO ELECTRONICS Digital Media Lab.				01 : BLOCK DIAGRAM	

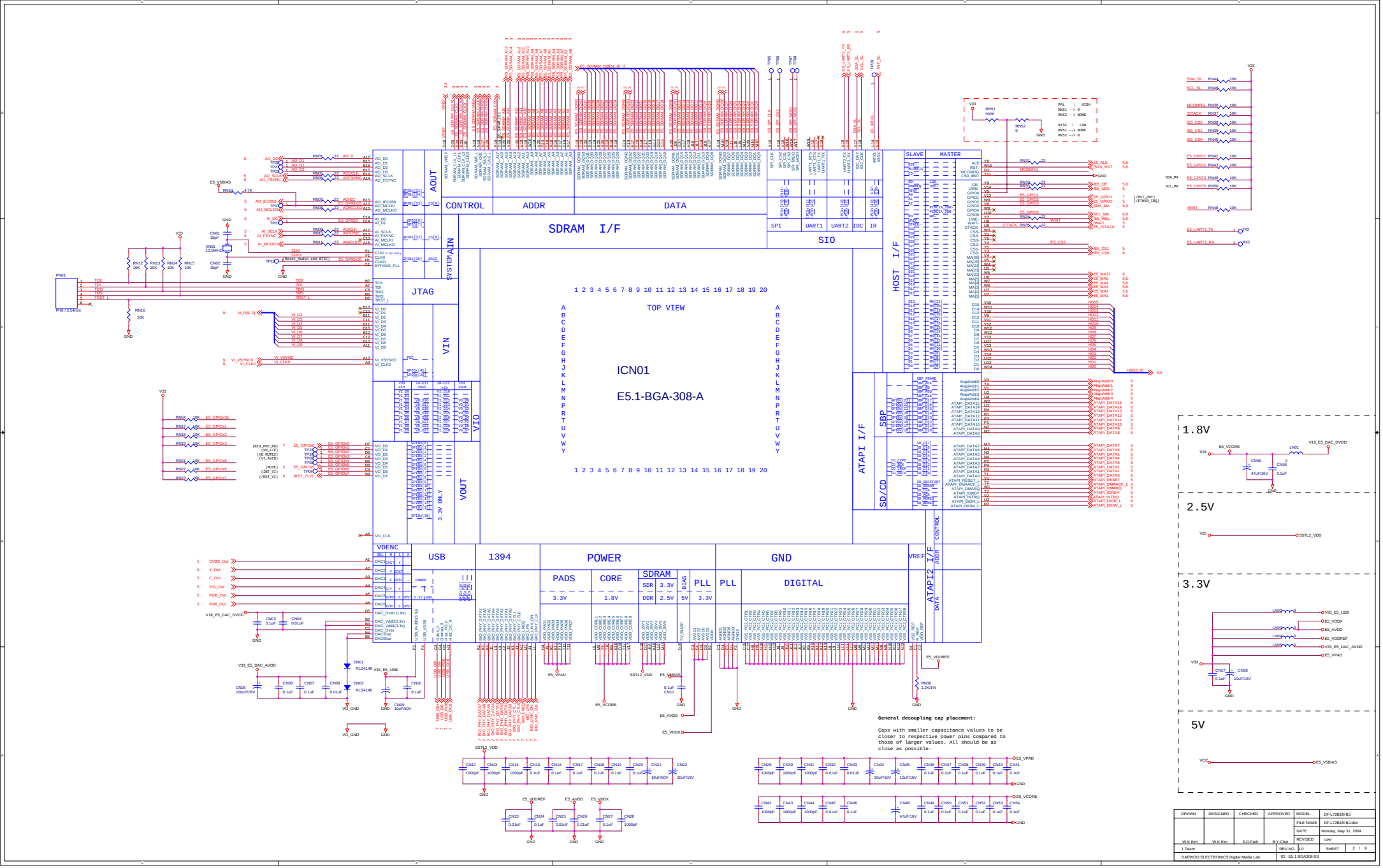
SHEET 1 / 9

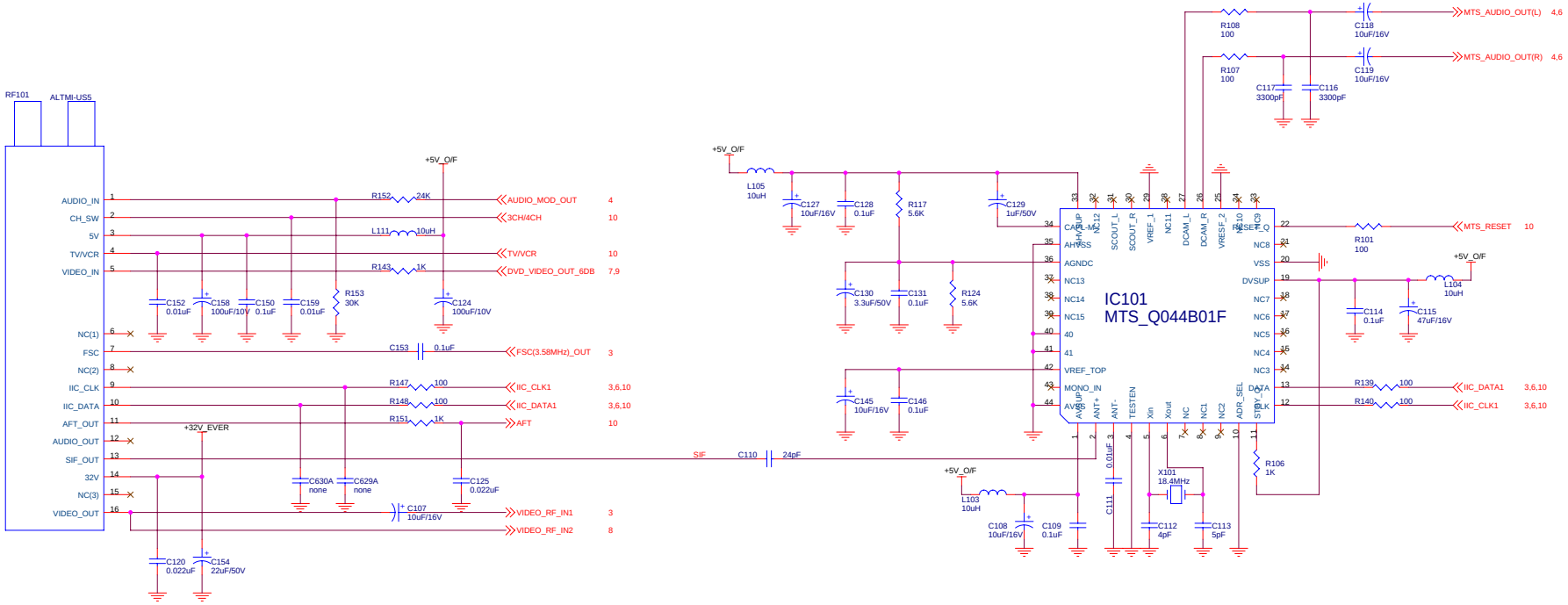


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
D.Y.Kwak	D.Y.Kwak	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 2.0	SHEET 1 / 1
DAEWOO ELECTRONICS Digital Media Lab.				01 : Front Board	



DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
J.H.Lim	J.H.Lim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team			REV NO. 2.0	SHEET	1 / 10
DAEWOO ELECTRONICS Digital Media Lab.			01 : POWER		


SDRAM I/F
CONTROL
ADDR
DATA
AOUT
SYSTEM
JTAG
VIN
VIO
VOUT
3.3V ONLY
HOST I/F
SLAVE
MASTER
SIO
SPI
UART1
UART2
IDC
IR
ATAPI I/F
SBP
SD/CD
CONTROL
ADDR
DATA
ICN01
E5.1-BGA-308-A
TOP VIEW
VDENC
USB
1394
POWER
PADS
CORE
SDRAM
SDR
DDR
3.3V
2.5V
BIAS
PLL
GND
DIGITAL
VREF
1.8V
5V
E5_VCORE
E5_VPAD
E5_VDDREF
E5_AVDD
E5_VDDX
E5_VSBIAS
SSTL2_VDD
V33_ES_USB
V33_ES_DAC_AVDD
VG_GND
General decoupling cap placement:
Caps with smaller capacitance values to be closer to respective power pins compared to those of larger values. All should be as close as possible.
DRAWN
DESIGNED
CHECKED
APPROVED
MODEL
DF-L72B1N-BJ
FILE NAME
DF-L72B1N-BJ.dsn
DATE
Monday, May 31, 2004
REVISED
LPP
W.K.Ihm
W.K.Ihm
S.D.Park
B.Y.Choi
1 Team
REV NO. 1.0
SHEET
2 / 9
DAEWOO ELECTRONICS Digital Media Lab.
02 . E5.1 BGA308-SS

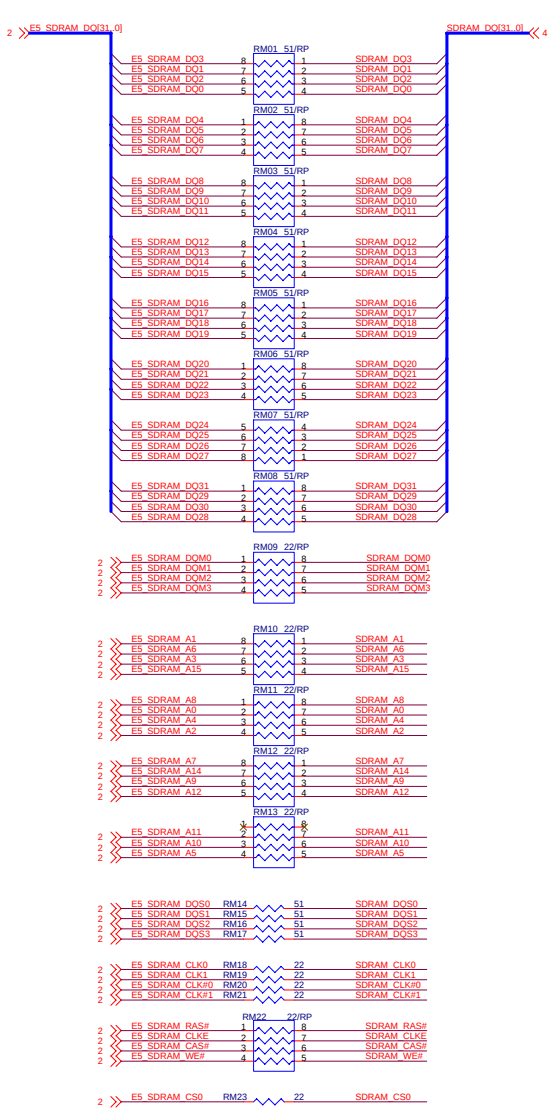


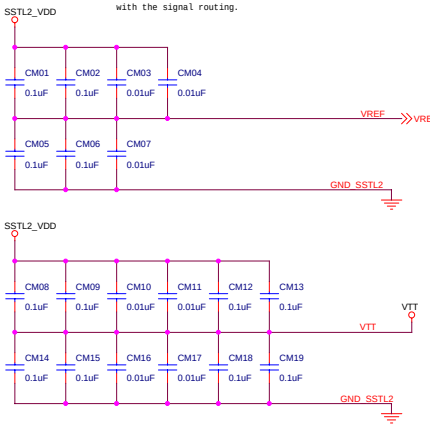
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.H.Cho	Y.H.Cho	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 2.0	SHEET 2 / 10
DAEWOO ELECTRONICS Digital Media Lab.				02 : RF & MTS	

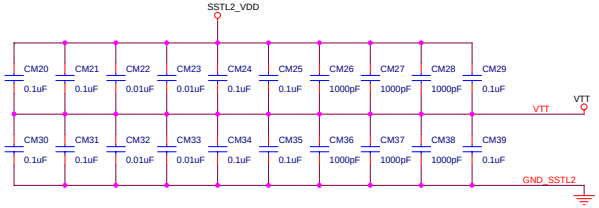
TERMINATION AT E5.1

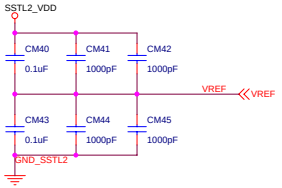
TERMINATION AT DDR

The VTT side of the terminaton resistors should be placed on a wide VTT island on the surface layer. The island is located at each end of the bus, so it does not interfere with the signal routing.





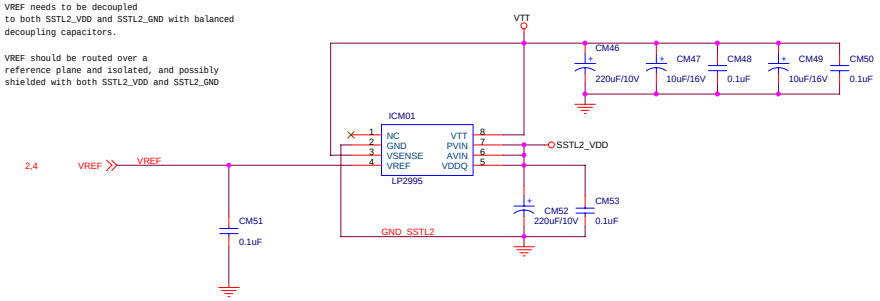




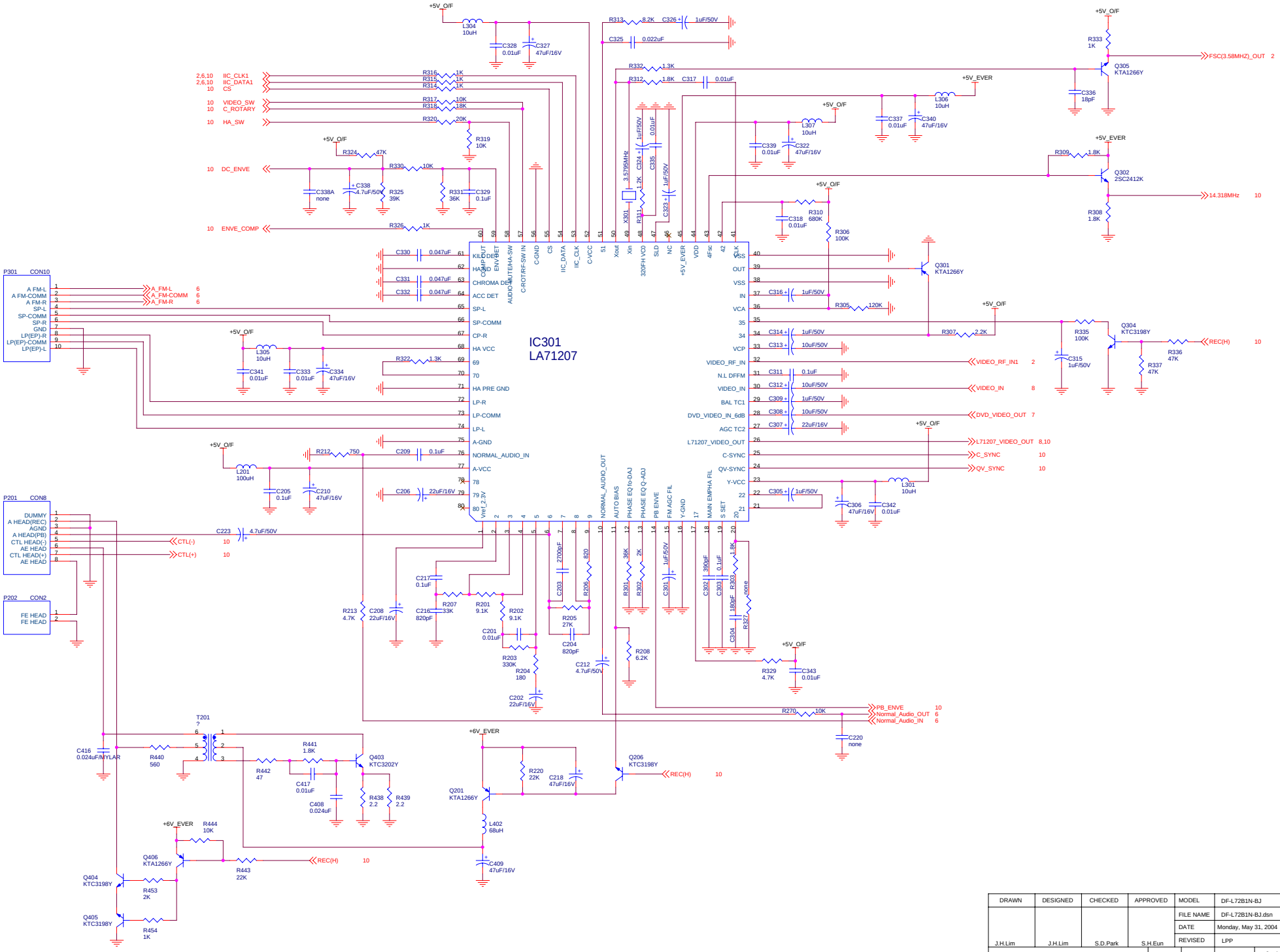
DDR TERMINATION VOLTAGE REGULATOR

VREF needs to be decoupled to both SSTL2_VDD and SSTL2_GND with balanced decoupling capacitors.

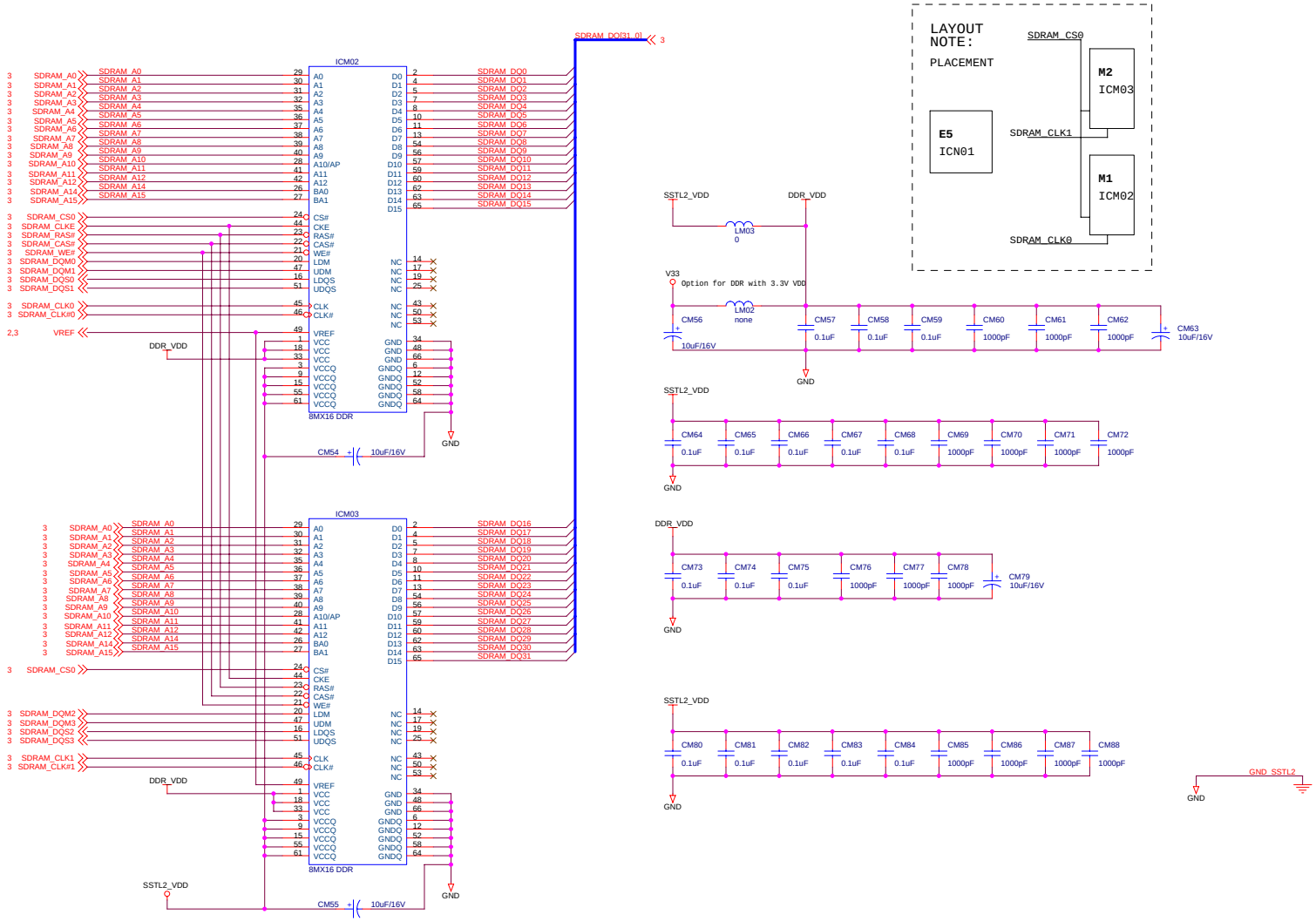
VREF should be routed over a reference plane and isolated, and possibly shielded with both SSTL2_VDD and SSTL2_GND



DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
M.K.Lee	M.K.Lee	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 3 / 9
DAEWOO ELECTRONICS Digital Media Lab.				03 : TERM AT E5 & DDR & VREF/VT	

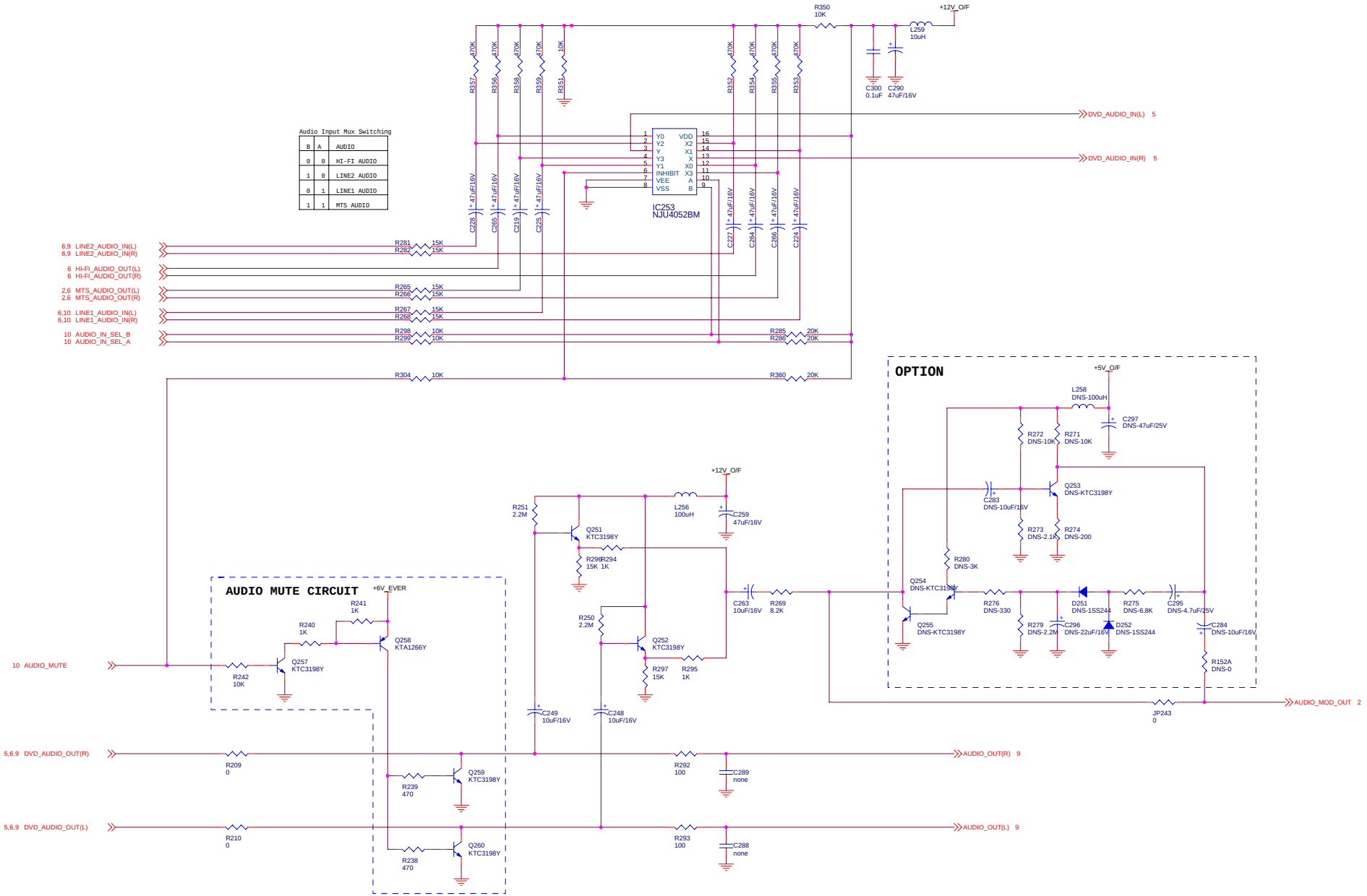


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
J.H.Lim	J.H.Lim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team			REV NO. 2.0	SHEET	3 / 10
DAEWOO ELECTRONICS Digital Media Lab.			03 : AV		



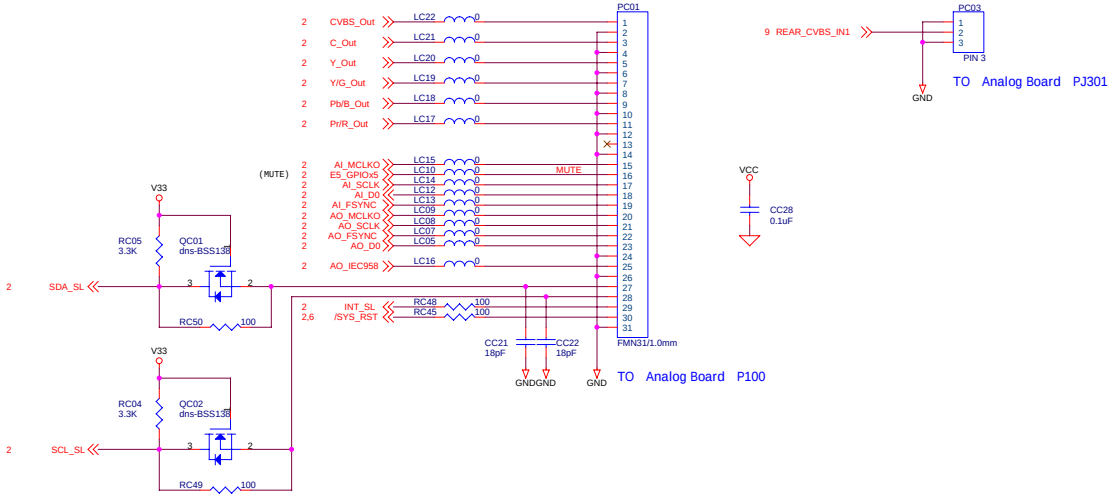
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
M.K.Lee	M.K.Lee	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 4 / 9
DAEWOO ELECTRONICS Digital Media Lab.				04 : 2 (8M BY 16) DDR SDRAM	

Audio Input Multiplexer

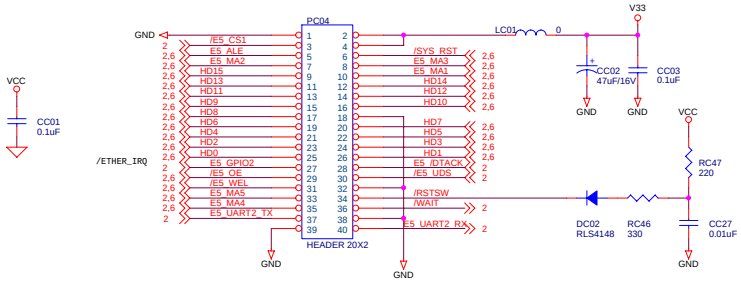


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.S.Kim	Y.S.Kim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO.	2.0
DAEWOO ELECTRONICS Digital Media Lab.				SHEET	4 / 10
				04 : AUDIO MULTIPLEXER	

To Analog Board
(Video & Audio & IIC)

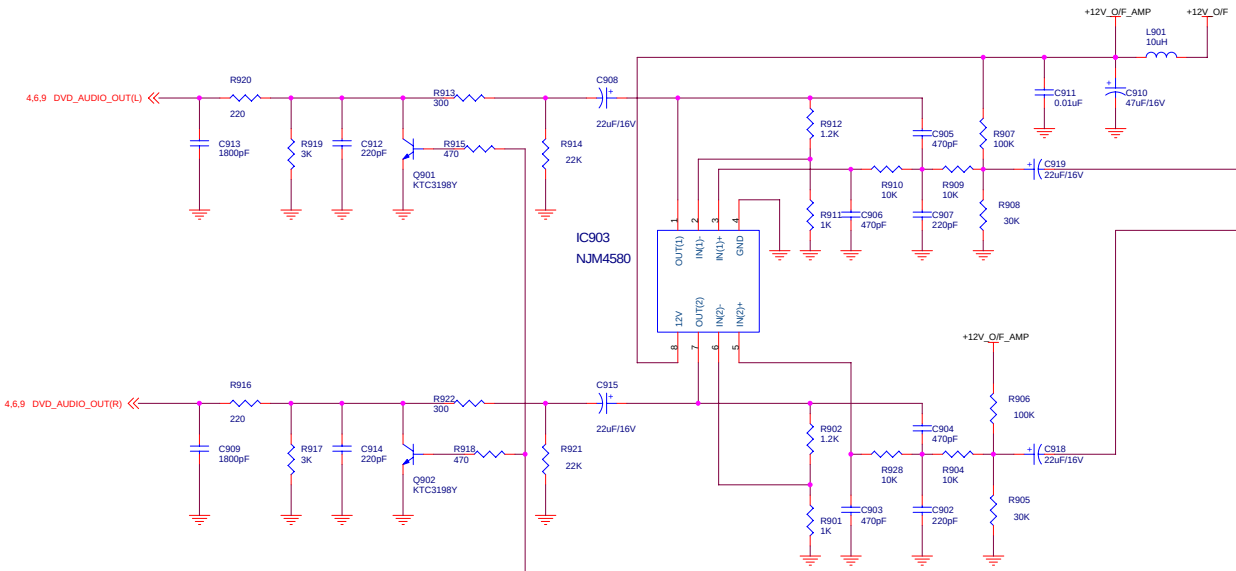


E-Link IV Connector

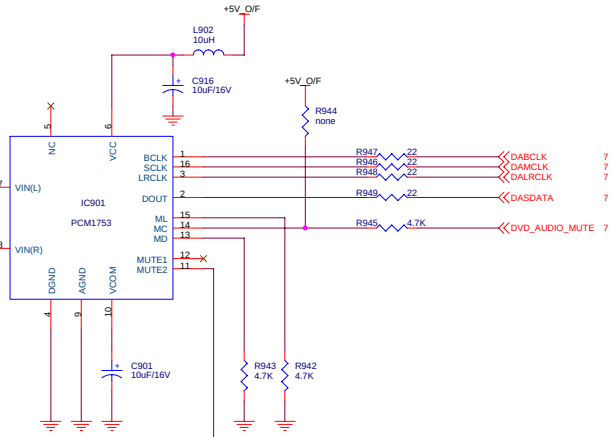


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.S.Kim	Y.S.Kim	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 5 / 9
DAEWOO ELECTRONICS Digital Media Lab.				05 : RST, IR, AV/ELINK CON,UART	

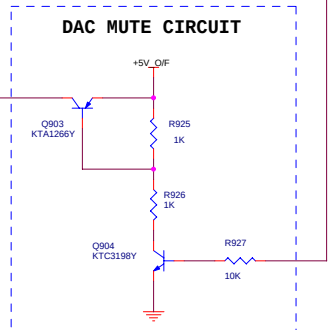
AUDIO AMP & FILTER



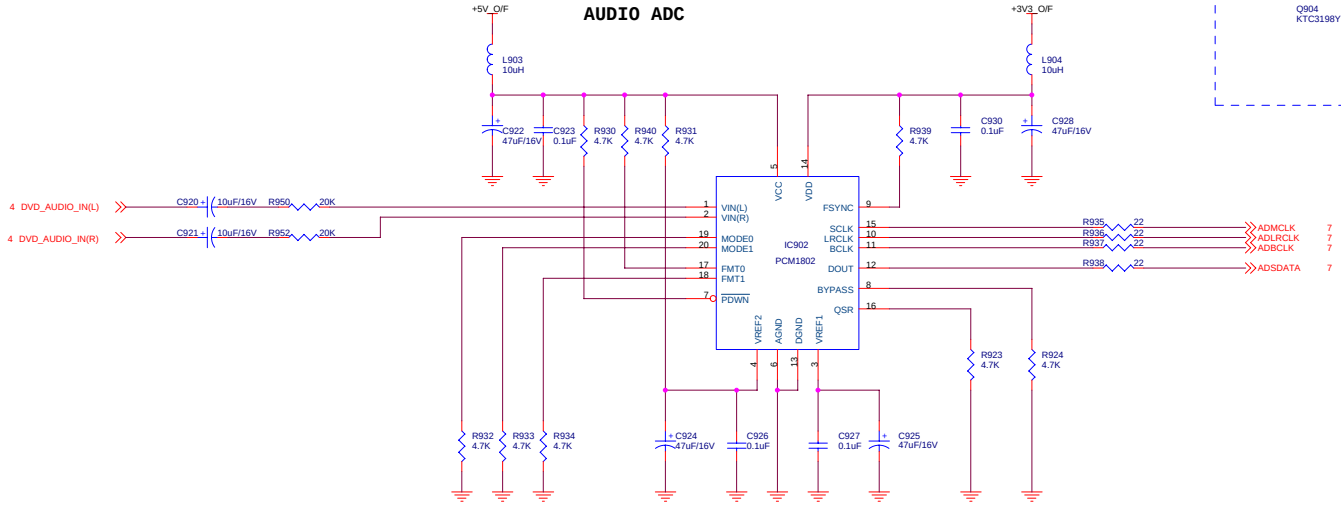
AUDIO DAC



DAC MUTE CIRCUIT

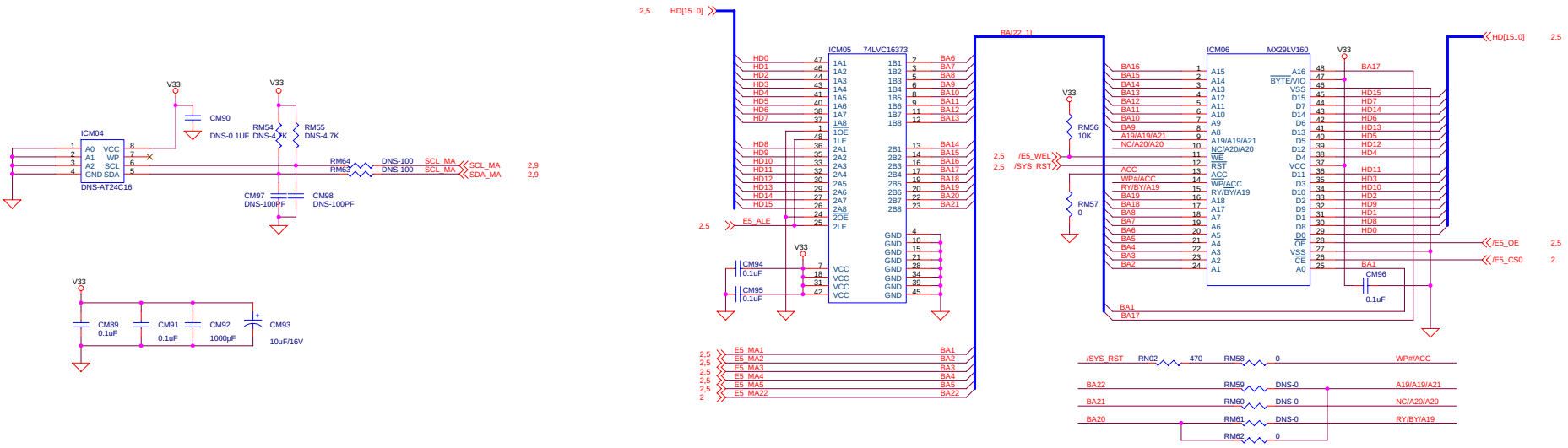


AUDIO ADC



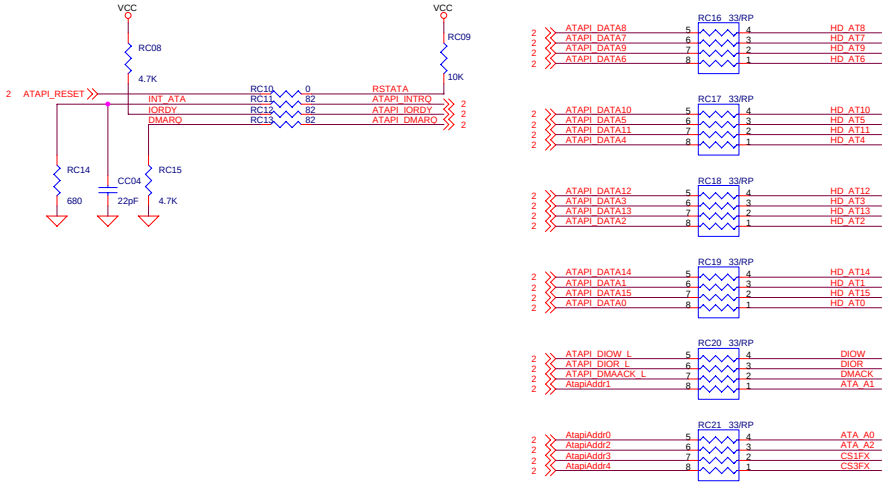
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.S.Kim	Y.S.Kim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 2.0	SHEET 5 / 10
DAEWOO ELECTRONICS Digital Media Lab.				05 : AUDIO AD & DA	

FLASH MEMORY(2 or 4 or 8 Mb)

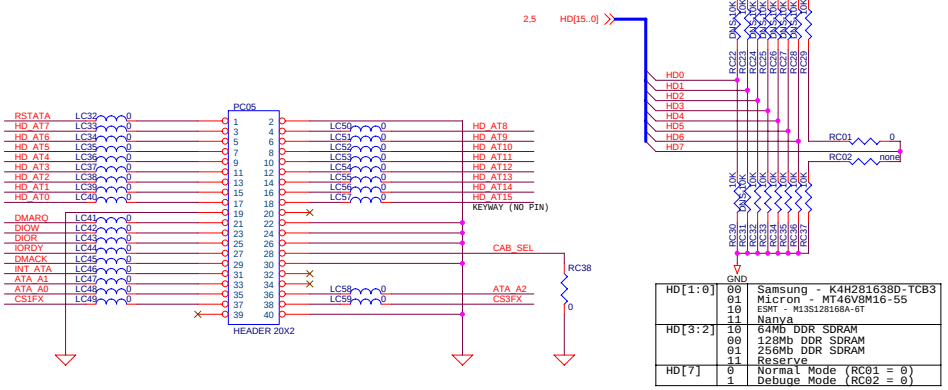


Size	Stuff	Not Stuff
1MB		RM59, RM60, RM61, RM62
2MB	RM62	RM59, RM60, RM61
4MB	RM62, RM60	RM59, RM61
8MB	RM59, RM60, RM61	RM62

DEDICATED ATAPI INTERFACE

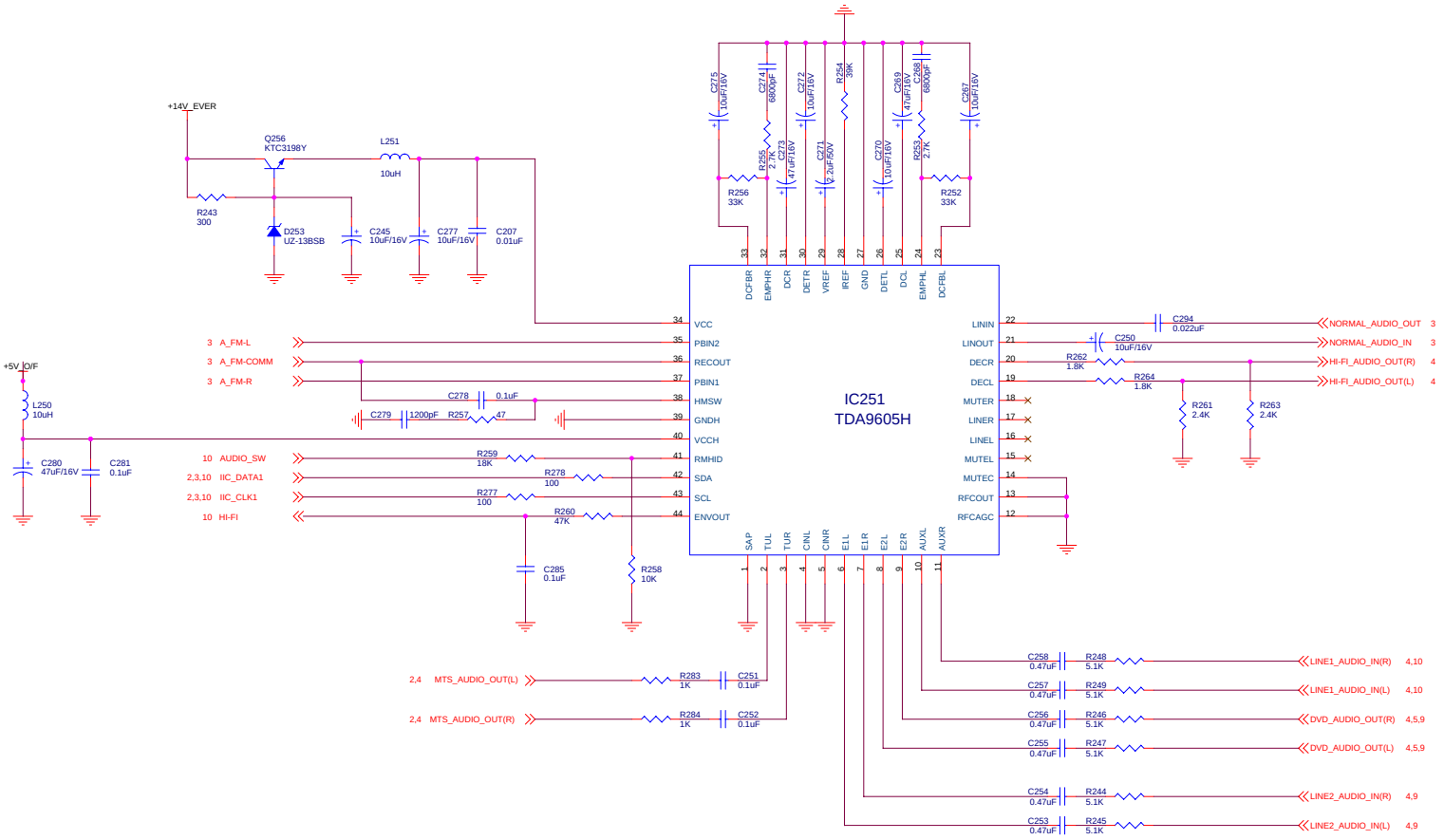


HOST Read



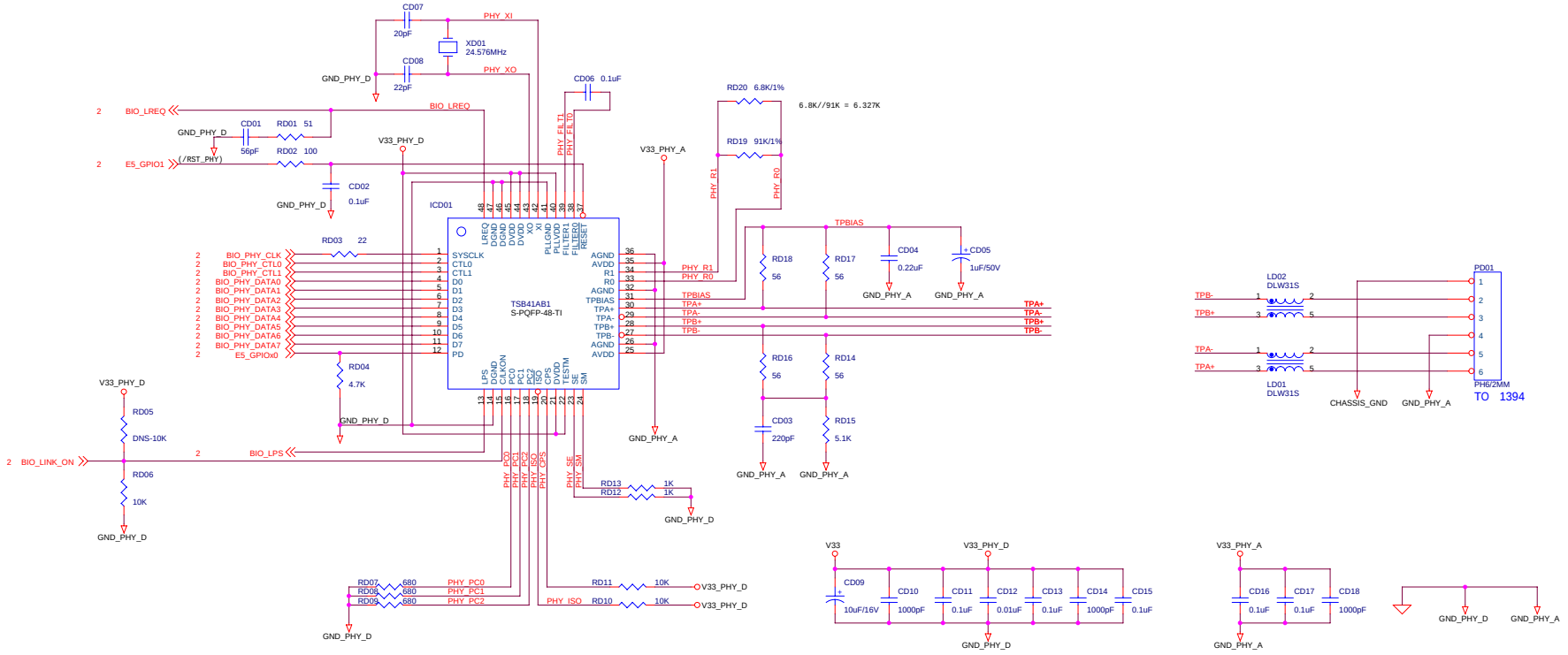
HD[1:0]	00	Samsung - K4H281638D-TCB3
	01	Micron - MT46V8M16-55
	10	ESMT - M13S128168A-6T
	11	Nanya
HD[3:2]	10	64Mb DDR SDRAM
	00	128Mb DDR SDRAM
	01	256Mb DDR SDRAM
	11	Reserve
HD[7]	0	Normal Mode (RC01 = 0)
	1	Debuge Mode (RC02 = 0)

DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
D.Y.Kwak	D.Y.Kwak	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 6 / 9
DAEWOO ELECTRONICS Digital Media Lab.				06 : FLASH & ATA	

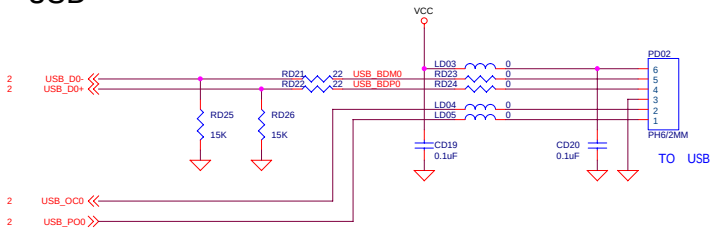


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.S.Kim	Y.S.Kim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO.	2.0
DAEWOO ELECTRONICS Digital Media Lab.				SHEET	6 / 10
				06 : HI-FI	

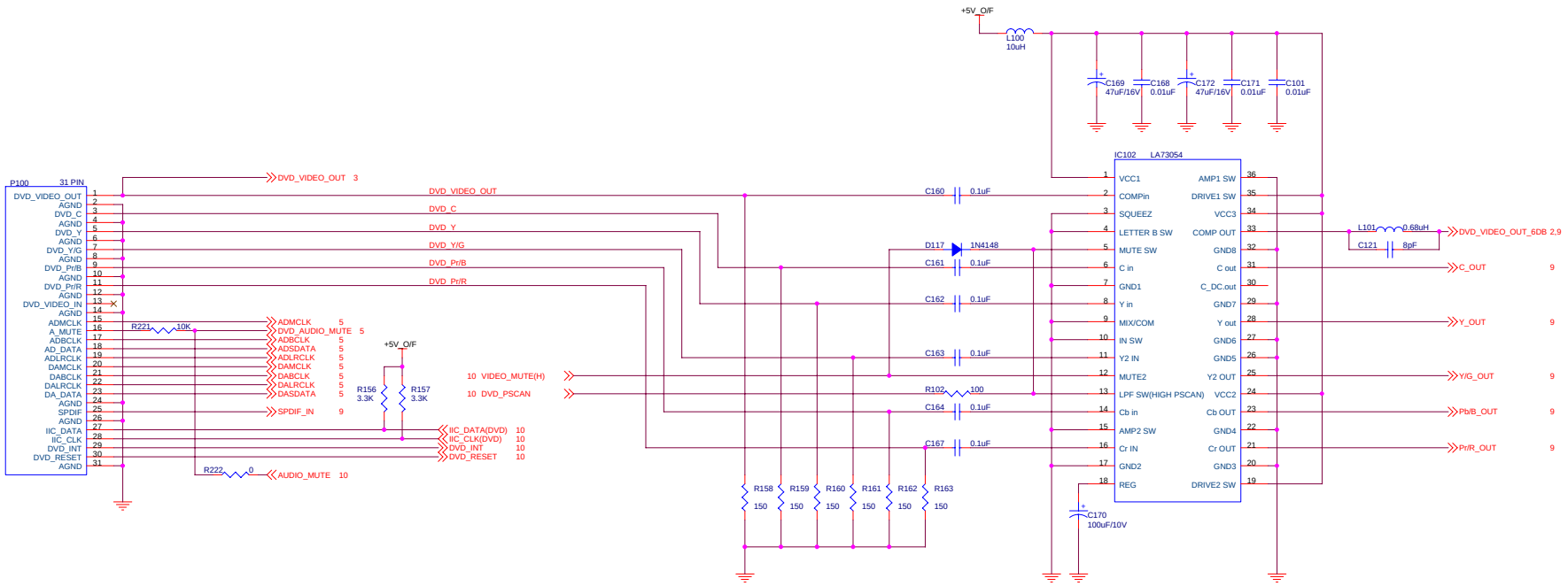
1394 FIREWIRE PHY



USB

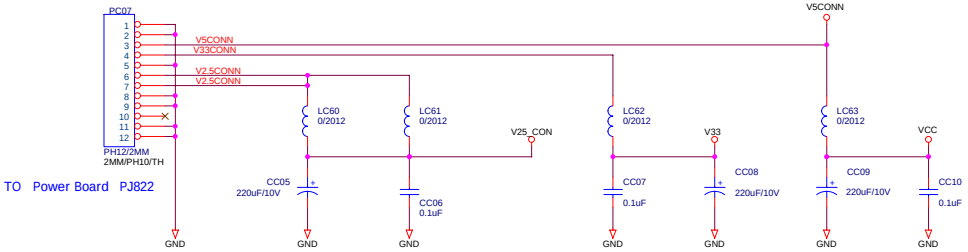


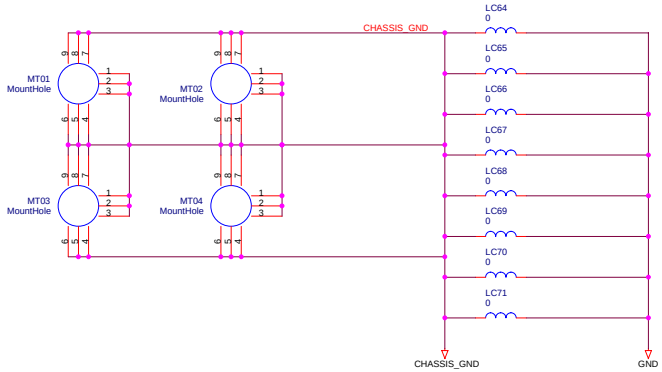
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
Y.H.Cho	Y.H.Cho	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 7 / 9
DAEWOO ELECTRONICS Digital Media Lab.				07 : 1394 PHY	

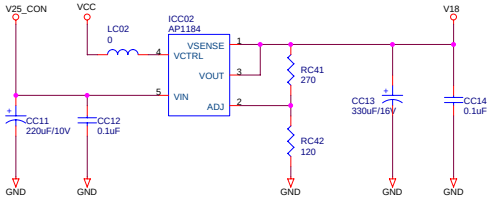


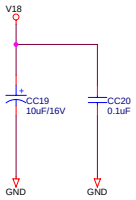
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
M.K.Lee	M.K.Lee	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 2.0	SHEET 7 / 10
DAEWOO ELECTRONICS Digital Media Lab.				07 : VIDEO IN/OUT	

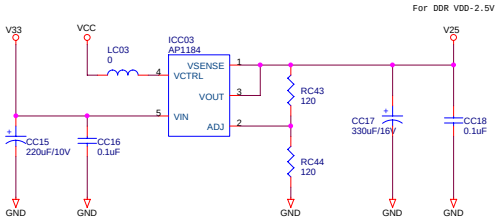
MAIN POWER CONN

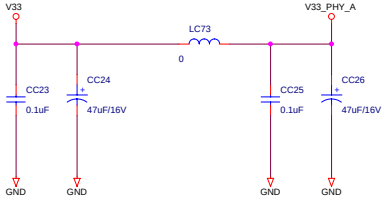






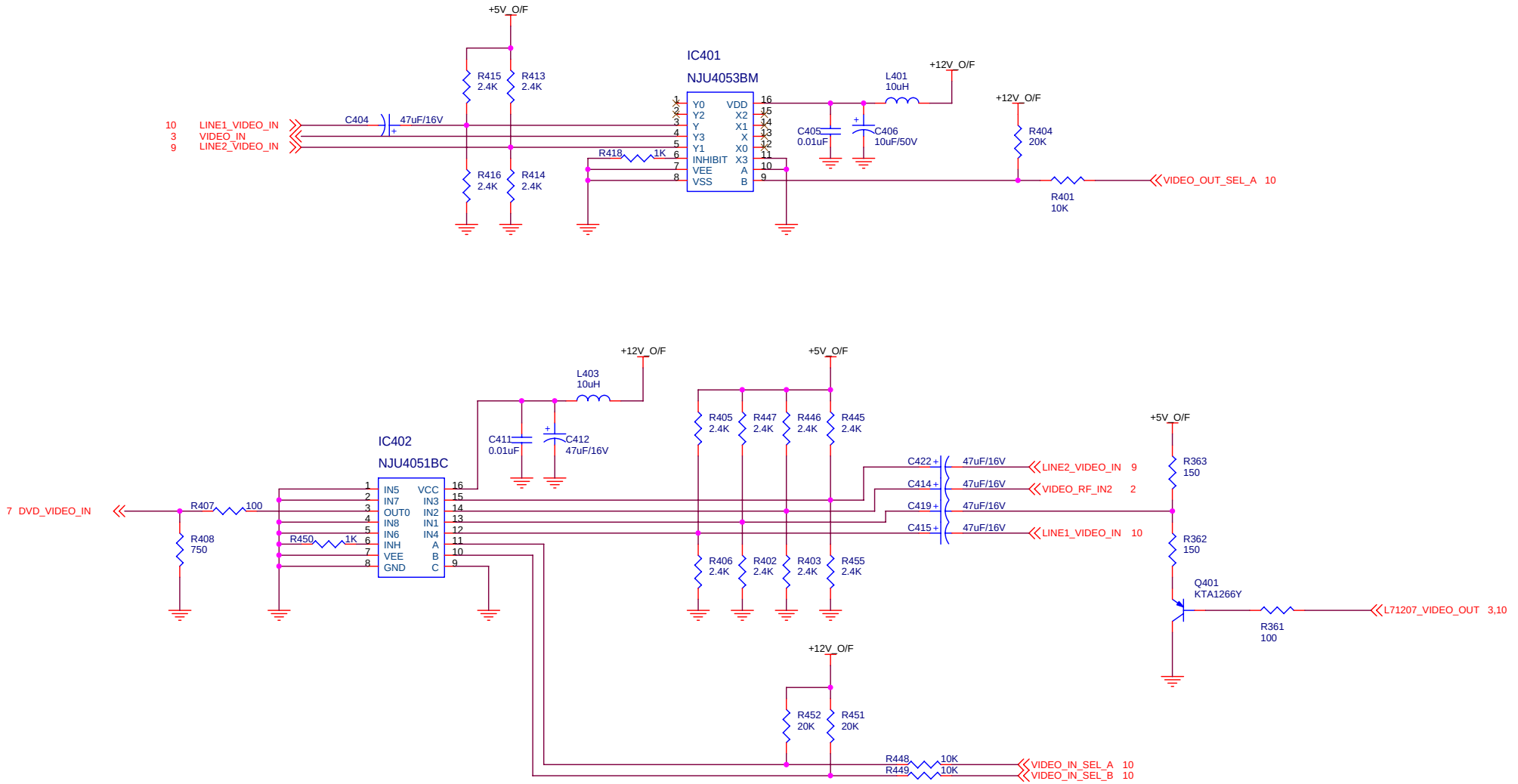




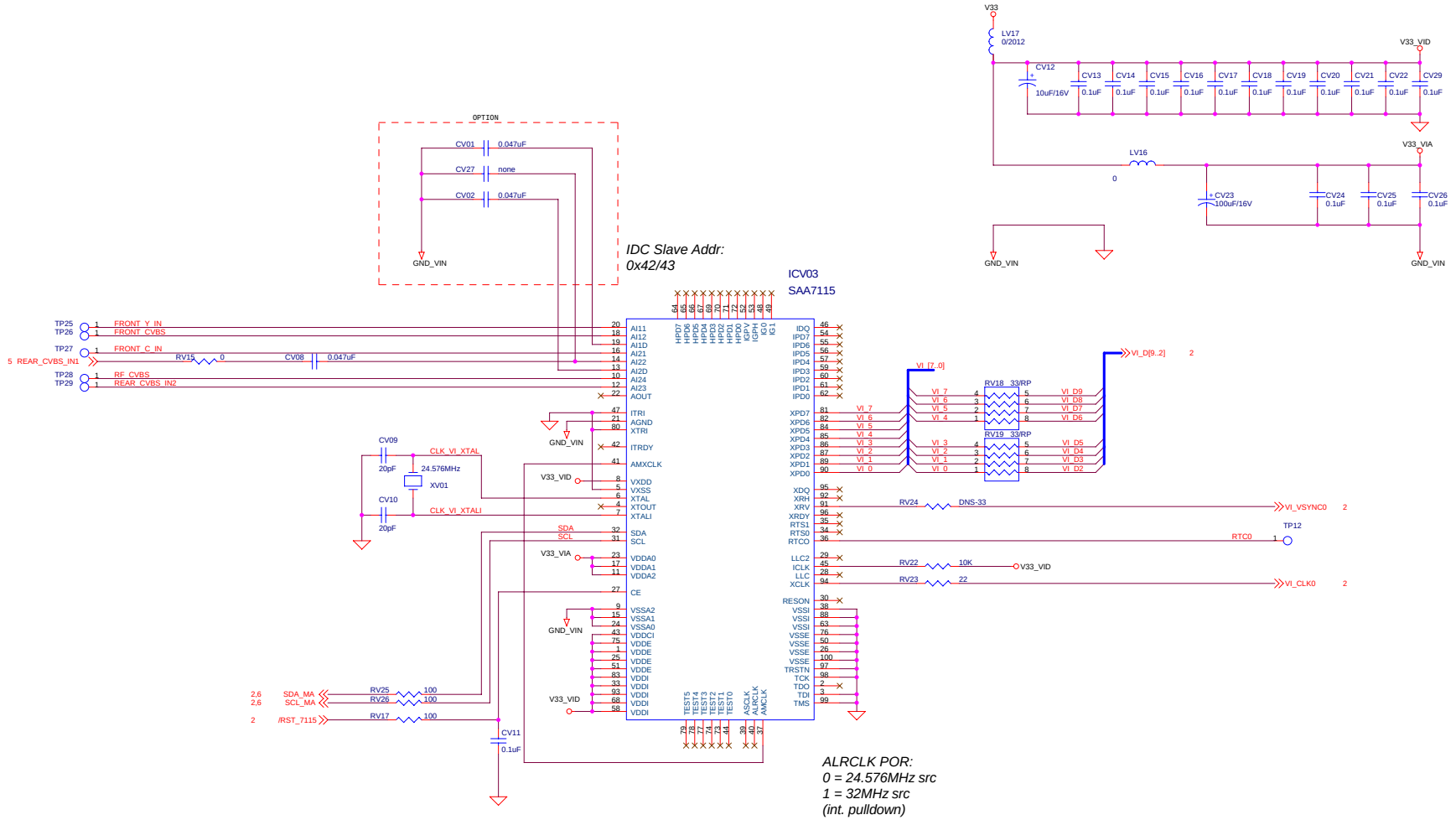


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
W.K.Ihm	W.K.Ihm	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO.	1.0
DAEWOO ELECTRONICS Digital Media Lab.				08 : PWR CONN	

SHEET 8 / 9

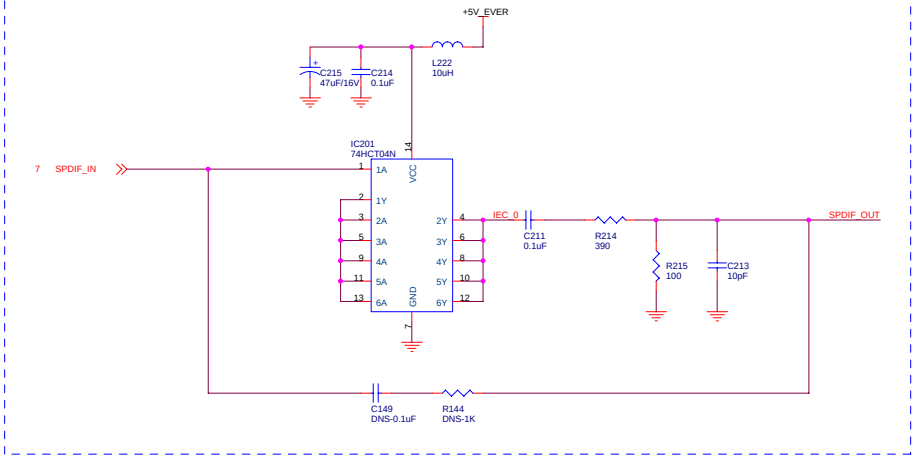


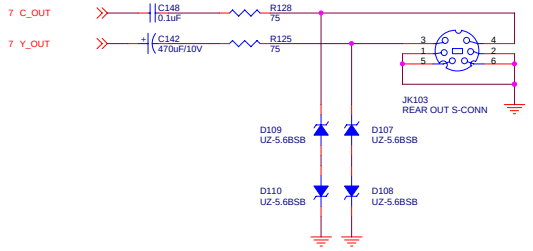
DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
J.H.Lim	J.H.Lim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team			REV NO. 2.0	SHEET	8 / 10
DAEWOO ELECTRONICS Digital Media Lab.			08 : VIDEO SWITCH		

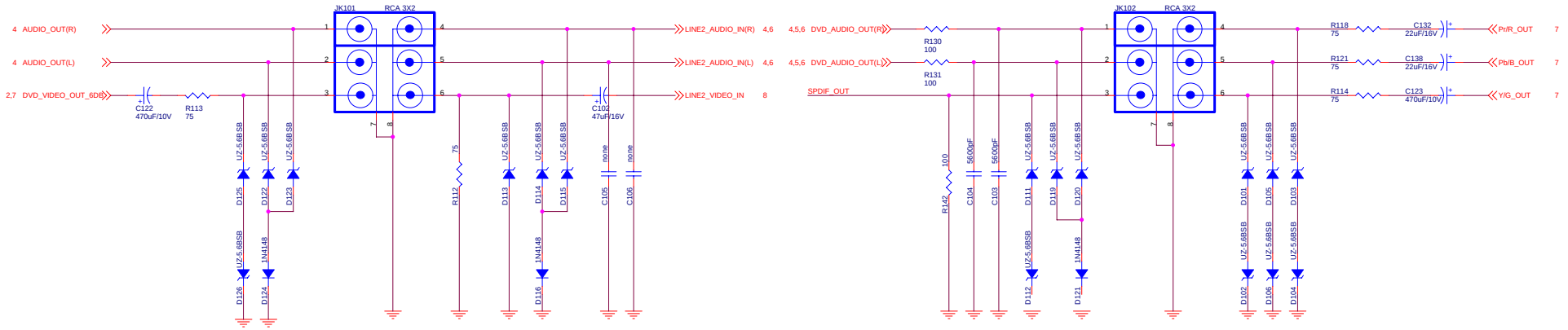


DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
M.K.Lee	M.K.Lee	S.D.Park	B.Y.Choi	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 1.0	SHEET 9 / 9
DAEWOO ELECTRONICS Digital Media Lab.				10 : VIDEO IN _SAA7115	

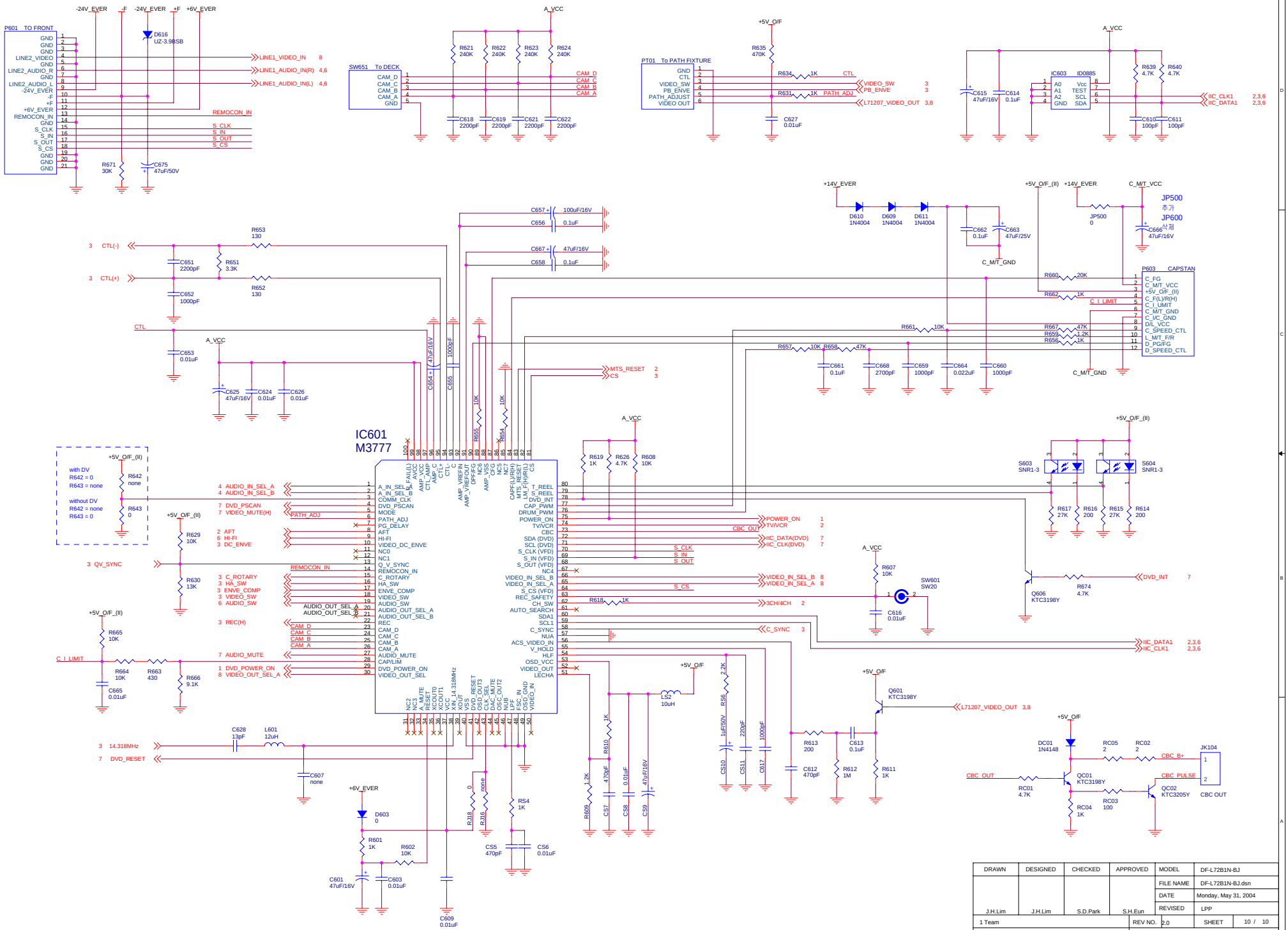
DIGITAL AUDIO OUT







DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
J.H.Lim	J.H.Lim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team				REV NO. 2.0	SHEET 9 / 10
DAEWOO ELECTRONICS Digital Media Lab.				09 : DIGITAL AUDIO OUT & JACK	



DRAWN	DESIGNED	CHECKED	APPROVED	MODEL	DF-L72B1N-BJ
				FILE NAME	DF-L72B1N-BJ.dsn
J.H.Lim	J.H.Lim	S.D.Park	S.H.Eun	DATE	Monday, May 31, 2004
				REVISED	LPP
1 Team			REV NO. 2.0	SHEET	10 / 10
DAEWOO ELECTRONICS Digital Media Lab.			10 : MICOM		

POWER SUPPLY SCHEMATIC DIAGRAM (VCR DVD+RW Combo AC120V)