

REALTEK

RTL8711AM

SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.0	2014/09/30	Preliminary release.
R1V7	2015/09/25	1. correct feature list 2. modify block diagram 3. correct programming space, IO space and extension memory space 4. correct pin function group table 5. correct memory system 6. modify electrical characteristics
R1V8	2015/11/10	1. modify ADC
R1V9	2015/12/10	1. add operating temperature for industrial standards
R1V10	2016/1/7	1. correct source clock of timer
R1V11	2016/2/16	1. correct pin function group table
R1V12	2016/5/13	1. correct power trap table

Revision	Release Date	Summary
R1V13	2016/10/1	1. modify boot scenario description 2. Modify pin mux table 3. add LS-UART
R1V14	2016/10/14	1. correct IO characteristic table
R1V15	2016/12/23	1. add power sequence
R1V16	2017/2/8	1. Correct package specification
R1V17	2017/7/18	1. Modify application diagram
R1V18	2017/7/19	1. Modify I2S/PCM

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1. General Description

Realtek RTL8711AM is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-Cortex M3 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

RTL8711AM integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

2. Features

General

- Package QFN56
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol
- WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- 1 high speed UART interface with baud rate up to 4MHz
- 1 log UART with standard baud rate support
- Maximum 3 I2C interface
- I2S with 8/16/24/32/48/96/44.1/88.2 KHz sampling rate
- Maximum 2 PCM with 8KHz sample rate
- 1 SPI supported. One supports baud rate up to 20.8 MHz
- Support 4 PWM with configurable duration and duty cycle from 0 ~ 100%
- Support 4 External Timer Trigger Event (ETE function) with configurable period in low power mode
- Support ADC with 1 channel
- Maximum 19 GPIO pins

3. Block Diagram

3.1. Functional Block Diagram

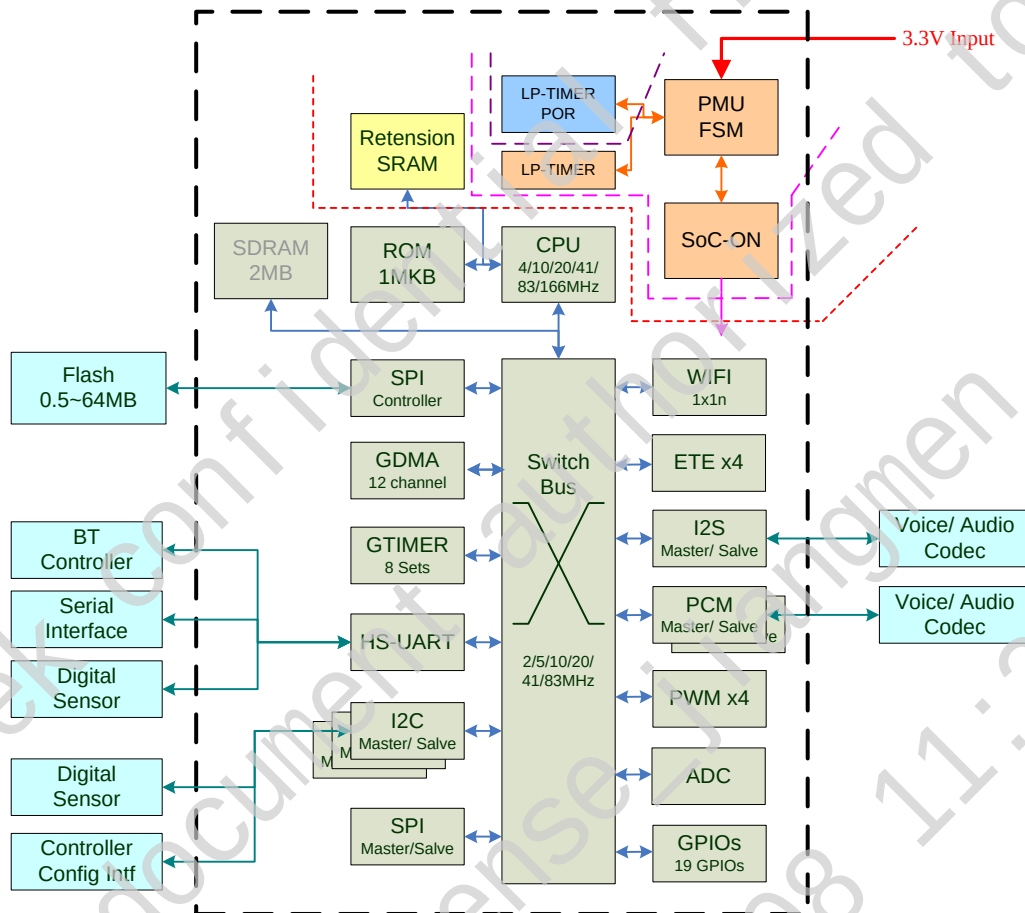


Figure 1. Block Diagram

3.2. WIFI and NFC Application Diagram

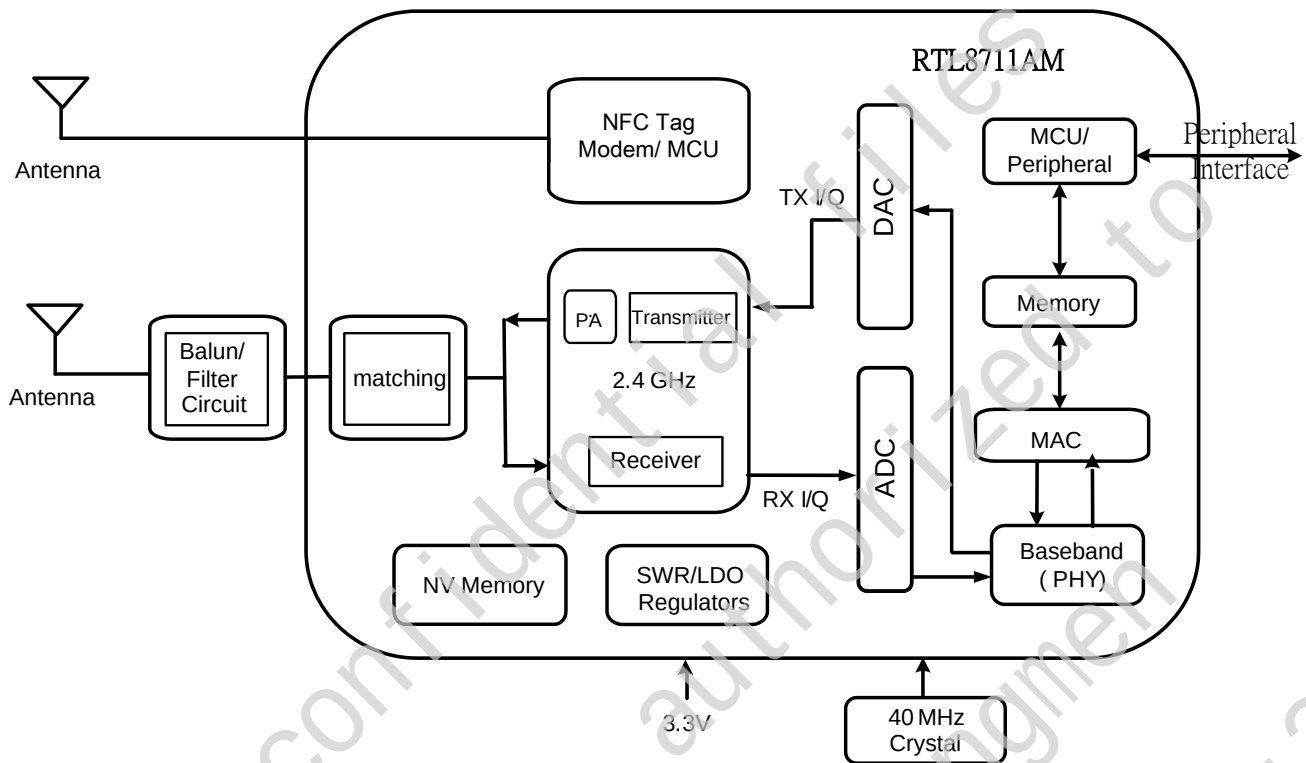


Figure 2. Single-Band 11n (1x1) and NFC Tag Solution

3.3. Power Supply Application Diagram

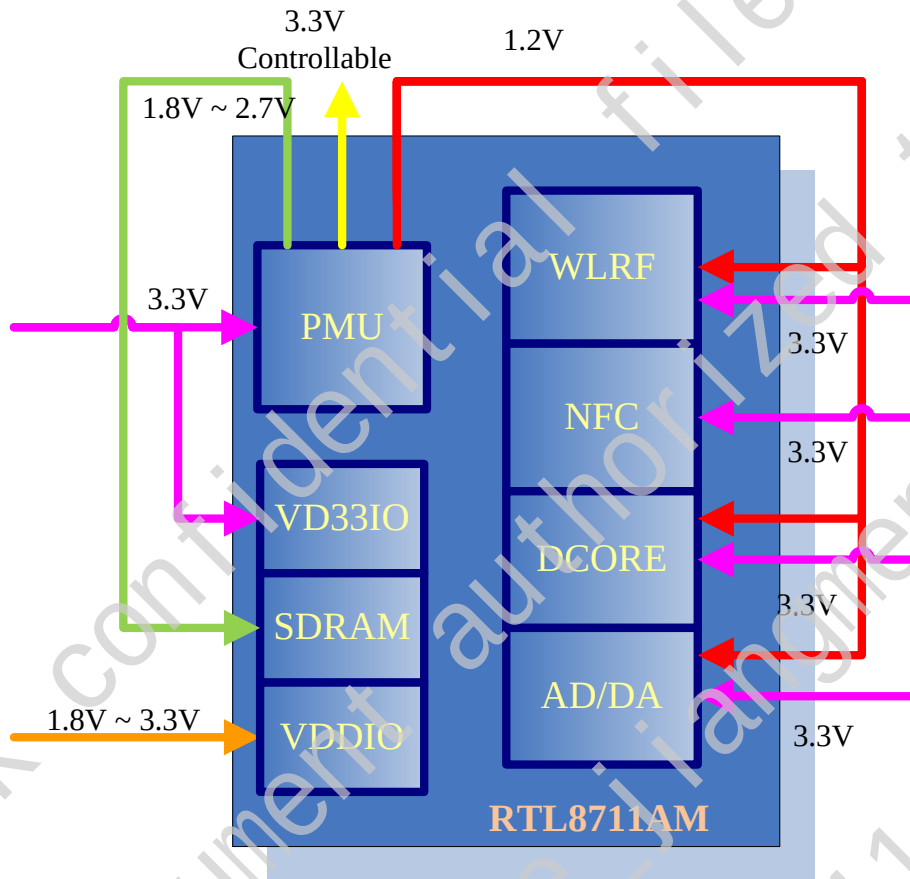


Figure 3. Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V power bulk or LDO selectable.
- 1.8~2.7V LDO
- 3.3V power source integrated power cut controlled by FW.

4. Memory Mapping

4.1. Programming Space

Name	Mode	Physical	Size	IP Function
Code		0x0000_0000	1MB	Instruction Memory (ROM)
		0x000F_FFFF		
		0x1000_0000	448KB	Inter SRAM: BD SRAM and Buffer SRAM share total 448KB physical sram
		0x1006_FFFF		
		0x1FFF_0000	64KB	TCM (Tightly-Coupled Memory) SRAM
		0x1FFF_FFFF		
SRAM		0x3000_0000	2MB	SDR SDRAM memory
		0x301F_FFFF		

4.2. IO Space

Name	Mode	Physical Address	Size	IP Function
Peripheral		0x4000_0000	4KB	SYS Control (SYSON)
		0x4000_0FFF		
		0x4000_1000	2KB	GPIO Control
		0x4000_17FF		
		0x4000_1800		RSVD
		0x4000_1FFF		
		0x4000_2000	4KB	Timer Control
		0x4000_2FFF		
		0x4000_3000	1KB	UART for Log
		0x4000_33FF		
		0x4000_3400	1KB	I2C_2 Control
		0x4000_37FF		
		0x4000_3800	1KB	I2C_3 Control
		0x4000_3BFF		
		0x4000_3C00		RSVD
		0x4000_4FFF		
		0x4000_5000	4KB	SDR SDRAM controller
		0x4000_5FFF		
		0x4000_6000	4KB	SPI flash controller
		0x4000_6FFF		
		0x4000_7000		RSVD
		0x4000_FFFF		
		0x4001_0000	4KB	ADC
		0x4001_0FFF		
		0x4001_1000	4KB	DAC
		0x4001_1FFF		

Name	Mode	Physical	Size	IP Function
Peripheral		0x4004_0000	1KB	UART_0 Control
		0x4004_03FF		
		0x4004_0400	1KB	RSVD
		0x4004_07FF		
		0x4004_0800	1KB	RSVD
		0x4004_0BFF		
		0x4004_0C00		RSVD
		0x4004_1FFF		
		0x4004_2000	1KB	SPI_0 Control
		0x4004_23FF		
		0x4004_2400	1KB	RSVD
		0x4004_27FF		
		0x4004_2800	1KB	RSVD
		0x4004_2BFF		
		0x4004_2C00		RSVD
		0x4004_3FFF		
		0x4004_4000	1KB	RSVD
		0x4004_43FF		
		0x4004_4400	1KB	I2C_1 Control
		0x4004_47FF		
		0x4004_4800		RSVD
		0x4004_FFFF		

Name	Mode	Physical	Size	IP Function
Peripheral		0x4005_0000	16KB	RSVD
		0x4005_3FFF		
		0x4005_4000		
		0x4005_7FFF	16KB	RSVD
		0x4005_8000		
		0x4005_BFFF		
		0x4005_C000	2KB	RSVD
		0x4005_FFFF		
		0x4006_0000		
		0x4006_07FF	2KB	GDMA0
		0x4006_0800		
		0x4006_0FFF		
		0x4006_1000	2KB	RSVD for other DMA
		0x4006_17FF		
		0x4006_1800		
		0x4006_1FFF		GDMA1



Name	Mode	Physical	Size	IP Function
Peripheral		0x4006_2000	1KB	RSVD
		0x4006_23FF		
		0x4006_2400	3KB	RSVD
		0x4006_2FFF		
		0x4006_3000	1KB	I2S_1 Control
		0x4006_33FF		
		0x4006_3400	3KB	RSVD
		0x4006_3FFF		
		0x4006_4000	1KB	PCM_0 Control
		0x4006_43FF		
		0x4006_4400		RSVD
		0x4006_4FFF		
		0x4006_5000	1KB	PCM_1 Control
		0x4006_53FF		
		0x4007_0000	16KB	Security Engine
		0x4007_3FFF		
		0x4007_4000	48KB	RSVD
		0x4007_FFFF		
		0x4008_0000	256KB	WIFI REG & TX/RX FIFO direct map
		0x400B_FFFF		
		0x400C_0000	256KB	RSVD
		0x400F_FFFF		
		0x403F_FFFF	1MB	RSVD

4.3. Extension Memory Space

Name	Mode	Physical	Size	IP Function
Flash		0x9800_0000	64MB	External flash memory
		0x9BFF_FFFF		

5. Pin Assignments

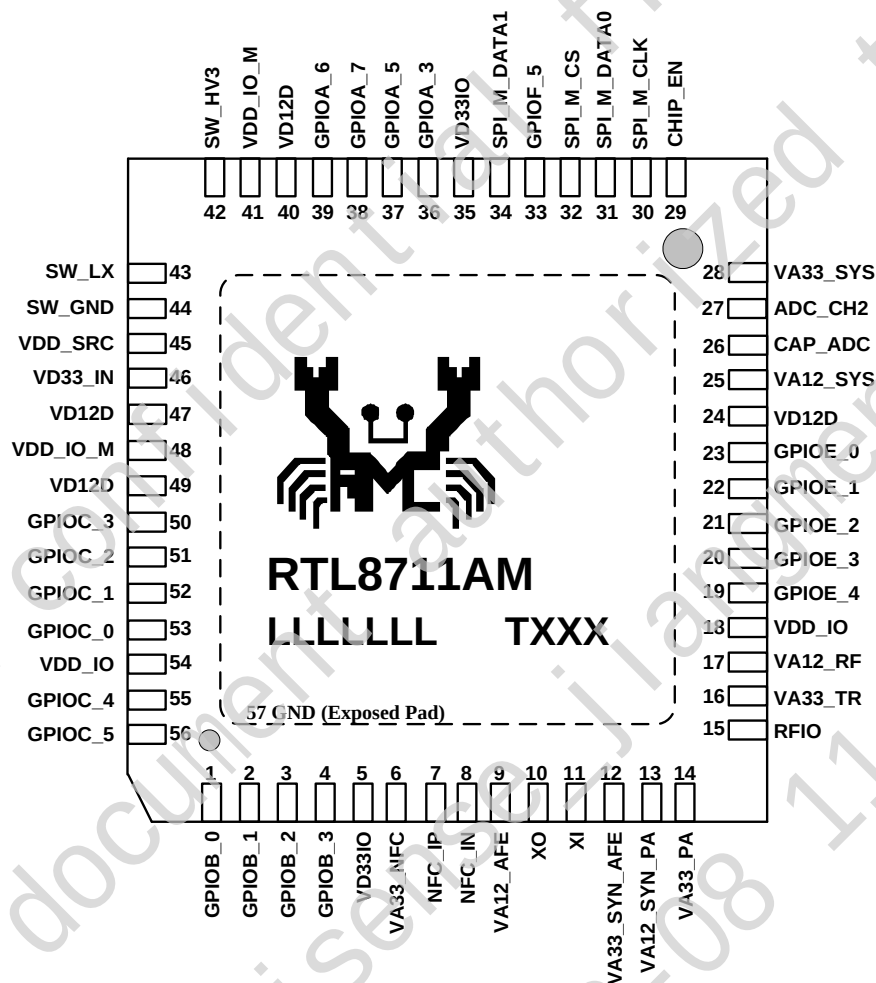


Figure 4. Pin Assignments

5.1. Package Identification

The version is shown in the location marked 'V' in Figure 4, e.g., A0=Version A0

6. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

6.1. Power On Trap Pin

Table 1. Power On Trap Pins

Symbol	Type	Pin No	Description
NORMAL_MODE_SEL	I	3	Shared with GPIOB_2 1: Normal operation mode 0: Enter into test/debug mode
BOOT_SCENARIO	I	1	Shared with GPIOB_0 0: Normal booting 1: Reserved for RTK testing
EEPROM_SEL	I	33	Shared with GPIOF_5 0: Internal NV memory select 1: reserved for RTK testing
SD_DEV_SEL	I	38	Shared with GPIOA_7 1: SDMMC Host mode 0: SDIO device mode (8711AM not support)
ICFG0	I	53	Shared with GPIOC_0 When NORMAL_MODE_SEL is "0", then ICFG0 is test mode BIT0.
ICFG1	I	52	Shared with GPIOC_1 When NORMAL_MODE_SEL is "0", then ICFG1 is test mode BIT1.

Symbol	Type	Pin No	Description
ICFG2	I	51	Shared with GPIOC_2 When NORMAL_MODE_SEL is "0", then ICFG2 is test mode BIT2.
ICFG3	I	50	Shared with GPIOC_3 When NORMAL_MODE_SEL is "0", then ICFG3 is test mode BIT3.

6.2. Analog to DC Converter

Table 2. ADC Pins

Symbol	Type	Pin No	Description
ADC_CH2	I	27	AD converter input
CAP_ADC	P	26	Capacitor for AD converter power.

NOTE: The unused pins are suggested to keep floating.

6.3. RF and NFC

Table 3. RF and NFC Pins

Symbol	Type	Pin No	Description
NFC_IP	I	7	NFC input differential signal
NFC_IN	I	8	NFC input differential signal
RF_IO	IO	15	WL RF signal

NOTE: The unused pins are suggested to keep floating.

6.4. Power Pins

Table 4. Power Pins

Symbol	Type	Pin No	Description
SW_LX	P	43	Switching Regulator Output
SW_HV3	P	42	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VA33	P	6, 12, 14, 16, 28,	3.3V for Analog Circuit
VD33IO	P	5, 35	VDD3.3V for Digital IO
VDD_IO	P	18, 54	GPIOE and GPIOC group IO power
VDD_IO_M	P	41, 48	Embedded SDR DRAM power
VD12D	P	24, 40, 47, 49	VDD 1.2V Digital Circuit
VA12	P	9, 13, 17, 25	1.2V for analog blocks
SW_GND	P	44	Switching Regulator Ground

6.5. Clock Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	11	40MHz OSC Input Input of 40MHz Crystal Clock Reference
XO	O	10	Output of 40MHz Crystal Clock Reference

6.6. Chip Enable Pin

Table 6. Chip Enable Pin

Symbol	Type	Pin No	Description
CHIP_EN	I	29	Whole chip enable control. When asserted, chip function is enabled; when de-asserted, whole chip is shutdown.

6.7. NOR Flash Interface

Table 7. NOR Flash Pins

Symbol	Type	Pin No	Description
SPI_M_CLK	IO	30	NOR Flash CLK signal. Multiplexed with GPIOF_1 .
SPI_M_DATA0	IO	31	NOR Flash CLK signal. Multiplexed with GPIOF_2 .
SPI_M_CS	IO	32	NOR Flash CLK signal. Multiplexed with GPIOF_0 .
SPI_M_DATA1	IO	34	NOR Flash CLK signal. Multiplexed with GPIOF_3 .

6.8. Digital IO Pins

Please refer to Section 7 Pin Function Table for more detailed information.

Table 8. IO Pins

Symbol	Type	Pin No	Description
GPIOB_0	IO	1	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_1	IO	2	GPIO pin. The MUX function can be referred to Pin Function Table.

Symbol	Type	Pin No	Description
GPIOB_2	IO	3	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_3	IO	4	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_0	IO	23	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_1	IO	22	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_2	IO	21	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_3	IO	20	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_4	IO	19	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_3	IO	36	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_5	IO	37	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_7	IO	38	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_6	IO	39	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_0	IO	53	GPIO pin. The MUX function can be referred to Pin Function Table.

Symbol	Type	Pin No	Description
GPIOC_1	IO	52	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_2	IO	51	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_3	IO	50	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_4	IO	55	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_5	IO	56	GPIO pin. The MUX function can be referred to Pin Function Table.

NOTE: GPIO group F is not open for customer.

NOTE: The unused pins are suggested to keep floating.

Table 9. GPIO Characteristic

Symbol	Interrupt	Schmitt trigger	Driving ¹ (mA)	Default state ²	Sleep Mode, shutdown
GPIOB_0	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOB_1	N	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOB_2	N	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOB_3	Y	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_0	N	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)

Symbol	Interrupt	Schmitt trigger	Driving ¹ (mA)	Default state ²	Sleep Mode, shutdown
GPIOE_1	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_2	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_3	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_4	N	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_3	N	Y	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_5	N	N	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_6	N	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_7	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_0	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_1	Y	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_2	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_3	Y	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_4	Y	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOC_5	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or

Symbol	Interrupt	Schmitt trigger	Driving ¹ (mA)	Default state ²	Sleep Mode, shutdown
					Hi (Configurable)

NOTE1: The driving configuration is operated by group.

NOTE2: PH = Pull-High, HI = High-impedance

7. Pin Function Table

7.1. Pin Configurable Function Group Summary Table

Table 10. Pin Function Group Table

PIN name	JTAG	UART Group	I2C Group	SPI Group	I2S Group	PCM Group	WL_LED	PWM	ETE	WKDT
GPIOA_3		UART0_RTS								
GPIOA_5		UART0_CTS								D_STBY0
GPIOA_6		UART0_IN								
GPIOA_7		UART0_OUT								
GPIOB_0		UART_LOG_OUT							ETE0	
GPIOB_1		UART_LOG_IN					WL_LED0		ETE1	D_SLPO
GPIOB_2			I2C3_SCL						ETE2	
GPIOB_3			I2C3_SDA						ETE3	
GPIOC_0		UART0_IN		SPI0_CS0	I2S1_WS	PCM1_SYNC		PWM0	ETE0	
GPIOC_1		UART0_CTS		SPI0_CLK	I2S1_CLK	PCM1_CLK		PWM1	ETE1	
GPIOC_2		UART0_RTS		SPI0_MOSI	I2S1_SD_TX	PCM1_OUT		PWM2	ETE2	
GPIOC_3		UART0_OUT		SPI0_MISO	I2S1_MCK	PCM1_IN		PWM3	ETE3	
GPIOC_4			I2C1_SDA	SPI0_CS1	I2S1_SD_RX					
GPIOC_5			I2C1_SCL	SPI0_CS2						
GPIOE_0	JTAG_TRST	UART0_OUT	I2C2_SCL	SPI0_CS0		PCM0_SYNC		PWM0		
GPIOE_1	JTAG_TDI	UART0_RTS	I2C2_SDA	SPI0_CLK		PCM0_CLK		PWM1		
GPIOE_2	JTAG_TDO	UART0_CTS	I2C3_SCL	SPI0_MOSI		PCM0_OUT		PWM2		
GPIOE_3	JTAG_TMS	UART0_IN	I2C3_SDA	SPI0_MISO		PCM0_IN		PWM3		D_STBY3
GPIOE_4	JTAG_CLK			SPI0_CS1						

NOTE1: The Function Pin is enabled via entire group, the un-used pin can not disable separately. Ex: if using JTAG in SWD mode, the pin: JTAG_TRST, JTAG_TDI and JTAG_TDO can not be used as GPIO in the same time.

NOTE2: GPIO group F is not open for customer.

8. Functional Description

8.1. Power Management Control Unit

8.1.1. Features

The PMU provides the following functions:

Bulk/LDO to output 1.2V

LDO to output 1.8V ~ 2.5V power source

Integrated power cut to output Vref (input from VD33_IN) with SW controllable

2 very Low power clock source with less accuracy: 1K and 250K

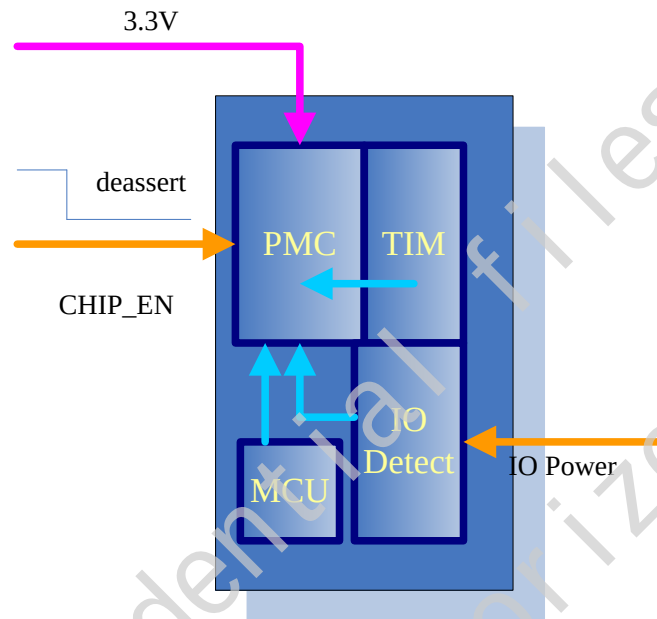
1 low power 32.768KHz clock source with moderate accuracy

Wakeup system detector to resume from low power state

8.1.2. Power Mode Description

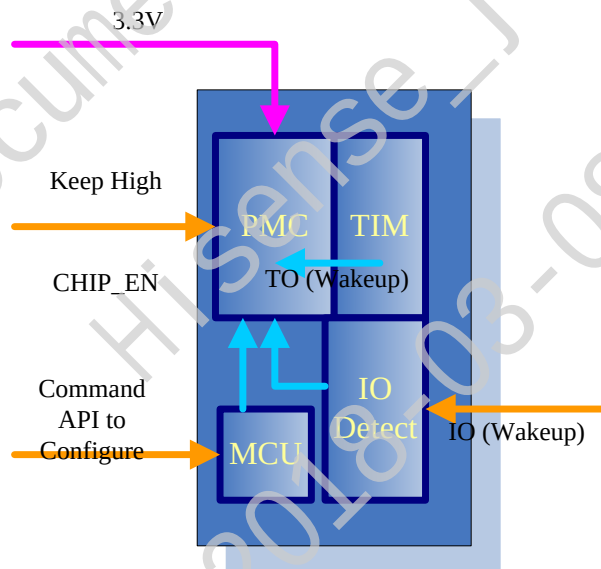
8.1.2.1 Shutdown Mode

CHIP_EN de-asserts to shutdown whole chip without external power cut components required.



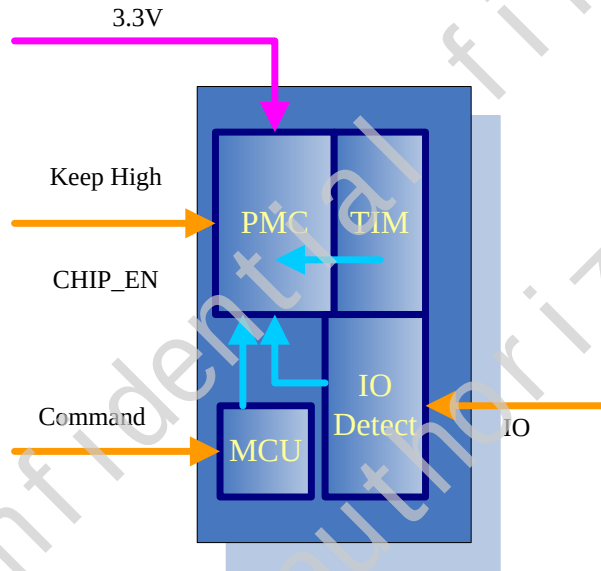
8.1.2.2 Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



8.1.2.3 Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



8.2. Memory System

8.2.1. Memory Architecture

RTL8711AM integrates ROM, internal SRAM, extended SDRAM, extended NOR flash to provide applications with a variety of memory requirements.

8.2.2. Internal ROM

RTL8711AM integrates a 1MB high access-speed and low leakage internal ROM. The internal ROM memory is clocked at a speed up to 166MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Default UART driver
- Non-flash booting functions and drivers

- Peripheral libraries
- Security function libraries

8.2.3. Internal SRAM

448KB SRAM is integrated to provide for instruction, data, and buffer usage. The maximum clock speed is up to 166MHz.

An additional 64KB fast access data memory (TCM) is provided for FW data section. The range is 0x1FFF-0000 ~ 0x1FFF-FFFF.

8.2.4. Extended SDR DRAM

8.2.4.1 Features

- Interface (Bus Width): 16-bit
- Targeted SDR Frequency: Up to 83MHz
- Supports one Chip Select (MCS0#) and 1 Band select (BA0)

8.2.4.2 SDR DRAM Input Timing

Table 11. SDR DRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
TSETUP	Input Setup Prior to Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	1.13	-	ns
THOLD	Input Hold Time after the Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	0	-	ns

Note: The RTL8196EU integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls).

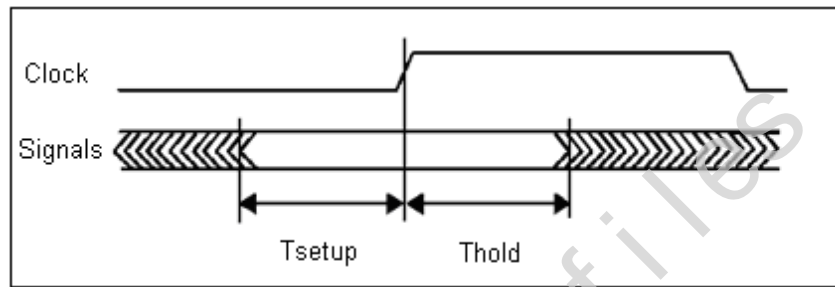


Figure 5. SDR DRAM Input Timing

8.2.4.3 SDR DRAM Output Timing

Table 12. SDR DRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
TCLK2O UT	Rising Edge of Clock-to-Signal Output Outputs include this timing are MD[15:0], MCS0#, MCS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation)	-	-	2.3	ns
THOLDO UT	Signal Output Hold Time after the Rising Edge of the Clock Outputs included in this timing are MD[15:0] (during a write operation)	0.8	-	-	ns

Note: Timing was tested with 75-pF capacitor to ground.

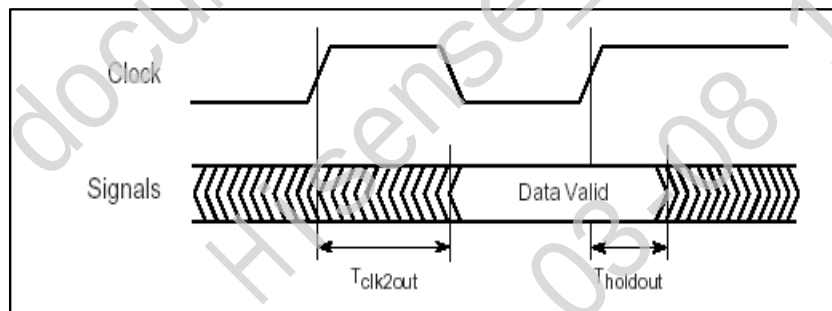


Figure 6. SDR DRAM Output Timing

8.2.4.4 SDR DRAM Access Control Timing

Table 13. SDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
TREFRESH	Auto-Refresh Timing Controlled by Reg. 0xB8001008 (DTR)	μs	-
TRCD	The Time Interval between RAS# Active and CAS# Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
TRP	The Time Interval between Pre-Charge and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
TRAS	The Time Interval between Active and Pre-Charge Controlled by Reg. 0xB8001008 (DTR)	ns	-
TRC	The Time Interval between Active and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	1
TRFC	The Time Interval between Auto-Refresh and Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
TCAS_LATE NCY	The Data Output Delay after CAS# Active Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

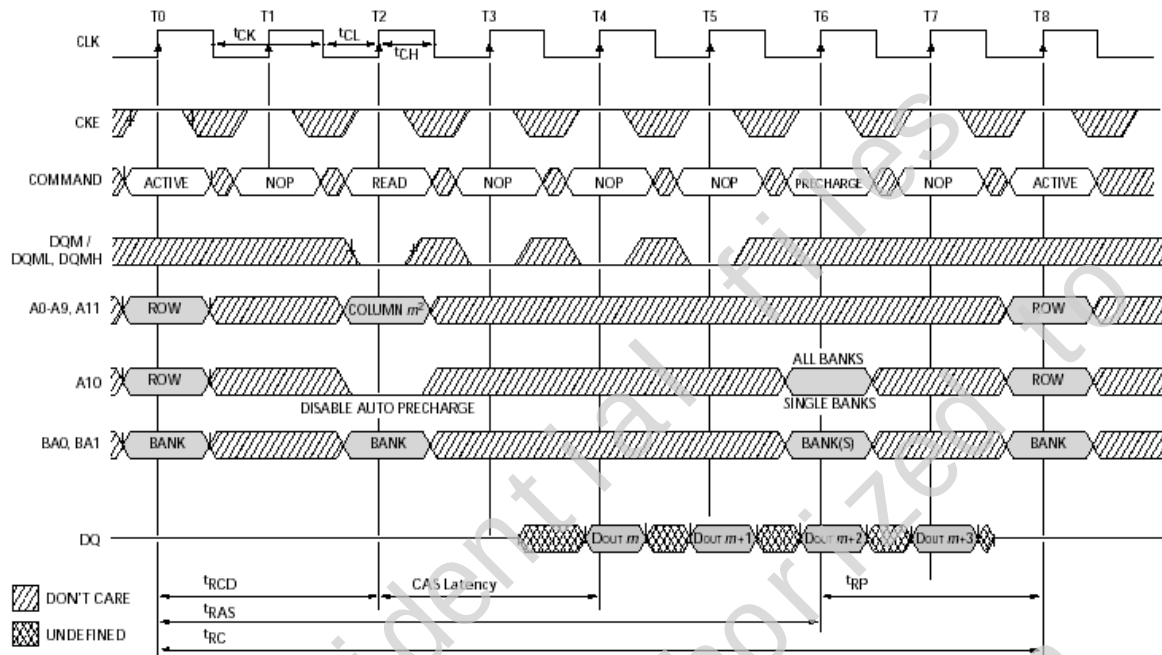


Figure 7. SDR DRAM Access Control Timing

8.2.5. SPI NOR Flash

8.2.5.1 Features

- Targeted SPI flash frequency: Up to 83.3MHz (when CPU clock is 166MHz)
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

8.2.5.2 Supported NOR Flash List

Table 14. Flash Bus DC Parameters

Vendor	Part Number	Density	Voltage	IO
MXIC	MXIC_MX25L4006E	4M Bits	3.3V	1I/2O
MXIC	MXIC_MX25L8073E	8M Bits	3.3V	1I/2O

Vendor	Part Number	Density	Voltage	IO
MXIC	MXIC_MX25L8006E	8M Bits	3.3V	1I/2O

8.2.5.3 Electrical Specifications

Table 15. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
VIH	Input-High Voltage	LVTTL	2.0	-	-	V	1
VIL	Input-Low Voltage	LVTTL	-	-	0.8	V	2
VOH	Output-High Voltage	-	2.4	-	-	V	3
VOL	Output-Low Voltage	-	-	-	0.4	V	3
IIL	Input-Leakage Current	VIN=3.3V or 0	-10	±1	10	μA	-
IOZ	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
RPU	Input Pull-Up Resistance	-	-	75	-	KΩ	4
RPD	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: $V_{IH} (MAX) = V_{DDH} + 2V$ for a pulse width $\leq 3ns$.

Note 2: V_{IL} undershoot: $V_{IL} (MIN) = -2V$ for a pulse width $\leq 3ns$.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

8.3. General Purpose DMA Controller

8.3.1. Features of GDMA

- Dual port DMA with totally 12 channels
- Configurable endian
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support block level flow control
- Support address auto-reload, link-listed mode
- Support scatter-gather mode

8.4. General Purpose Timer (GTimer)

8.4.1. Features of GTIMER

- 8 Gtimers supported
- Source clock is 32.768KHz
- Support Counter mode and timer mode

8.5. GPIO Functions

8.5.1. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

8.6. UART Interface Characteristics

The RTL8711AM UART is used for serial communication with a peripheral, modem (data carrier equipment, or data set).

8.6.1. Features of UART

- Support 1 HS-UART (max baud rate 4MHz and DMA mode) and 1 low speed UART (IO mode)
- UART (RS232 Standard) Serial Data Format
- Transmit and Receive Data FIFO
- Programmable Asynchronous Clock Support
- Auto Flow Control (HS-UART only)
- Programmable Receive Data FIFO Trigger Level (HS-UART only)
- DMA data moving support to save CPU loading (HS-UART only)

8.6.2. High Speed UART Specification

HS-UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the RTL8711AM provides multiple UART clocks.

Table 16. HS-UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)	Desired Baud Rate	Actual Baud Rate	Error (%)
100	110.002288	0.00208004	14400	14412.54468	0.0871158
300	300.0192012	0.00640041	19200	19201.22888	0.00640041
600	600.0384025	0.00640041	28800	28815.12218	0.0525076
1200	1200.076805	0.00640041	38400	38402.45776	0.00640041
2400	2400.15361	0.00640041	57600	57710.06464	0.1910844
3600	4800.30722	0.00640041	76800	76946.75285	0.1910844
4800	9600.614439	0.00640041	115200	115420.1293	0.1910844
9600	9600.614439	0.00640041	128000	128205.1282	0.1602564

Desired Baud Rate	Actual Baud Rate	Error (%)
153600	153622.7026	0.0147804
230400	230840.2585	0.1910844
230400	380044.2233	0.093527
460800	460868.1079	0.0147804
500000	499001.996	0.1996008
921600	921273.0318	0.0354783
1000000	1005116.959	0.5116959
1382400	1382604.324	0.0147804
1444400	1448130.595	0.2582799
1500000	1502732.24	0.1821494

Desired Baud Rate	Actual Baud Rate	Error (%)
1843200	1840696.118	0.1358443
2000000	2010233.918	0.5116959
2100000	2107279.693	0.3466521
2764800	2761044.177	0.1358443
3000000	3015350.877	0.5116959
3250000	3273809.524	0.7326007
3692300	3696236.559	0.1066154
3750000	3756330.601	0.1821494
4000000	4020467.836	0.5116959
6000000	6030701.754	0.5116959

8.6.3. Low Speed UART Specification

Data is written from CPU over the bus to the LS-UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the LS-UART and stored for the CPU to read back. The LS-UART can not support HW flow control.

Table 17. LS-UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)
600	600	0.01
1200	1200	0.01
2400	2400	0.01
4800	4796	0.09
9600	9609	0.10
14400	14388	0.09
19200	19148	0.27
38400	38297	0.27
57600	57870	0.47
115200	115741	0.47

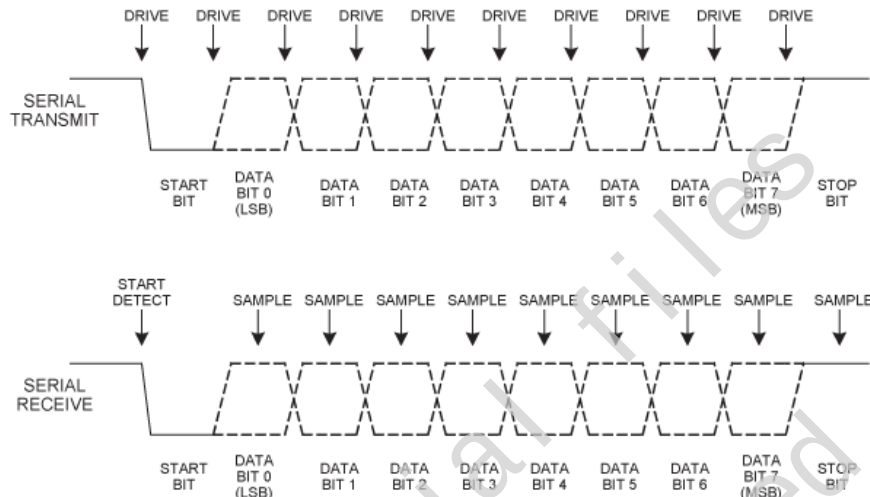


Figure 8. UART Interface Waveform

8.6.4. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AM UART interface via the IO power.

8.7. SPI Interface

8.7.1. Features of SPI

- Support 1 SPI port
- Support Master/Slave mode
- Support DMA to offload CPU bandwidth
- 1 high speed SPI
 - Support up to 3 CS (multi-slave mode up to 3 slave)
 - Support baud rate up to 20MHz (Master mode)
 - Support baud rate up to 5MHz (Slave mode Rx only)
 - Support baud rate up to 4MHz (Slave mode TRx)
- Programmable clock bit-rate

- Programmable clock polarity and phase
- Multiple Serial Interface Operations support
 - Motorola - SPI
 - Texas Instruments - SSI
 - National Semiconductor - Microwire

8.8. I²C Interface

8.8.1. Features of I²C

- Support maximum 3 I2C port
- Three speeds:
 - Standard mode (0 to 100 Kb/s)
 - Fast mode (<400 Kb/s)
 - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers
- TX and RX DMA support (I2C-1 only)

8.9. PWM Interface

8.9.1. Features of PWM

- Support maximum 4 PWM functions
- 0~100% duty can be configurable
- Use selected Gtimer interrupt as counter source
- Minimum resolution is 64us

- The period can be configured up to 8 seconds

8.10. External Trigger Event Interface

8.10.1. Features of External Trigger Event

- Support maximum 4 External Trigger Event functions without CPU active
- Triggered by GTIMER

8.11. I2S Interface Characteristics

8.11.1. Features of I2S

- Support 8/12/16/24/32/48/64/96KHz, 7.35/11.025/14.7/22.05/29/44.1/58.8/88.2KHz
- Support 16 or 24 bits format
- Integrated DMA engine to minimize SW efforts
- Support TX and RX direction
- Master or Slave mode support

8.12. PCM Interface Characteristics

8.12.1. Features of PCM

- The RTL8711AM supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:
- Supports Master and Slave mode
- Supports short Frame Sync
- Supports 8-bit A-law/ μ -law, and 16-bit linear PCM formats
- Supports 16 channels and 32 time slots
- Supports 8KHz sample rate

- Supports SCO/ESCO link

8.13. AD Converter

8.13.1. Features

- 1 16-bit high resolution A/D converter (ADC_CH2 only)
 - Bandwidth 48KHz
 - Input signal range: 0.01V ~ VREF - 0.2V
- Support DMA mode
- Support One-Shot sampling mode without CPU active to save power
 - Pre-configured period to auto-sampling
 - Support two wakeup method: buffer threshold interrupt and event trigger

8.14. Security Engine

8.14.1. Features

- Provide low SW computing and high performance encryption
- Supported authentication algorithms:
 - MD5
 - SHA-1
 - SHA-2 (SHA-224 / SHA-256)
 - HMAC-MD5
 - HMAC-SHA1
 - HMAC-SHA2
- Supported Encryption / Decryption mechanisms:

- DES (CBC / ECB)
- 3DES (CBC / ECB)
- AES-128 (CBC / ECB / CTR)
- AES-192 (CBC / ECB / CTR)
- AES-256 (CBC / ECB / CTR)

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 18. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature(CS)	-20	+85	°C
Ambient Operating Temperature(IS) ¹	-40	+105	°C
Junction Temperature	0	+125	°C

NOTE1: ONLY RTL8711AM-VT1-CG satisfies the industrial standards (IS).

9.2. Temperature Characteristics

Table 19. Thermal Properties

Power (w)	PCB (layer)	Theta ja (C/W)	Theta jc (C/W)	Psi jt (C/W)
1	2	31	10.1	0.27
1	4	24.5	9.4	0.21

9.3. Power Supply DC Characteristics

Table 20. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33, VD33IO, SW_HV3	3.3V Supply Voltage	3.0	3.3	3.6	V
VDD_IO	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V
VA12_AFE, VA12_SYN, VA12_RF	1.2V Core Supply Voltage	1.08	1.2	1.32	V

Symbol	Parameter	Minimum	Typical	Maximum	Units
IDD33	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA
IDD_IO	IO Rating Current (including VDD_IO)			200	mA
IDD_IO_33	3.3V IO Rating Current			50	mA

9.4. Power Sequence

9.4.1. Power On or Resume from Deep Sleep

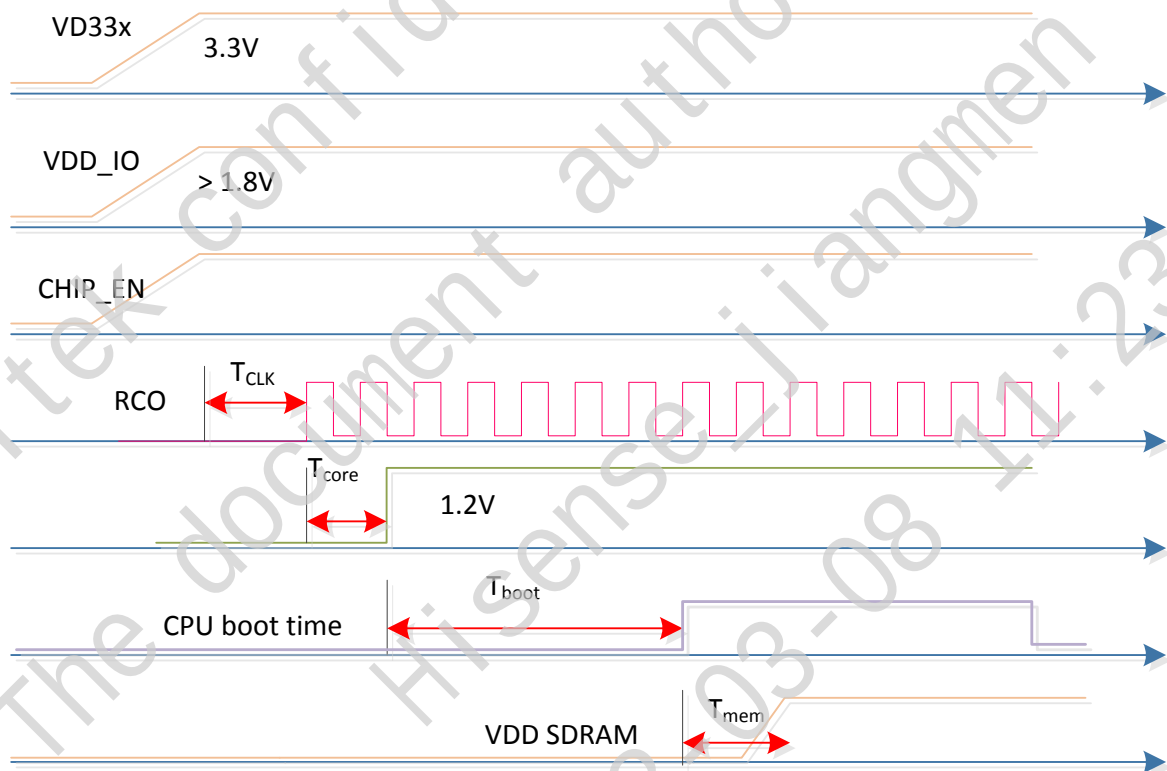


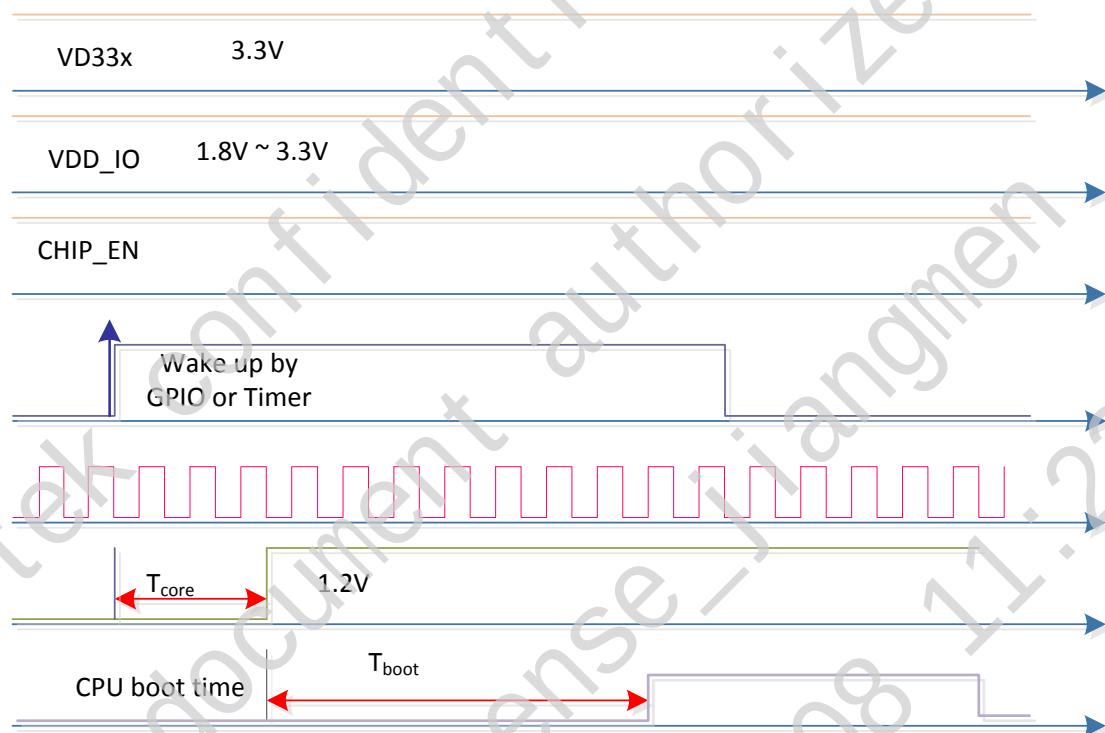
Figure 9. Power-On Sequence or Resume from Deep Sleep

Table 21. Timing spec for power on sequence

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{CLK}	Internal ring clock stable time after 3.3V ready	1			ms
T_{core}	Core power ready time	1.5	1.5		ms
T_{boot}	1.2V Core Supply Voltage	200	200		ms

T_{mem} : SW controlled memory power ready time.

9.4.2. Resume from Deep Standby


Figure 10. Timing Sequence resume from Deep Standby

9.5. Digital IO Pin DC Characteristics

9.5.1. Electrical Specifications

Table 22. Typical Digital IO DC Parameters (3.3V Case)

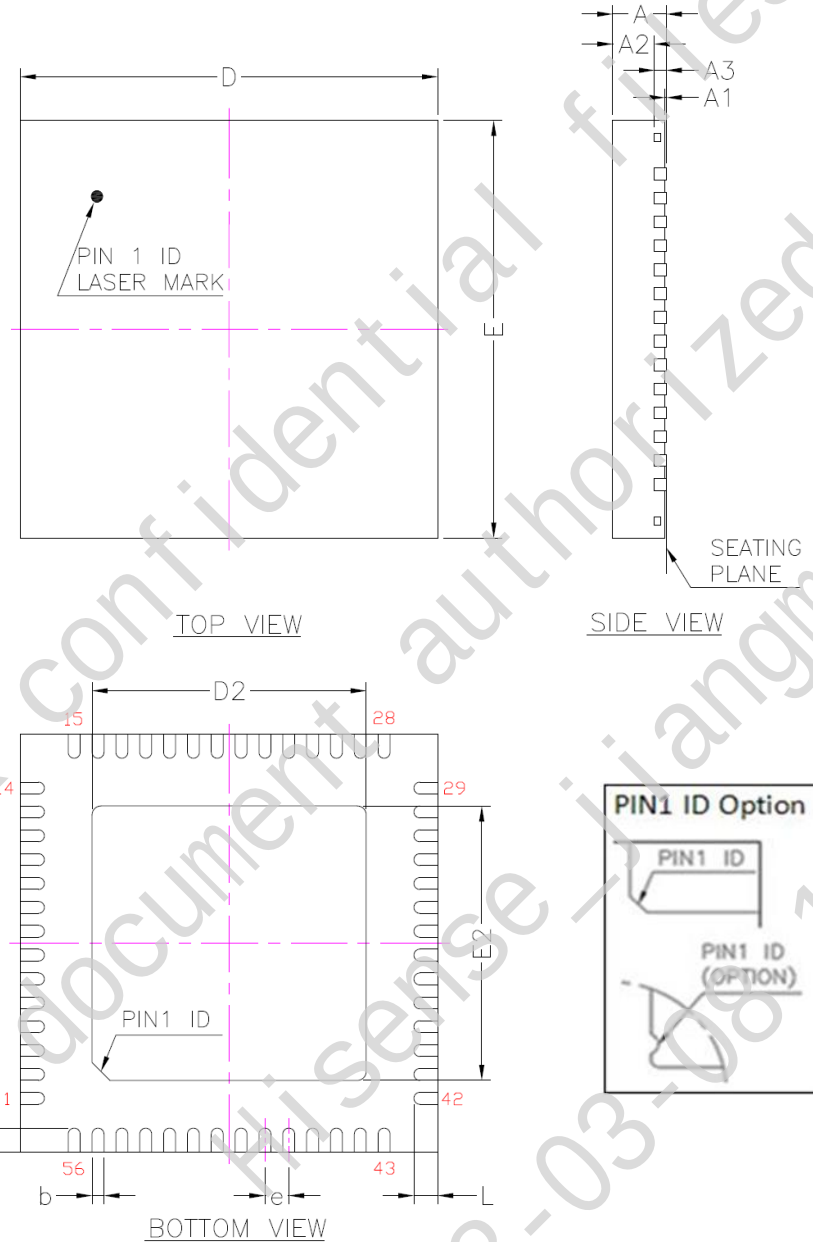
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level		1.78	1.87	1.97	V
V_{T-}	Schmitt-trigger Low Level		1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	$V_{IN}=3.3V$ or 0	-10	± 1	10	μA

Table 23. Typical Digital IO DC Parameters (1.8V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	CMOS	$0.65 \times V_{CC}$	-	-	V
V_{IL}	Input-Low Voltage	CMOS	-	-	$0.35 \times V_{CC}$	V
V_{OH}	Output-High Voltage	CMOS	$V_{CC}-0.45$	-	-	V
V_{OL}	Output-Low Voltage	CMOS	-	-	0.45	V
V_{T+}	Schmitt-trigger High Level		1.02	1.09	1.14	V
V_{T-}	Schmitt-trigger Low Level		0.67	0.73	0.8	V
I_{IL}	Input-Leakage Current	$V_{IN}=1.8V$ or 0	-10	± 1	10	μA

10. Mechanical Dimensions

10.1. Package Specification





10.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₂	---	0.65	0.70	---	0.026	0.028
A ₃	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D ₂ /E ₂	4.35	4.60	4.85	0.171	0.181	0.191
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

11. Ordering Information

Table 24. Ordering Information

Part Number	Package	Status
RTL8711AM-VA0-CG	QFN-56, 'Green' Package	Mass Production
RTL8711AM-VB1-CG	QFN-56, 'Green' Package	Mass Production
RTL8711AM-VT1-CG	QFN-56, 'Green' Package	Mass Production

Note: See page 13 for package identification.

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