

Propagator Production Testing

Rev 2, 4/18/2001 JLA

1.0 Scope

This document describes the procedures, equipment and set-ups required to manufacture and test the model PCS1900-XX Propagator repeaters.

2.0 Test Equipment

Vector Network Analyzer , 100-10000MHz
CDMA Signal Generator, 1850-1990MHz
Vector Signal Analyzer, 1850-1990 MHz
Automatic Noise Figure Meter & Noise Source, 1850-1990MHz
Spectrum Analyzer, 100-10000MHz
Current Limiting Power Supply, 8-10 volts @10 amps
Oscilloscope, 100 MHz. 1 mv
VOM
PCS 1900 Rx Band Filter
PCS 1900 Tx Band Filter
Temperature Cycling Chamber, -50 to +100 degrees centigrade

3.0 Figures Illustrations and Data Sheets

3.1 Amplifier Circuit Board Layout.
See Figure 3.1.

3.2 Amplifier Circuit Board Gain Test Set-Ups
Configure & Calibrate the VNA to measure gain (S21 and/or S12) and Return Loss (S11 and/or S22) over the 1800 to 2050 MHz range using 801 points and -10 dBm test power level prior to testing. Figure 3.2 a is the set-up for uplink channel measurements and Figure 3.2b is the set-up for downlink channel measurements.

3.3 Amplifier Circuit Board ACPR & AGC Test Set-Ups
Configure the CDMA signal generator to produce a simulated IS-95 CDMA signal with 18 active channels and configure the Vector Signal Analyzer (or Spectrum Analyzer) to measure ACPR & integrated channel power prior to testing. Figure 3.3 a is the set-up for uplink channel measurements and Figure 3.3b is the set-up for downlink channel measurements.

3.4 Amplifier Circuit Board Noise Figure Test Set-Ups
Configure the Automatic Noise figure Meter to measure noise figure over the frequency range of 1850-1990 MHz. Figure 3.4 a is the set-up for uplink channel measurements and Figure 3.4b is the set-up for downlink channel measurements.

- 3.5 Diplexer Tuning & Electronic Assembly Gain & Return Loss Test Set-Ups.
See Figure 3.5a, 3.5b & 3.5c. Configure and calibrate the VNA to measure gain (S21 and/or S12) and Return Loss (S11 and/or S22) over the 1800 to 2050 MHz range using 801 points and -10 dBm test power level prior to testing. Figure 3.5a shows the test set-up for diplexer tuning. Figures 3.5 b & 3.5c show the test set-up for Gain & Return Loss measurements.
- 3.6 Electronic Assembly ACPR & AGC Test Set-Ups
Configure the CDMA signal generator to produce a simulated IS-95 CDMA signal with 18 active channels and configure the Vector Signal Analyzer (or Spectrum Analyzer) to measure ACPR & integrated channel power prior to testing. Figure 3.6a is the set-up for uplink channel measurements and Figure 3.6b is the set-up for downlink channel measurements.
- 3.7 Electronic Assembly Noise Figure Test Set-Ups
Configure the Automatic Noise figure Meter to measure noise figure over the frequency range of 1850-1990 MHz. Figure 3.7a is the set-up for uplink channel measurements and Figure 3.7b is the set-up for downlink channel measurements.
- 3.8 Final Functional Test Set-up
See Figure 3.8
- 3.9 Amplifier Circuit Board Data Sheet
See Figure 3.9
- 3.10 Electronics Assembly and Complete Repeater Data Sheet
See Figure 3.10

4.0 Tests and Procedure Descriptions

4.1 Temperature Cycling

After all electronic components have been installed on the amplifier circuit board, the assembled board shall be subjected to 10 thermal cycles consisting of a 30 minute dwell at -50 degrees centigrade and +100 degrees centigrade with a 30 minute ramp time between temperature plateaus. The boards shall be in a non-powered state.

4.2 Initial Amplifier Board Testing:

This testing sequence occurs after the amplifier circuit boards have completed surface mount assembly and non operational temperature cycling. The purpose of this testing sequence is to confirm that the amplifier circuit board

is operating within the acceptable performance range and to complete the initial adjustment of the board mounted trimmer pots. Proceed as follows:

- 4.2.1 Mount Amplifier Circuit Board in Amplifier Test Fixture. Remove jumpers J3 & J5; set R10, R23, R30, R53, R59 & R78 to full CCW; if installed, set R32 & R49 to full CW.
- 4.2.2 Apply DC power; adjust voltage to 9 volts. Check and confirm that green power good LED D7 is illuminated. Measure and record current supplied to DUT. If red fault LED D6 is illuminated, then disconnect DC power, remove amplifier circuit board and route to the diagnosis and repair center.
- 4.2.3 When the following procedures call for measuring input return loss of either amplifier channel it will be necessary to set trimmer pots R30 & R53 to full CW and remove the 50 dB attenuator. The trimmer pots and 50 dB attenuator must be returned to their initial positions for gain measurements and subsequent adjustments.
- 4.2.4 Configure the test set-up per Figure 3.2a for uplink channel measurements or Figure 3.2b for downlink channel measurements. Carefully observe the gain and output return loss of both the uplink and down link amplifier channels over the 1800 to 2050 MHz range. The current settings will produce maximum amplifier gains. The VNA display should show smooth monotonic sweeps for all measured parameters. The minimum acceptable gain is 62 dB and the minimum acceptable return loss is 14 dB; over the 1850-1910 MHz band for the uplink amplifier, and over the 1930-1990 MHz band for the downlink amplifier. Amplifier Boards that do not meet the minimum performance specifications and/or exhibit discontinuities in the sweep performance data should be removed from the test fixture and routed to the diagnosis and repair center.
- 4.2.5 Install jumpers J3 & J5; adjust R10 & R78 to set the gain of each amplifier channel to 63 dB over the 1850-1910 MHz range for the uplink amplifier and over the 1930-1990 MHz for the downlink amplifier. If the 63 dB gain cannot be achieved in either or both channels with the jumpers in place, skip the following high gain setting resistor installation procedure for the subject channel(s) and go to 4.2.6.

Disconnect DC power. Remove jumpers J3 & J5; use the VOM to measure the resistance between terminals 1 & 3 on pots R10 & R78. Select two fixed resistors with values closest to the measured resistances of R10 & R78. Install the resistor with the value

closest to the measured resistance of R10 between the positive terminal of C20 and the junction of C126 & L67. Install the resistor with the value closest to the measured resistance of R78 between the positive terminal of C18 and the junction of C107 & L56.

- 4.2.6 Reconnect DC power. Measure and record gains and return losses over the 1850-1910 MHz range for the uplink amplifier and over the 1930-1990 MHz for the downlink amplifier. The minimum gain for each amplifier should be 63 ± 1 dB and the return losses should be 14 dB minimum. Re-install jumpers J3 & J5; now adjust R10 & R78 to set the gain of each amplifier to 53 dB. Measure and record gain over the 1850-1910 MHz range for the uplink amplifier and over the 1930-1990 MHz for the downlink amplifier. The minimum gain for each amplifier should be 53 ± 1 dB. Disconnect DC power.
- 4.2.7 Reconfigure the test set-up to measure ACPR & AGC action per Figure 3.3a. Set the CDMA input signal level to the amplifier for either the uplink or downlink channels to -93 dBm and set the center frequency to 1902.5 MHz of the uplink amplifier and/or 1982.5 MHz for the downlink amplifier. Connect DC power. Use the VSA integrated channel power measurement function to confirm the gain of both amplifier channels is 53 ± 1 dB, i.e. the amplifier output level should be -40 ± 1 dBm. Remove jumper J3 and/or J5 and confirm that the amplifier gain of both channels increases by 10 dB, i.e. output level should be -30 ± 2 dBm. Use the oscilloscope to monitor the output of the video amplifier (pin 6 of U7 or U18) of the RF amplifier channel under test while adjusting R23 or R59 to increase the gain of the video amplifier. Set the gain at a level slightly below the level at which low level sine wave oscillations in the 1-10 MHz range are detectable on the most sensitive input range for the oscilloscope. After setting the video amplifier gain of both the uplink and downlink amplifiers, incrementally increase the signal level in each amplifier until the green RSSI LED (D5 and/or D10) turns on. Record the signal level that triggers the RSSI LED for each amplifier channel.
- 4.2.8 After measuring and recording the RSSI turn-on level for each amplifier channels set the ACG controlled output power level as follows: Increase the signal level into the amplifier until the output power level is +16 dBm, then adjust the appropriate pot (R30 or R53) to reduce the output power level to +12 dBm. Now increase the input test power level by 16 dB and record the output power level of each amplifier; the maximum level is +15 dBm. Reduce the input test power level to provide a 0 dBm amplifier output

power level. Measure and record the ACPR for the three adjacent carrier channels above and below the test frequency for both the uplink and downlink amplifiers. Confirm that the ACPR levels do not exceed -45 dBc at $\pm 885\text{KHz}$, -60 dBc at $\pm 1.98\text{ MHz}$ and -50 dBc at $\pm 2.25\text{ MHz}$. Also measure and record the current sense voltages at J2 for each amplifier channel. The sense voltage can be converted to amplifier current using the formula, $\text{Current(ma)} = 100 * (\text{Sense Voltage} - 0.3)$. Increase the input test signal level to provide a AGC limited output power level of +12 dBm and measure and record the ACPR as above of both the uplink and downlink amplifiers. Again, measure and record the current sense voltages for each amplifier channel.

Now briefly short circuit board point E30 to ground with a 15 (or less) ohm, 1 watt leaded resistor; this should cause the over-current fault (red) LED D6 to turn on and the DC voltage at E63 & E64 to drop to 0 volts. Disconnect DC power from the amplifier circuit board for 2 seconds, then reconnect. The red LED should turn off when power is disconnected and the green power good LED D7 should turn on when power is reconnected. Now briefly short circuit board point E33 and confirm the same scenario of events as for the E30 short. Disconnect the DC power supply.

- 4.2.9 Reconfigure the test set-up to measure noise figure per Figure 3.4a. Connect the DC power supply. Measure and record the noise figure of both amplifier channels for both gain settings at 1903 MHz for the uplink amplifier channel and 1983 MHz for the downlink amplifier channel.

4.3 Diplexer Tuning and Final Electronics Assembly Testing

The amplifier board and two diplexer boards are assembled into the top and bottom electronic housings to form the electronics housing Assembly (PN# 740387). The purpose of this testing sequence is to tune the diplexer filters to the proper operating frequency bands and confirm all electrical performance parameters are within the acceptable range.

4.3.1 REFER TO THE MANUFACTURING ORDER PAPERWORK TO DETERMINE THE CORRECT DASH NUMBER (Frequency Band) TO BE MANUFACTURED.

- 4.3.2 Configure the test equipment per the Diplexer Tuning Test Set-Up, Figure 3.5a. Connect DC power and set the amplifier channels gain to the 63 dB position. Carefully review Figure 3.5a to determine the locations of the uplink and downlink filters (CAUTION!! each filter can be tuned to any frequency within the PCS band; double check that the filters are tuned to the proper

frequency). Tune the diplexer filters using the shorted resonator phase technique to the appropriate frequencies as indicated in the following table:

Repeater Dash #	Uplink Tune Center Frequency (MHz)	Downlink Tune Center Frequency (MHz)
-AD	1855	1945
-BE	1875	1965
-FC	1895	1985

- 4.3.3 Configure the test equipment per Figure 3.5b for Uplink Gain and Return Loss measurements and Figure 3.5c for Downlink Gain and Return Loss measurements. Measure and record gain (S21 & S12) and return loss (S11 & S22) over the 1800 to 2050 MHz frequency range. Confirm that the gains and return losses meet the requirements of the following table:

Dash #	Parameter	Frequency Range (MHz)	Gain Reqmt. (dB)	S11 & S22 (dB)
-AD	S21	1850-1870	60±1	-14 max
-AD	S21	1930-1950	-20 max	NA
-AD	S12	1930-1950	60±1	-14 max
-AD	S12	1850-1870	-20 max	NA
-BE	S21	1870-1890	60±1	-14 max
-BE	S21	1950-1970	-20 max	NA
-BE	S12	1950-1970	60±1	-14 Max
-BE	S12	1870-1890	-20 max	NA
-FC	S21	1890-1910	60±1	-14 max
-FC	S21	1970-1990	-20 max	NA
-FC	S12	1970-1990	60±1	-14 max
-FC	S12	1890-1910	-20 max	NA

- 4.3.4 Remove jumpers J3 and J5 to configure the amplifiers for 53 dB gain. Using the test set-up as described in paragraph 4.3.3, measure and record gain (S21 & S12) and return loss (S11 & S22) over the 1800 to 2050 MHz frequency range. Confirm that the gains and return losses meet the requirements of the following table:

Dash #	Parameter	Frequency Range (MHz)	Gain Reqmt. (dB)	S11 & S22 (dB)
-AD	S21	1850-1870	50±1	-14 max
-AD	S21	1930-1950	-20 max	NA
-AD	S12	1930-1950	50±1	-14 max
-AD	S12	1850-1870	-15 max	NA
-BE	S21	1870-1890	50±1	-14 max
-BE	S21	1950-1970	-20 max	NA
-BE	S12	1950-1970	50±1	-14 Max
-BE	S12	1870-1890	-20 max	NA
-FC	S21	1890-1910	50±1	-14 max
-FC	S21	1970-1990	-20 max	NA
-FC	S12	1970-1990	50±1	-14 max
-FC	S12	1890-1910	-20 max	NA

4.3.5 Configure the test set-up to measure ACPR & AGC action per Figure 3.6a or 3.6b. Using the appropriate test frequency as indicated in the Table in paragraph 4.3.1, measure and record output power level and amplifier current draw for input power levels of -70 dBm to -30 dBm in 10 dB steps. Re-adjust R30 & R53 as necessary to obtain +11 dBm output power level for -40 dBm input power level with amplifiers set for 63 dB gain or -30 dBm input power level for amplifiers set for 53 dB gain. With the amplifier channels configured for 63 dB gain, measure and record the minimum input power level that causes the RSSI LEDs D5 & D10 to turn on. Measure and record the ACPR for output power levels of 0 dBm and +11 dBm. Confirm that the ACPR levels do not exceed the requirements described in paragraph 4.2.7.

4.3.6 Configure the test set-up to measure Noise figure per Figure 3.4b. With the amplifier channels configured for 63 dB gain, measure and record the noise figure for the uplink and downlink amplifier channels at the test frequencies described in the Table in paragraph 4.3.2.

4.3.7 SET THE GAIN OF THE AMPLIFIER CHANNELS TO THE VALUE INDICATED ON THE MANUFACTURING ORDER PAPERWORK.

4.4 Burn-In

The purpose of this test is to screen out units subject to infant failure mechanisms in a high temperature operational environment. This test also stresses the power supply that is to be shipped with the unit. This test is performed on the completely assembled unit. Place the completed unit in a

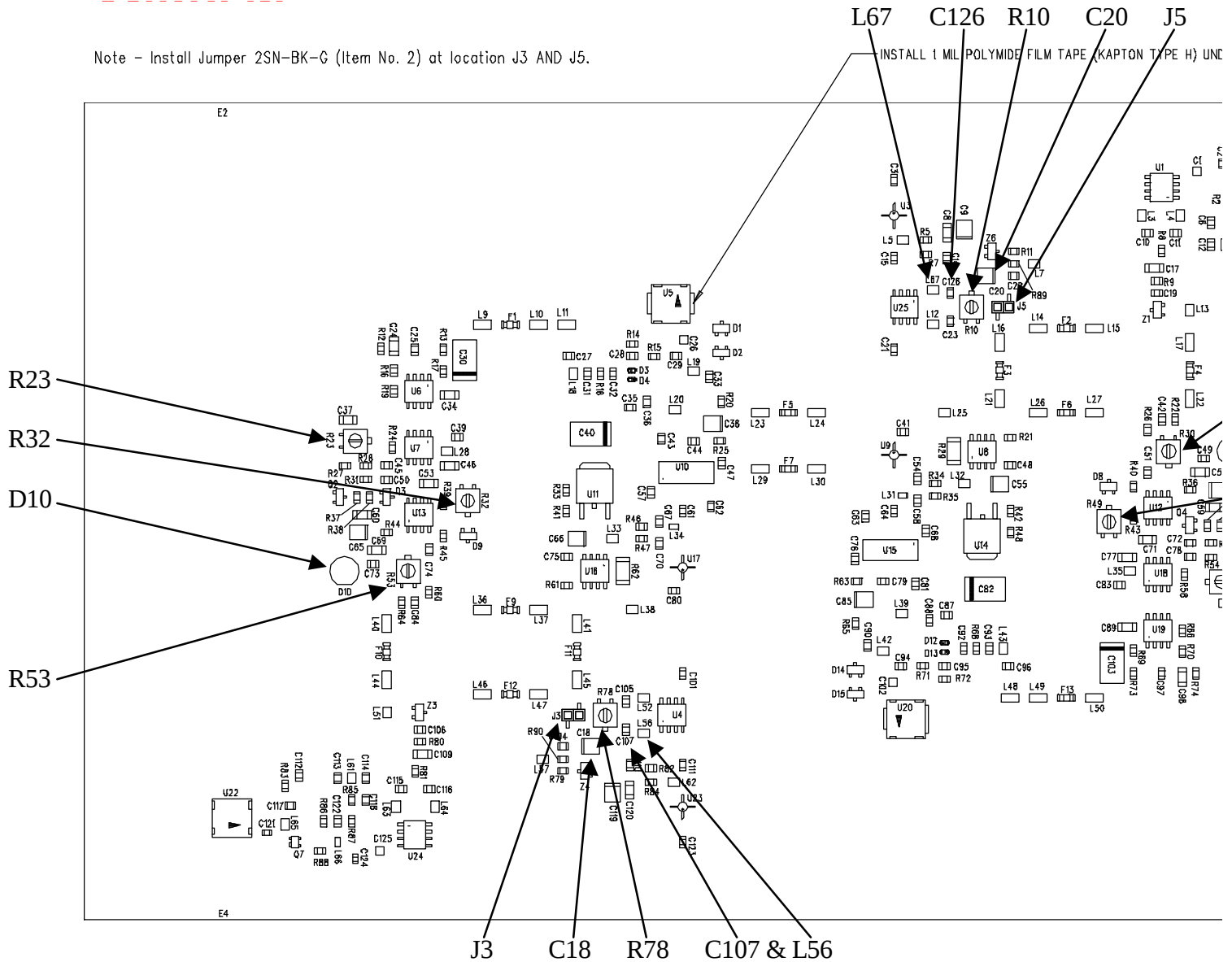
chamber where the ambient temperature is controlled at 45 ± 5 degrees centigrade. Both antenna faces should be covered with a low VSWR free space microwave absorber material to prevent undesired microwave oscillations. Attach the power supply to each unit and plug the power supply into a Ac power outlet. Confirm that the green power good LED is turned on; if the green LED is not on , or, the red fault LED is on the unit should be disconnected from the power sources and routed to the diagnosis and repair center. Leave the unit in an operational state in the chamber for at least 10 hours. At the end of the 10 hour period, re-confirm that the green power good LED is turned on; if the green LED is not on , or, the red fault LED is on the unit should be disconnected from the power sources and routed to the diagnosis and repair center.

4.5 Final Operational Check

The purpose of this test is to confirm that the DUT has retained functional RF operational performance through all previous stress testing. Configure a test set-up per Figure 3.8. Use the appropriate test signal frequencies as indicated by the table in paragraph 4.3.2 to stimulate the DUT. Place the DUT in position in the measurement chamber. Confirm that the test signal level with the DUT power off is -70 ± 3 dBm. Apply DC power to the DUT and confirm that the test signal level increases to -23 ± 3 dBm for 53 dB gain units or -13 ± 3 dBm for 63 dBm units. Rotate the repeater 180 degrees about its vertical axis to check the other amplifier channel.

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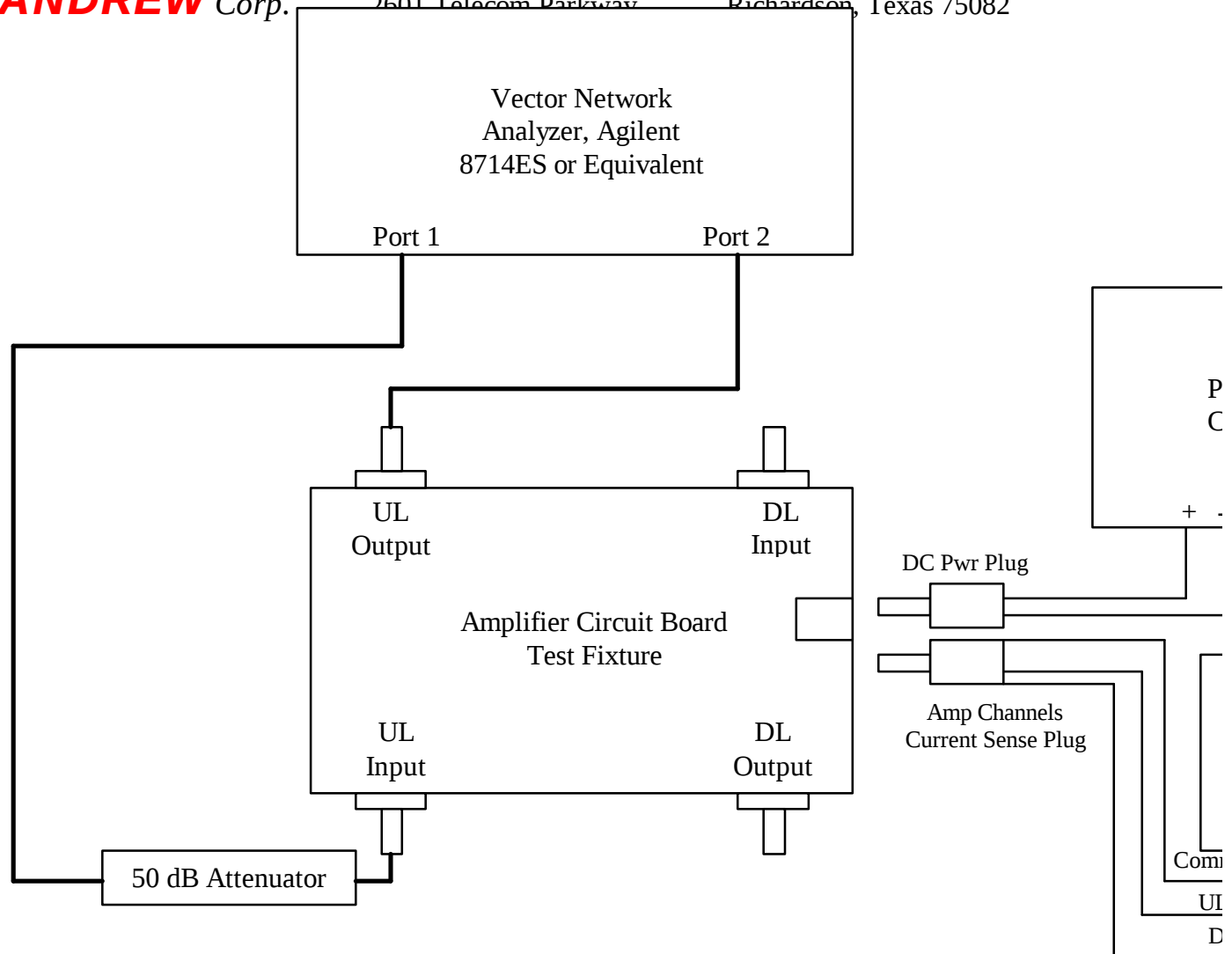
Note - Install Jumper 2SN-BK-G (Item No. 2) at location J3 AND J5.



ANDREW CORP.
SIDE-TO-SIDE REPEATER BOARD
740377 REV 0

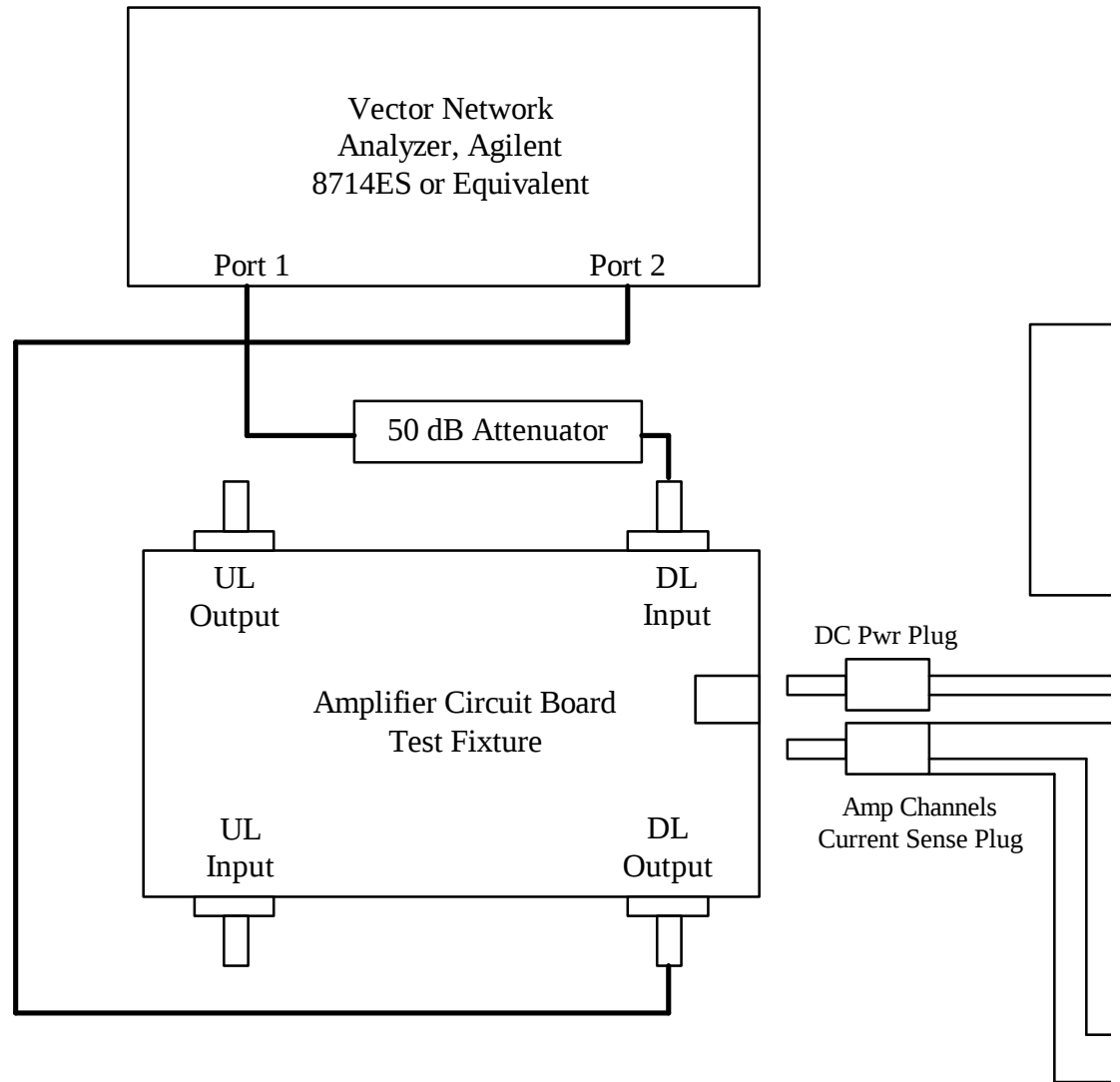
Figure 3.1 Amplifier Circuit Board Layout

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- Notes: 1) Terminate DL Input & DL Output Ports with matched Loads
2) Calibrate VNA for 1800 to 2050 MHz with 801 points at -10 dBm test power
3) Remove 50 dB Attenuator and set R53 full CW for Input RL measurement

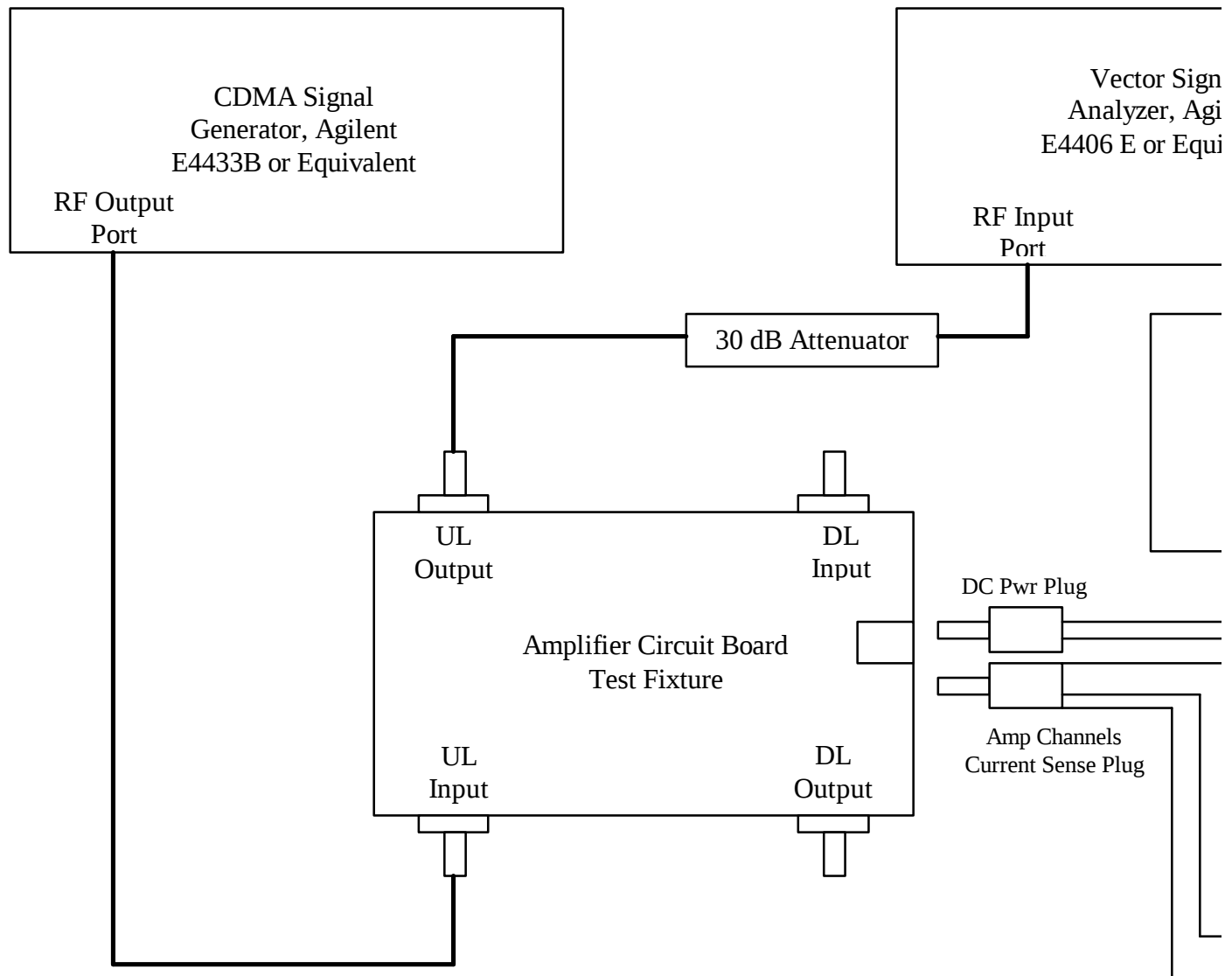
Figure 3.2a Uplink Channel Gain & RL Measurement Set-
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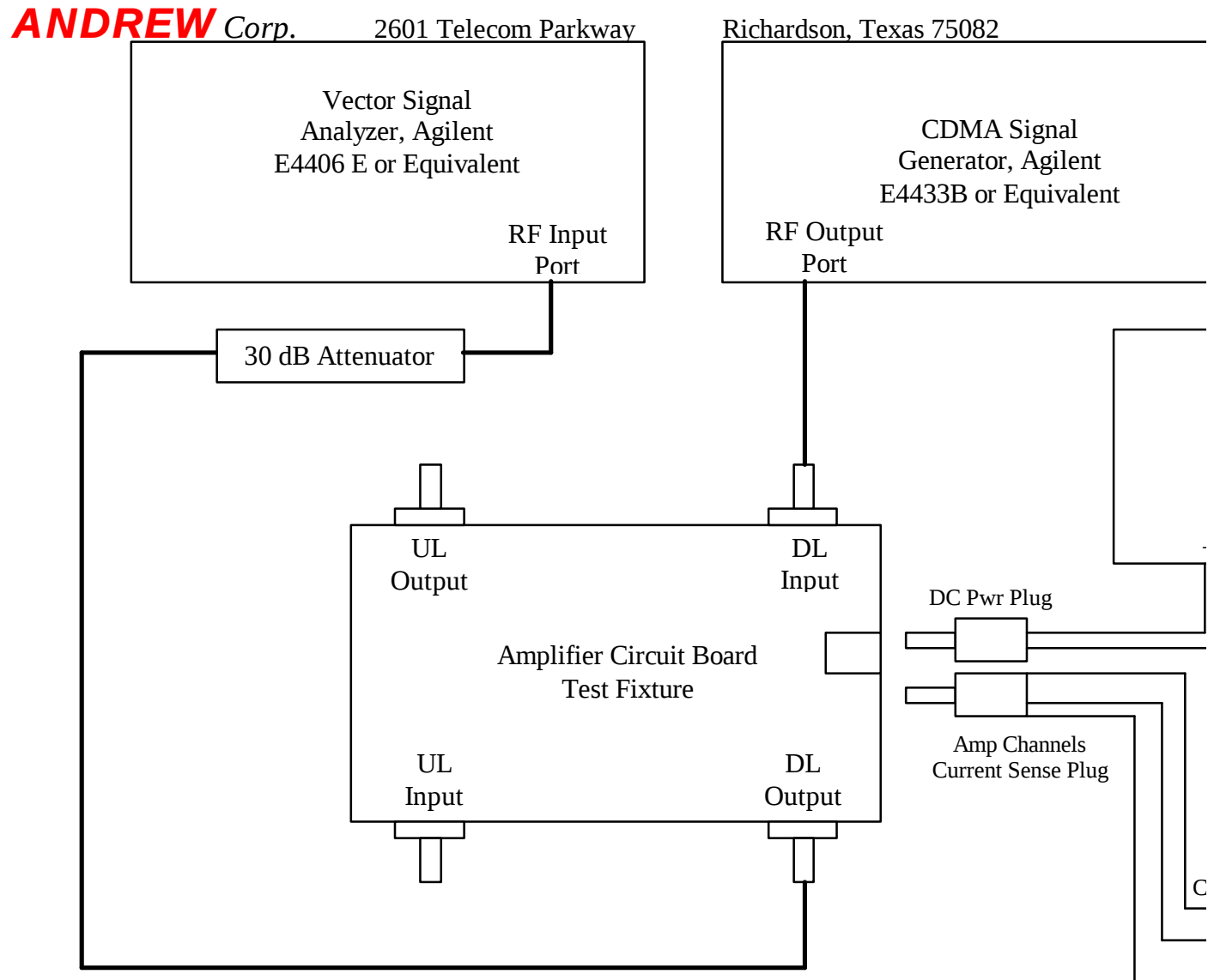
- Notes: 1) Terminate UL Input & DL Output Ports with matched Loads
2) Calibrate VNA for 1800 to 2050 MHz with 801 points at -10 dBm test
3) Remove 50 dB Attenuator and set R30 full CW for Input RL measure

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Figure 3.2b Downlink Channel Gain & RL Measurement



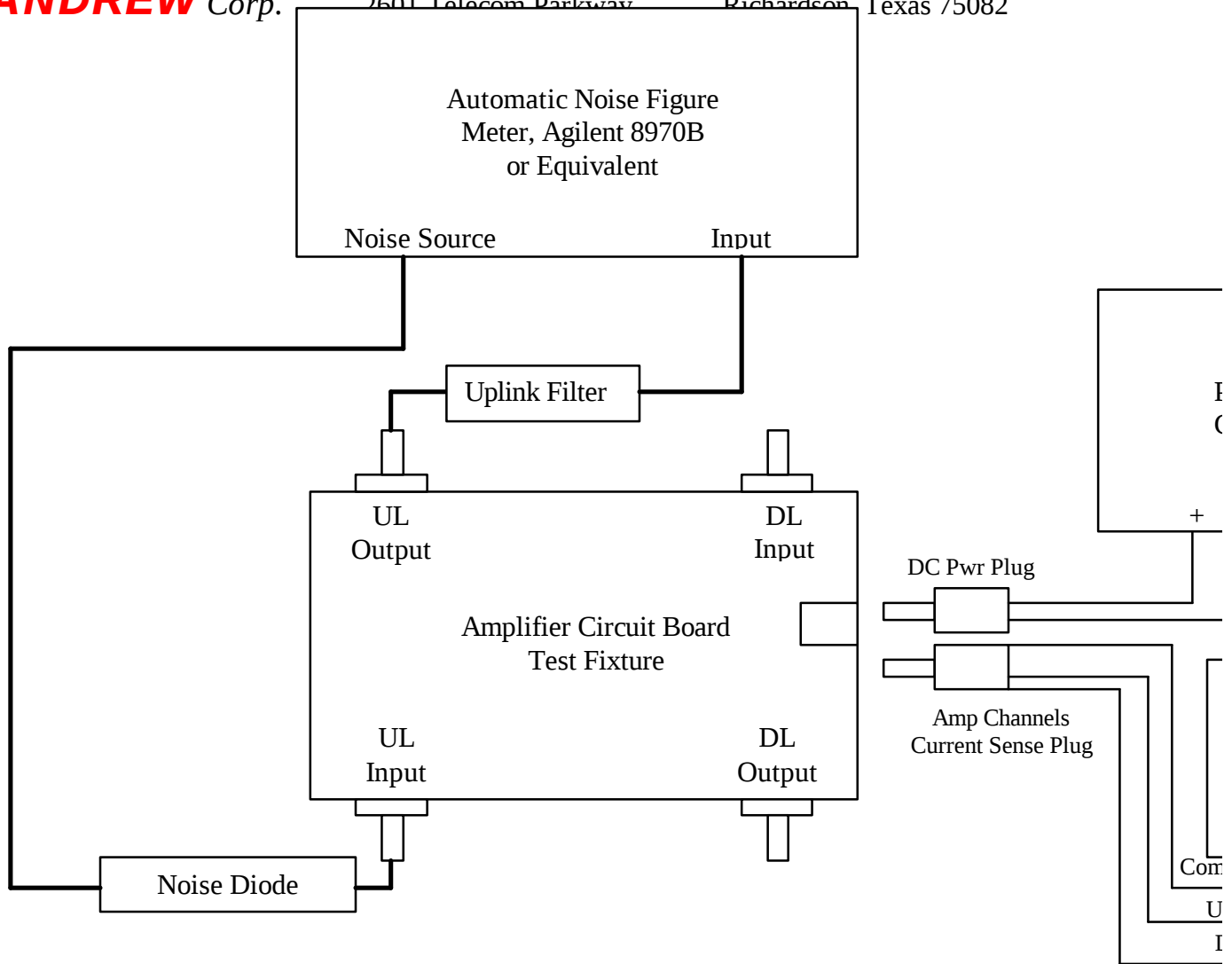
- Notes: 1) Terminate DL Input & DL Output Ports with matched Loads
2) Set-Up VSA to measure IS-95 ACPR over the 1850-1990 MHz range



- Notes: 1) Terminate UL Input & UL Output Ports with matched Loads
2) Set-Up VSA to measure IS-95 ACPR over the 1850-1990 MHz range

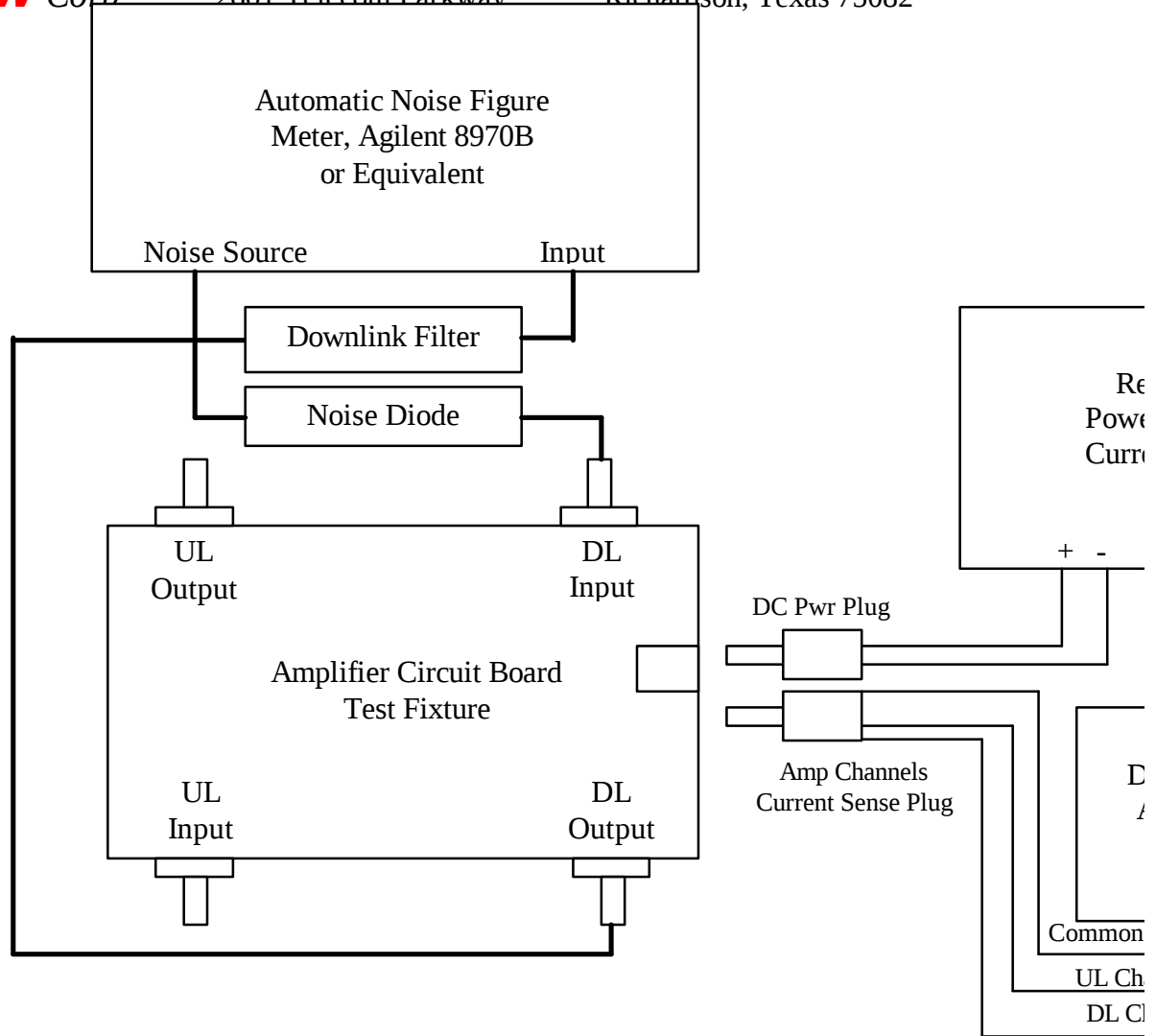
Figure 3.3b Downlink ACPR Measurement & AGC Adjustm

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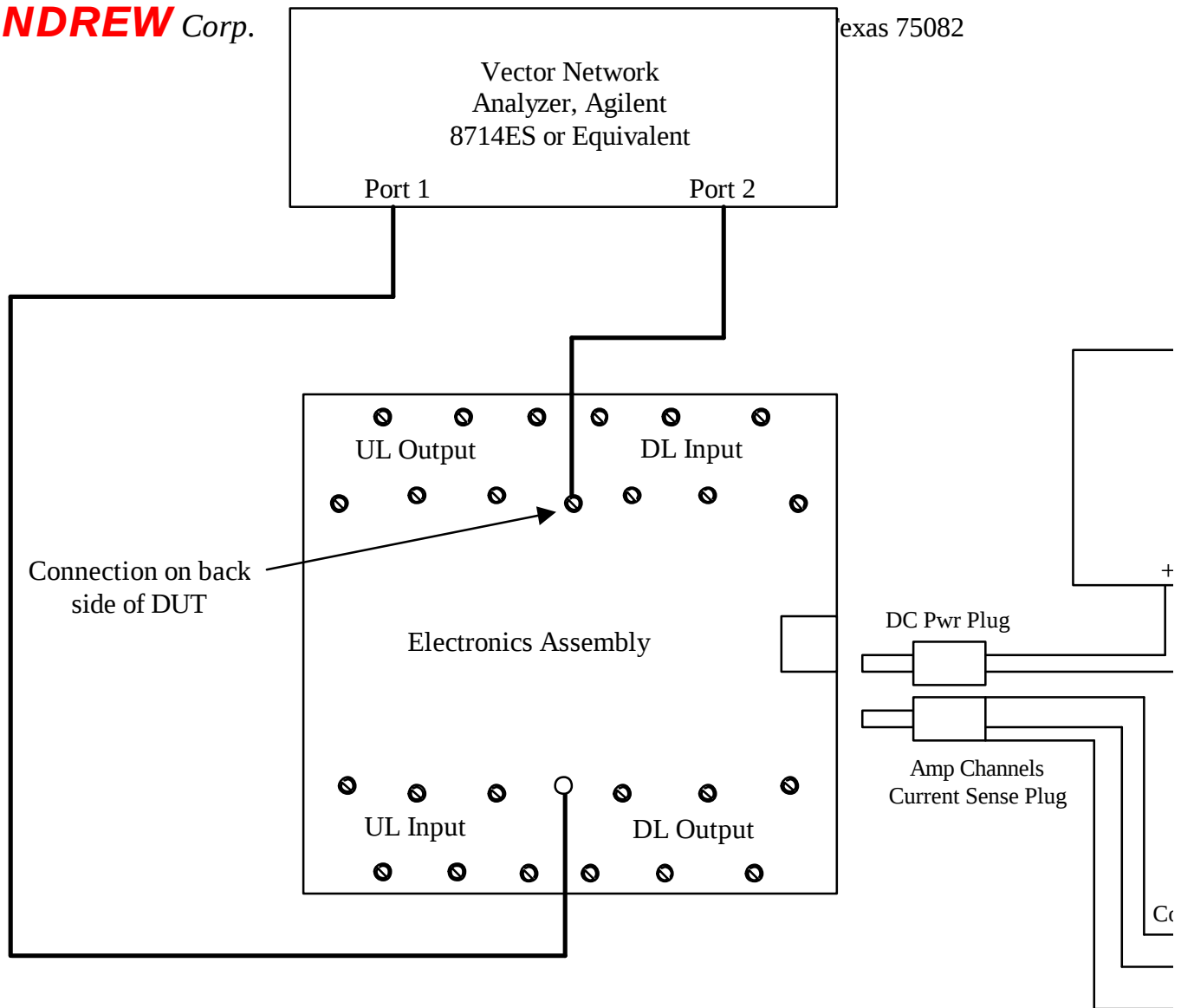
- Notes: 1) Terminate DL Input & DL Output Ports with matched Loads
2) Measure and Record Noise Figure at 1903 MHz
3) Set Amplifier Channel Gain to 63 dB

Figure 3.4a Uplink Channel Noise Figure Measurement Set
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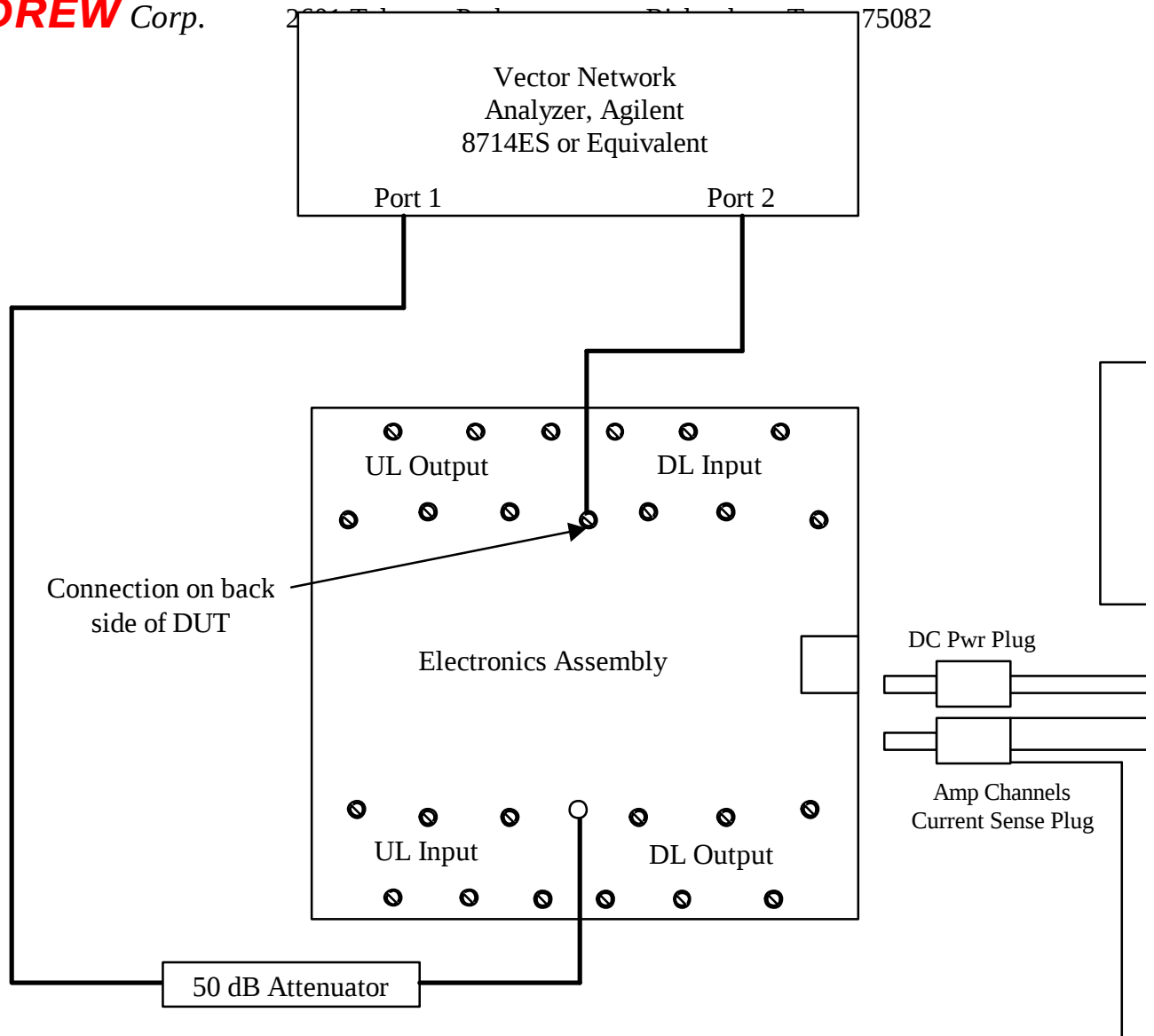


- Notes: 1) Terminate UL Input & UL Output Ports with matched Loads
4) Measure and Record Noise Figure at 1983 MHz
5) Set Amplifier Channel Gain to 63 dB

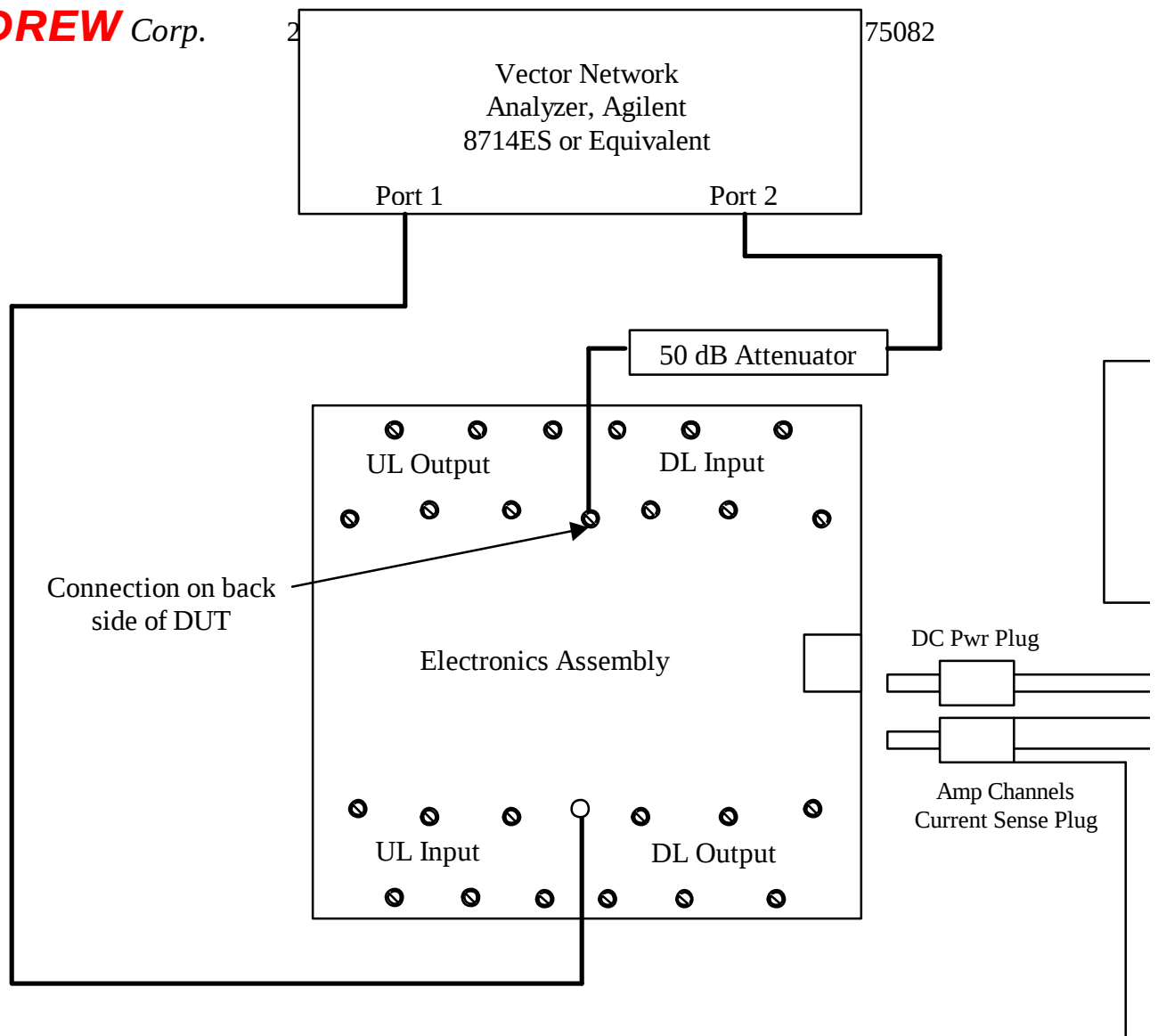
Figure 3.4b Downlink Channel Noise Figure Measurement Se
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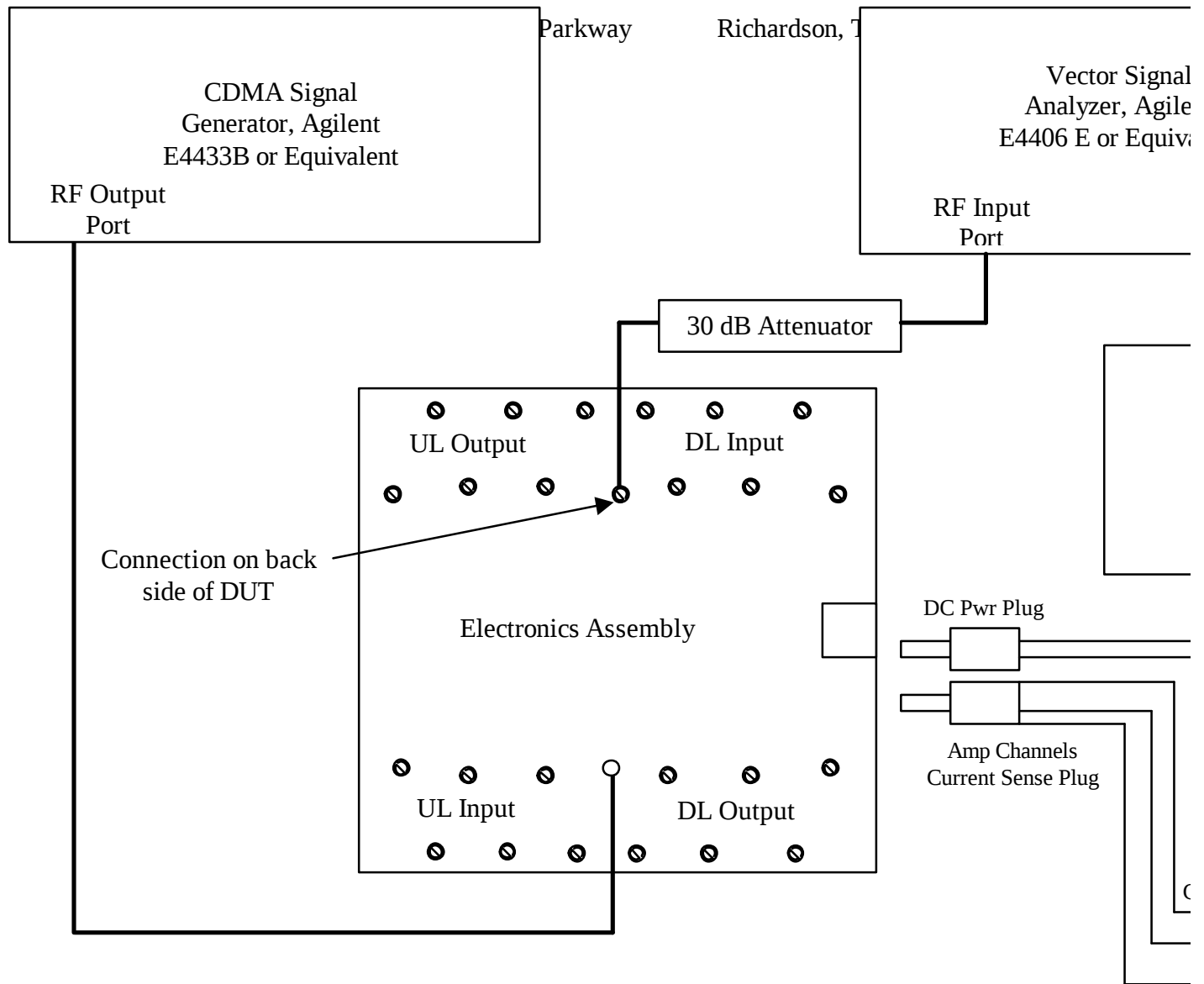
- Notes: 1) Calibrate VNA for 1850 to 1990 MHz with 801 points at -10 dBm test power level.
2) Configure for shorted resonator phase shift tuning technique.
3) Set R30 & R53 full CW for Input RL measurement.



- Notes: 1) Calibrate VNA for 1850 to 1990 MHz with 801 points at -10 dBm test power level.
2) Remove 50 dB Attenuator and Set R53 full CW for Input RL measurement.



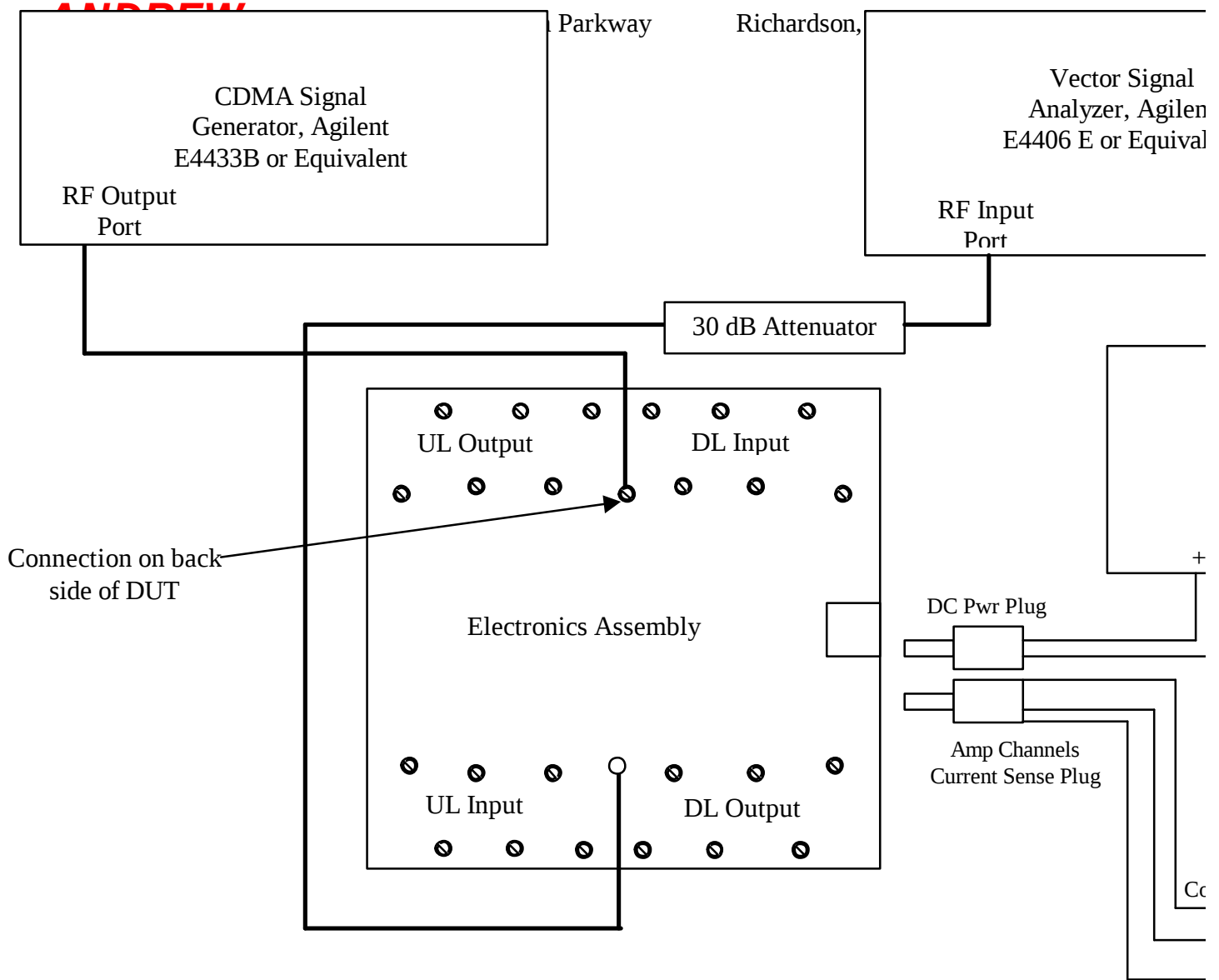
- Notes: 1) Calibrate VNA for 1850 to 1990 MHz with 801 points at -10 dBm test power level.
2) Remove 50 dB Attenuator and Set R30 full CW for Input RL measurement.



- Notes: 1) Set-Up VSA to measure IS-95 ACPR over the 1850-1990 MHz range.
 2) Configure Signal Generation for IS-95 CDMA carrier with 18 active channels

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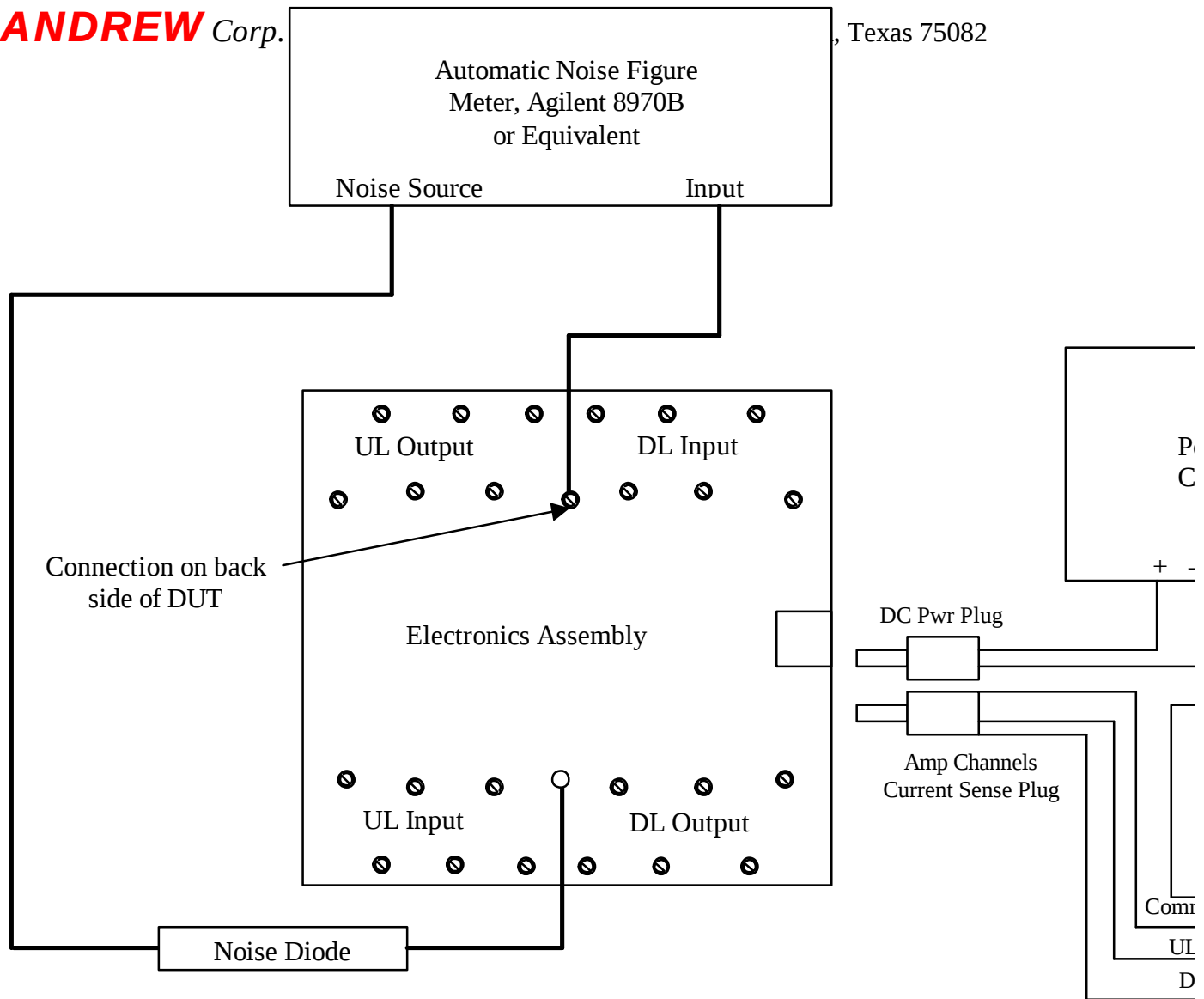
Figure 3.6a Uplink ACPR & AGC Test Set-up



- Notes: 1) Set-Up VSA to measure IS-95 ACPR over the 1850-1990 MHz range.
 2) Configure Signal Generation for IS-95 CDMA carrier with 18 active channels

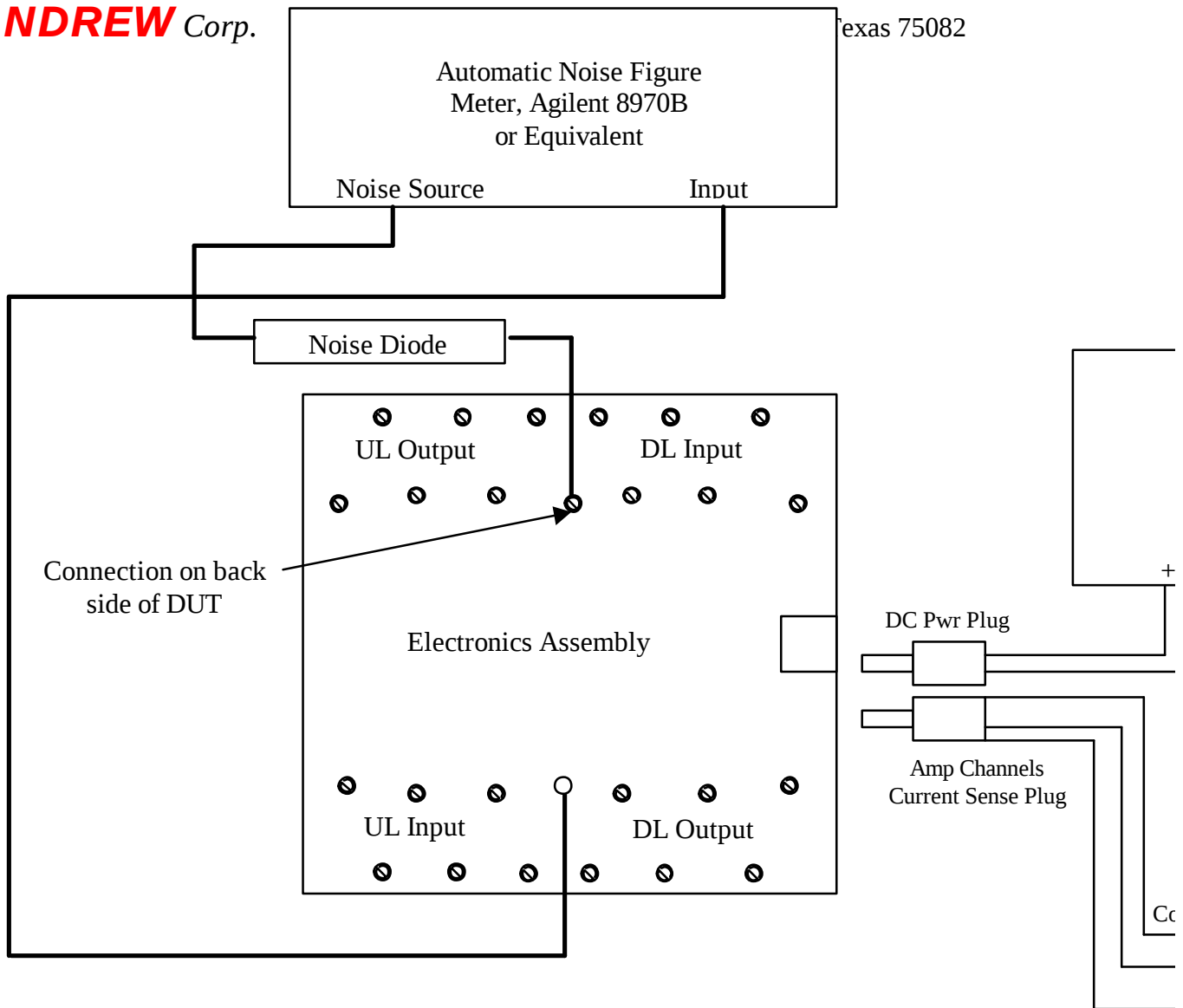
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Figure 3.6b Downlink ACPR & AGC Test Set-up

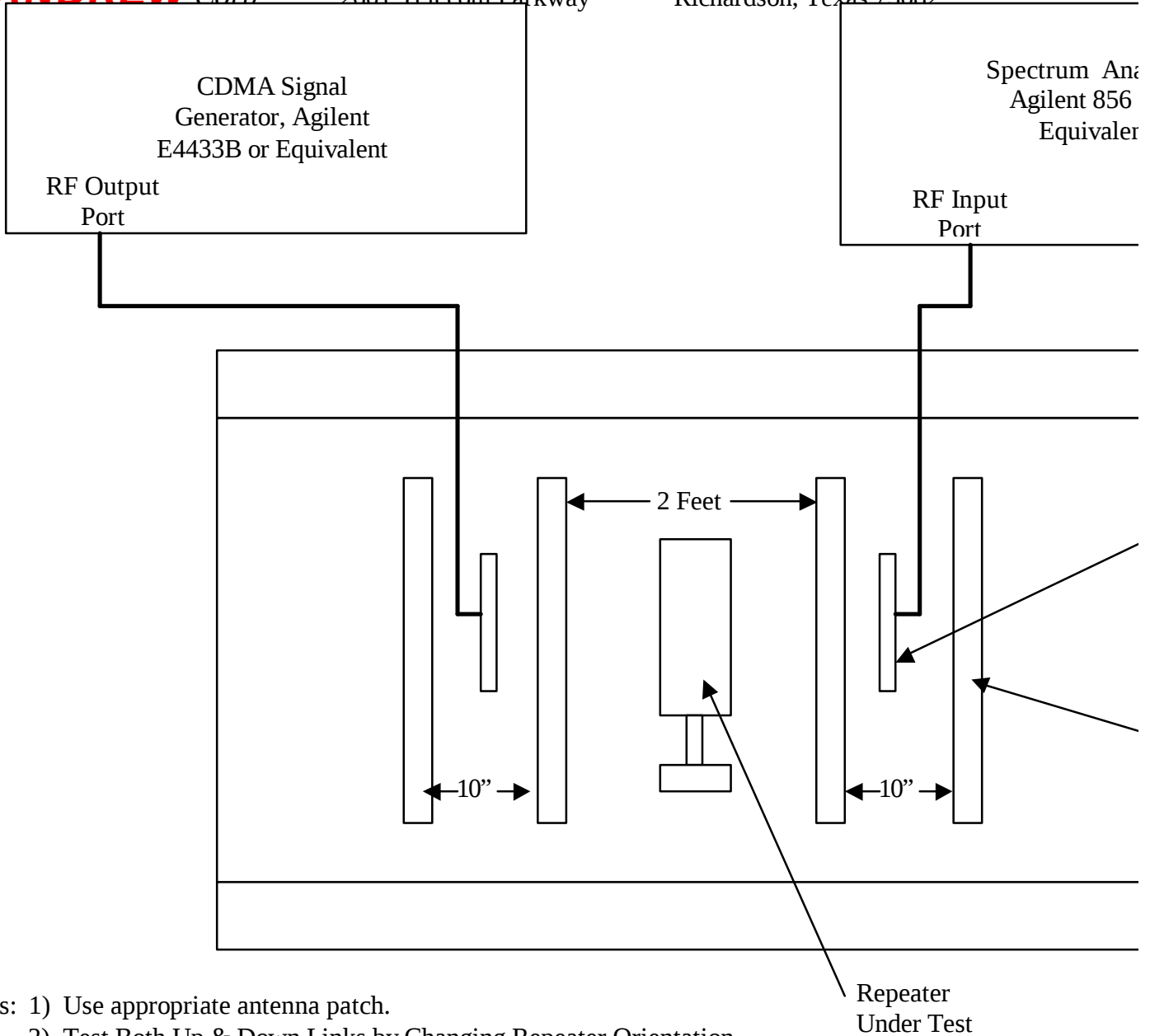


- Notes: 1) Set Uplink Amplifier Channel Gain for 63dB.
 2) Measure Noise Figure at the appropriate frequency as indicated in the Table in Paragraph 4.3.

Figure 3.7a Uplink Channel Noise Figure Test Set-up



- Notes: 1) Set Downlink Amplifier Channel Gain for 63dB.
2) Measure Noise Figure at the appropriate frequency as indicated in the Table in Paragraph 4.



- Notes: 1) Use appropriate antenna patch.
2) Test Both Up & Down Links by Changing Repeater Orientation

ANDREW Corp.

2601 Telecom Parkway

Richardson, Texas 75082

PCS 1900 “PROPAGATOR” Side to Side Repeater Amplifier Circuit Board Test Data

Mfg. Order #:		Mfg. Seq. #:			
Procedure Paragraph Reference	Date	Values	Units	Reqmt.	Tech
4.1 Temp Cycling			Cycles	10 min	
4.2.2 Current Draw			ma	800 max	
4.2.2 D7 Turn on			Yes/No	Yes	
4.2.6 High Uplink Gain (min/max 1.85-1.91GHz)			dB	63±1	
4.2.6 High Downlink Gain (min/max 1.93-1.99GHz)					
				-14min	
4.2.6 Uplink Output RL (1.85-1.91GHz)					
4.2.6 Downlink Output RL (1.93-1.99GHz)					
4.2.6 Uplink Input RL (1.85-1.91GHz)					
4.2.6 Downlink Input RL (1.93-1.99GHz)					
4.2.6 Low Uplink Gain (min/max 1.85-1.91GHz)				53±1	
4.2.6 Low Downlink Gain (min/max 1.93-1.99GHz)					
4.2.7 VSA 53 dB UL Gain Check (1.85-1.91GHz)			Yes/No	Yes	
4.2.7 VSA 53 dB DL Gain Check (1.93-1.99 GHz)					
4.2.7 VSA 63 dB UL Gain Check (1.85-1.91GHz)					
4.2.7 VSA 63 dB DL Gain Check (1.93-1.99 GHz)					
4.2.7 Max UL RSSI Sensitivity (1.85-1.93 GHz)			dBm	-70 max	
4.2.7 Max DL RSSI Sensitivity (1.93-1.99 GHz)					
4.2.8 Uplink AGC Control Action (1.903 GHz)				+15 max	
4.2.8 Downlink AGC Control Action (1.983 GHz)					
4.2.8 UL ±885kHz ACPR (0 dBm Output, 1.903GHz)			dBc	-45 max	
4.2.8 DL ±885kHz ACPR (0 dBm Output, 1.983GHz)					
4.2.8 UL Current Sense Voltage @ 0 dBm Output			Volts	3.0 max	
4.2.8 DL Current Sense Voltage @ 0 dBm Output					
4.2.8 UL ±885kHz ACPR (13 dBm Output, 1.903GHz)			dBc	-45 max	
4.2.8 DL ±885kHz ACPR (13 dBm Output, 1.983GHz)					
4.2.8 UL Current Sense Voltage @ 13 dBm Output			Volts	3.2 max	
4.2.8 DL Current Sense Voltage @ 13 dBm Output					
4.2.8 UL Over-current Circuit Operation			Yes/No	Yes	
4.2.8 DL Over-current Circuit Operation					
4.2.9 Uplink Noise Figure (1.903 GHz)			dB	3 max	
4.2.9 Downlink Noise Figure (1.983 GHz)					

Figure 3.9 Amplifier Circuit Board Data Sheet.

**PCS 1900 “PROPAGATOR” Side to Side Repeater
Electronics Assembly & Completed Repeater Test Data
Page 1 of 2**

Mfg. Order #		Model #	PRB-1900-	Serial #	
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Reference Procedure Paragraph 4.3.3, 60 dB Gain Response Parameters:

Dash #	Parameter	Frequency Range (MHz)	Min/Max Gain Value (dB)	Gain Reqmt. (dB)	Max RL Value (dB)	S11 & S22 (dB)
	S21			60 +/- 1		-14 max
	S21			-20 max		NA
	S12			60 +/- 1		-14 max
	S12			-20 max		NA

Tech:		Date:	
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Reference Procedure Paragraph 4.3.4, 50 dB Gain Response Parameters:

Dash #	Parameter	Frequency Range (MHz)	Min/Max Gain Value (dB)	Gain Reqmt. (dB)	Max RL Value (dB)	S11 & S22 (dB)
	S21			50 +/- 1		-14 max
	S21			-20 max		NA
	S12			50 +/- 1		-14 max
	S12			-20 max		NA

Tech:		Date:	
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**PCS 1900 “PROPAGATOR” Side to Side Repeater
Electronics Assembly & Completed Repeater Test Data**

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Mfg. Order #		Model #	PRB-1900-	Serial #	
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Reference Procedure Paragraph 4.3.5, Amplifier AGC Action and Current Draw:

UL Test Freq:	(MHz)	DL Test Freq:	(MHz)
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Input Power (dBm)	UL Output Power (dBm)	UL Current Sense (volts)	DL Output Power (dBm)	DL Current Sense (volts)
-70				
-60				
-50				
-40				
-30				

UL RSSI Level:	(dBm)	DL RSSI Level	(dBm)
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Tech:		Date:	
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Reference Procedure Paragraph 4.3.6, Amplifier Noise Figure:

UL Noise Figure:	(dB)	DL Noise Figure:	(dB)
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Tech:		Date:	
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Reference Procedure Paragraph 4.4, Burn-In:

Duration (hrs):	Tech:		Date:	
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Reference Procedure Paragraph 4.5, Final Operational Check:

Unit Gain (dB)	UL On Level	DL On Level	50 dB Reqmt.	60 dB Reqmt.
			-23±3	-13±3

Tech:		Date:	
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