AW-XM549 , AW-XM549-I
AW-XM553 , AW-XM553-I

IEEE 802.11 1X1 a/b/g/n/ac/ax Wireless LAN + Bluetooth 5.3 + 802.15.4 Tri-radio 12 x 12 LGA Module

Datasheet

Rev. B

DF

For Standard

Features

WLAN

- IEEE 802.11a/b/g/n/ac/ax, 1x1 SISO 2.4 GHz and 5 GHz, up to 80 MHz channel
- Integrated high power PA up to +21 dBm transmit power
- Integrated LNA and T/R switches
- UL/DL OFDMA, UL/DL MU-MIMO
- 802.11ax ER, DCM, TWT
- 802.11az accurate ranging
- Security: WPA3 security with hardware encryption engines

Bluetooth

- Supports Bluetooth 5.3 Class 2 and Bluetooth Low Energy
- BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (/4-DQPSK), 3 Mbps (8DPSK)
- Bluetooth LE long range (125/500 kbps) support improving range by 4x
- Bluetooth LE 2 Mbps
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting Bluetooth Low Energy (LE) audio
- Security: AES

802.15.4

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Wi-Fi and Bluetooth
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

Revision History

Document NO: R2-2549-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2022/07/01	DCN026641	● Draft version	Roger Liu	N.C Chen
B	2023/08/05	DCN029872	● Update BT feature to 5.3 ● Update RF specification Update power consumption	Roger Liu	N.C Chen

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax 1x1 dual band WLAN, BT, and 802.15.4 tri-radio module – **AW-XM549.** With full-feature Wi-Fi subsystem integrated into a module, **AW-XM549** provides the best and most convenient SMT process. The module is targeted to smart entertainment, gateways, hubs, bridges, smart home, industrial, point of sale (POS) terminal, smart appliances which need convenient SMT process.

By using **AW-XM549**, the customers can easily integrate the Wi-Fi, BT, 802.15.4 by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11 a/b/g/n/ac/ax standard, the **AW-XM549** uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using **AW-XM549**.

The **AW-XM549** supports standard interface **SDIO3.0 for WLAN**, **UART for BT and SPI for 802.15.4**. AW-XM549 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the **AW-XM549** is the best solution for the consumer electronics and smart applications.

1.2 Block Diagram

TBD

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi with Bluetooth 5.3 and 802.15.4 tri-radio Module
Major Chipset	NXP IW612 WLCSP (140pins)
Host Interface	WiFi + BT + 802.15.4 ● SDIO + UART + SPI
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 48 pins
Antenna	For LGA, “1T1R, external” ANT(Main)：Wi-Fi / Bluetooth/802.15.4→ TX / RX
Weight	0.6 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM, OFDMA

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries -36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>15</td><td>17</td><td>19</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8) @EVM≦-31 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>11ax(HE80 MCS11)
@EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-85</td><td>-82</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-63</td><td>-60</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>-62</td><td>-59</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9)</td><td>-</td><td>-58</td><td>-55</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>-54</td><td>-51</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)</td><td>-</td><td>-53</td><td>-50</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)
802.11ac: Maximum data rates up to 433 Mbps (80 MHz channel)
802.11ax: Maximum data rates up to 600 Mbps (80 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES
■ 802.15.4 :AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.3 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-89</td><td>-86</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-81</td><td>-78</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-91</td><td>-88</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 Thread

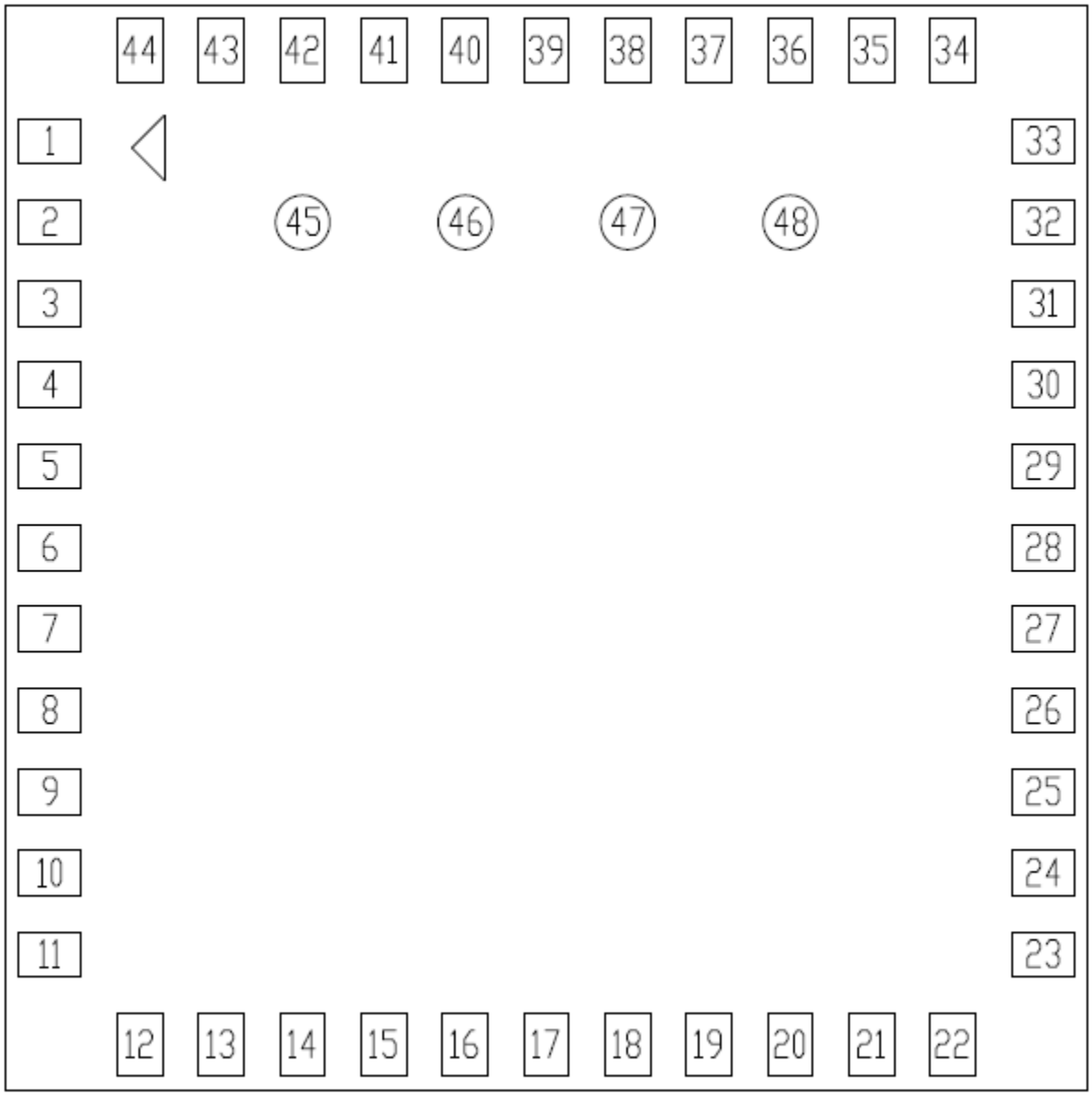
<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Thread Standard</td><td>IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band</td></tr>
<tr><td>Frequency Rage</td><td>2400MHz~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>O-QPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Thread</td><td>2</td><td>4</td><td>6</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>Thread Sensitivity (PER<1%)
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Thread</td><td>-</td><td>-95</td><td>-92</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.5 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 °C to +70 °C
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 °C to +85 °C
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	+-2kV
Changed Device Model	+-500V

2. Pin Definition

2.1 Pin Map



AW-XM549 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	RF pin out	---	I/O
3	GND3	Ground	---	---
4	SPI_TXD	SPI receive output signal	VDDIO	I/O
5	SPI_RXD	SPI receive input signal	VDDIO	I/O
6	HOST_WAKE_ BT	GPIO Mode : GPIO[18]. BT Device Wake	VDDIO	I/O
7	BT_WAKE_HOST	GPIO Mode : GPIO[19]. BT Host Wake	VDDIO	I/O
8	SPI_FRM	SPI_FRM - SPI frame signal	VDDIO	I/O
9	VBAT	3.3V power voltage source input	3.3V	P
10	JTAG_TMS	JTAG test mode select input signal. GPIO[29]	VDDIO	I/O
11	SPI_CLK	SPI_CLK - SPI clock signal	VDDIO	I/O
12	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode (Need external pull high 51k resistor to VDDIO)	1.8V/3.3V	I
13	WL_WAKE_HOST	GPIO Mode : GPIO[17]. Wi-Fi radio wake-up output signal	VDDIO	O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND20	Ground	---	---
21	DCDC_1V8_OUT	Internal DC-DC output (Need external 1uH power inductor)	1.8V	P
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	1V8_IN	1.8V power voltage source input	1.8V	P
24	NC24	Floating Pin, No connect to anything.	---	Floating
25	BT_PCM_OUT	PCM Data output / GPIO[5]	VDDIO	O
26	BT_PCM_CLK	PCM Clock / GPIO[4]	VDDIO	I/O
27	BT_PCM_IN	PCM data input / GPIO[6]	VDDIO	I
28	BT_PCM_SYNC	PCM sync signal / GPIO[7]	VDDIO	I/O
29	JTAG_TDO	JTAG test data output signal. GPIO[31]	VDDIO	O
30	JTAG_TDI	JTAG test data input signal. GPIO[30]	VDDIO	I
31	GND31	Ground	---	---
32	NC32	Floating Pin, No connect to anything.	---	Floating
33	GND33	Ground	---	---
34	BT_DIS	Host-to-BT reset /IND_RST_BT - Independent software reset for Bluetooth / GPIO[2]	VDDIO	I
35	JTAG_TCK	JTAG test clock input signal. GPIO[28]	VDDIO	I

36	GND36	Ground	---	---
37	Host-to-Wi-Fi reset	GPIO Mode : GPIO[1]. Independent software reset for Wi-Fi	VDDIO	I
38	MWS_SOUT	WCI-2 MWS coexistence serial transport interface(TX) / GPIO[26]	VDDIO	I/O
39	MWS_SIN	WCI-2 MWS coexistence serial transport interface(RX) / GPIO[25]	VDDIO	I/O
40	HOST_WAKE_WL	GPIO Mode : GPIO[16]. Host-to-WLAN wake / Wi-Fi radio wake-up input signal	VDDIO	I
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN(active high)	VDDIO	I
44	UART_CTS	UART_CTS(active high)	VDDIO	I
45	GND45	Ground	---	---
46	IND_RST_15.4	Independent software reset for 802.15.4 / GPIO[24]	VDDIO	I/O
47	RST_IND	Independent software reset indicator output signal to host / GPIO[22]	VDDIO	I/O
48	SPI_INT	SPI interrupt signal / GPIO[20]	VDDIO	I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	3.96	V
		-	1.8	2.16	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM549 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM549 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

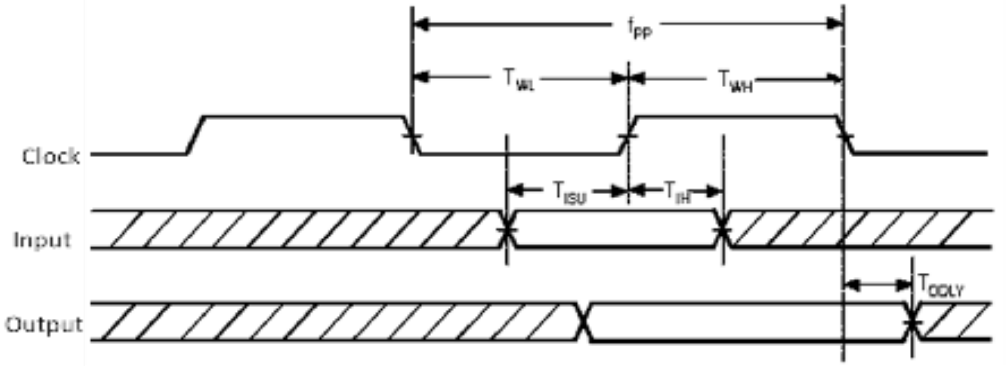
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

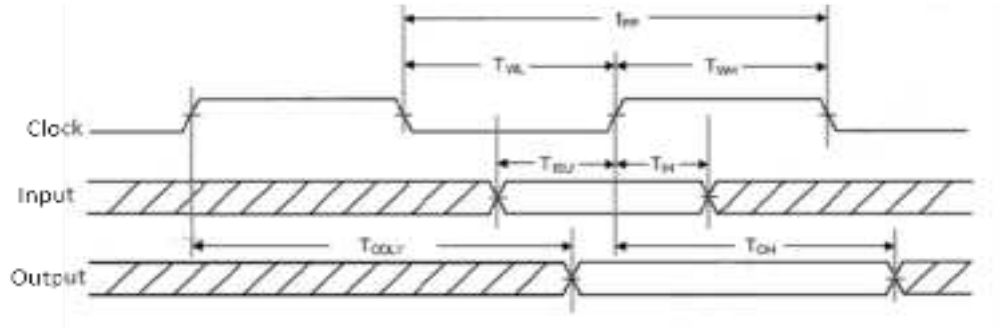
AW-XM549 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

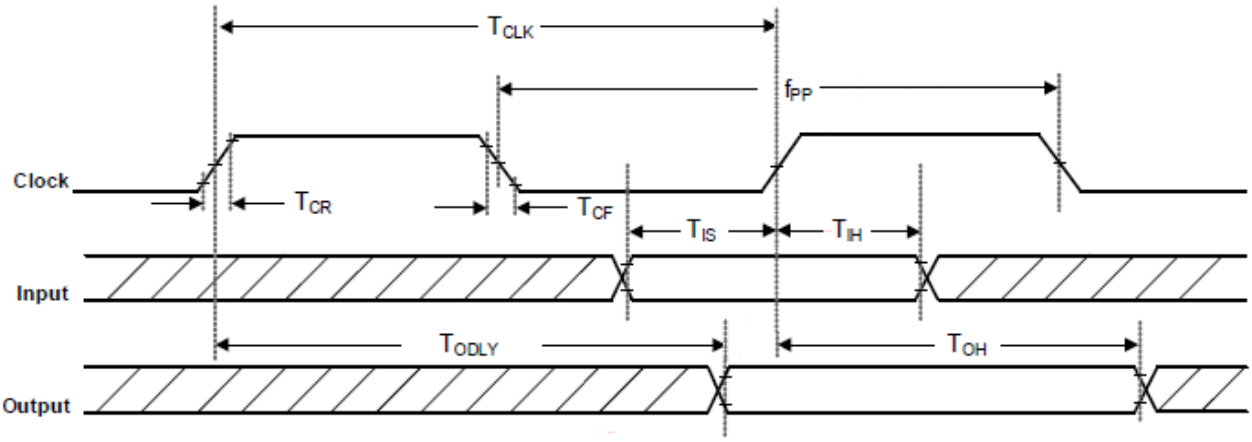


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

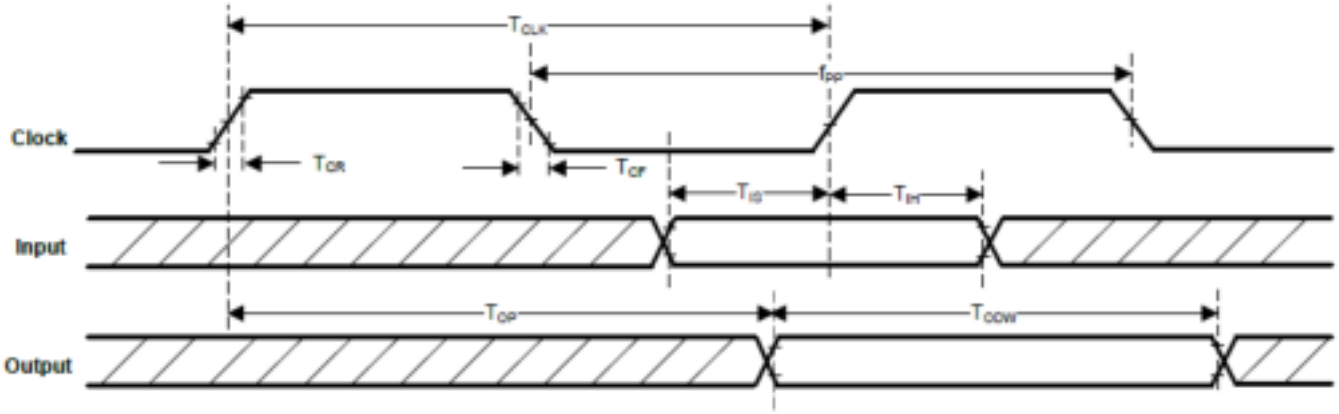


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

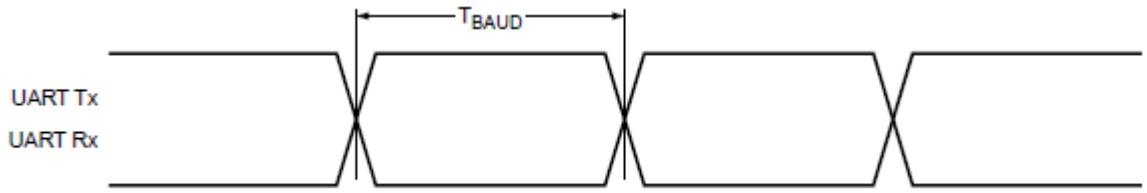
3.4.2.3 SDR104 mode (208MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR,TCF<0.96ns(max) at 208MHz CCARD =10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.3.High-Speed UART Interface

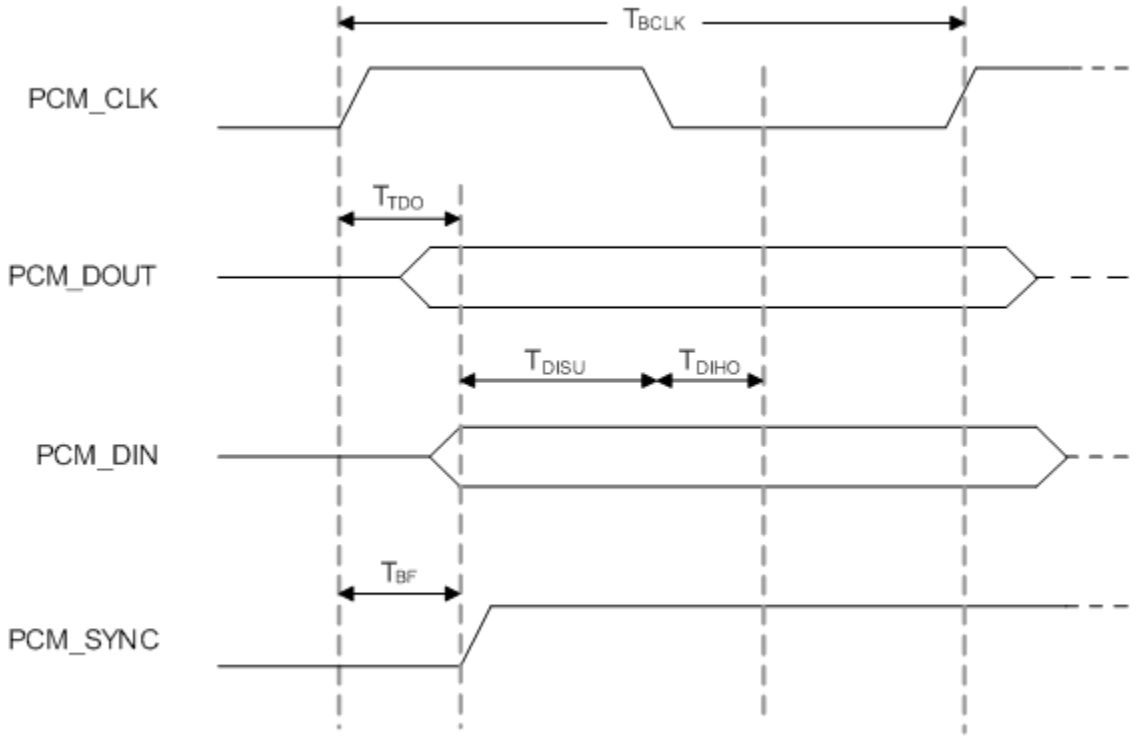
The AW-XM549 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

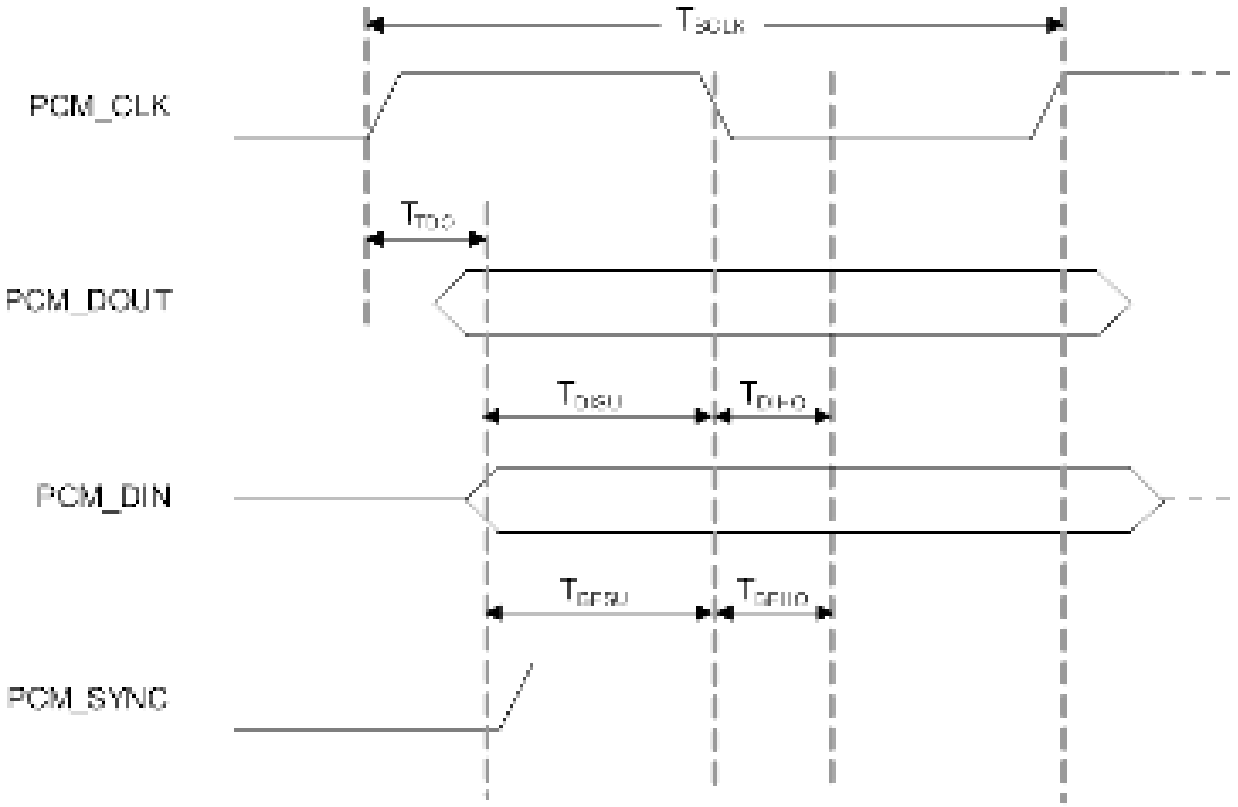
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



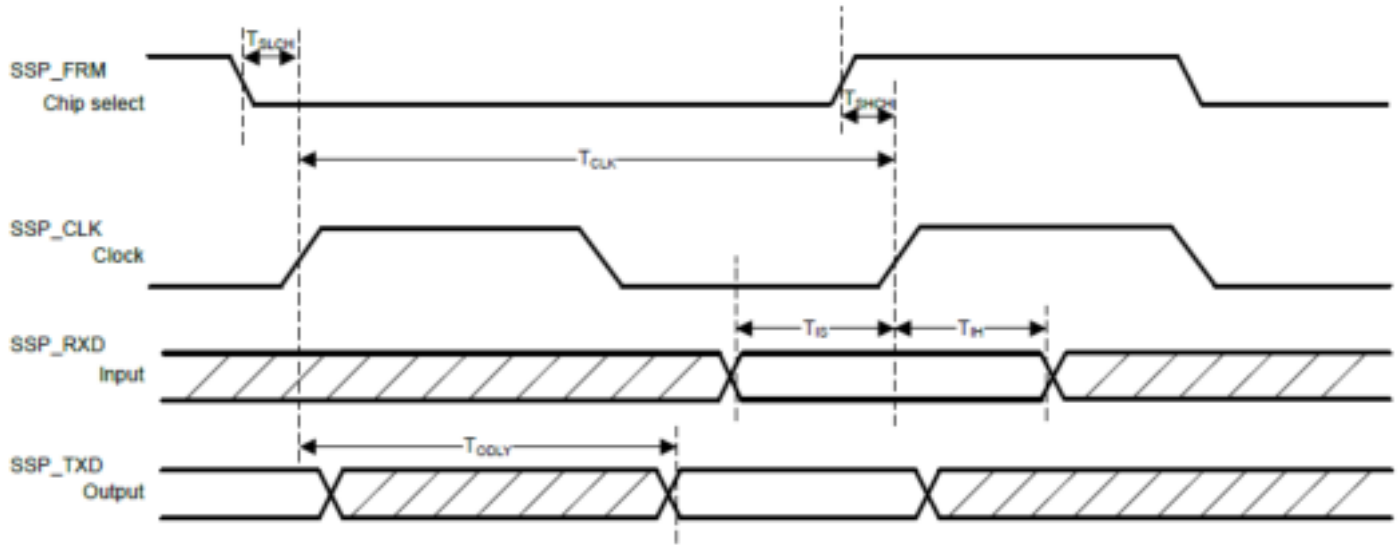
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

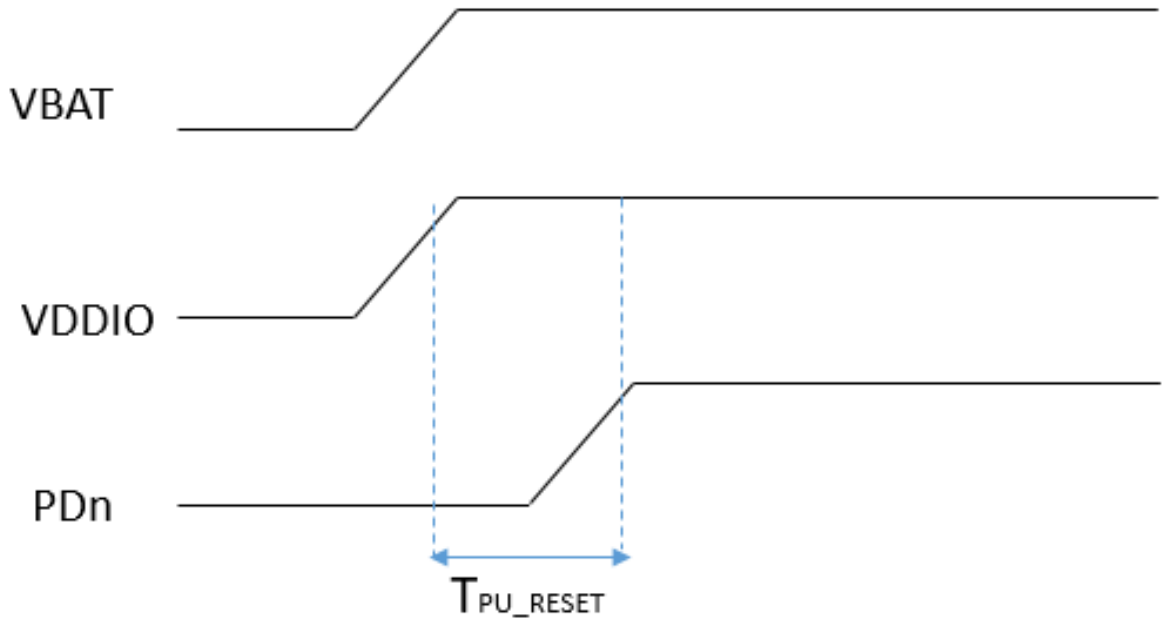
3.4.5 SPI Interface



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SLCH}	Chip select setup time	--	12	--	--	ns
T_{SHCH}	Chip select hold time	--	12	--	--	ns
T_{CLK}	Clock period	--	40	--	--	ns
T_{IS}	Input setup time	--	12	--	--	ns
T_{IH}	Input hold time	--	0	--	--	ns
T_{ODLY}	Output delay	--	--	--	12	ns

3.5 Timing Sequence

AW-XM549 power up timing sequence.



Symbol	Parameter	Min	Typ	Max	Units
TPU_RESET	Valid power to PDn deasserted	0	-	-	ms
VIH	Input high voltage	1.4	-	4.5	V
VIL	Input low voltage	-0.4	-	0.5	V

3.6 Power Consumption*

3.6.1 WLAN

No.	Item			JP1_PIN2 VBAT_3.3V (mA)		
				Max.		Avg.
1	Pdn *(1)(2)			0.18		0.02
2	Deepsleep*(2)(3)			0.4		0.3
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)			62		1.7
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)			69		1.1
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (mA)		
				Max.	Avg.	Duty Cycle Avg. (%)
2.4	11b@1Mbps	20	17	295	294	99
	11g@54Mbps	20	16	278	276	88
	11n@MCS0	40	14	271	269	96
	11n@MCS7	40	14	251	248	81
	11ax@MCS0 NSS1	40	12	258	255	96
	11ax@MCS11 NSS1	40	12	232	231	77
5	11a@6Mbps	20	16	410	404	98
	11n@MCS0	40	16	415	410	96
	11n@MCS7	40	16	375	369	80
	11ac@MSC0 NSS1	80	14	378	372	93
	11ac@MSC9 NSS1	80	14	332	328	72
	11ax@MSC0 NSS1	80	11	327	324	92
	11ax@MSC11 NSS1	80	11	296	294	76
Band (GHz)	Mode	BW(MHz)		Receive (mA)		
				Max.		Avg.
2.4	11b@11Mbps	20		61		58
	11n@MCS7	40		73		71
	11ax@MCS11 NSS1	40		73		69
5	11a@54Mbps	20		73		72
	11n@MCS7	40		83		82
	11ac@MCS9 NSS1	80		101		100
	11ax@MCS11 NSS1	80		100		98

No.	Item			JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Pdn *(1)(2)			23	23
2	Deepsleep*(2)(3)			181	181
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)			327	189
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)			327	187
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (uA)	
				Max.	Avg.
2.4	11b@1Mbps	20	17	480	479
	11ax@MCS11 NSS1	40	12	473	472
5	11a@6Mbps	20	16	498	496
	11ax@MSC11 NSS1	80	11	484	484
Band (GHz)	Mode	BW(MHz)		Receive (uA)	
				Max.	Avg.
2.4	11b@11Mbps	20		448	447
5	11ax@MCS11 NSS1	80		453	453

No.	Item			JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Pdn *(1)(2)			2	2
2	Deepsleep*(2)(3)			61	61
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)(5)			61	61
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)(5)			61	61
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (uA)	
				Max.	Avg.
2.4	11b@1Mbps	20	17	44	44
	11ax@MCS11 NSS1	40	12	44	44
5	11a@6Mbps	20	16	45	44
	11ax@MSC11 NSS1	80	11	45	44
Band (GHz)	Mode	BW(MHz)		Receive (uA)	
				Max.	Avg.
2.4	11b@11Mbps	20		44	44
5	11ax@MCS11 NSS1	80		44	44

3.6.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	JP1_PIN2 VBAT_3.3V (mA)	
				Max.	Avg.

1	Deepsleep*(1)	N/A		0.6	0.4
2	Transmit*(2)	DH5	2	53	36
3	Receive*(2)	DH5	N/A	53	31

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Deepsleep*(1)	N/A		180	179
2	Transmit*(2)	DH5	2	437	436
3	Receive*(2)	DH5	N/A	437	436

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Deepsleep*(1)	N/A		61	61
2	Transmit*(2)	DH5	2	43	42
3	Receive*(2)	DH5	N/A	43	42

3.6.3 802.15.4

No.	Mode	Modulation Type	RF Power (dBm)	JP1_PIN2 VBAT_3.3V (mA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		0.3	0.13
2	Transmit*(3)(4)	O-QPSK	4	81	53
3	Receive*(3)(5)	O-QPSK	N/A	43	42

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		457	457
2	Transmit*(3)(4)	O-QPSK	4	571	570
3	Receive*(3)(5)	O-QPSK	N/A	571	570

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		118	118
2	Transmit*(3)(4)	O-QPSK	4	194	193
3	Receive*(3)(5)	O-QPSK	N/A	194	193

3.7 Sleep Clock (Optional)

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In

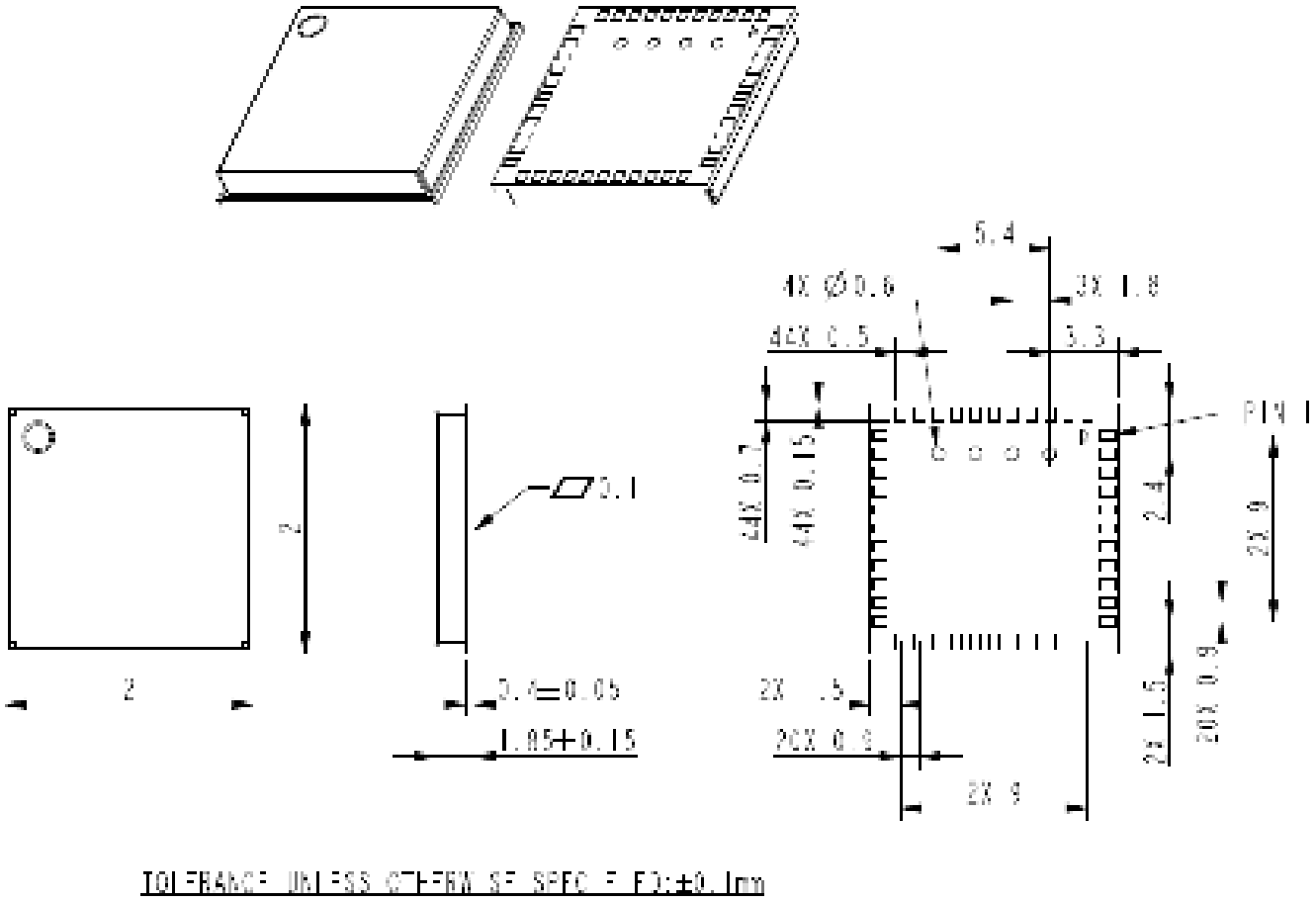
addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

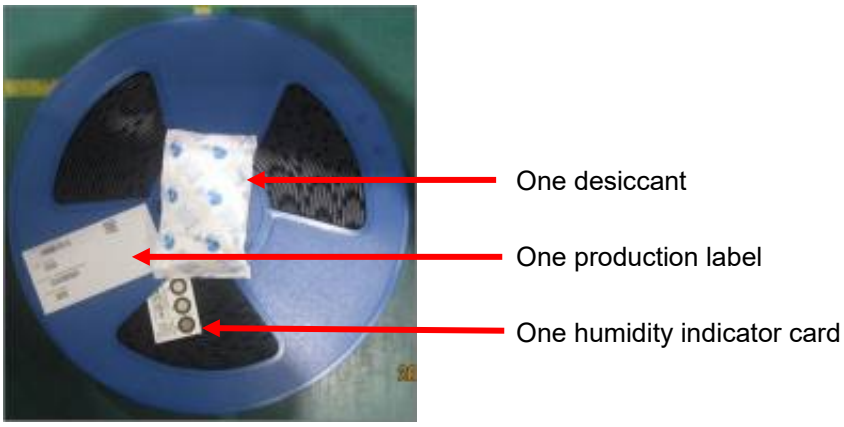
4. Mechanical Information

4.1 Mechanical Drawing

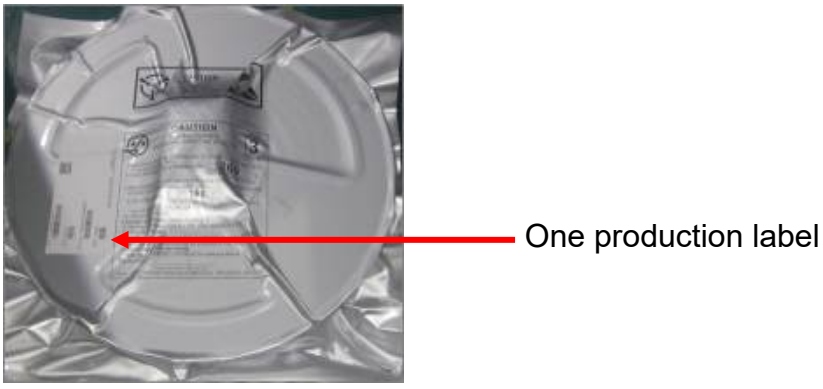


5. Packing Information

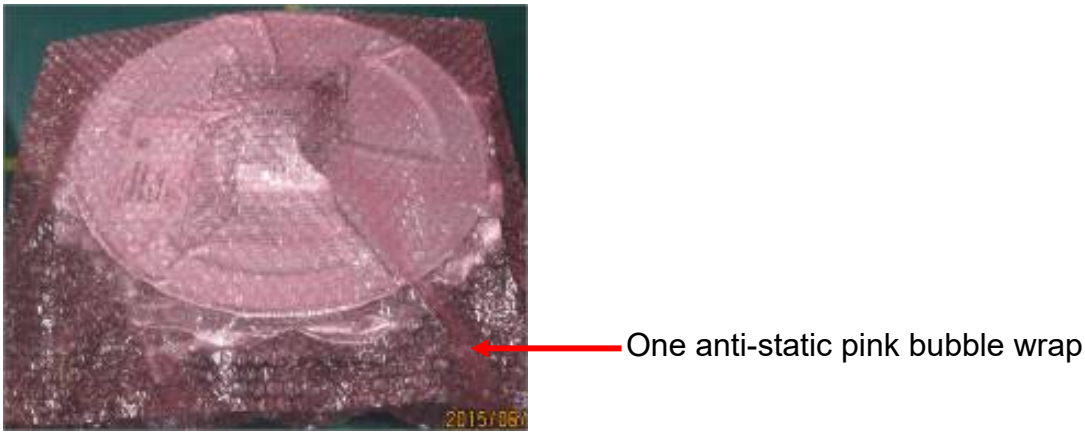
1. One reel can pack 1,500pcs 12x12 LGA modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap



5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

6. 5 inner boxes could be put into one carton

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

One carton label

One box label

FCC:

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Additional testing and certification may be necessary when multiple modules are used.

The host manufacturer should reference KDB Publication 996369 D04 Module Integration Guide.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-XM549".

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

IC:
This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:
(1) This device may not cause interference.
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient des émetteurs / récepteurs exempts de licence qui sont conformes au (x) RSS (s) exemptés de licence d'Innovation, Sciences et Développement économique Canada. L'opération est soumise aux deux conditions suivantes:
(1) Cet appareil ne doit pas provoquer d'interférences.
(2) Cet appareil doit accepter toute interférence, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil.

This device and its antenna(s) must not be co-located with any other transmitters except in accordance with IC multi-transmitter product procedures.
Referring to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously without reassessment permissive change.
Cet appareil et son antenne (s) ne doit pas être co-localisés ou fonctionnement en association avec une autre antenne ou transmetteur.

This radio transmitter [6100A-XM549] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio (6100A-XM549) a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal d'antenne. Les types d'antennes non inclus dans cette liste qui ont un gain supérieur au gain maximal indiqué pour tout type listé sont strictement interdits pour une utilisation avec cet appareil.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.
les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

The maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit.
le gain maximal d'antenne permis pour les dispositifs utilisant les bandes 5250-5350 MHz et 5470-5725 MHz doit se conformer à la limite de p.i.r.e.

The maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate.
le gain maximal d'antenne permis (pour les dispositifs utilisant la bande 5725-5850 MHz) doit se conformer à la limite de p.i.r.e. spécifiée pour l'exploitation point à point et non point à point, selon le cas.

For indoor use only.
Pour une utilisation en intérieur uniquement.

IMPORTANT NOTE:
IC Radiation Exposure Statement:
This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

IMPORTANT NOTE:
This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated. Additional testing and certification may be necessary when multiple modules are used.
Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. Operation is subject to the following two conditions: (1) this device may not cause harmful interference (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains IC: 6100A-XM549 ".

The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

JP:

W52/W53 屋内使用限定

Ant list

Ant.	Port	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	1	MAG. LAYERS	MSA-4008-25GC1-A2	PIFA Antenna	I-PEX	Note1
2	-	CEL	0032-02-07-00-001	PIFA Antenna	I-PEX	

Note1:

Ant.	Gain (dBi)	
	WLAN 2.4GHz/Bluetooth/Thread	WLAN 5GHz
1	2.98	5.16
2	1.30	4.30

AW-XM549

AW-XM553

IEEE 802.11 1X1 a/b/g/n/ac/ax Wireless LAN + Bluetooth 5.3 + 802.15.4 Tri-radio

12mm x 12mm LGA module

Layout Guide

Rev. 01

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
01	2022/04/06	● Initial Version	Roger Liu	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-XM553 layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- GENERAL RF GUIDELINES
- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- Antenna
- Antenna Matching
- GENERAL LAYOUT GUIDELINES
- THE OTHER LAYOUT GUIDE INFORMATION

1. GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
   - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
   - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
   - Keep all trace routing inside the ground plane area by at least the width of a trace.
   - Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:
   - Do not route any digital or analog signal traces between the RF traces and the reference ground.
   - Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
   - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:
   - Confirm antenna ground keep-outs.
   - Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.

- Do not use thermals on RF traces because of their high loss.
- The RF traces between AW-XM553 RF_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

2. Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

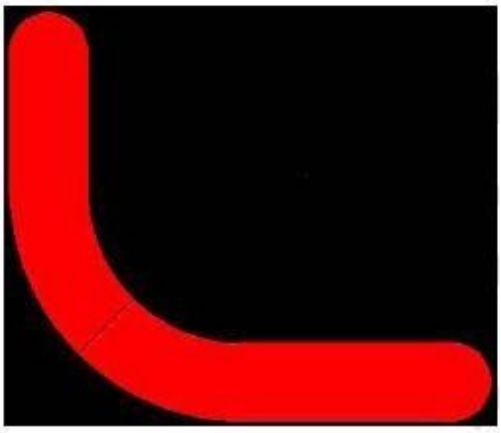
5. RF Trace and RF PAD

A. RF Trace

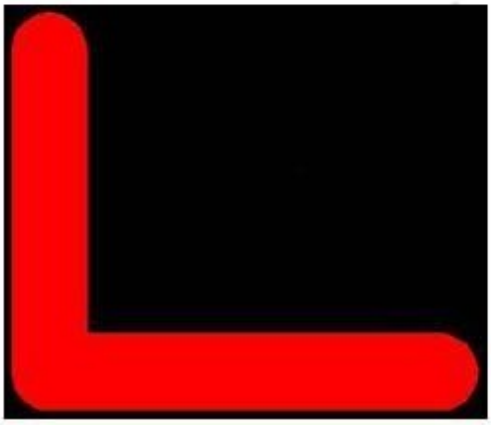
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

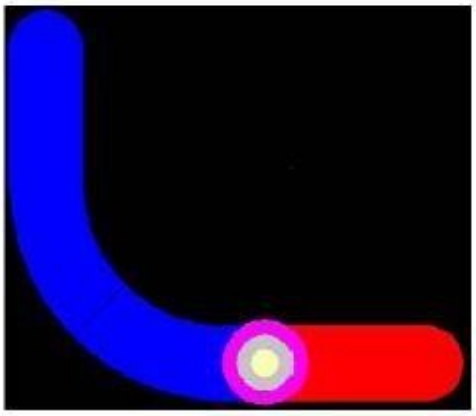
If the customers have any problem in calculation of trace impedance, please contact AzureWave.



Correct RF trace



Right-angled corner

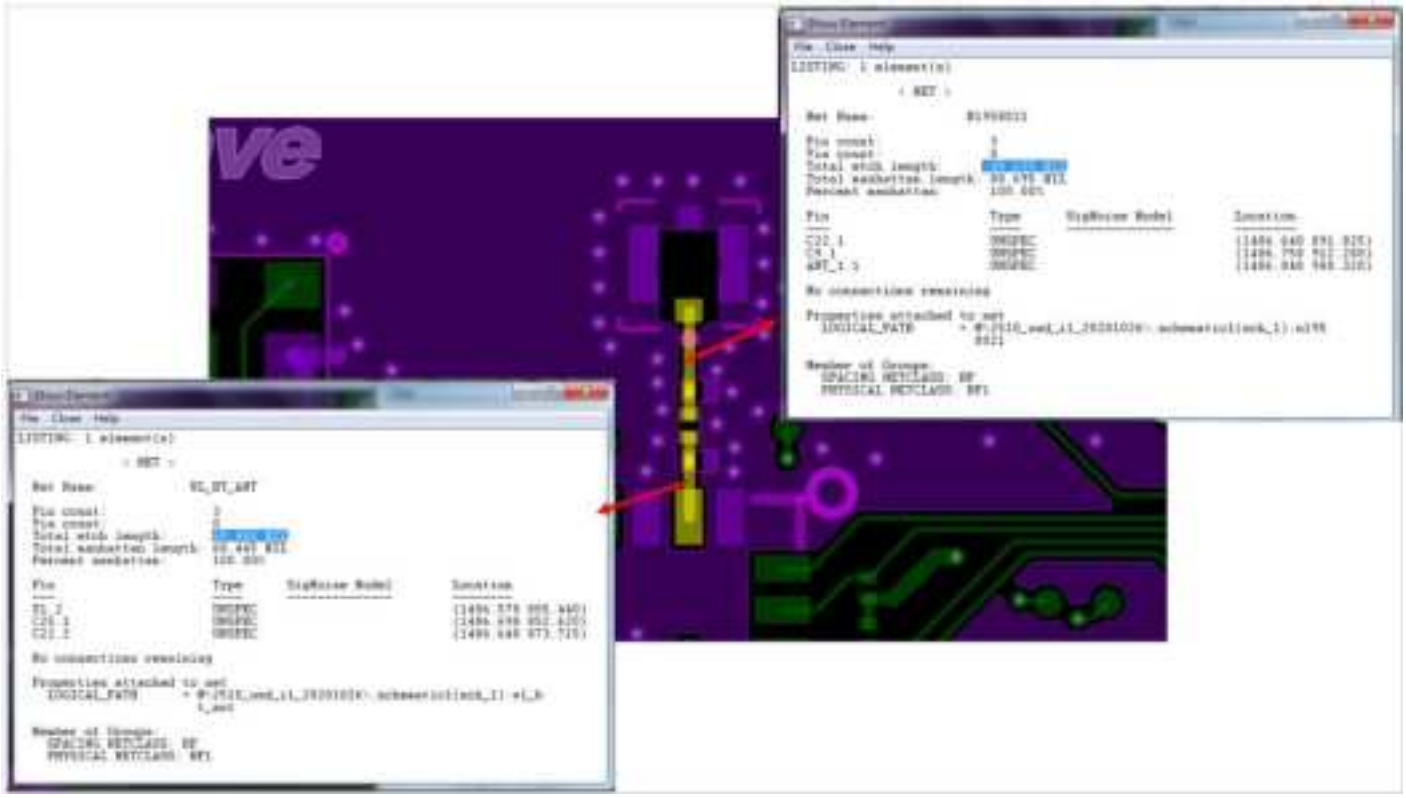


Via on RF trace

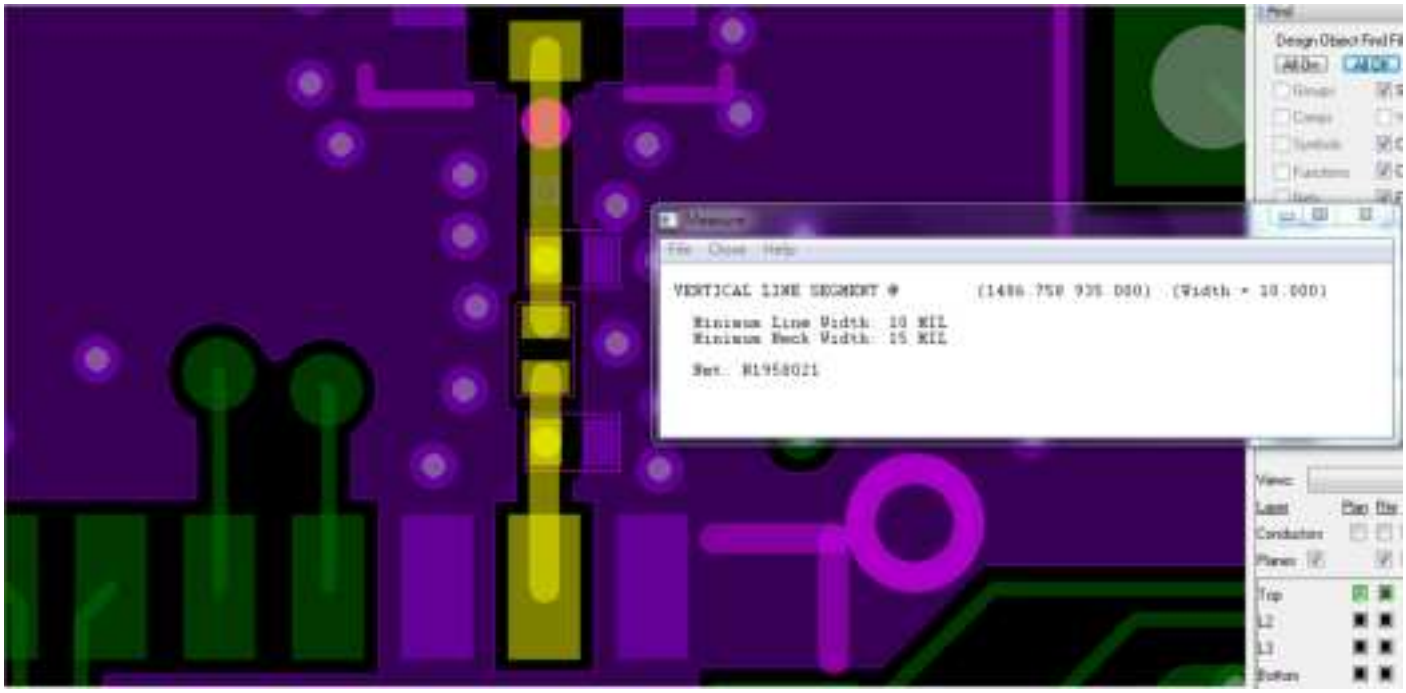
Incorrect RF trace

AW-XM553 RF trace should be follow the rules as below

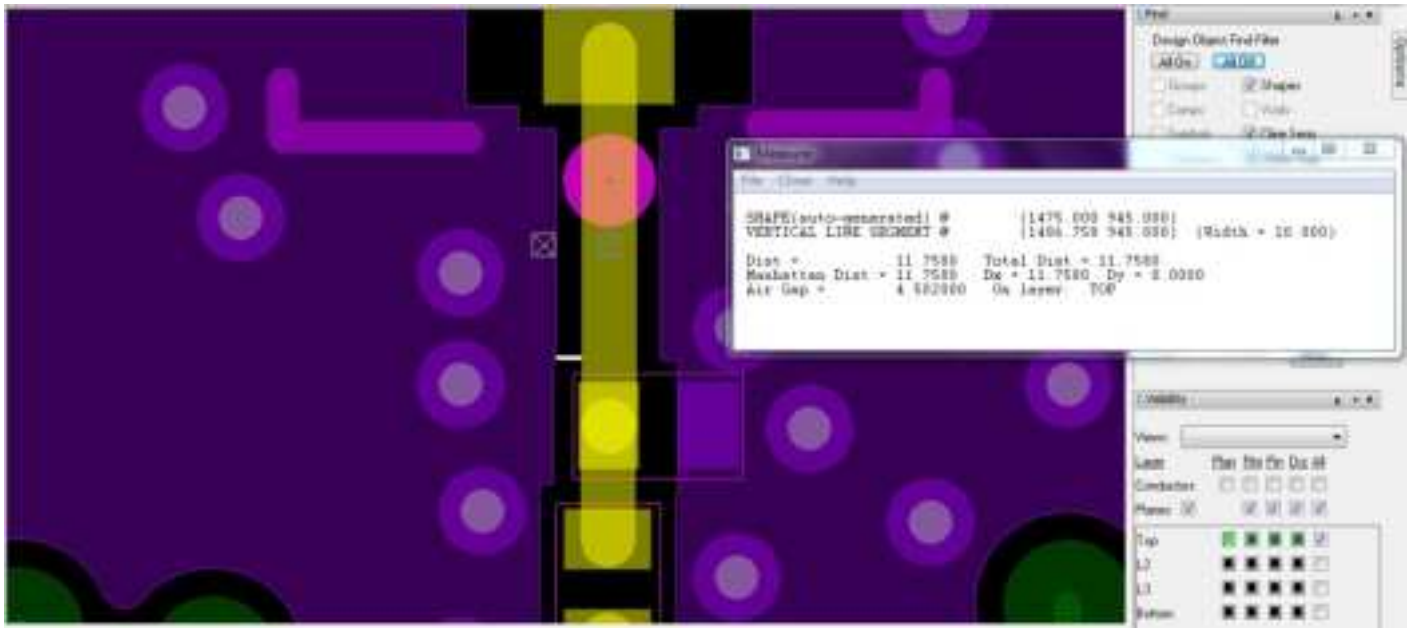
a. Line length of Antenna trace about 88.7mi and 68.5 mil



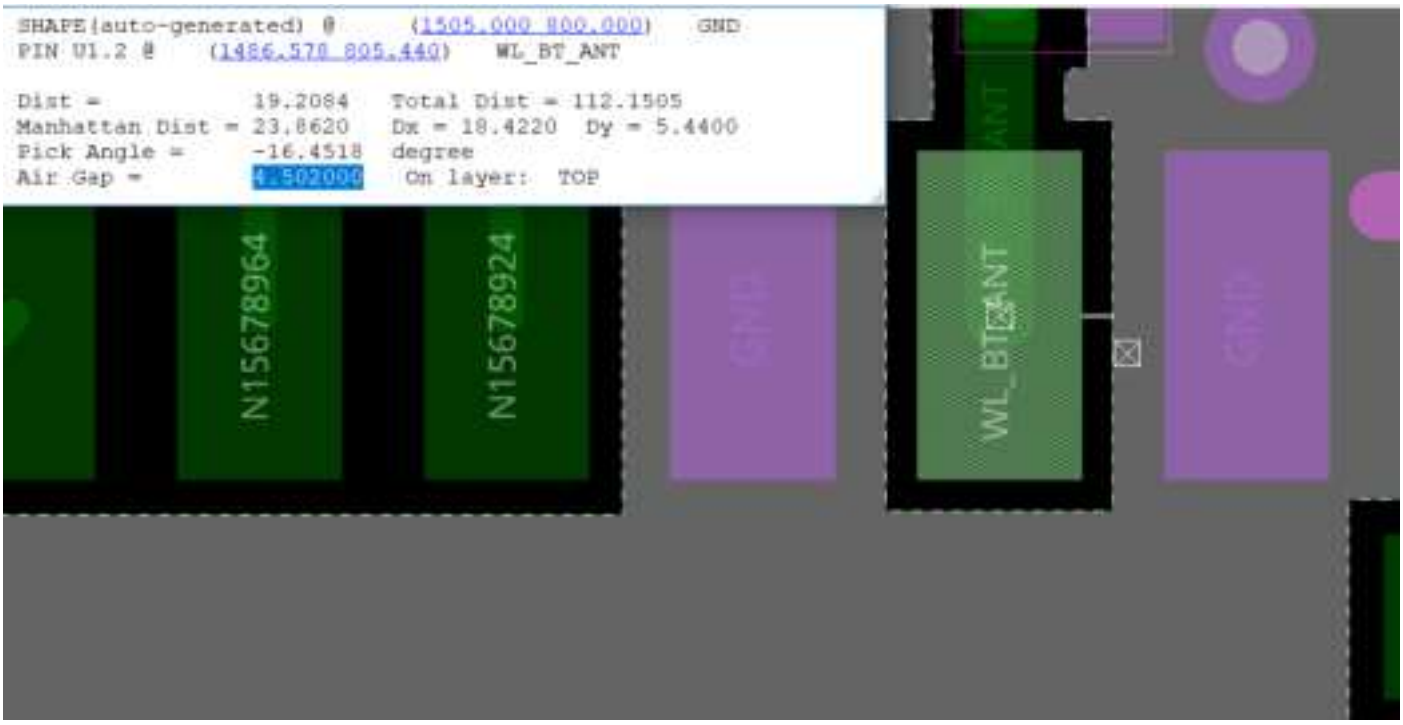
b. Line width of Antenna trace about 10 mil



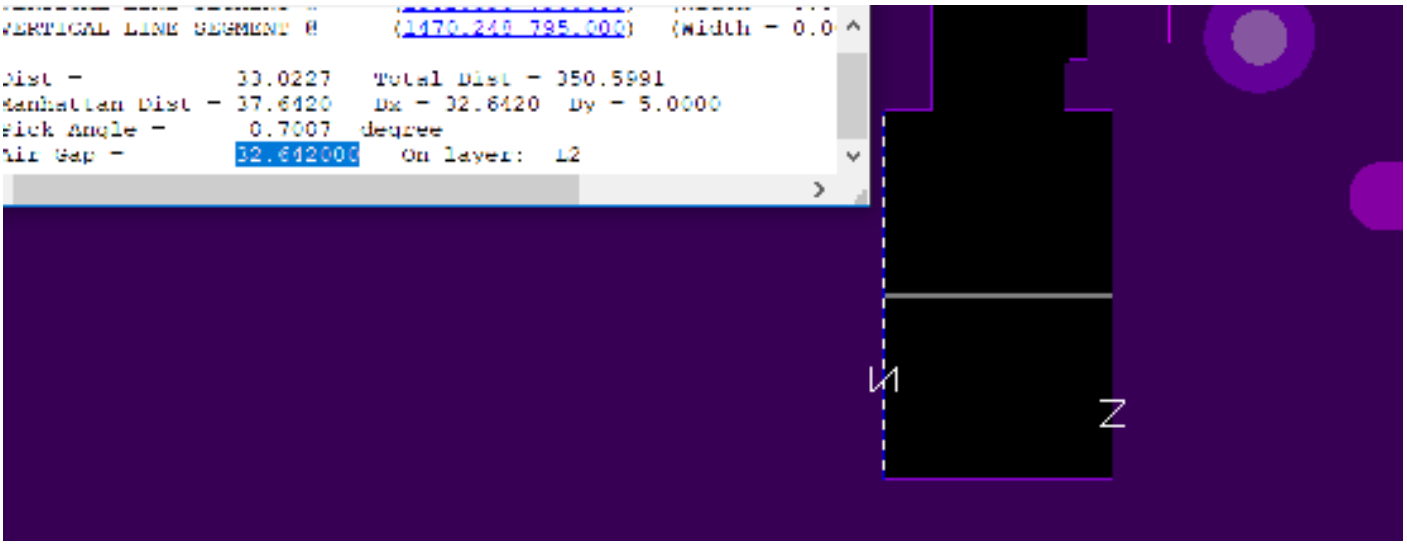
c. Air gap between RF trace and ground about 4.5 mil

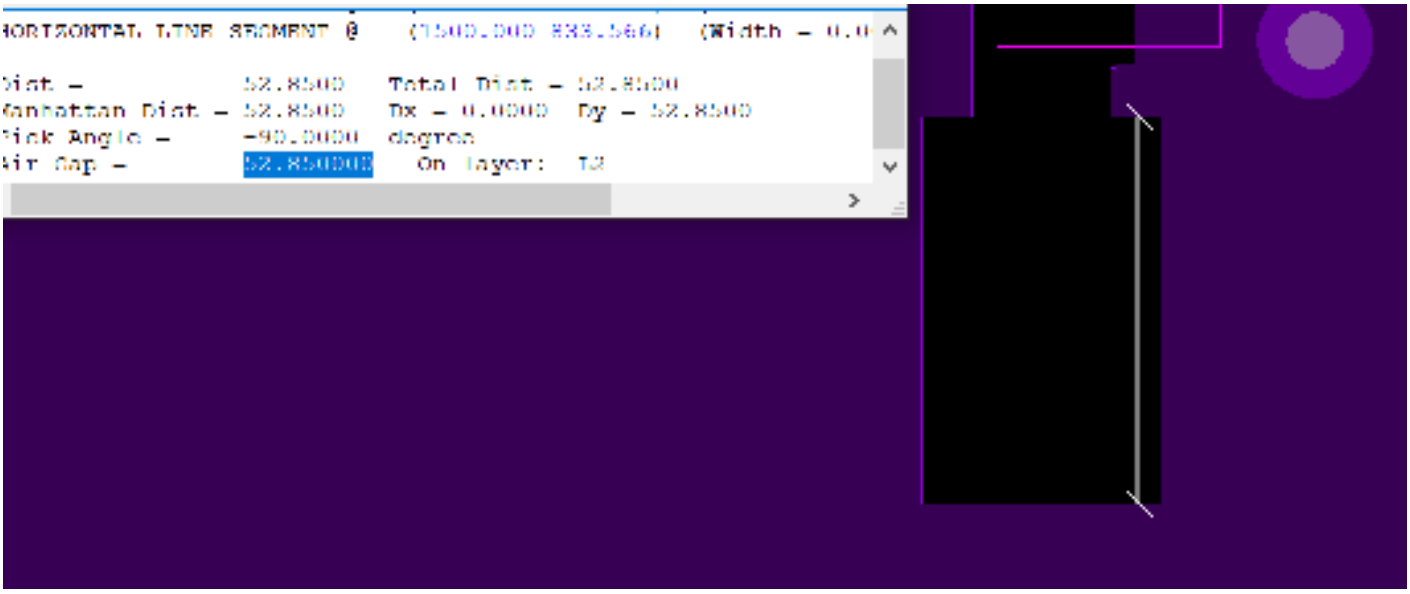


B. RF PAD
TOP layer: Air gap between RF PAD and ground is 4.5 mil



Inner Layer(L2): The length and width of keep out under RF PAD is 32.6 and 52.8 mil.





Inner Layer(L3): Must be continuous reference ground plane

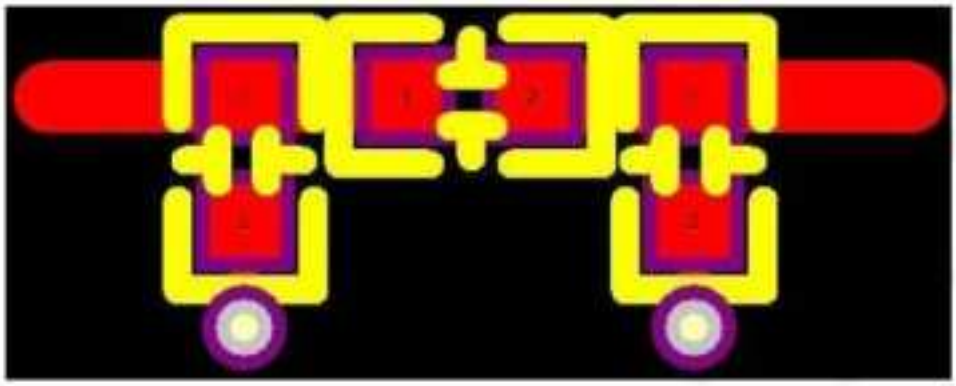
Bot Layer: Must be continuous reference ground plane

6. Antenna

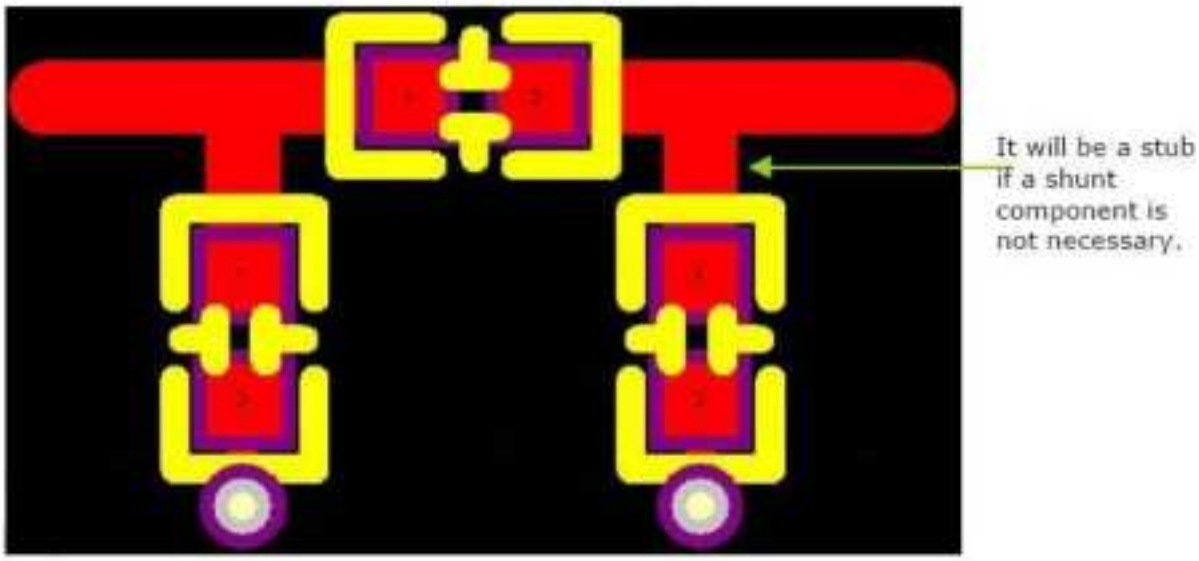
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

7. Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



Incorrent layut for antenna matching

8. SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

9. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   - Keep analog and digital circuits in separate areas.
   - Identify all high-bandwidth signals and their return paths. Treat all critical signals as current

loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.

• Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.

• Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.

However, RF traces should be routed on outside layers to avoid the use of vias on these traces.

• Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.

2. Consider the following with respect to ground and power supply planes:

• Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).

• Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.

• Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

3. Consider these power supply decoupling practices:

• Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.

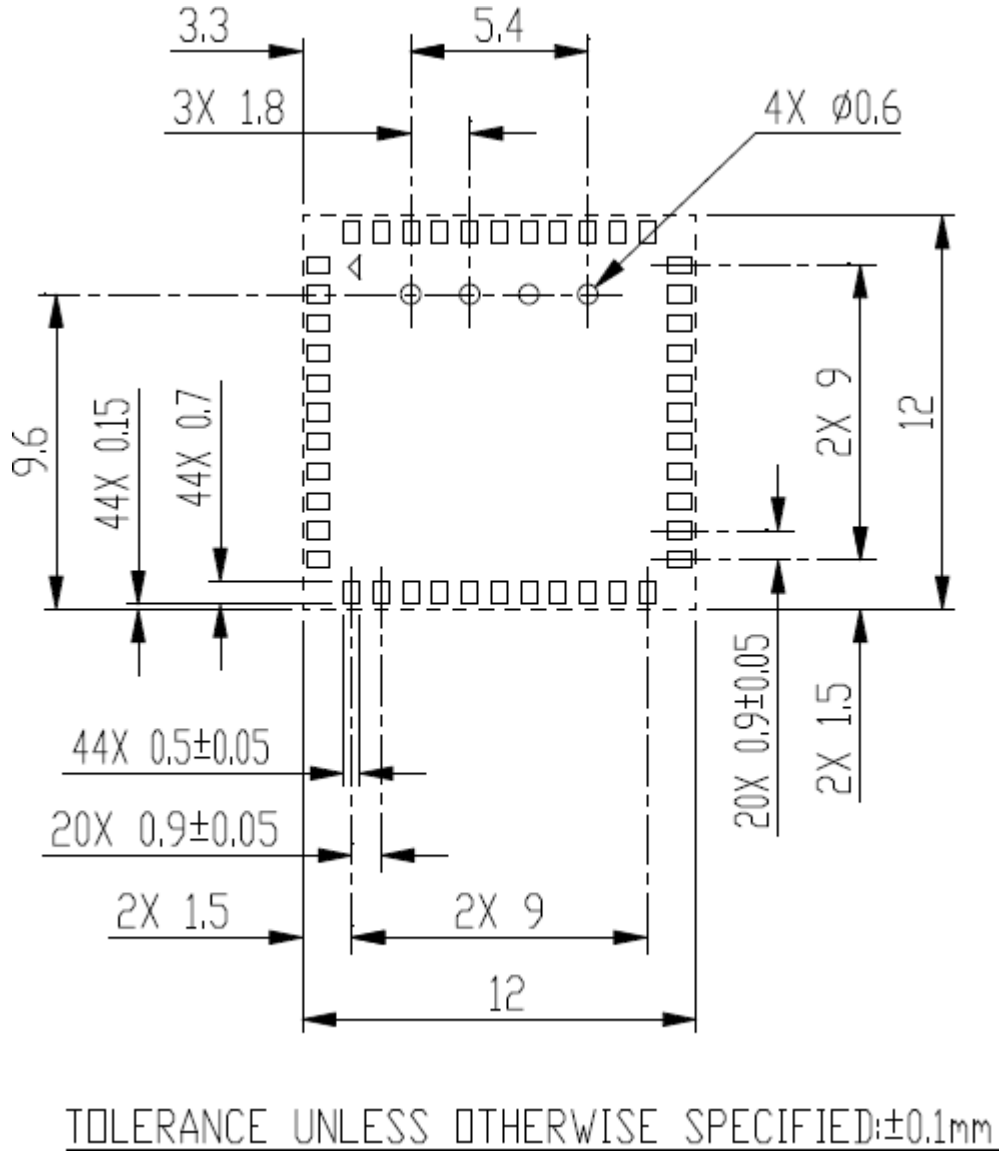
• Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

10. Module stencil and Pad opening Suggestion

- Stencil thickness：0.10~0.12mm
- Function Pad opening size suggestion: Max. 1:1

PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- Solder Printer Opening and Customer PCB Footprint suggestion.
- Example:



(Top View)

11. The other layout guide Information

• Make sure every power traces have good return path (ground path).

• Connect the input pins of unused internal regulators to ground.

• Leave the output pins of unused internal regulators floating.

• High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.

• Good power integrity of VDDIO will improve the signal integrity of digital interfaces.

• Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.

• RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.

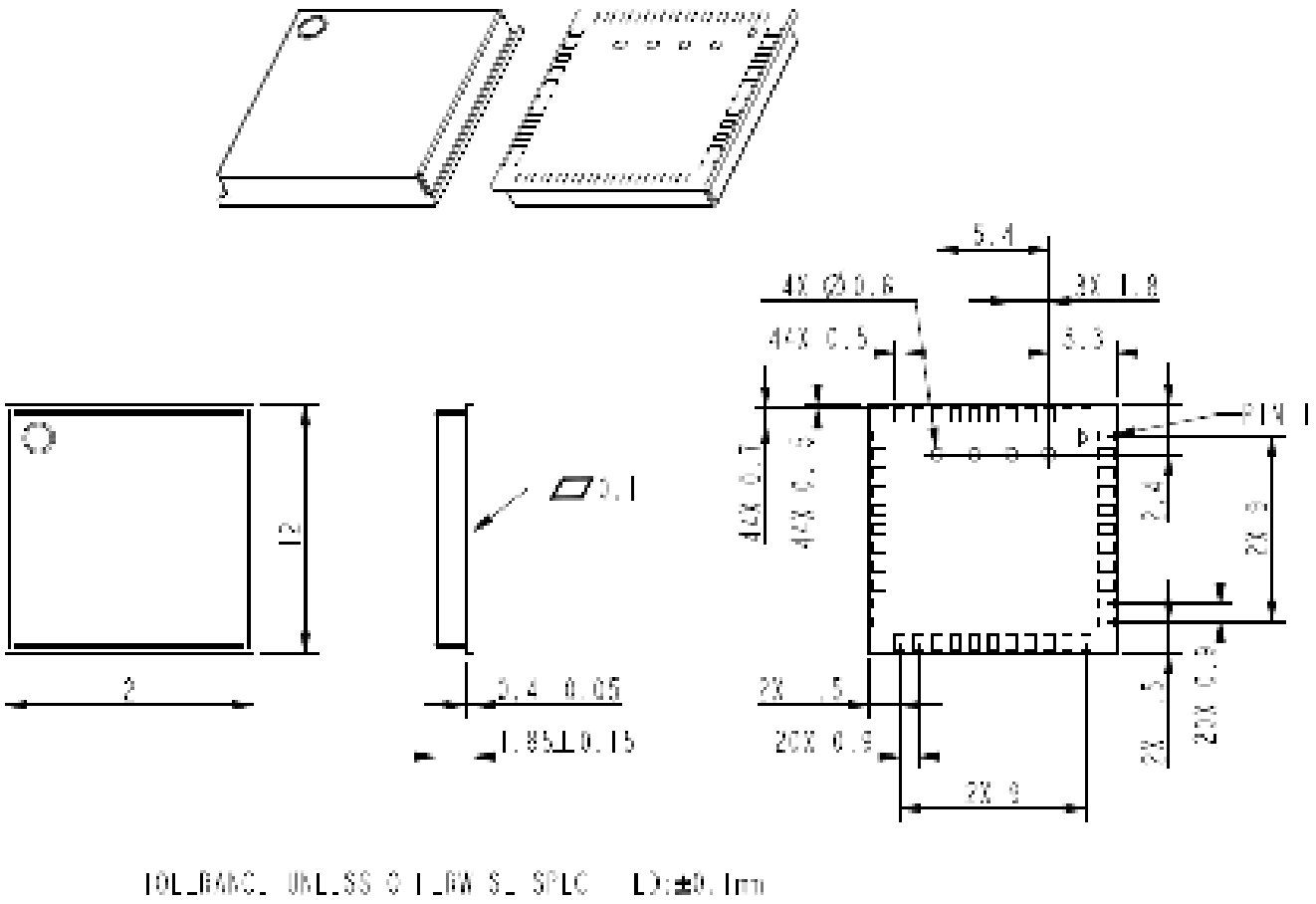
• Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).

• Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).

• Discuss with AzureWave Engineer after you finish schematic and layout job.

12. Mechanical Drawing

•Package Outline Drawing



·Top View of PCB Layout Foot Print