Response to FCC for the 05/07/03 audit:

EMC

1) Data demonstrating compliance at all block edges A-F. Please include data within the first and second 1 MHZ band outside the edge.

Please see the file "EMC_blockEdge.pdf" for the block edges A-F data.

2) Clarification of conducted power measurements. Specification states 32 dBm while measurements show 14.33 dBm. Please include details of how conducted power was measured given the statement on page 7 of 21 that there is no connector.

Please see the file "Detail to measure the conductive output power.doc" for the detail of conducted power measurements. The specification has been corrected. Please see the updated tune up procedure "CMCS Amadeus Tune Up Procedures.pdf" page 4 and 5.

3) Tune-up procedure.

The tune up procedure has been updated. Please see file "CMCS Amadeus Tune Up Procedures.pdf"

SAR

1) Details of power measurement procedures used for SAR testing. Please confirm that power was measured for each scan. Exact agreement with EMC radiated power measurement was not expected.

We measured the conducted power for SAR testing. Please see section 4 in the updated SAR test report "R0302191S.pdf" page 11-14.

2) Maximum number of time slots GPRS mode is capable of. Please provide SAR results with maximum number of time slots if other than one.

The maximum number of time slots is 2. The test results are provided in the updated SAR report "R0302191S.pdf" Section 7, page 31.

3) Additional details of system verification. Please provide SAR data plots used to develop body target value. Please provide head liquid SAR taken on same day as body target development measurements. Details of power scaling used for head SAR re-measurement value. Alternatively please provide manufacturer support information.

Please see the file "SAR Question 3.doc" for the answer of this question.

4) SAR results with and without a typical memory chip as mentioned in the user manual. Please test in worst case position for both head and body.

The user manual mentioning a typical memory chip is a wrong one (submitted on 4/4/03). We already superceded it with the correct one on 4/8/03. There is no typical memory chip. Please check out the one submitted on 4/8/03.